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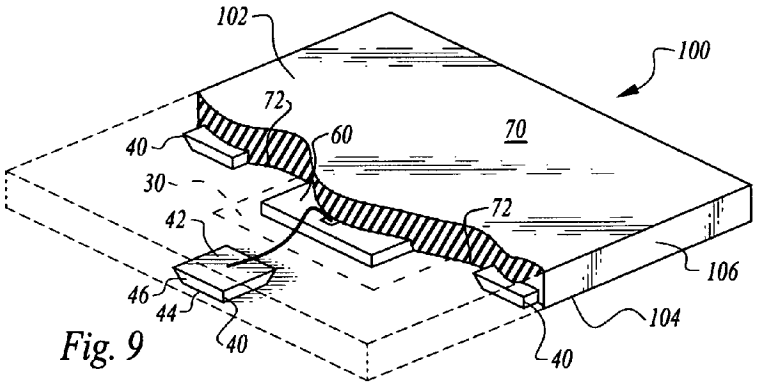

Fig. 9

(57) Abstract: A lead carrier provides support for an integrated circuit chip and associated leads during manufacture as packages containing such chips. The lead carrier includes a temporary support member with multiple package sites. Each package site includes a plurality of terminal pads surrounding a die attach region. The pads are formed of sintered electrically conductive material. A chip is placed at the die attach region and wire bonds extend from the chip to the terminal pads. The pads, chip and wire bonds are all encapsulated within a mold compound. The temporary support member can be peeled away and then the individual package sites can be isolated from each other to provide completed packages including multiple surface mount joints for mounting within an electronic system board. Edges of the pads are contoured to cause the pads to engage with the mold compound to securely hold the pads within the package.

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LEAD CARRIER WITH PRINT-FORMED TERMINAL PADS

Technical Field

The following invention relates to lead carrier based packages for use with an integrated circuit chip for effective interconnection of the integrated circuit chip in an electrical system. More particularly, this invention relates to lead frames and other lead carriers which are manufactured as an array of multiple package sites within a common assembly before and during combination with the integrated circuit, attachment of wire bonds and encapsulation within non-conductive material, before isolation into individual packages for use upon an electronics system board, such as a printed circuit board.

Background Art

The demand for smaller and more capable, portable electronic systems, combined with the increased level of integration in today's semiconductors, is driving a need for smaller semi-conductor packages with greater numbers of input/output terminals. At the same time, there is relentless pressure to reduce the cost of all the components of consumer electronic systems. The quad flat no lead ("QFN") semiconductor package family is among the smallest and most cost effective of all semiconductor packaging types, but when fabricated with conventional techniques and materials, has significant limitations. For instance, with QFN technology the number of I/O terminals and the electrical performance that the technology can support is limited.

QFN packages P (Figures 5-7) are conventionally assembled on an area array lead frame 1 (Figures 1 and 2) etched from a copper sheet. A lead frame 1 can contain from tens to thousands of package sites, each comprised of a die attach pad 2 (Figures 1, 2 and 5-7) surrounded by one or more rows of wire bond pads 4 (Figures 2 and 5-7). All of these package P components are attached to a common frame 1 by pieces of copper to maintain the position of the package P components relative to the rest of the lead frame 1 and to provide an electrical connection to all of the components, to facilitate plating of the bonding and soldering surfaces.

These connected structures, commonly known as tie bars 3 (Figures 1, 2 and 5-7) short all of the components of the lead frame 1 together. Therefore, these tie bars 3 must be designed such that they can all be disconnected from the common shorting structure 6 (Figures 1 and 2) surrounding each package P site during singulation of the individual packages P from the lead frame 1, leaving each die attach pad 2 and wire bond pad 4 electrically isolated. Typically, the design to facilitate severing the electrical connection of the tie bars 3 to the lead frame 1 involves connecting the tie bars 3 to the copper shorting structure 6 (Figures 1 and 2) surrounding each package P site, just outside of the final package P footprint. This shorting structure 6 is sawn away (along line X of Figure 2) during the singulation process, leaving the tie bars 3 exposed at the edge of the package P.

The QFN lead frame 1 provides the parts of the package P that facilitate fixing the semiconductor die, such as an integrated circuit chip 7 (Figures 5-7) within the package P and the terminals that can be connected to the integrated circuit 7 through wire bonds 8 (Figures 5 and 6). The terminals, in the form of the wire bond pads 4, also provide a means of connecting to the electronic system board (such as a printed circuit board) through a solder joint 5 (Figures 5-7) on the surface opposite that of the wire bond 8 surface.

The requirement that all of the package P components be connected to the lead frame 1 by a metal structure, severely limits the number of leads that can be implemented in any given package P outline. For instance, wire bond pads 4 can be provided in multiple rows surrounding the die attach pads 2 with each row being a different distance away from the die attach pads 2. For any wire bond pads 4 inside the outermost row of wire bond pads 4, the tie bar 3 connecting structures must be routed between the pads 4 of the outer row, so that such tie bars 3 can extend to the common sorting structure 6 outboard of the package P isolation (along line X). The minimum scale of these tie bars 3 is such that only one can be routed between two adjacent pads 4. Thus, only two rows of pads 4 may be implemented in a standard QFN lead frame 1. Because of the current relationship between die size and lead count, standard QFN packages are limited to around one hundred terminals, with a majority of packages P having no more than about sixty terminals. This limitation rules out the use of QFN packaging by many types of dies that would otherwise benefit from the smaller size and lower cost of QFN technology.

While conventional QFN technology is very cost effective, there are still opportunities to further reduce the cost. After the integrated circuit chips 7 are attached and connected to the external lead wire bond pads 4 with wire bonds 8, the assembled lead frame 1 of multiple packages P is completely encapsulated with epoxy mold compound 9 (Figures 6 and 7), such as in a transfer molding process. Because the lead frame 1 is largely open front to back, a layer of high temperature tape T is applied to the back of the lead frame 1, prior to the assembly process, to define the back plane of each package P during molding. Because this tape T must withstand the high temperature bonding and the molding process, without adverse effect from the hot processes, the tape is relatively expensive. The process of applying the tape T, removing the tape T and removing adhesive residues, can add significant cost to processing each lead frame 1.

The most common method of singulation of the individual packages P from the lead frame 1 is by sawing (along line X of Figure 2). Because the saw must remove all of the shorting structures 6 just outside the package P outline, in addition to cutting the epoxy mold compound 9, the process is substantially slower and blade life considerably shorter, as if only mold compound 9 is cut. Because the shorting structures 6 are not removed until the singulation process, this means that the dies cannot be tested until after singulation. Handling thousands of tiny packages P, and assuring each is presented to the tester in the correct orientation is much more expensive than being able to test the whole strip with each passage P in a known location.

A lead frame 1 based process, known as punch singulation, to some extent addresses the problem associated with saw singulation and allows testing in the lead frame 1 strip, but substantially increases cost by cutting utilization of the lead frame 1 to less than fifty percent of that of a saw singulated lead frame 1. Punch singulation also imposes a requirement for dedicated mold tooling for every basic lead frame design. Standard lead frames 1 designed for saw singulation use a single mold cap for all lead frames 1 of the same dimensions.

In both saw singulated and punch singulated packages P, the tie bars 3 are left in the completed packages P and represent both capacitive and inductive parasitic elements that cannot be removed. These now superfluous pieces of metal significantly impact the performance of the completed package P, precluding the use

of QFN packages P for many high performance integrated circuit chips 7 and applications. Furthermore, the cost of this potentially rather valuable superfluous metal can be substantial and is wasted by the QFN process.

Several concepts have been advanced for QFN type substrates that eliminate the limitations of etched lead frames. Among those is a process that deposits the array of package components on a sacrificial carrier by electroplating. The carrier is first patterned with plating resist and the carrier, usually stainless steel, is slightly etched to enhance adhesion. The strip is then plated with gold and palladium to create an adhesion/barrier layer, then plated with Ni to around sixty microns thick. The top of the Ni bump is finished with a layer of electroplated Ag to facilitate wire bonding. After the strip is assembled and molded, the carrier strip is peeled away to leave a sheet of packaged dies that can be tested in the sheet and singulated at higher rates and yields than with conventional lead frames. This electroplated approach eliminates all of the issues associated with connective metal structures within the package and allows for very fine features. The plating process, however, results in strips that are very expensive compared to standard etched lead frames.

Another approach is a modification of the etched lead frame process wherein the front side pattern is etched to about half the thickness of the lead frame, and the backside of the lead frame strip is left intact, until after the molding process is complete. Once molding is complete, the backside pattern is printed and the lead frame etched to remove all of the metal except for the backside portion of the wire bond pads and die paddle. This double etch process eliminates all of the issues associated with connective metal structures within the package. The cost of the double etched lead frame is less than the electroplated version, but still more expensive than standard etched lead frames, and the etching and plating processes are environmentally undesirable. One failure mode for a lead frame packaged integrated circuit is for the wire bond pads 4 to become disconnected from wire bonds 8 coupled thereto, especially when a shock load is experienced by the package (such as when an electronic device incorporating the package therein is dropped and hits a hard surface). The wire bond pad 4 can remain mounted to a printed circuit board or other electronic system board while separating slightly from surrounding epoxy mold compound, allowing the wire bond 8 to be severed from the wire bond pad 4.

Accordingly, a further need exists for a lead carrier package which better holds the wire bond pads 4 within the entire package, especially when shock loads are experienced.

Disclosure of the Invention

With this invention a lead carrier is provided with an array of separate package sites in the form of a multi-package lead carrier. A sintered material, typically beginning as silver powder, is placed upon a temporary layer formed of high temperature resistant material, such as stainless steel. The stainless steel or other material forming the temporary layer supports the sintered material while it is heated to a sintering temperature.

The sintered material is located upon the temporary layer in separate structures preferably electrically isolated from each other (other than through the temporary layer) in the form of terminal pads. The present invention avoids the requirement for a structure to be present on the temporary layer specifically for the purpose of receiving and holding a semiconductor device, because such a semiconductor device can be temporarily placed, or affixed (such as with adhesive) to the temporary layer. Therefore, the present invention is designed to provide die attach regions rather than die attach pads. One or more terminal pads are associated with each die attach region. Each die attach region is configured to have an integrated circuit or other semiconductor device supported thereon. Wire bonds can be routed from the integrated circuit upon the die attach region to the separate terminal pads surrounding each die attach region. Mold compound can then be applied which encapsulates the integrated circuits, terminal pads and wire bonds. Only surface mount joints defining under portions of the integrated circuit and terminal pads remain unencapsulated because they are adjacent the temporary layer.

Once the mold compound has hardened, the temporary layer can be peeled away from the remaining portions of the lead carrier, leaving a plurality of package sites with individual die attach regions and associated integrated circuits, terminal pads and wire bonds all embedded within a common mold compound. The individual package sites can then be cut from each other by cutting along boundaries between the package sites and surface mounted through the surface mount joints to an electronics system board or other support.

Because the package sites and individual pads within the package sites are each electrically isolated from each other, other than through the temporary layer, these individual pads can be tested for electrical continuity and other electrical performance characteristics at a variety of different times, such as before mounting of the integrated circuit or after encapsulation within the mold compound and removal of the temporary layer, but before singulation into separate packages. Such testing can occur while the array of pads is supported upon the temporary layer or after removal from the temporary layer. Furthermore, such packages could be tested after isolation from adjacent packages on the lead carrier utilizing known testing equipment utilized with QFN packages or other testing equipment.

Additionally, each pad preferably has edges around peripheries thereof which are configured to mechanically engage with the mold compound somewhat. In particular, these edges can taper in an overhanging fashion, or be stepped in an overhanging fashion, or otherwise be configured so that at least a portion of each edge spaced from a bottom thereof extends further laterally than portions of each edge closer to a bottom portion of each edge. Thus, the mold compound, once hardened, locks the pads securely into the mold compound. In this way, the pads resist detachment from the wire bonds or otherwise becoming detached from the mold compound, and keep the entire package as a single unitary package.

Brief Description of Drawings

Figure 1 is a perspective view of a QFN lead frame of a simplified variety and illustrating prior art lead frame technology.

Figure 2 is a perspective view of a detail of a portion of that which is shown in Figure 1, along with dashed lines indicative of where cut lines are followed to separate individual package sites from the lead frame.

Figure 3 is a perspective view of a lead carrier according to this invention with multiple separate package sites thereon and mounted upon a temporary support member.

Figure 4 is a perspective view of a detail of a portion of that which is shown in Figure 3 and further illustrating details of each package site before mounting of an integrated circuit chip, attachment of wire bonds and encapsulation within mold compound.

Figure 5 is a perspective view of a prior art QFN package showing placement of an integrated circuit chip and wire bonds and illustrating in broken lines how encapsulation material is placed relative to other conductive structures within the package.

Figure 6 is a perspective view similar to that which is shown in Figure 5 but with the encapsulating mold compound in place, and with portions of the encapsulating mold compound cut away to reveal interior structures of the package.

Figure 7 is a perspective view similar to that which is shown in Figure 6 but from below to illustrate solder joints available for surface mounting of the package upon an electronic system board or other interface within an electrical system.

Figure 8 is a perspective view of an individual package site on the lead carrier of this invention after placement of an integrated circuit chip and wire bonds, and illustrating in broken lines the position of mold compound.

Figure 9 is a perspective view similar to Figure 8 but with the mold compound shown in place encapsulating conductive structures within the package, and with portions of the mold compound cut away to reveal interior details of the package.

Figure 10 is a perspective view from below of the package and illustrating surface mount joints of the package according to this invention.

Figures 11-17 are full sectional views of a temporary support member and lead carrier during the process of manufacturing the semiconductor supporting package according to this invention.

Figure 18 is a perspective view of an alternative lead carrier with alternative pads illustrated having different edge contours to exhibit different engagement properties with surrounding encapsulating mold compound.

Best Modes for Carrying Out the Invention

Referring to the drawings, wherein like reference numerals represent like parts throughout the various drawing figures, reference numeral 10 is directed to a lead carrier (Figures 3 and 4) which can support a plurality of package sites 12 thereon upon a temporary support member 20 for manufacture of a plurality of packages 100 (Figures 9 and 10) including an integrated circuit chip 60 and to provide for a large number of inputs and outputs into the integrated circuit chip 60. The

invention is also directed to the plurality of resulting packages 100 isolated from the plurality of package sites 12 and a lead carrier 10' (Figure 17) after manufacture of the individual packages 100 and removal of the packages 100 from the common temporary support member 20 of the lead carrier 10.

In essence, and with particular reference to Figures 3, 4, 8 and 9, basic details of the lead carrier 10 and package 100 are described, according to a preferred embodiment of this invention. The lead carrier 10 includes a temporary support member 20 of thin planar high temperature resistant material, such as stainless steel. A plurality of die attach regions 30 and terminal pads 40 are arrayed on the temporary support member 20 at package sites 12, with multiple terminal pads 40 surrounding each die attach region 30.

An integrated circuit chip 60 is located at the die attach region 30 (Figures 8 and 9). Wire bonds 50 are joined between input output terminals on the chip 60 and the terminal pads 40. The entire package 100 including the terminal pads 40, wire bonds 50 and chip 60 are encapsulated within a mold compound 70 other than surface mount joint 90 portions (Figure 10) defining an underside of the package 100. The mold compound 70 is typically applied to the lead carrier 10 to surround each of the package sites 12. Later isolation of each package 100 occurs by cutting of the mold compound 70 to provide multiple packages 100 from the original lead carrier 10.

With particular reference to Figures 1 and 2, details of a prior art lead frame 1 of a "quad flat no lead" (QFN) variety are described for comparison and contrast to the detail of the lead carrier 10 of this invention. In the embodiment shown, the QFN lead frame 1 is a planar structure of etched conductive material. This etched conductive material is etched into distinct die attach pads 2 and wire bond pads 4, each joined to a common shorting structure 6 through tie bars 3. This entire etched QFN lead frame 1 is mounted upon molding tape T so that epoxy mold compound 9 can be applied to the lead frame 1 and encapsulate the pads 2, 4 (Figures 5-7).

Before such encapsulation, an integration of the chip 7 is mounted upon the die attach pad 2. Wire bonds 8 are placed between the wire bond pads 4 and input/output terminals on the chip 7. The mold compound 9 can then entirely encapsulate the pads 2, 4 as well as the chip 7 and wire bonds 8. The mold compound is prevented from encapsulating an underside of the pads 2, 4 by the tape

T. After the mold compound 9 has hardened, the tape T can be peeled away so that solder joints 5 (Figure 7) are presented on an underside of the lead frame 1. Finally, the separate QFN packages P are isolated by cutting (along cut lines X of Figure 2) to isolate each package P from the overall lead frame 1.

Importantly, it should be noted that portions of the tie bars 3 extending from the die attach pads 2 and the wire bond pads 4 remain within the package P. Some portions of these tie bars 3 actually extend out of an edge of the package P (Figures 6 and 7). Furthermore, the common shorting structure 6 (Figures 1 and 2) is not part of any package P. Thus, the common shorting structure 6 is typically wasted. Furthermore, remaining portions of the tie bars 3 within each package P do not provide any beneficial purpose and hence are also wasted within the package P. Such tie bar 3 remnants can also have a negative impact on the performance of the package P and the chip 7 within the package P. For instance, a portion of the tie bars 3 extending out of edges of the mold compound 9 of the package P presents an opportunity for undesirable shorting or for electromagnetic interference and "noise," such that certain electronics applications are not well served by prior art QFN packages P. Even when such prior art QFN packages are suitable, waste associated with the common shorting structure 6 and tie bars 3 embedded within the package P is undesirable. Furthermore, the tape T is not reusable and is another wasted expense utilizing known prior art QFN lead frame 1 and package P techniques.

Referring to Figures 3 and 4, specific details of the lead carrier 10 of this invention as well as the temporary layer, such as the temporary support member 20, and pads 40 are described, according to an exemplary embodiment. This exemplary embodiment is significantly simplified over a typical preferred embodiment in that each package site 12 only shows four terminal pads 40 surrounding each die attach region 30. Typically, such terminal pads 40 would be presented in numbers of dozens or potentially even hundreds surrounding each die attach region 30. Such terminal pads 40 would typically be presented in multiple rows including an innermost row closest to the die attach region 30, an outermost row of terminal pads 40 most distant from the die attach region 30 and potentially multiple intermediate rows between an innermost row and an outermost row of terminal pads 40.

The lead carrier 10 is a planar structure that is manufactured to include multiple package sites 12 and to support these package sites 12 during their

manufacture and through testing and integration with integrated circuit chips 60 (or other semiconductor devices, such as diodes or transistors) and wire bonds 50 (Figures 8 and 9) to facilitate the ultimate production of multiple packages 100 (Figures 9 and 10). The lead carrier 10 includes a temporary support member 20. This temporary support member 20 is a thin planar sheet of high temperature resistant material, most preferably stainless steel. This member 20 includes a top surface 22 upon which other portions of the lead carrier 10 are manufactured. An edge 24 of the temporary support member 20 defines a perimeter of the temporary support member 20. In this exemplary embodiment, this edge 24 is generally rectangular.

The temporary support member 20 is preferably sufficiently thin that it can flex somewhat and facilitate peeling removal of the temporary support member 20 from the lead carrier 10 (or vice versa) after full manufacture of packages 100 at the package sites 12 and lead carrier 10 (Figures 8-10 and 17). The lead carrier 10' (Figure 17) refers to the lead carrier after it has had the temporary support member 20 removed therefrom.

The top surface 22 of the temporary support member 20 supports a plurality of package sites 12 thereon with each package site 12 including at least one die attach region 30 and a plurality of terminal pads 40 associated with each die attach region 30. Cut lines Y generally define boundaries of each package site 12 (Figure 4).

The terminal pads 40 may exhibit a different geometry and location, but are preferably formed of similar material. In particular, these pads 40 are preferably formed of a sintered material. According to a preferred embodiment, these pads 40 begin as a powder of electrically conductive material, preferably silver, mixed with a suspension component. This suspension component generally acts as a binding liquid to give the silver powder a consistency of paste or other flowable material characteristics so that the silver powder can best be handled and maneuvered to exhibit the desired geometry for the pads 40.

A mixture of this suspension component and the silver powder or other electrically conductive metal powder is heated to a sintering temperature for the metal powder. The suspension component boils into a gas (or otherwise volatilizes) and is evacuated from the lead carrier 10. The metal powder is sintered into a unitary mass having the shape desired for the terminal pads 40.

The temporary support member 20 is configured to have thermal characteristics such that it maintains its flexibility and desired degree of strength and other properties up to this sintering temperature for the electrically conductive material forming the pads 40. Typically this sintering temperature is approaching the melting point for the metal powder that is sintered into the pads 40.

With reference to Figures 11-14, a depiction of the lead carrier 10 is presented in sequential steps for forming of the pads 40. Note from Figure 12 that a temporary form material 80 is first placed upon the temporary support member 20. This form material 80 can be printed onto the top surface 22 of the temporary support member 20 or could be etched into a continuous material pre-placed upon the temporary support member 20, or otherwise formed. Lateral surfaces 82 of the temporary form material 80 define edges of voids 84 between areas of the temporary form material 80. These voids 84 are then filled with the mixture of metal powder and the suspension component by flowing this mixture into these voids 84. When the sintering process occurs and the temporary support member 20 as well as the temporary form material 80 and metal powder and suspension mixture are heated, not only is the metal powder sintered and the suspension component volatilized and removed, but also the temporary form material 80 is volatilized and removed from the package sites 12 on the lead carrier 10. Thus, after sintering only the pads 40 of sintered material remain upon the temporary support member 20 (Figure 14).

The terminal pad 40 can have a variety of different sizes and geometries. Most preferably, the terminal pad 40 will include a substantially planar top side 42 opposite a substantially bottom side which rests upon the top surface 22 of the temporary support member 20. An edge 46 of the terminal pad 40 defines a perimeter shape of the terminal pad 40. This edge 46 preferably is not oriented within a plane perpendicular to the temporary support member 20, but has a taper or otherwise is configured to be contoured so that an at least partial overhang exists with an upper extent of each edge 46 overhanging a lower extent of each edge 46. This taper is preferably provided by beveling of the lateral surfaces 82 of the temporary form material 80 (Figures 12-14).

This overhang relationship can be continuous, such as by tapering the edge 46 as shown. In alternative forms (Figure 18) the edge 46 can have other contours

such as a stepped contour and still provide some form of overhang. In other forms, so long as at least some portion of the edge 46 overhangs a portion of the edge 46 closer to a lower extent of the edge 46, a form of overhang is provided. As can be seen in Figures 16 and 17, after the mold compound 70 has encapsulated pads 40 this overhang in the edges 46 of the terminal pads 40 cause the terminal pads 40 to be held within the mold compound 70, especially during removal of the temporary support member 20.

While only four terminal pads 40 are shown around each die attach region 30 in the exemplary embodiment depicted in Figures 3 and 4, preferably the number of terminal pads 40 surrounding each die attach region 30 would be on the order of dozens or hundreds of terminal pads 40 surrounding each die attach region 30. Also, typically the terminal pads 40 would be arrayed in rows surrounding each die attach region 30. The terminal pads 40 could be smaller or larger relative to the die attach region 30 as depicted in this exemplary embodiment. While the edges 46 of the pads 40 are each shown having an overhanging contour, it is conceivable that only some of the edges 46 of each pad 40 would have such an overhanging contour and still provide some benefits according to this aspect of this invention.

Preferably, the upper side 42 of each terminal pad 40 are in a common plane. However, it is conceivable that upper sides 42 could have differing heights, and that these sides 42 could be in a form other than completely planar and still provide some of the benefits according to this invention. The bottom sides 44 define surface mount joints 90 within each package 100 after completion of the manufacturing process (Figure 10).

With particular reference to Figures 8-10, details of each package 100 after further manufacture upon the lead carrier 10 at the various package sites 12 are described, according to this exemplary embodiment. An integrated circuit chip 60 is mounted at the die attach region 30. Such mounting could be as simple as placing the chip 60 upon the temporary support member 20 at the region 30 (Figures 4, 14 and 15). An adhesive could be used to hold the chip 60 upon the temporary support member 20, or other forms of attachment could be employed, such as static attraction, magnetic attraction, suction or fasteners.

Optionally, a lower side of the integrated circuit chip 60 is electrically coupled at the die attach region 30. Such electric coupling can be common to "ground" for

the chip 60 or common to some other reference for the chip 60, or can have some other electrical state within an overall electrical system in which the package 100 is utilized. The electric coupling can be initially with the temporary support member 20 and then electric coupling to a terminal of a test structure configured to test the packages 100 while still in a common lead carrier 10' after removal from the temporary support member 20 (Figure 17). The chip 60 includes a base 62 defining a lower portion thereof substantially co-planar with the die attach region 30. An upper surface 64 of the chip 60 is provided opposite the base 62. This upper surface 64 has a plurality of input output junctions which can be terminated to one end of a wire bond 50 (Figures 8 and 9).

One wire bond 50 is preferably terminated between each input output junction on the chip 60 and a surrounding terminal pad 40. Thus, each wire bond 50 has a chip end opposite a terminal end. As another alternative, at least one terminal pad 40 can be left without a wire bond 50, such as when a single package 100 is designed to be generic to two or more specific designs and one of the designs requires more terminal pads 40 than the other. Also, wire bonds 50 can be provided between sets of terminal pads 40, where such an electrical interconnection is called for by the circuit design. Using known wire bond 50 terminating techniques, such as those used with QFN lead frames, these wire bonds 50 are coupled between the chip 60 and the terminal pads 40 or between sets of terminal pads 40.

To complete the package 100 forming process, mold compound 70 is flowed over the lead carrier 10 and allowed to harden in a manner completely encapsulating each of the terminal pads 40, wire bonds 50 and integrated circuit chips 60. This mold compound 70 can mold against the top surface 22 of the temporary support member 20. Thus, the surface mount joints 90 of each pad 40 and the base 62 of each chip 60 remain exposed after removal of the temporary support member 20 (Figure 10). The mold compound 70 is typically of a variety which is in a fluid form at a first temperature but which can harden when adjusted to a second temperature.

The mold compound 70 is formed of a substantially non-conductive material such that the pads 40 and base 62 of the chip 60 are electrically isolated from each other. The mold compound 70 flows between the pads 40 to provide interlocks 72 (Figures 16 and 17) which tend to hold the pads 40 and chip 60 within the overall package 100 and together with the mold compound 70. Such interlocks 72 keep the

terminal pads 40 from becoming detached from the wire bonds 50. Such detachment propensity is first resisted when the temporary support member 20 is removed from the lead carrier 10, and again beneficially is resisted when the package 100 is in use and might experience shock loads that might otherwise detach the terminal pads 40 from the package 100. These interlocks 72 can have a variety of different shapes as defined above associated with the edges 46 of the pads 40, and originally based on the contour of the lateral surfaces 82 of the temporary form material 80 (Figures 12 and 13).

After hardening of the mold compound 70, the package 100 is provided in an array on the lead carrier 10 with each package 100 including a top 102 (Figures 9 and 10) opposite a bottom 104 and with perimeter sides 106. Beneficially, the perimeter sides 106 are not required to have any electrically conductive material extending therefrom, in contrast to prior art QFN packages P (Figures 6 and 7), which must.

With reference to Figure 18, details of an alternative lead carrier 110 are described. In this alternative lead carrier 110 a temporary support member 120 has alternative pads 130 resting thereon. These alternative pads 130 include a top side 132 opposite a bottom side 134 and with a stepped edge 136 thereon. This stepped edge 136 is an alternative edge to the edges provides on the terminal pads 40 described above. Such a stepped edge 136 still provides a form of interlocking with the mold compound 70 to beneficially hold the pads 40 within the entire package 100.

This disclosure is provided to reveal a preferred embodiment of the invention and a best mode for practicing the invention. Having thus described the invention in this way, it should be apparent that various different modifications can be made to the preferred embodiment without departing from the scope and spirit of this invention disclosure. When structures are identified as a means to perform a function, the identification is intended to include all structures which can perform the function specified. When structures of this invention are identified as being coupled together, such language should be interpreted broadly to include the structures being coupled directly together or coupled together through intervening structures. Such coupling could be permanent or temporary and either in a rigid fashion or in a fashion which allows pivoting, sliding or other relative motion while still providing some form of attachment, unless specifically restricted.

Industrial Applicability

This invention exhibits industrial applicability in that it provides a system for proving the electrical interconnect components of a semi-conductor package that allows for the implementation of a simplified QFN process to more easily produce QFN packaged semiconductor dies.

Another object of the present invention is to provide a system and method for providing the electrical interconnect components of a semiconductor package arrayed on a sacrificial carrier that can be peeled away after molding, to yield a continuous strip of multiple semiconductor packages with pads with no electrical connection between any two pads, to facilitate testing at various different stages of manufacture and avoidance of material waste.

Another object of the present invention is to provide the electrical interconnect components of a semiconductor package in a manner that enables higher electrical performance while utilizing a minimum amount of metal therein to facilitate electrical connection of a semiconductor die to the system board of an electronic system.

Another object of the present invention is to provide the electrical interconnect components of a semiconductor package that lowers the assembly cost of the package by simplifying and eliminating steps from a standard QFN assembly process.

Another object of the present invention is to provide the electrical interconnect components of a semiconductor package that allow for the inclusion of more than two rows of input/output terminals and many times the number of input/output terminals than are practical with prior art lead frame based QFN packages.

Another object of the present invention is to provide electrical interconnect components of a semiconductor package that allows greater design flexibility to incorporate features, such as multiple power and ground structures and multiple die attach regions, when compared to lead frame based QFN packages.

Another object of the present invention is to provide a lead carrier with multiple integrated circuit mounting package sites thereon which can be manufactured in a low cost high quality manner.

Another object of the present invention is to provide a semiconductor package for electrical interconnection to adjacent components which is highly resistant to damage associated with shock loads thereto.

Another object of the present invention is to provide a lead carrier with multiple integrated circuit mounting package sites which exhibits high performance electrically by minimizing excess conducting portions therein.

Another object of the present invention is to provide a lead carrier which has package sites thereon which can be tested at multiple stages in the manufacturing process in a simple and automated fashion.

Another object of the present invention is to provide a vehicle for manufacturing QFN or land grid array type packages that do not require a separate structure for mounting and holding the semiconductor device during the semiconductor assembly process.

Other further objects of this invention which demonstrate its industrial applicability, will become apparent from a careful reading of the included detailed description, from a review of the enclosed drawings and from review of the claims included herein.

CLAIMS

What is claimed is:

Claim 1: A lead carrier and semiconductor combination, comprising in combination:

a plurality of terminal pads formed of electrically conductive material;

said terminal pads each having an upper side opposite a lower side, with edges between said upper side and said lower side;

said terminal pads each being a sintered structure of electrically conductive material;

a semiconductor having a base opposite an upper surface;

a wire bond between at least one of said terminal pads and said semiconductor;

said terminal pads, said semiconductor and said wire bonds at least partially encapsulated within a substantially electrically non-conductive material; and

wherein said lower side of each said terminal pad and said base of said integrated circuit are each located within a substantially common plane.

Claim 2: The combination of claim 1 wherein at least one of said plurality of terminal pads has a contoured edge which is at least partially contoured to hold said pad to said substantially electrically non-conductive material.

Claim 3: The combination of claim 2 wherein said contoured edge has an upper extent opposite a lower extent, at least a first portion of said contoured edge spaced from said lower extent defining a lateral pad width greater than a second portion of said edge closer to said lower extent than said first portion, such that said first portion overhangs said second portion.

Claim 4: The combination of claim 3 wherein said contoured edge has a stepped contour with portions above said step and closer to said upper extent of said edge defining an overhang relative to portions of said edge below said step and closer to said lower extent of said contoured edge.

Claim 5: The combination of claim 3 wherein said contoured edge exhibits a taper with portions of said contoured edge most distant from said lower extent overhanging portions of said contoured edge closer to said lower extent.

Claim 6: The combination of claim 1 wherein said semiconductor and said plurality of terminal pads are each fully encapsulated within said substantially electrically non-conductive material, except on said base of said semiconductor and said lower sides of said terminal pads.

Claim 7: The combination of claim 1 wherein said plurality of terminal pads, said semiconductor and said wire bonds form a package, and wherein said package is one of a plurality of packages encapsulated within a common said substantially electrically non-conductive material.

Claim 8: The combination of claim 7 wherein said plurality of packages are each located upon a common flexible support layer having a melting point higher than a sintering temperature of said electrically conductive material forming said terminal pads.

Claim 9: The combination of claim 8 wherein an adhesive is located between said base of said semiconductor and said common flexible support layer.

Claim 10: A lead carrier for supporting electronic devices having a plurality of inputs and/or outputs, the lead carrier comprising in combination:

a plurality of electrically conductive terminal pads spaced from each other and adjacent a die attach region;

said terminal pads formed of a sintered electrically conductive material; and

said terminal pads located upon a temporary layer with a melting point greater than a sintering temperature of said material forming said terminal pads.

Claim 11: The lead carrier of claim 10 wherein said terminal pads surround one of said die attach regions.

Claim 12: The lead carrier of claim 10 wherein at least one of said plurality of electrically conductive terminal pads has an edge with an upper extent opposite a lower extent, said lower extent adjacent said temporary layer, at least a first portion of said edge spaced from said lower extent defining a lateral pad width greater than a second portion of said edge closer to said lower extent of said edge than said first portion, such that said first portion overhangs said second portion.

Claim 13: The lead carrier of claim 12 wherein said contoured edge has a stepped contour with portions above said step and closer to said upper extent of said edge defining an overhang relative to portions of said edge below said step and closer to said lower extent of said contoured edge.

Claim 14: The lead carrier of claim 12 wherein said contoured edge exhibits a taper with portions of said contoured edge most distant from said lower extent overhanging portions of said contoured edge closer to said lower extent.

Claim 15: The lead carrier of claim 10 wherein a semiconductor is located at each of said die attach regions, said semiconductor having a base opposite an upper surface, with a plurality of wire bonds extending from said semiconductor to a plurality of said electrically conductive terminal pads adjacent said die attach region, said terminal pads, said wire bonds and said semiconductor at least partially encapsulated with a substantially electrically non-conductive material.

Claim 16: The lead carrier of claim 15 wherein said layer of substantially electrically non-conductive material encapsulates said plurality of electrically conductive terminal pads and said semiconductor on all sides thereof other than portions of said terminal pads and said semiconductor facing said temporary layer.

Claim 17: The lead carrier of claim 16 wherein said temporary layer is sufficiently flexible to allow peeling removal from said terminal pads and said base of said semiconductor and said encapsulating substantially non-conductive material layer.

Claim 18: A method for forming a plurality of integrated circuit chip containing packages, including the steps of:

providing a temporary layer having a top surface;

placing electrically conductive terminal pads on the top surface of the temporary layer;

positioning integrated circuits upon the top surface, the integrated circuits each having a base opposite an upper surface;

attaching wire bonds between the terminal pads and each integrated circuit;

encapsulating the terminal pads, wire bonds and integrated circuits within substantially electrically non-conductive material; and

removing the temporary layer, leaving a bottom side of the terminal pads and the bases of the integrated circuits exposed.

Claim 19: The method of claim 18 wherein said placing step includes placing temporary form material upon the top surface of the temporary layer, providing voids in the temporary form material, filling the voids with a flowable material including electrically conductive metal powder and a binding liquid, heating the flowable material to a temperature causing the binding liquid to volatilize and be removed, causing the temporary form material to volatilize and be removed, and sintering the metal powder into the terminal pads, while remaining below a melting point for the temporary layer.

Claim 20: The method of claim 18 wherein said positioning step includes applying an adhesive between the bases of the integrated circuits and the top surface of the temporary layer.

Claim 21: The method of claim 18 including the further step of singulating a plurality of integrated circuit containing packages into individual packages with each package having at least one integrated circuit chip, a plurality of terminal pads and wire bonds extending from the terminal pads to the integrated circuit chip, with the wire bonds and portions of the terminal pads and integrated circuit encapsulated within the substantially electrically non-conductive material.

Claim 22: The method of claim 18 including the further step of testing electrical performance of the electrically conductive terminal pads after said placing step and before said attaching step.

Claim 23: The method of claim 18 including the further step of testing electrical performance of the plurality of integrated circuit chip containing packages before singulating the plurality of packages into individual packages.

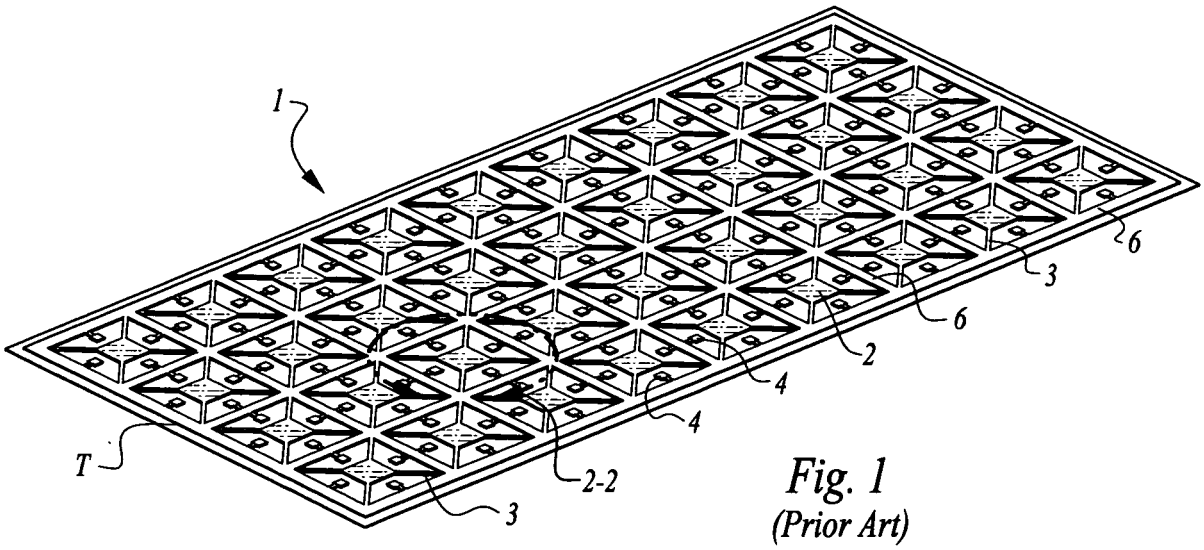

Fig. 1
(Prior Art)

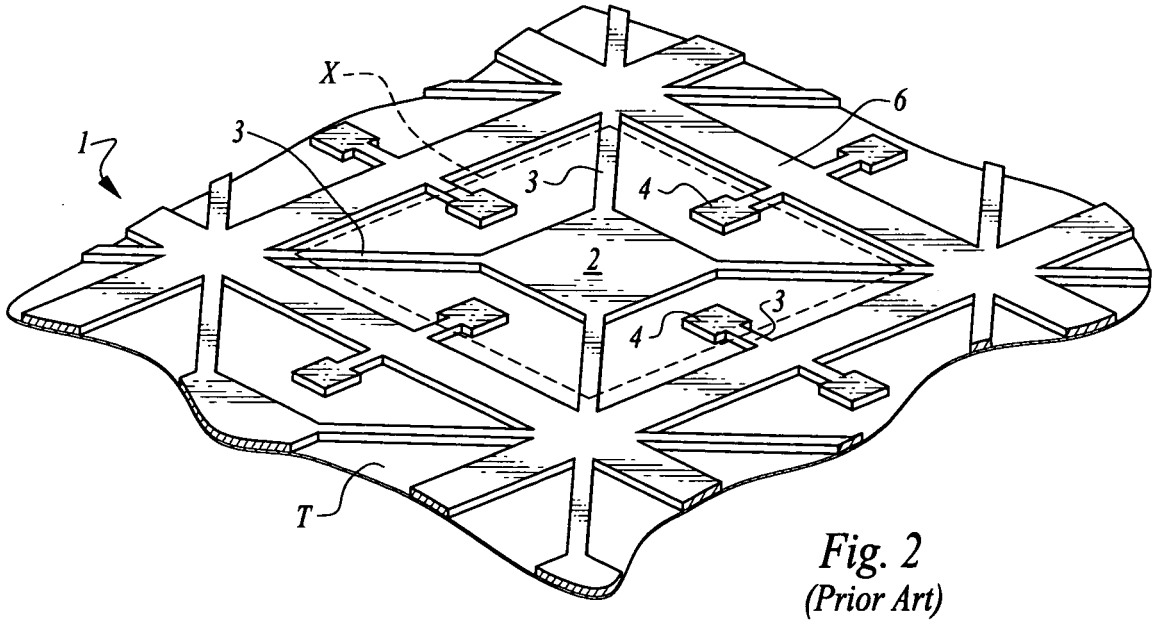

Fig. 2
(Prior Art)

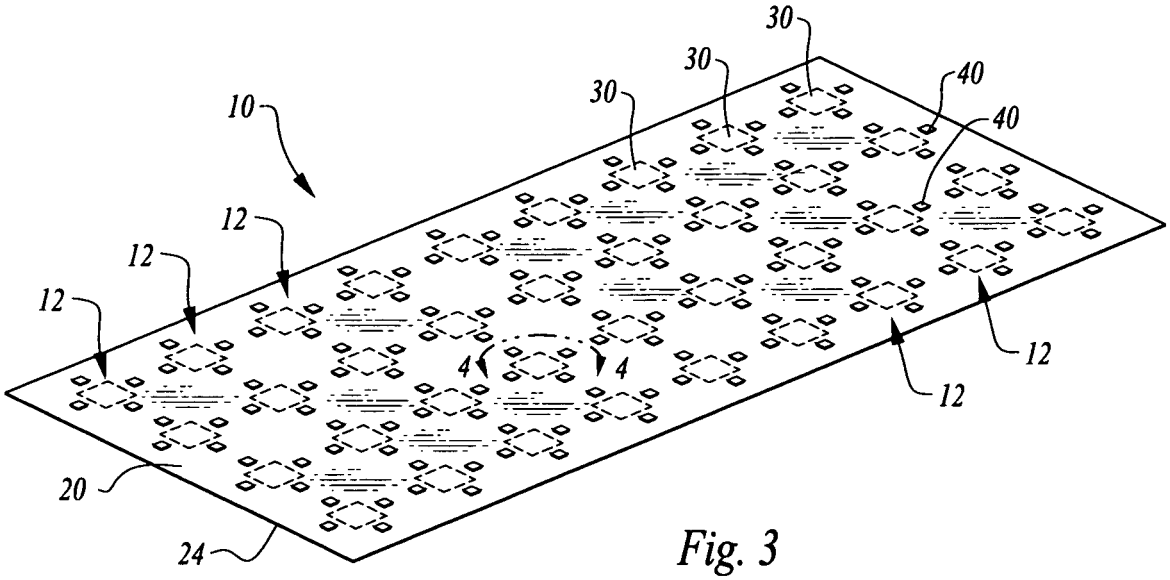
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Fig. 3

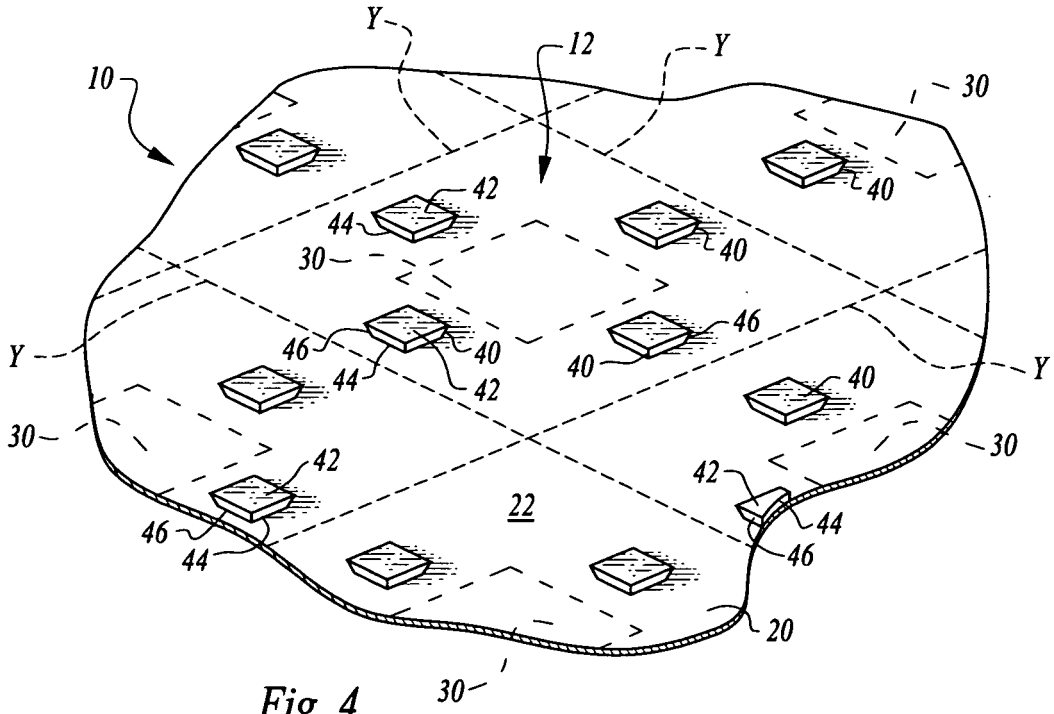
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Fig. 4

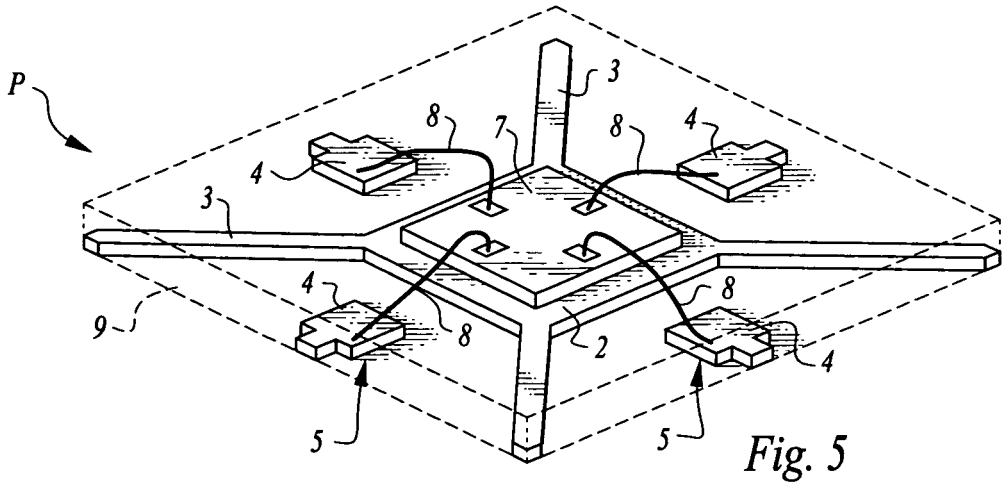

Fig. 5
(Prior Art)

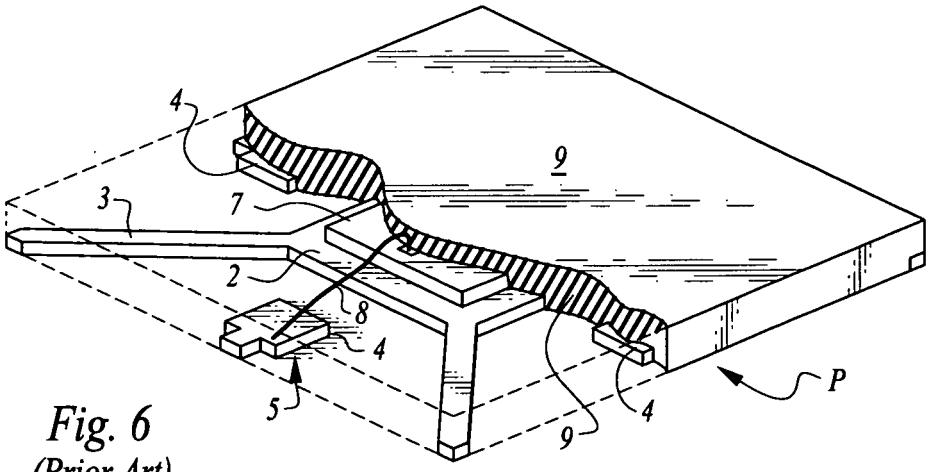

Fig. 6
(Prior Art)

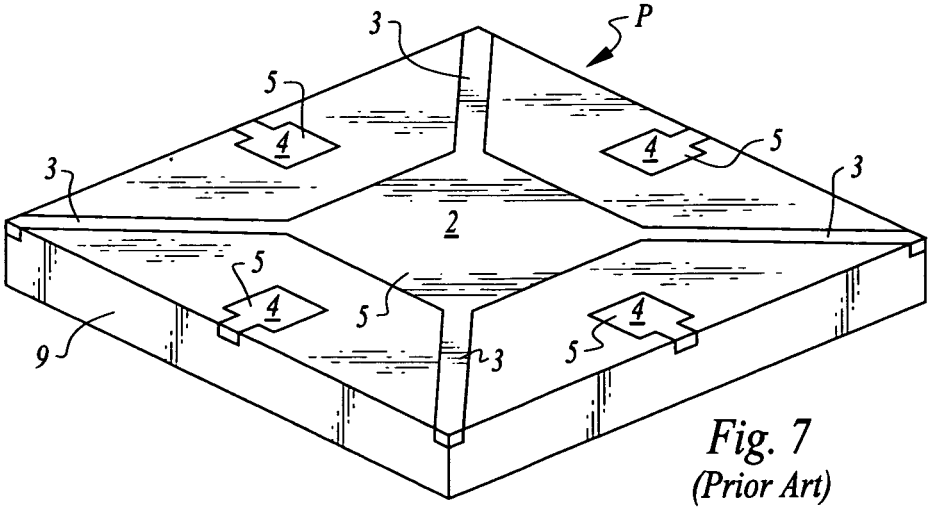

Fig. 7
(Prior Art)

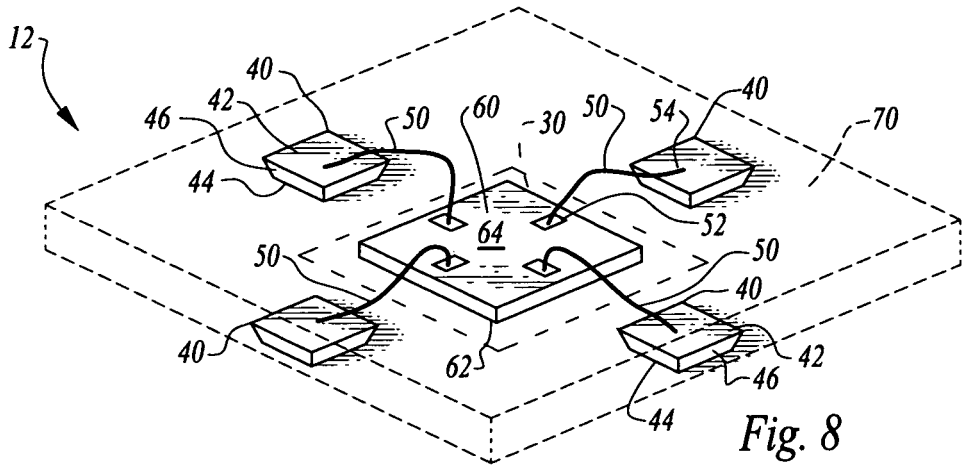

Fig. 8

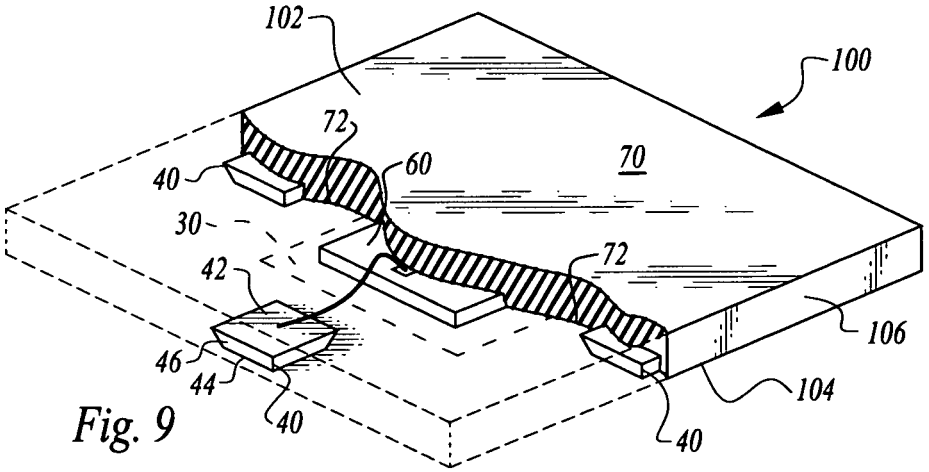

Fig. 9

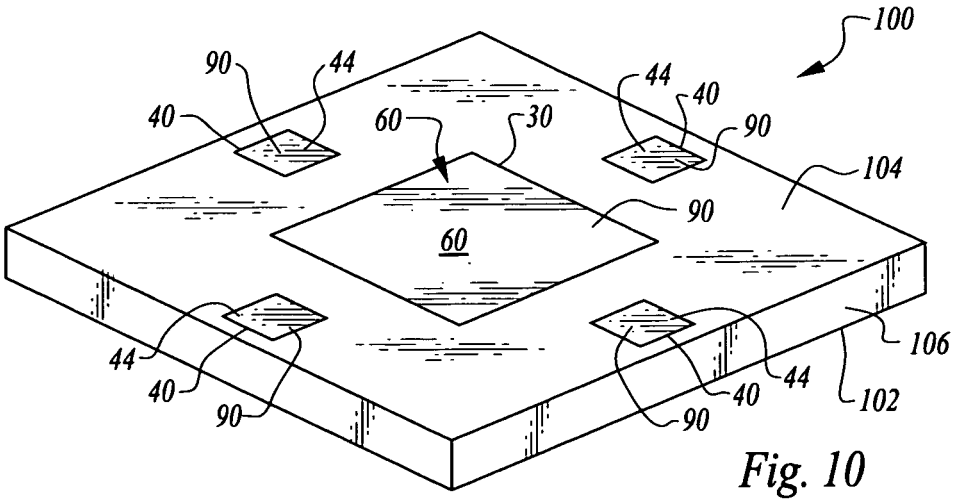

Fig. 10

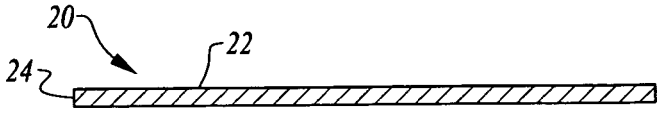

Fig. 11

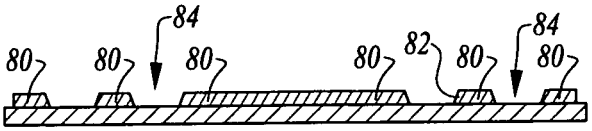

Fig. 12

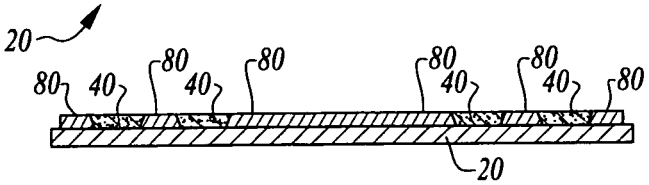

Fig. 13

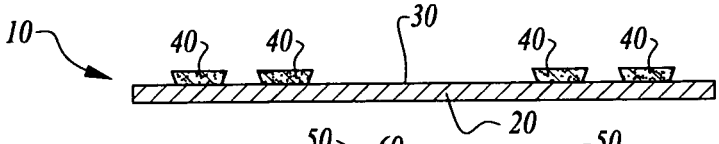

Fig. 14

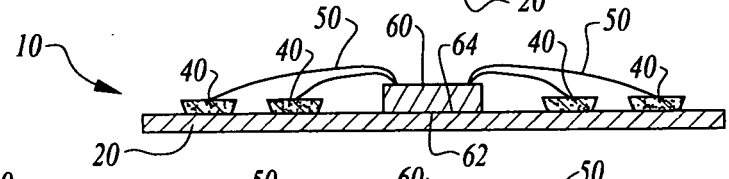

Fig. 15

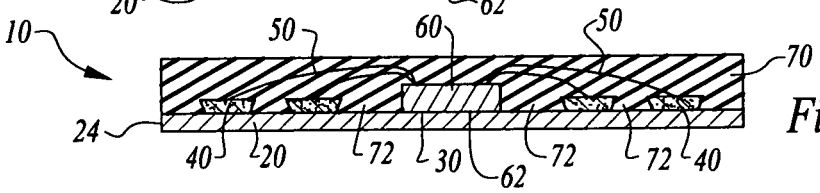

Fig. 16

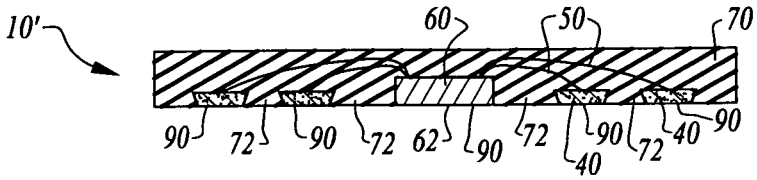

Fig. 17

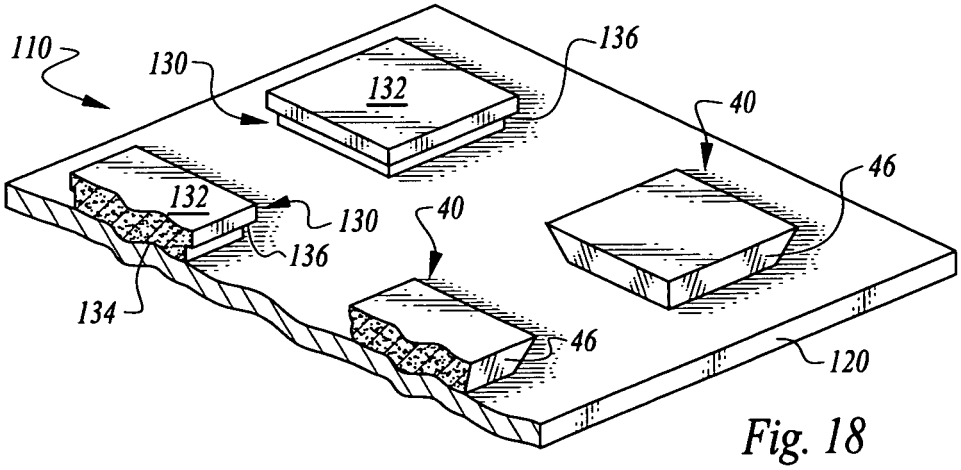

Fig. 18