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(12) United States Design Patent

Iida et al.

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(54) **ARM FOR WAFER TRANSPORTATION FOR MANUFACTURING SEMICONDUCTOR**

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(*) Notice: This patent is subject to a terminal disclaimer.

(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; 118/500, 725, 728, 729; 294/103.1; 414/217, 222.01, 416.03, 414/941
See application file for complete search history.

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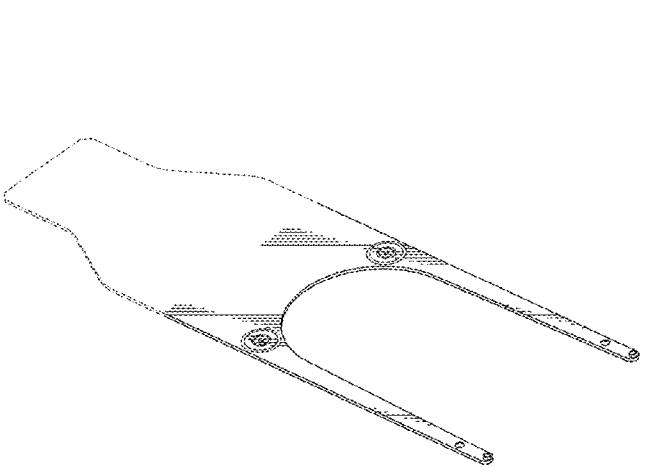
(57) **CLAIM**

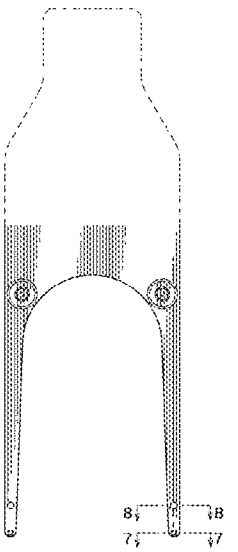
The ornamental design for arm for wafer transportation for manufacturing semiconductor, as shown and described.

DESCRIPTION

FIG. **1** is perspective view of an arm for wafer transportation for manufacturing semiconductor showing our new design;
FIG. **2** is a top plan view thereof;
FIG. **3** is a bottom plan view thereof;
FIG. **4** is a front view thereof;
FIG. **5** is a rear view thereof;
FIG. **6** is a left side view thereof, the right side view being a mirror image;
FIG. **7** is an enlarged sectional view taken along line **7-7** of FIG. **2**; and,
FIG. **8** is an enlarged sectional view taken along line **8-8** of FIG. **2**.
The broken lines shown in the drawings represent portions of the arm for wafer transportation for manufacturing semiconductor that form no part of the claimed design.

1 Claim, 5 Drawing Sheets





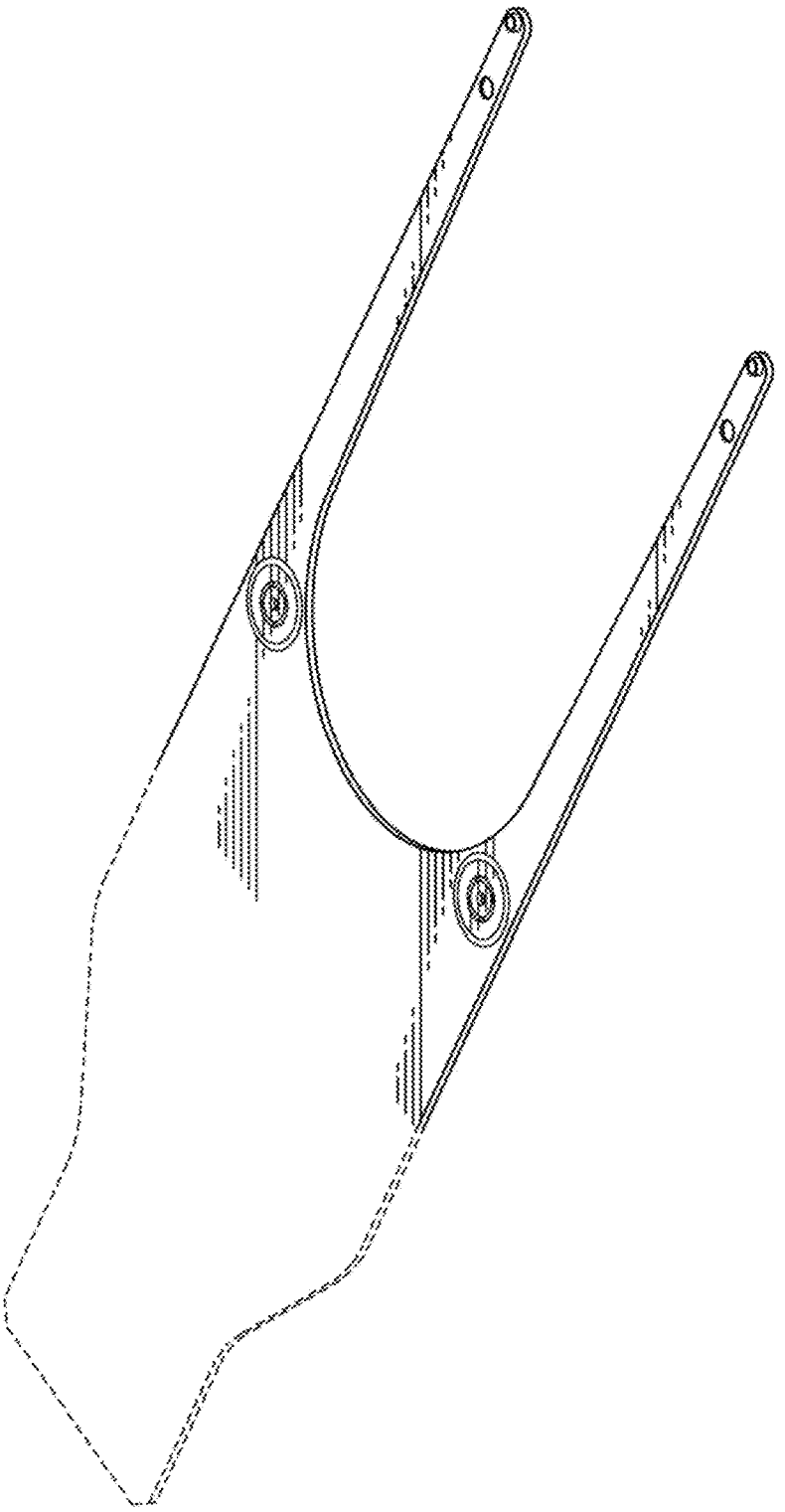


FIG. 1

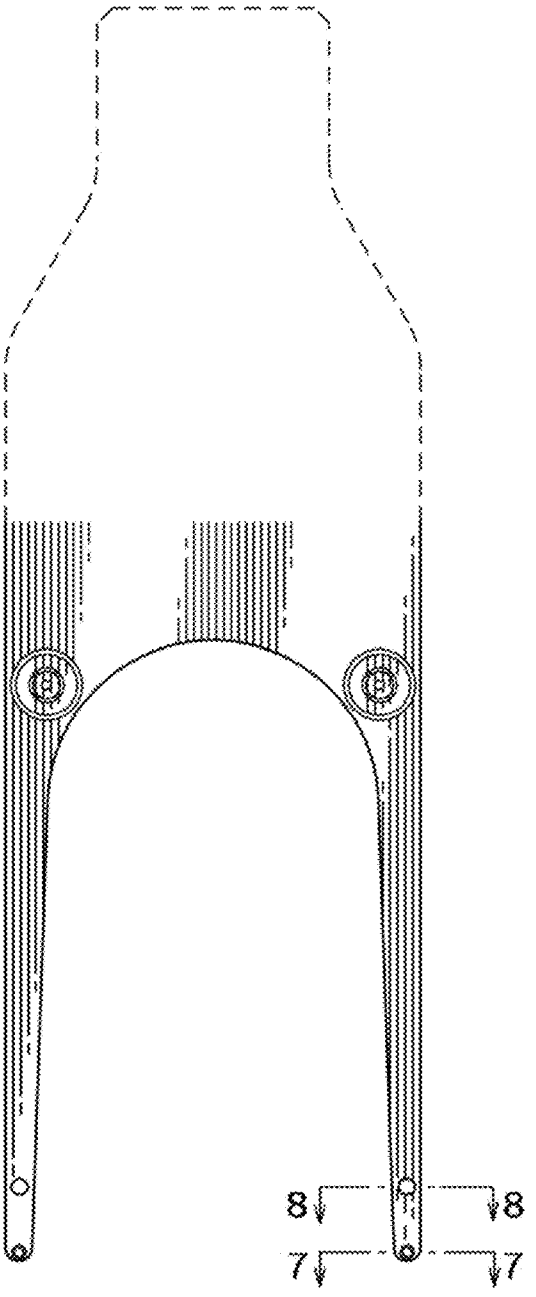


FIG. 2

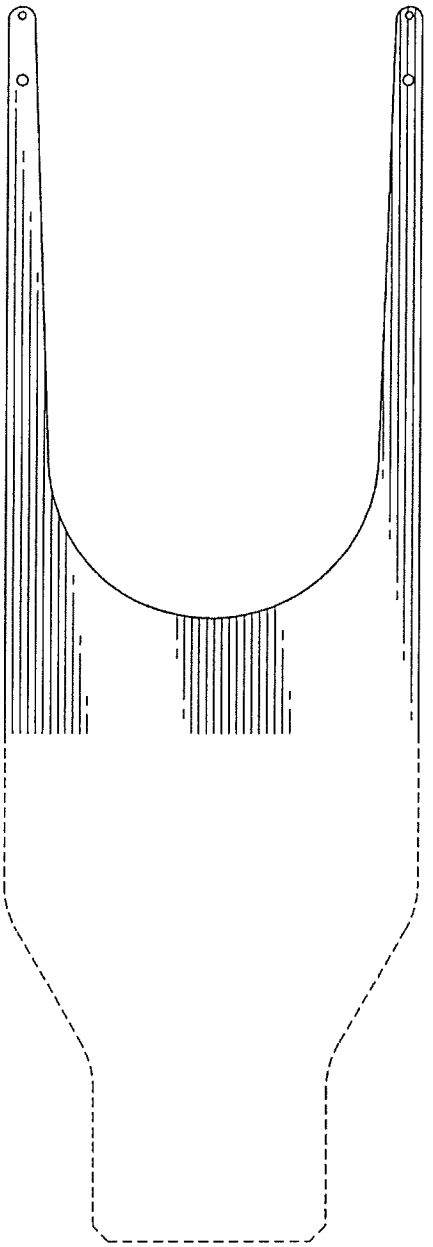


FIG. 3

FIG. 4

FIG. 5

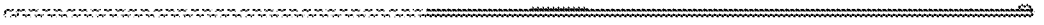


FIG. 6

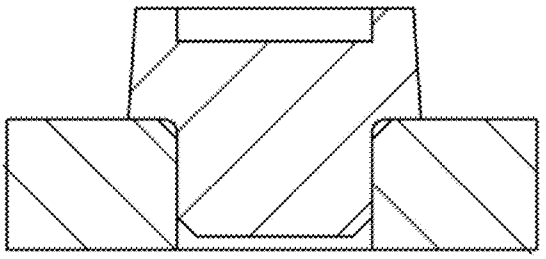


FIG. 7

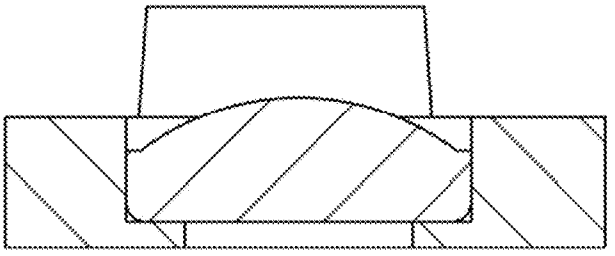


FIG. 8