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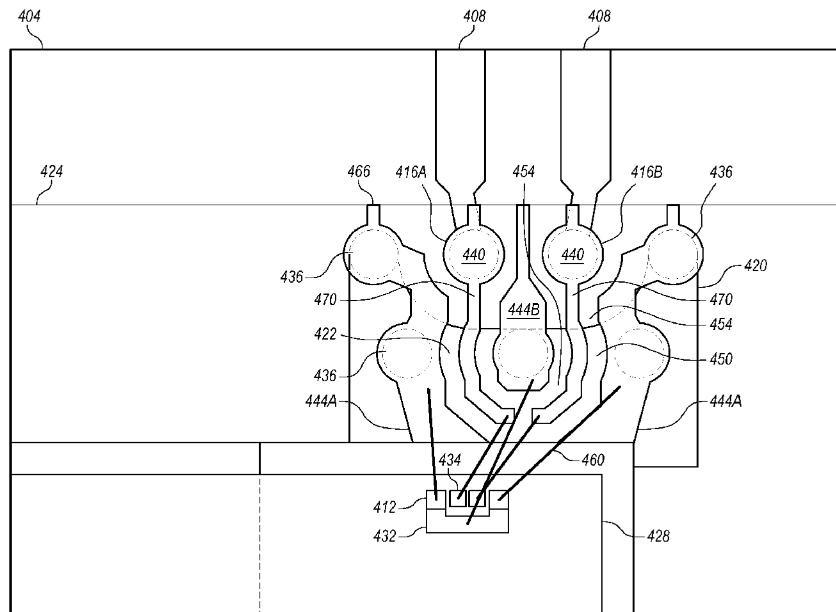

FIG. 4

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(57) Abstract: A circuit board and package assembly electrically connecting a die to a circuit board. The circuit board has signal paths terminating in a signal pad located on an insulating layer. The circuit board also includes a ground pad on the insulating layer that has a concave shaped side forming a recess, the with a signal pad at least partially within the recess. A package has package ground pads aligned with the circuit board ground pads and package signal pads aligned with circuit board signal pads. The package ground pads extend through the package to connect to package ground paths, which extend toward the die. The package signal pads extend through the package to connect to package signal paths and the package signal paths extend toward the die, maintaining a consistent distance from the package ground paths. Multiple-tier bond wires connect the package bond locations to the die bond pads.

[Continued on next page]

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ELECTRICAL INTERFACE FOR PRINTED CIRCUIT BOARD, PACKAGE AND DIE

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1. Field of the Invention.

[0001] The innovation relates to electrical connections between a printed circuit boards and a die and in particular to a novel layout for a printed circuit board to lead frame to
10 die interface.

2. Related Art.

[0002] Modern electronic circuits are contained on a die which is typically formed from a silicon wafer, but other materials or configuration are possible. The electronic circuits on the die perform the signal processing or other operations on the electrical signals as
15 is understood in the art.

[0003] The die is typically contained within a package. The package surrounds the die and is formed from an insulating plastic, resin, or epoxy material. One or more pins extends outward from the package and the pins may be located on the sides or periphery of the package or on the bottom. An electrical connection must be made between the
20 die and the pins of the package so that an electrical signal may be presented to the die and received from the die at the exterior of the package (or, presented to the package and received from the package at the die).

[0004] Supporting the package is a circuit board, which are common in the art. The circuit board is typically a multilayer structure of alternating insulating and conductive layers. The pins from the package connect to electrical conductors in the circuit board. The circuit board is then built to an electrical device, such as but not limited to 5 communication equipment, computer devices, mobile communication devices, or any number of other devices that utilize electronic circuits.

[0005] One challenge and limiting factor to the advancement of circuit operation and data rates is the interface between the circuit board and the die. The path between the circuit board and the die can affect overall performance and be the limiting factor to 10 performance.

[0006] The need was to create a low cost wire bonded package to achieve comparable electrical performance to a chip-scale package (CSP). While CSP has the advantage of not requiring bond wires which can impact and limit performance, CSP can suffer from other drawbacks – namely excess capacitive loading and hence system performance 15 impairment. The issue with low cost wire-bonded packages (QFN or other technologies that use bond wires) is that it is difficult to achieve proper differential-mode and common-mode impedances in order to obtain desirable device-level return losses. The wire bonds also create bandwidth limitations that affect signal transmission, for example, rise/fall time and inter-symbol interference (ISI) jitter. In the design disclosed 20 herein the bandwidth for the prior art configuration was limited in range from 20 GHz to 48 GHz depending on the application.

[0007] Prior solutions to overcome the drawbacks of the prior art typically optimize each segment individually and simply utilize known-configurations. The prior art does not address the interrelation between segments and does not account for modal transmission or propagation characteristics.

5 [0008] Figure 1 illustrates an exemplary prior art conductor layout within a package for a circuit board to die interface. As shown, a die 104 is presented and asserted to include one or more electronic circuits (not shown). Around the die 104 is a package 120 (shown in cut away to aid in understanding). The package 120 includes conductive areas 116 and 124, namely ground node 116 and signal paths 124. The ground nodes 10 electrically connect to the die 104 through one or more bond wires 108. The signal paths electrically connect to the die 104 through one or more bond wires 110. Also part of the package are ground pad 138 and signal path pad 130A, 130B. Through these pads 138, 130A, 130B in connection with one or more vias and conductive traces of the circuit board, the die electrically connects to the circuit board.

15 [0009] This prior art configuration shown in Figure 1 suffers from the drawbacks mentioned above including poor return paths to ground, inductive and capacitive coupling, limited bandwidth performance, phase distortion, and other performance limiting drawbacks. An additional drawback with prior art designs is that each segment is evaluated alone which leads to performance characteristics that neglect the overall 20 collective performance behavior under all operating circumstances.

SUMMARY

[0010] To overcome the drawbacks of the prior art and provide additional benefits, an assembly is disclosed that comprises an arrangement of insulating material and conductive material configured to establish an electrical connection between a circuit board and a die. The disclosed designs were created to provide a cost effective manufacturable design that eliminates or minimizes differential-mode and common-mode mismatches along the transmission path made up of 1) die bond pads, 2) bond wires, 3) lead frame bond pads, 4) lead frame, 5) lead frame-to-pin transition, 6) pin-to-PCB transition, and 7) PCB transmission line.

[0011] In one embodiment, the assembly comprises a circuit board, a package and a die. The circuit board includes a circuit board conductive layer serving and configured as a ground plane, a circuit board insulating layer on the conductive layer, one or more ground vias electrically connected to the circuit board conductive layer, one or more signal solder pads on the insulating layer, one or more signal transmission lines formed from conductive material on the insulating layer such that the one or more signal transmission lines terminate at the one or more signal solder pads, and a circuit board ground pad electrically connected to two or more ground vias such that the two or more ground vias are electrically connected to the circuit board conductive layer. The ground pad has a concave shaped edge facing the one or more signal solder pads.

[0012] The package comprises an insulating material and conductive material. The package comprises two or more conductors exposed on a package exterior including at least one conductor comprising an exterior ground conductor and at least one conductor

comprising an exterior signal conductor such that the exterior signal conductor is configured to electrically connect to at least one signal solder pad on the circuit board and the exterior ground conductor is configured to electrically connect to at least one ground via on the circuit board.

5 [0013] The package may further comprise a right hand side ground path electrically connected to the circuit board ground pad, a left hand side ground path electrically connected to the circuit board ground pad, a center ground path electrically connected to the circuit board ground pad, a first signal path between the right hand side ground path and the center ground path such that the first signal path connects at a first end to 10 at least one signal transmission line of the circuit board and connects at a second end to a first bond wire, and a second signal path between the left hand side ground path and the center ground path such that the second signal path connected at a first end to at least one signal transmission line of the circuit board and connected at a second end to a second bond wire such that the first and second bond wires electrically connect to a 15 die.

[0014] In one embodiment, a generally uniform distance is maintained between the left hand side ground path and the first signal path and a generally uniform distance is maintained between the right hand side ground path and the second signal path. In addition, a generally uniform distance may be maintained between the first signal path 20 and the center ground path and a generally uniform distance may be maintained between the second signal path and the center ground path.

[0015] In this assembly, the first signal path and the second signal path may be traces having a uniform width. In addition, the ground bond wires electrically connect the die ground to the right hand side ground path, left hand side ground path, and center ground path. In one embodiment there are five ground vias extending upward through the circuit board and in alignment with exterior ground conductors exposed on a package exterior.

[0016] It is further contemplated that the one or more signal solder pads of the circuit board may comprise a first signal solder pad and second signal solder pad, the first signal solder pad electrically connects to the first signal path of the package and the second signal solder pad electrically connects to the second signal path of the package.

[0017] Disclosed herein is an assembly comprising an arrangement of insulating material and conductive material configured to establish an electrical connection between a circuit board and a die. In this embodiment, the assembly comprises a circuit board ground layer formed of conducting material and a circuit board insulating layer on the conductive layer. At least one signal transmission line terminating at and electrically connects to the at least one signal solder pad on the circuit board insulating layer. A circuit board ground pad electrically connects to the circuit board ground layer such that the ground pad has a concave shaped edge facing at least one signal solder pad. Also part of this embodiment is a package comprising insulating material and conductive material such that the package includes two or more package ground pads exposed on a package exterior electrically connected to the circuit board ground pad and one or more package signal pads exposed on a package exterior electrically

connected to the signal solder pad. Within the package, there is at least a right hand side ground path electrically connected to at least one package ground pad and at least a left hand side ground path electrically connected to at least one package ground pad. A package signal path is between the right hand side ground path and the left hand side
5 ground path such that the package signal path electrically connects at a first end to at least one package signal pad and electrically connects at a second end to a signal bond wire.

[0018] One embodiment further comprises a second package signal path within the package and a center ground path electrically connected to the right hand side ground
10 path and the left hand side ground path such that the center ground path is located between the package signal path and second package signal path. The center ground path may have a bond wire attachment point to which a bond wire attaches, the right hand side ground path may have a bond wire attachment point to which a bond wire attaches, and the left hand side ground path may have a bond wire attachment point to
15 which a bond wire attaches. In this embodiment, the distance between the center ground path and the package signal is generally uniform and a distance between the center ground path and the second package signal path may be generally uniform.

[0019] The two or more package ground pads on the exterior of the package are aligned above the circuit board ground pad such that the concave shaped edge faces at least one
20 signal solder pad. In one embodiment, the package signal path and second package signal path have a generally uniform width along at least fifty percent of its length.

[0020] Also disclosed herein is a circuit board and package assembly configured to electrically connect a die to a circuit board. In this embodiment the assembly comprises a circuit board signal path on an insulating layer of the circuit board terminating in a signal pad and a ground pad on the insulating layer of the circuit board. The circuit board ground pad has a concave shaped side that forms a recess such that at least one signal pad is at least partially within the recess formed by the concave shaped side. A package is part of the assembly and is located on the circuit board such that two or more package ground pads align along the concave shaped side of the circuit board ground pad and at least one package signal pad is at least partially within the recess formed by the concave shaped side of the ground pad. The two or more package ground pads extend upward into the package to electrically connect to package ground paths and the at least one package signal pad extends upward into the package to electrically connect to a package signal path.

[0021] In one embodiment, the at least one package signal path extends from the package signal pad toward the die and has a generally constant width. The two or more package ground pads may consist of five package ground pads, all of which are contained within an area defined by the circuit board ground pad and electrically connect to the circuit board ground pad to form a ground return path of controlled characteristics. It is also contemplated that the assembly may include two circuit board signal paths, each connecting to a signal pad and also include two package signal pads which connect to a first package signal path and a second package signal path, both of the first package signal path and a second package signal path extend toward the die

and a center ground pad on the circuit board which electrically connects to a center package ground pad, which electrically connects to a package center ground path.

[0022] In this embodiment the package center ground path is located between the first package signal path and a second package signal path. Furthermore, the package ground paths may comprise a first package ground path and a second package ground path, both of which extend toward the die, such that the first package signal path is between the first package ground path and the package center ground path and the second package signal path is between the second package ground path and the package center ground path. It is further contemplated that a distance between the first package signal path and the first package ground path is generally consistent as the first package signal path extends toward the die and a distance between the second package signal path and the second package ground path is generally consistent as the second package signal path extends toward the die.

[0023] Other systems, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. In the figures, like reference numerals designate corresponding parts throughout the different views.

5 [0025] Figure 1 is a perspective view of a prior art package to die interface.

[0026] Figure 2A is a plot of signal magnitude and a plot of return loss in differential mode in a prior art system at various frequencies.

[0027] Figure 2B is a plot of signal magnitude and a plot of return loss in differential mode in a system embodied with the disclosed innovation at various frequencies.

10 [0028] Figure 3A is a plot of return loss in common mode in a prior art system operating at various frequencies.

[0029] Figure 3B is a plot of signal magnitude and a plot of return loss in common mode in a system embodied with the disclosed innovation operating at various frequencies.

15 [0030] Figure 4 a top plan view of the circuit board, package, and die with associated electrical connectivity.

[0031] Figure 5 is a side plan cut-away view of the circuit board, package, and die with associated electrical connectivity.

[0032] Figure 6 is a perspective cut-away view of the circuit board, package, and die with associated electrical connectivity.

[0033] Figure 7A illustrates a top view of a layer of the circuit board formed of conductive material.

5 [0034] Figure 7B illustrates a top view of an additional layer of the circuit board formed of insulating material.

[0035] Figure 7C illustrates a top view of an additional layer of the circuit board formed of conductive material.

[0036] Figure 7D illustrates a bottom view of a layer of the package formed of
10 conductive material.

[0037] Figure 7E illustrates a bottom view of a layer of the package formed of insulating and conductive material.

[0038] Figure 7F illustrates a top view of an additional layer of the package formed of conductive material.

15 [0039] Figure 7G illustrates a view of a layer of the package and die formed of insulating material.

[0040] Figure 7H illustrates a top view of a layer of the package and die formed of conductive material.

DETAILED DESCRIPTION

[0041] Figure 2A is a plot of signal magnitude and a plot of return loss in differential mode in a prior art system at various frequencies. As shown in Figure 2A, in the graph 200 the vertical axis 208 represents dB of signal loss while the horizontal axis 212 represents frequency in GHz. On the vertical axis a -3 dB point 216 is a relevant point for this discussion and may be used to define or compare system performance. A signal plot 202 is shown as plot 220. This signal plot is -3 dB down in signal magnitude at about 40 GHz of signal frequency 224. This is typical of prior art system performance.

[0042] Also shown in Figure 2A is return loss plots 230A, 230B for differential mode operation. One plot is referenced looking into or toward the die from the circuit board while another of the plots is looking toward or into the circuit board from the die. As can be viewed from the return loss plots 230A, 230B for differential mode operation, the prior art systems suffer from significant return loss and the return loss behavior is inconsistent over the illustrated frequency range.

[0043] Figure 2B is a plot of signal magnitude and a plot of return loss in differential mode in a system embodied with the disclosed innovation at various frequencies. As compared to Figure 2A, similar elements are identified with similar reference numbers. As shown in Figure 2B, in the graph 200 the vertical axis 208 represents dB of signal loss while the horizontal axis 212 represents frequency in GHz. In contrast to Figure 2A, the plot of signal magnitude 258 is significantly better such that the -3 dB transition 216 [in signal magnitude is at or near 100 GHz 250. This is a significant improvement in performance and enables operation at significantly higher frequencies.

[0044] Also shown in Figure 2B is return loss plots 254A, 254B. One plot is referenced looking into or toward the die from the circuit board while another of the plots is looking from die into or toward package. As can be viewed from the return loss plots 230A, 230B, the system incorporating the disclosed innovation greatly improves performance
5 in relation to return loss compared to the prior art system plots shown in Figure 2A. The return loss plot 254A, 254B are better over the shown frequencies and do not suffer from significant variation.

[0045] Figure 3A is a plot of return loss in common mode in a prior art system operating at various frequencies. As shown in Figure 3A, in the graph 300 the vertical axis 308
10 represents dB of signal loss while the horizontal axis 312 represents frequency in GHz. Also shown in Figure 3A is return loss plots 320, 324 for common mode operation. Plot 320 is referenced looking into or toward the die from the circuit board while plot 324 is looking from the circuit board into or toward die. As can be viewed from the return loss plots 320, 324 for common mode operation, the prior art system suffers from
15 significant return loss and the return loss behavior is inconsistent and include numerous spikes over the illustrated frequency range.

[0046] Figure 3B is a plot of signal magnitude and a plot of return loss in common mode in a system embodied with the disclosed innovation operating at various frequencies. As shown in Figure 3B, in the graph 3020 the vertical axis 308 represents
20 dB of signal loss while the horizontal axis 312 represents frequency in GHz. Also shown in Figure 3B is return loss plots 350, 354 for common mode operation. Plot 350 is referenced looking into or toward the die from the circuit board while plot 354 is

looking from the circuit board into or toward the die. As can be viewed from the return loss plots 350, 354 for common mode operation, the system incorporating the innovation disclosed herein has a significant improvement in return loss and the return loss behavior is more consistent and include fewer spikes over the illustrated frequency range as compared to the prior art plots shown in Figure 3A.

[0047] Figure 4 a top plan view of the circuit board, package, and die with associated electrical connectivity. Figure 5 is a side plan cut-away view of the circuit board, package, and die with associated electrical connectivity. Figure 6 is a perspective cut-away view of the circuit board, package, and die with associated electrical connectivity. Figure 4, 5, and 6 are jointly discussed below to avoid redundancy between elements which are generally similar but shown in different views. In general, Figures 4, 5, and 6 illustrate an electrical interface between a circuit board 404, package 424, and die 428. This interface is a built-up three dimensional arrangement of insulating elements and conductive elements arranged to electrically interface the circuit board 404 to the die 428.

[0048] As is commonly understood, a circuit board 404, which may be a multi-layer printed circuit board, is composed of various conductive and insulating layers. In this embodiment, a lower conductive layer 504 serves as a base layer. Above the lower conductive layer 504 is an insulating layer 508. In turn, above insulating layer 508 is another conductive layer 512 which when combined with selective conductor location control and insulating material location control may be made to establish one or more signal transmission line 408 on the circuit board 404 and a ground plane 420. As shown

in Figure 6, the signal transmission line 408 are part of the circuit board 404 and terminate at a signal via 440. The signal transmission line 408 may operate in differential mode, common mode, or both, subject to other elements including the die and the components which connected to the circuit board 404.

5 [0049] The signal transmission line 408 connects to the vias 440 which extended through the circuit board 404 to present a signal solder pad at the top of the circuit board. Subsequent figures illustrates the location of the signal solder pads in relation to the package. In this example embodiment the signal solder pads may be for use with a traditional package design with pins extending from the periphery of the package or 10 arranged in an array for a flip chip configuration. Also part of the circuit board 404 is a ground path or ground plane that connects to ground vias 436. The ground vias present an electrical connection from a ground path or ground plane from the circuit board to the package. As with the signal solder pads for the signal path, the ground connects are also presented to the upper level of the circuit board for connection to the 15 package 428.

[0050] Turning now to the package 424, several electrical connections are provided to electrically connect the package to the die 428. In general, there is a signal path and a ground path. With regard to the signal path, the circuit board transmission lines 408 connect to the package through conductive vias 440 and then to package signal paths 20 470. Pads electrically connect the vias 440 to the package signal paths 470. The package signal paths 470 extend toward the die 428 as shown and terminate near the die 428 and within connection distance to the die.

[0051] In addition to the signal paths 470, ground nodes are provided which include outer ground node (paths) 444A, located on each side of the signal paths 470 as shown, and an inner ground node (path) 444B located between the signal paths 470. Both the ground nodes 444A, 444B, and the signal paths 470 may comprise any type of conductive material. The ground nodes 444A connect to outer ground vias 436 and solder pads (not shown) which extend through and upward from the circuit board 404. A center (inner) ground node 444B connects to an electrically conductive via 438, which in turn connects to the lower ground plane 420.

[0052] The lower ground plane 420 that extends outward from each via 436, 438 to form a conductive ground plane as shown. The ground plane includes a concave arc 422 that opposes the two signal vias 440. The concave side 420 of the ground extends to each side of the signal vias 440. One or more ground vias 436 are located near the outer most portions of the ends of the concave arc.

[0053] Bond wire contact points are located generally near the die to which bond wires 460 connect to the package signal paths 470. The opposing end of the bond wires 460 connect to bond wire pads on the die 428. Although labeled with a single reference number 460, the certain bond wires conduct the signal while others conduct or function as ground conductors. Bond wires 460 which connect to the signal path on the package 424 and die 428 are signal bond wires while bond wires which connect to ground paths on the package and die are ground bond wires. Additional details regarding the bond wire 460 contact points are provided below.

[0054] Between the outer ground nodes 444A and the signal path 470 is a space or void comprised of insulating material. An inner insulating section 454 is placed between inner ground node 444B and the signal paths 470. An outer insulating section 450 is provided between the signal path 470 and the outer ground nodes 444A. As shown in this embodiment the arrangement is symmetric such that both sides of the inner ground node are mirrored images of the other. In other embodiments the arrangement may be non-symmetric. Further and as discussed herein, the performance improvements are based at least in part on the configuration shown but deviations may occur from this configuration without departing from the claims that follow. Deviations in configuration shape and layout which gain the benefits described herein are contemplated and should be considered as covered directly or by the doctrine of equivalents.

[0055] In this example embodiment, which was configured for simulation and manufacturing, the nature of the manufacturing process leaves tails 466 extending from the features of the design and in particular the ground nodes 444A, 444B and the package signal paths 470. Element 416B is a bond pad or connection pad between the vias 440 that extends upward from the lower levels of the package 424 and the signal transmission lines 408.

[0056] Figure 5 and Figure 6 also illustrate the multiple tier bonding arrangement for the ground areas. As shown in Figure 5, the top most bond wires 460 connect to a ground area, which in turn electrically connects to a lower tier ground area through the conductive vias 436, 440. One or more lower tiers may be connected in this manner.

This is also shown in Figure 6 such that the upper ground areas 444A, 444B connect to lower ground tiers through vias, such as vias 436. Using two or more tiers with bonding to lower ground layers provides the benefit of flexibility to assign and arrange conductors to facilitate management of modal impedance characteristics within the
5 constraints of technology and manufacturing design rules as well as for specific product needs.

[0057] The present design has several advantages over prior art systems. Present design is optimized and designed to meet specification for both common mode and differential mode behavior. Thus, the modal impedances are both optimized. As to
10 the modality designed into the system, the design disclosed improves greatly upon prior art designs by better balancing modal impedances to achieve the lowest possible impedance variation for each of the major modes – differential and common modes Achieving the lowest possible impedance variation manifests as improved bandwidth, improved return loss, and reduced signal distortion due to resonances caused by
15 interaction of mismatches.

[0058] Figures 7A-7H illustrates the various layers of an exemplary embodiment of the circuit board, package, and die for the configuration described herein. This is but on one possible layer stack up. Figure 7A illustrates a top view of a layer of the circuit board formed of conductive material. The area shown generally is a portion of the
20 circuit board 700 which is a conductive layer 704 covering the circuit board while via locations 708 are shown as circles or other conductive access areas where the vias are located. The conductive layer 704 forms an RF ground layer. The circuit board 700

may be any type circuit board, such as a layered circuit board, printed circuit board, or other type of support structure. That circuit board 700 may be of any shape and the view shown in Figure 7A is just a section of the overall board. The layer shown in Figure 7A may be considered a base layer, such that the other layers or elements shown 5 in Figure 7B-7H reside on top of the layer shown in Figure 7A.

[0059] Figure 7B illustrates a top view of an additional layer of the circuit board formed of insulating material. This insulating layer 712 is on top of the conductive layer 704 shown in Figure 7A. Shown through the insulating layer 712 are the conductive via locations 708, which electrically connect to the conductive layer below and conductive 10 layer above.

[0060] Figure 7C illustrates a top view of an additional layer of the circuit board formed of conductive material. This layer includes the upper ground plane 716 that electrically connects to the via locations 708, which in turn connect to the conductive ground plane 704 shown in Figure 7A. This layer also includes the signal transmission lines 720 15 which electrically connect to solder pads 722. The signal transmission lines 720 may be micro-strip lines. One skilled in the art may contemplate that if the signal transmission lines 720 were sandwiched between adjacent (above and below) ground planes, then stripline transmission lines would result. While the figures and illustrated embodiment do not detail this case, the case should be contemplated included and 20 considered as covered by subsequent claims either directly or by the doctrine of equivalents. Returning to Figure 7C, the features described reside atop the insulating layer 712 of the circuit board 700. The upper ground plan 716 may be referred to as a

metal flood. As shown, the edge that faces or opposes the transmission lines solder pads 722 is concave to at least partially curve around the solder pads. In this embodiment there are seven vias that are part of the ground path but in other embodiments greater or fewer vias may be used. In this embodiment the ground vias
5 708 are located and spaced in a uniform manner in relation to the signal solder pads. Analogous to the description of multi-tiered bond wire use and arrangement, the placement of the ground pads and vias has the benefit of allowing management of modal impedance characteristics within the constraints of technology and manufacturing design rules as well as for specific product needs. It should be
10 understood that the locations, dimensions, and quantity of connections may differ in other embodiments. However, all possible variations should be covered within the scope of claims and in particular following the pattern of forming a generally concave ground shape opposing the signals. Heat dissipation vias are used for heat dissipation from the die to the package to the circuit board and are not shown in this figure. The
15 via locations are not limited to the locations shown.

[0061] Figure 7D illustrates a bottom view of a layer of the package formed of conductive material. As shown, the package 730 has a bottom which is comprise primarily of insulating material 736 such as an epoxy overmold. The package pins 734 protrude from the package 730 as shown. The pin 734 may comprise solder bumps,
20 pins, solder balls, or any other conductive feature on the package. Figure 7E illustrates a bottom view of a layer of the package formed of insulating and conductive material. This view is generally similar to Figure 7D, but the package edge 738 is shown imposed on top of the circuit board 712. In the present embodiment an array of pins are

illustrated. In other embodiments the pins may reside along the package edge 738 in what is commonly known as a peripheral array of pins.

[0062] Figure 7F illustrates a top view of an additional layer of the package formed of conductive material. This layer is one layer up within the package assembly and the sections shown are conductive layers. The package pins 734 of the package electrically connect to the conductors 746, 744 which are established as conductive areas of this layer. The package pins 1-5 are all part of a common ground which includes package ground conductive areas 740 and conductive wings 746. The package ground conductive areas 740 electrically connects all the package grounds together. The signal package pins 734 are established within the package as shown such there is a signal path 744 which extends from the package pins 734 as shown. The signal pins may carry signals in differential mode or common mode. There is a uniform distance between the ground wings 746 and the signal paths 744. Between the signal paths 744 is a ground pin (3) with associated ground conductor established as shown. The ground pin (3) and the associated ground area that is located at a uniform distance from the signal paths 744 provides an important return path to ground for the signals. Presence of this ground allows adjustment of electro-magnetic coupling between the two signal paths 744 and hence allows adjustment of modal impedance within the package planar signal routing region. A uniform distance is maintained between the ground pin conductor and the signal paths 744. Also shown in Figure 7F are the bond wire contact points 750. The bond wires (not shown) connect the package 730 to the die (not shown). Certain bond wires will electrically connect to the signal conductors 744 to the die while other bond wires will electrically connect the ground path 740, 746, and package pin (3) to the die.

As a benefit to this arrangement, the size and distance of the arrangement shown may ratio up or down in size to accommodate other sizes of dies and/or other package technology design and manufacturing rules. The scaling may occur left to right or top to bottom and is contemplated that the scaling would also occur in the Z-axis.

5 [0063] Figure 7G illustrates a view of a layer of the package and die. In this view the die 766 is on the package 730. Figure 7H illustrates a top view of the die with die bond pad 768, 770. The bond pads 770 are for the signal path and the bond pads 768 connect the die to the ground conductor of the package. The dots at the center of each bond pad 768, 770 are bond wire contact points.

10 [0064] While various embodiments of the invention have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations are possible that are within the scope of this invention. In addition, the various features, elements, and embodiments described herein may be claimed or combined in any combination or arrangement.

15

CLAIMS

What is claimed is:

1. An assembly comprising an arrangement of insulating material and conductive material configured to establish an electrical connection between a circuit board to a die, the assembly comprising:

a circuit board comprising:

a circuit board conductive layer serving configured as a ground plane;

an circuit board insulating layer on the conductive layer;

one or more ground vias electrically connected to the circuit board conductive layer;

one or more signal solder pads on the insulating layer;

one or more signal transmission lines formed from conductive material on the insulating layer, the one or more signal transmission lines terminating at the one or more signal solder pads;

a circuit board ground pad electrically connected to two or more ground vias, the two or more ground vias electrically connected to the circuit board conductive layer, the ground pad having a generally concave shaped edge facing the one or more signal solder pads;

a package comprising insulating material and conductive material, the package comprising:

two or more conductors exposed on a package exterior, at least one conductor comprising an exterior ground conductor and at least

one conductor comprising an exterior signal conductor such that the exterior signal conductor is configured to electrically connect to at least one signal solder pad on the circuit board and the exterior ground conductor is configured to electrically connect to at least one ground vias on the circuit board;

2. The assembly of claim 1 further comprising:

a right hand side ground path electrically connected to the circuit board ground pad;

a left hand side ground path electrically connected to the circuit board ground pad;

a center ground path electrically connected to the circuit board ground pad;

a first signal path between the right hand side ground path and the center ground path, the first signal path connected at a first end to at least one signal transmission line of the circuit board and connected at a second end to a first bond wire;

a second signal path between the left hand side ground path and the center ground path, the second signal path connected at a first end to at least one signal transmission line of the circuit board and connected at a second end to a second bond wire, the first and second bond wires electrically connecting to a die.

3. The assembly of claim 2 wherein a generally uniform distance is maintained between the left hand side ground path and the first signal path and a generally uniform distance is maintained between the right hand side ground path and the second signal path.

5

4. The assembly of claim 3 wherein a generally uniform distance is maintained between the first signal path and the center ground path and a generally uniform distance is maintained between the second signal path and the center ground path.

10

5. The assembly of claim 2 wherein the first signal path and the second signal path are traces having a uniform width.

6. The assembly of claim 1 wherein ground bond wires electrically connect the die

15 ground to the right hand side ground path, left hand side ground path, and center ground path.

7. The assembly of claim 1 wherein there are five or more ground vias extending upward through the circuit board and in alignment with exterior ground

20 conductors exposed on a package exterior.

8. The assembly of claim 1 wherein the one or more signal solder pads of the circuit board comprise a first signal solder pad and second signal solder pad, the

first signal solder pad electrically connects to the first signal path of the package and the second signal solder pad electrically connects to the second signal path of the package.

5 9. An assembly comprising an arrangement of insulating material and conductive material configured to establish an electrical connection between a circuit board and a die, the assembly comprising:

a circuit board comprising:

a circuit board ground layer formed of conducting material;

10 an circuit board insulating layer on the conductive layer;

at least one signal transmission line terminating at and electrically connect to at least one signal solder pad on the circuit board insulating layer;

a circuit board ground pad electrically connected to the circuit board ground layer the ground pad having a generally concave shaped edge facing at 15 least one signal solder pads;

a package comprising insulating material and conductive material, the package comprising:

two or more package ground pads exposed on a package exterior electrically connected to the circuit board ground pad;

20 one or more package signal pads exposed on a package exterior electrically connected to the signal solder pad; and

within the package, at least a right hand side ground path electrically connected to at least one package ground pad and left hand side ground path electrically connected to at least one package ground pad;

a package signal path between the right hand side ground path and the
5 left hand side ground path, the package signal path electrically connected at a first end to at least one package signal pad and electrically connected at a second end to signal bond wire.

10. The assembly of claim 9 further comprising a second package signal path within
10 the package and a center ground path electrically connected to the right hand side ground path and the left hand side ground path, the center ground path electrically connected to the right hand side ground path and the left hand side ground path and located between the package signal path and second package signal path.

15

11. The assembly of claim 10 wherein the center ground path has a bond wire attachment point to which a bond wire attaches, the right hand side ground path has a bond wire attachment point to which a bond wire attaches, and the left hand side ground path has a bond wire attachment point to which a bond wire
20 attaches.

12. The assembly of claim 10 wherein a distance between the center ground path and the package signal and is generally uniform and a distance between the center ground path and the second package signal path is generally uniform.

5 13. The assembly of claim 9 wherein the two or more package ground pads on the exterior of the package are aligned above the circuit board ground pad such that the generally concave shaped edge faces at least one signal solder pads.

14. The assembly of claim 9 wherein the package signal path and second package 10 signal path has a generally uniform width along at least fifty percent of its length.

15. A circuit board and package assembly configured to electrically connect a die to a circuit board, the assembly comprising:

15 a circuit board signal path on an insulating layer of the circuit board terminating in a signal pad;

a ground pad on the insulating layer of the circuit board, the circuit board ground pad having a generally concave shaped side that forms a recess such that at least one signal pad is at least partially within the recess formed by 20 the concave shaped side;

a package located on the circuit board such that two or more package ground pad align along the concave shaped side of the circuit board ground pad and at least one package signal pad is at least partially within the recess

formed by the concave shaped side of the ground pad, the two or more package ground pads extending upward into the package to electrically connect to package ground paths and the at least one package signal pad extending upward into the package to electrically connect to a package signal
5 path.

16. The assembly of claim 15 wherein the at least one package signal path extends from the package signal pad toward the die and has a generally constant width.

10 17. The assembly of claim 15 wherein the two or more package ground pads consists of five package ground pads, all of which are contained within an area defined by the circuit board ground pad and electrically connect to the circuit board ground pad to form an RF signal reference and ground return path.

15 18. The assembly of claim 15 wherein the assembly includes two circuit board signal paths, each connecting to a signal pad and two package signal pads which connect to a first package signal path and a second package signal path, both of the first package signal path and a second package signal path extending toward the die; and

20 a center ground pad on the circuit board which electrically connects to a center package ground pad, which electrically connects to a package center ground path, the package center ground path located between the first package signal path and a second package signal path.

19. The assembly of claim 18 wherein the package ground paths comprise a first package ground path and a second package ground path, both of which extend toward the die, such that the first package signal path is between the first package ground path and the package center ground path and the second package signal path is between the second package ground path and the package center ground path.

20. The assembly of claim 19 wherein a distance between the first package signal path and the first package ground path is generally consistent as the first package signal path extends toward the die and a distance between the second package signal path and the second package ground path is generally consistent as the second package signal path extends toward the die.

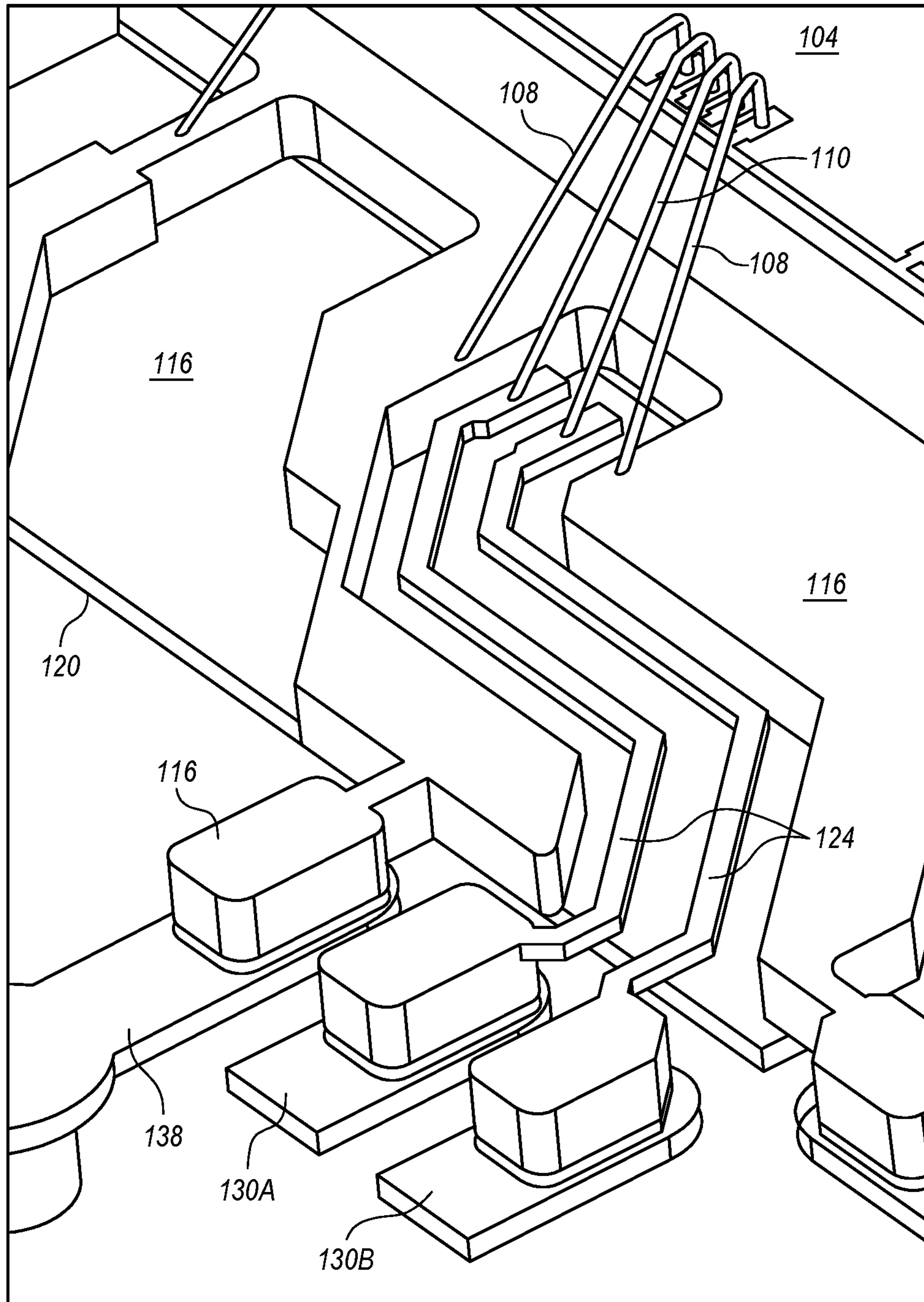


FIG. 1
Prior Art

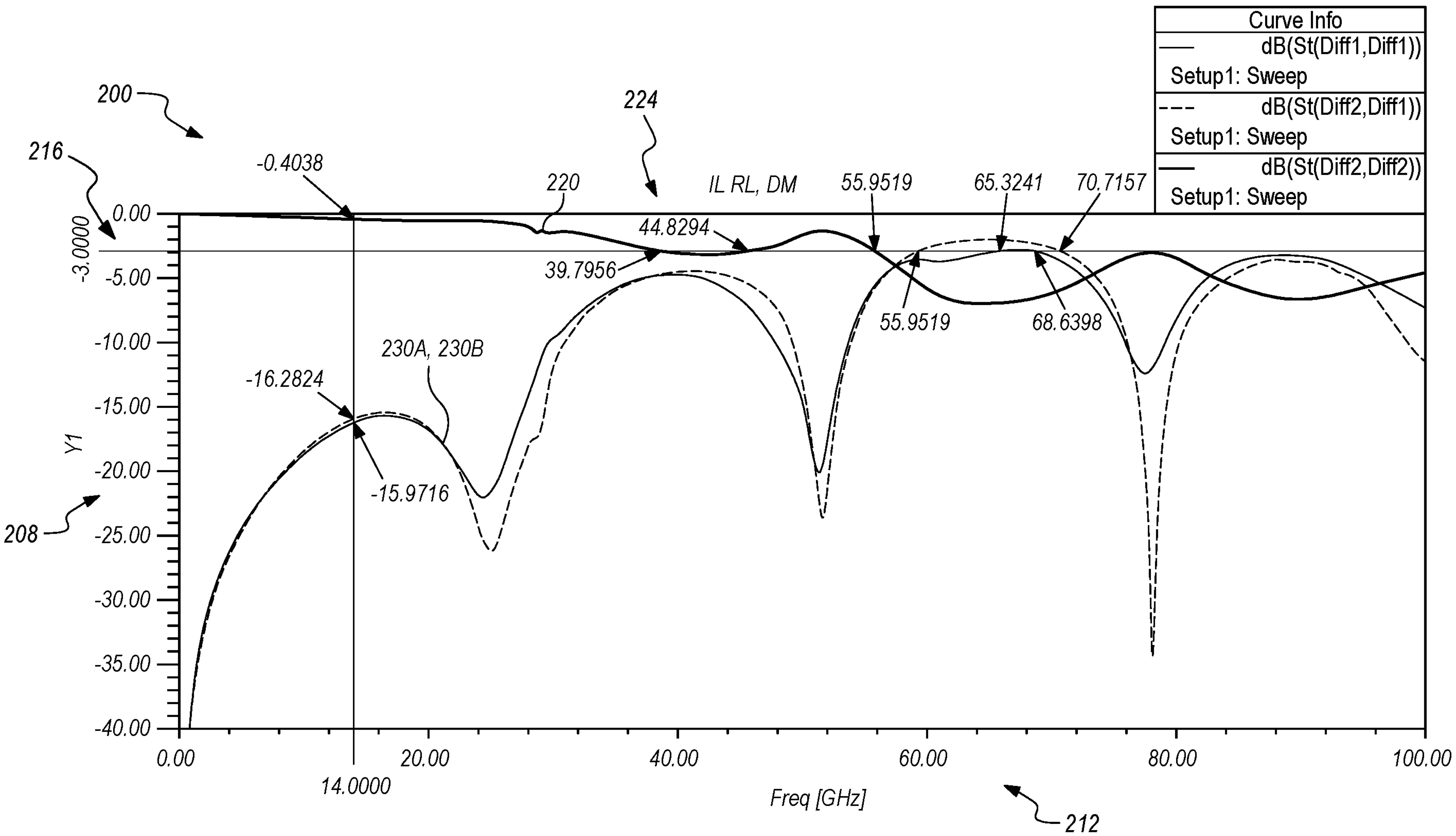


FIG. 2A
Prior Art

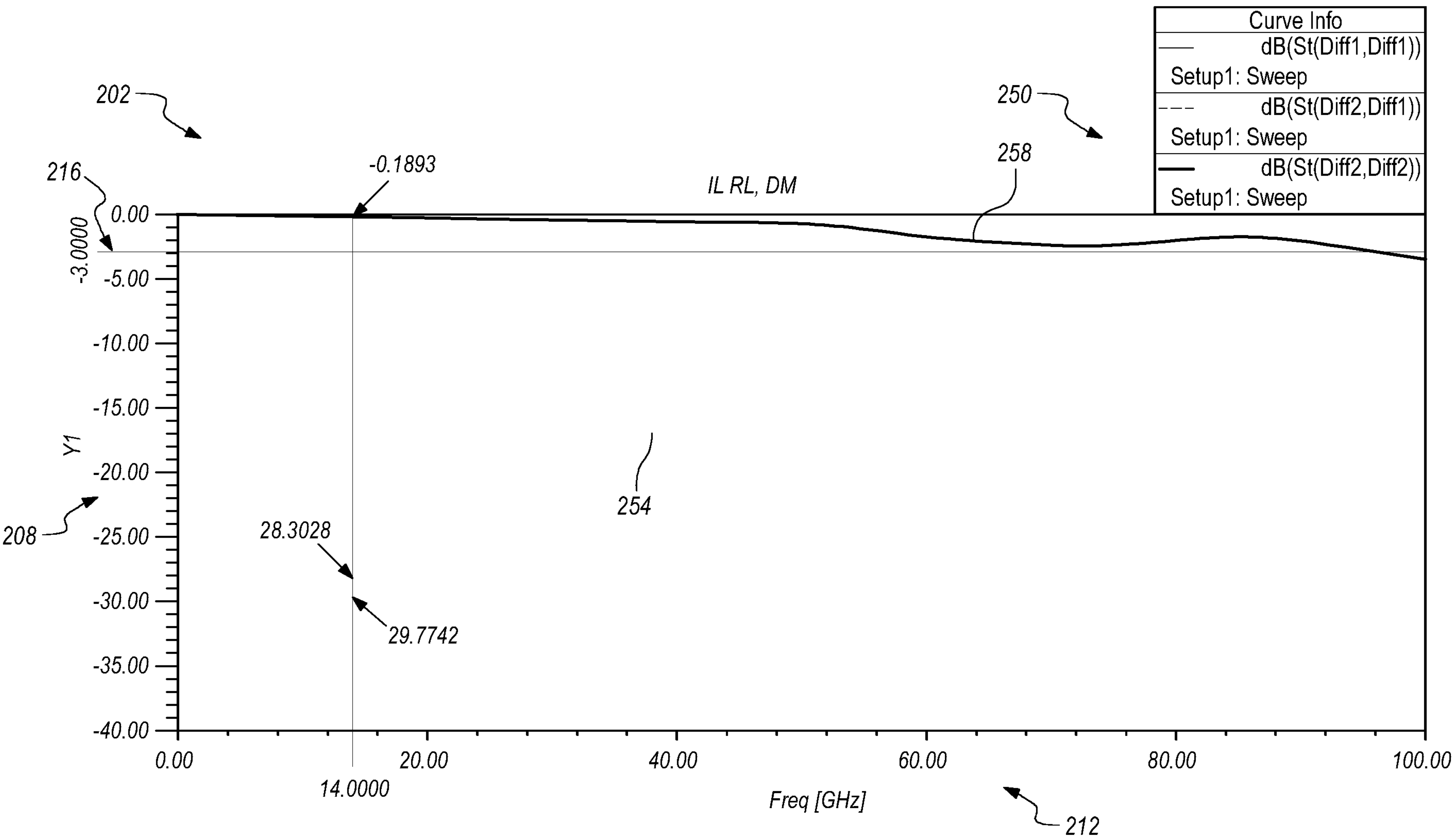


FIG. 2B

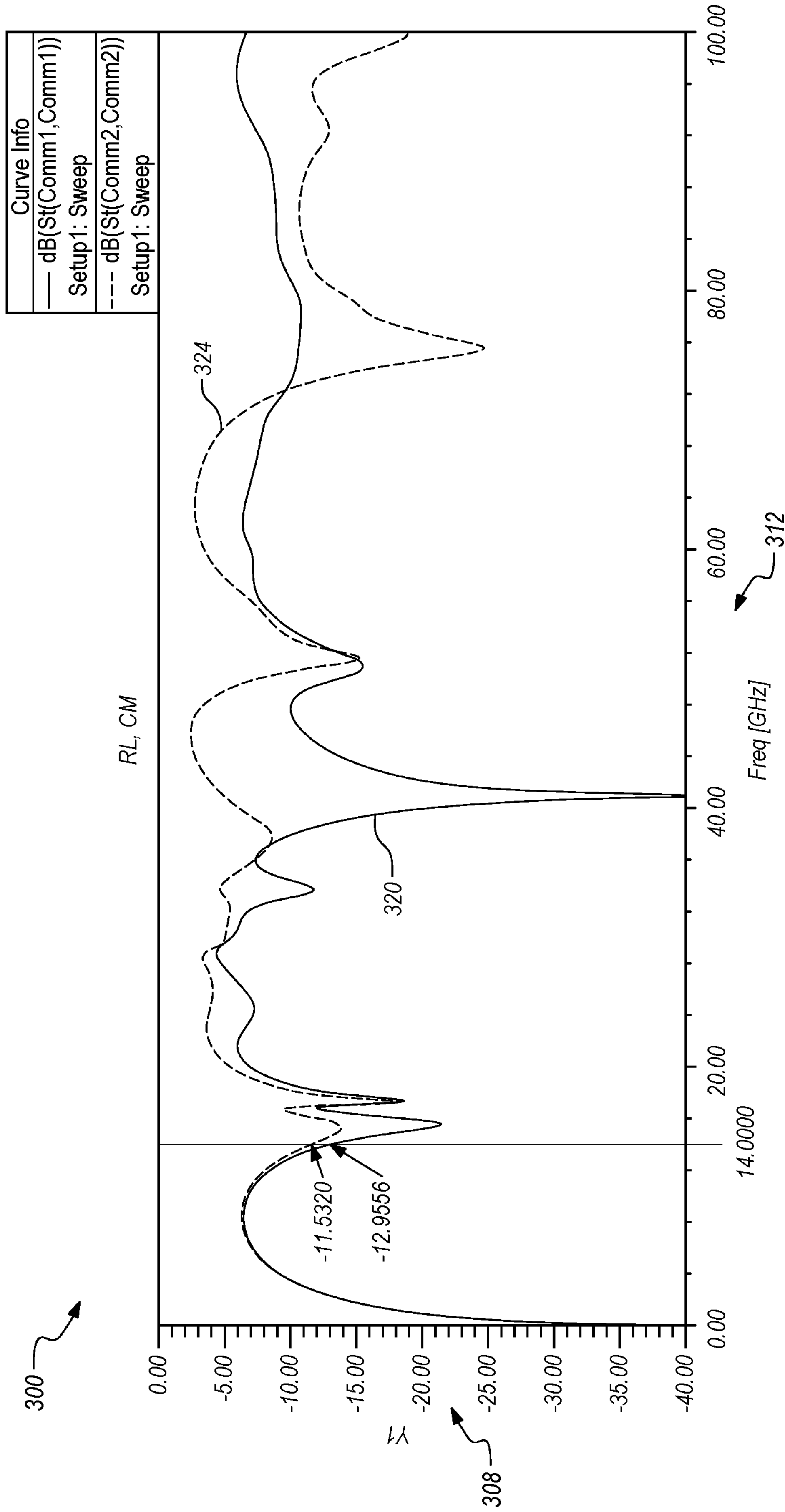


FIG. 3A
Prior Art

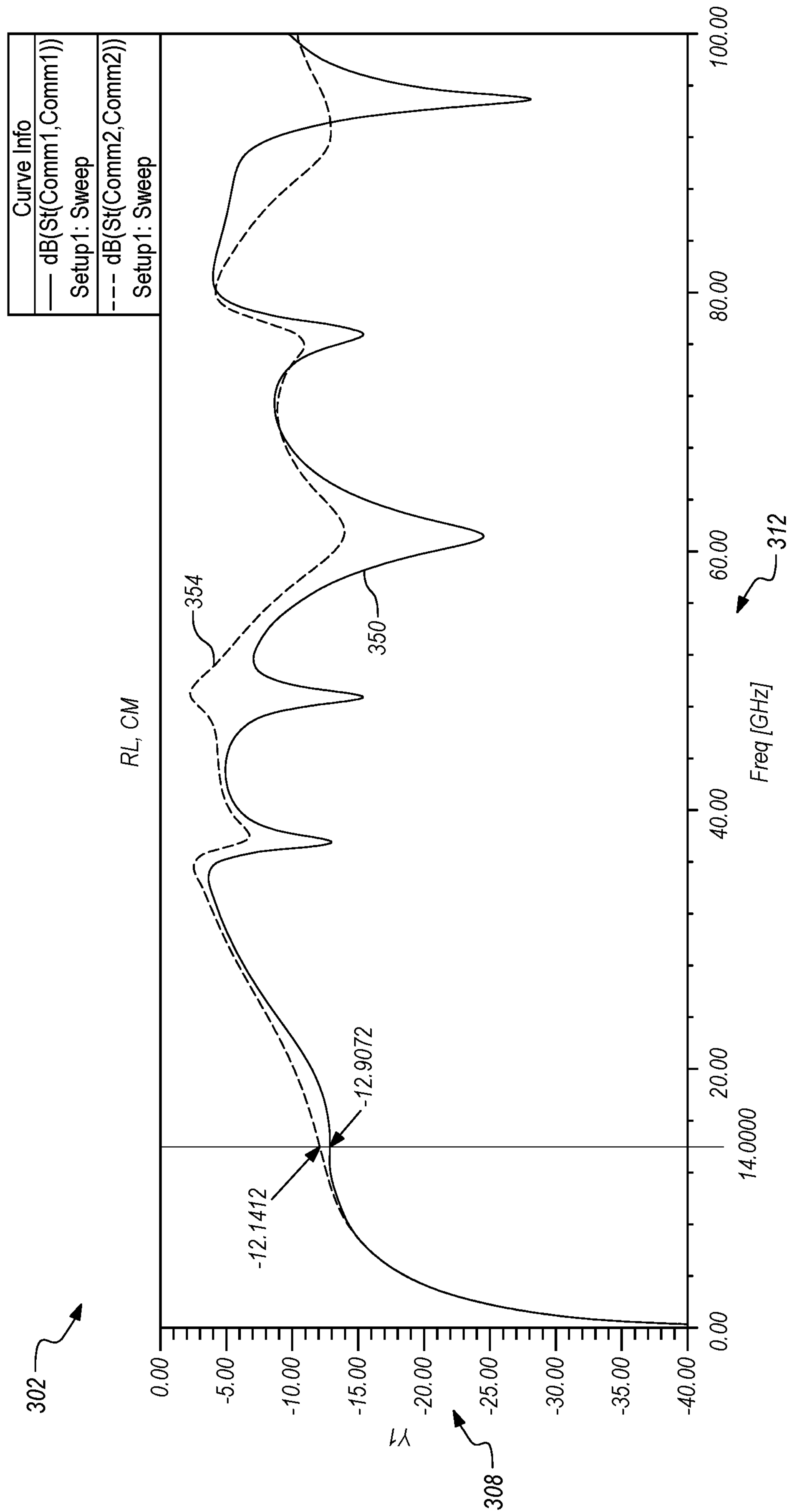


FIG. 3B

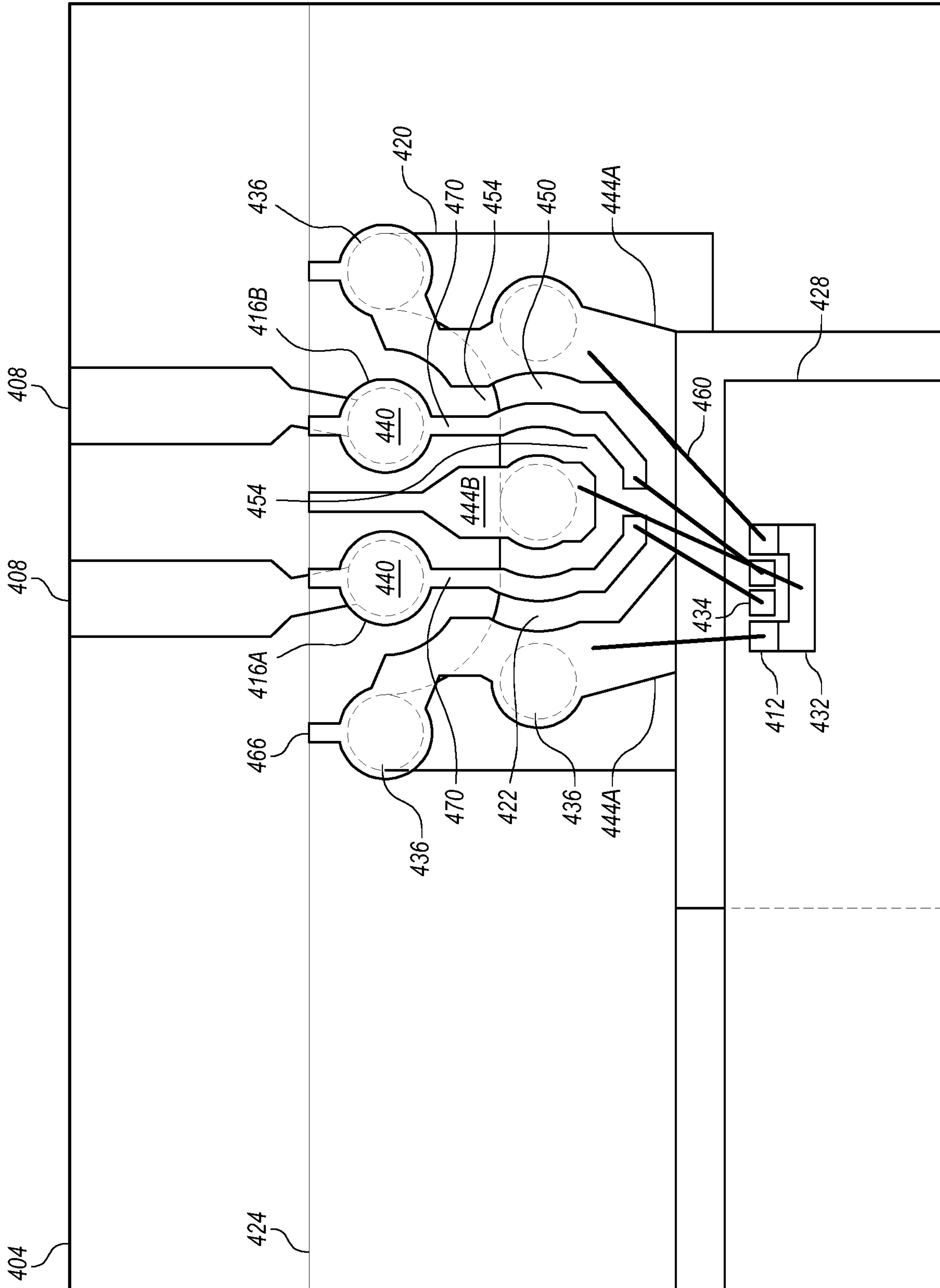


FIG. 4

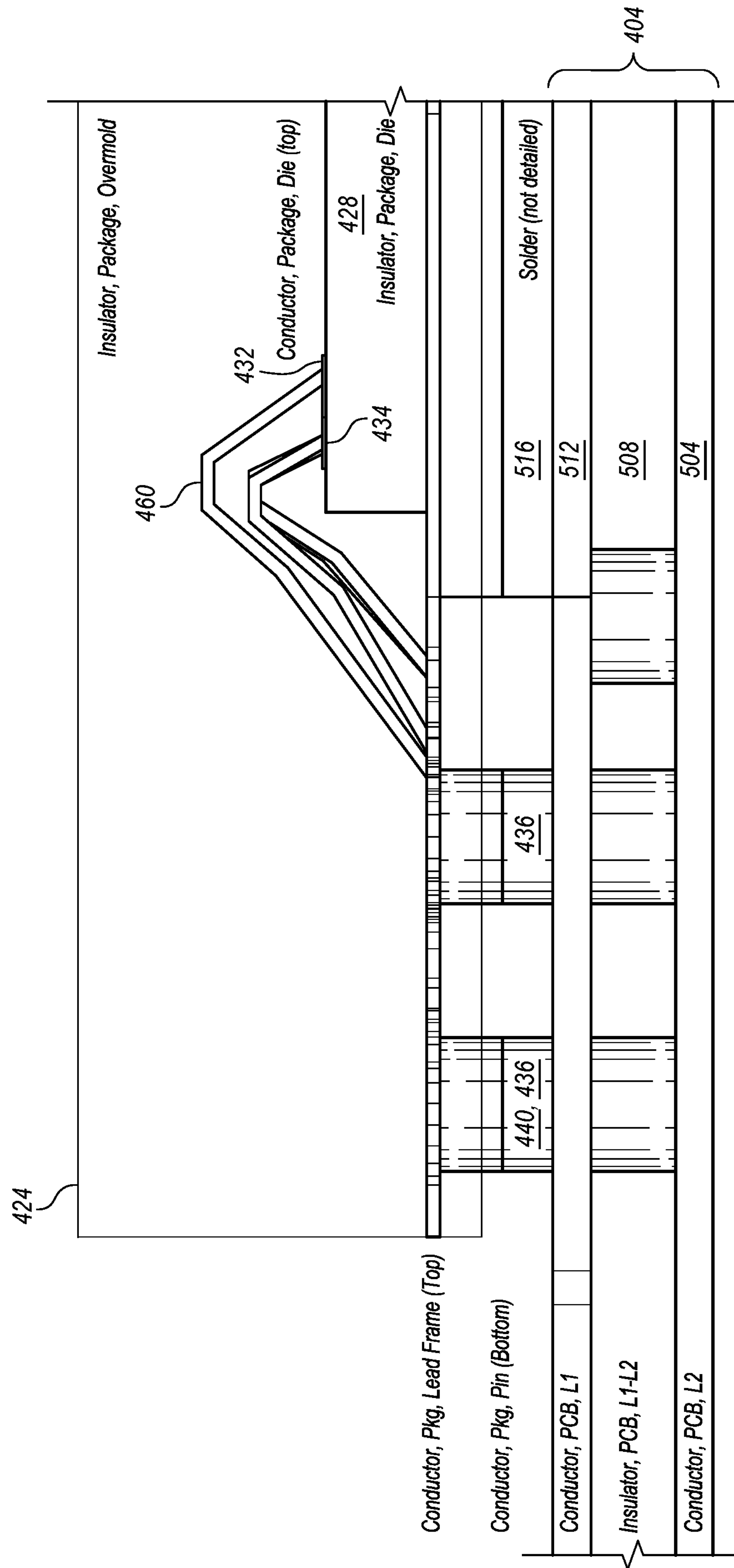


FIG. 5

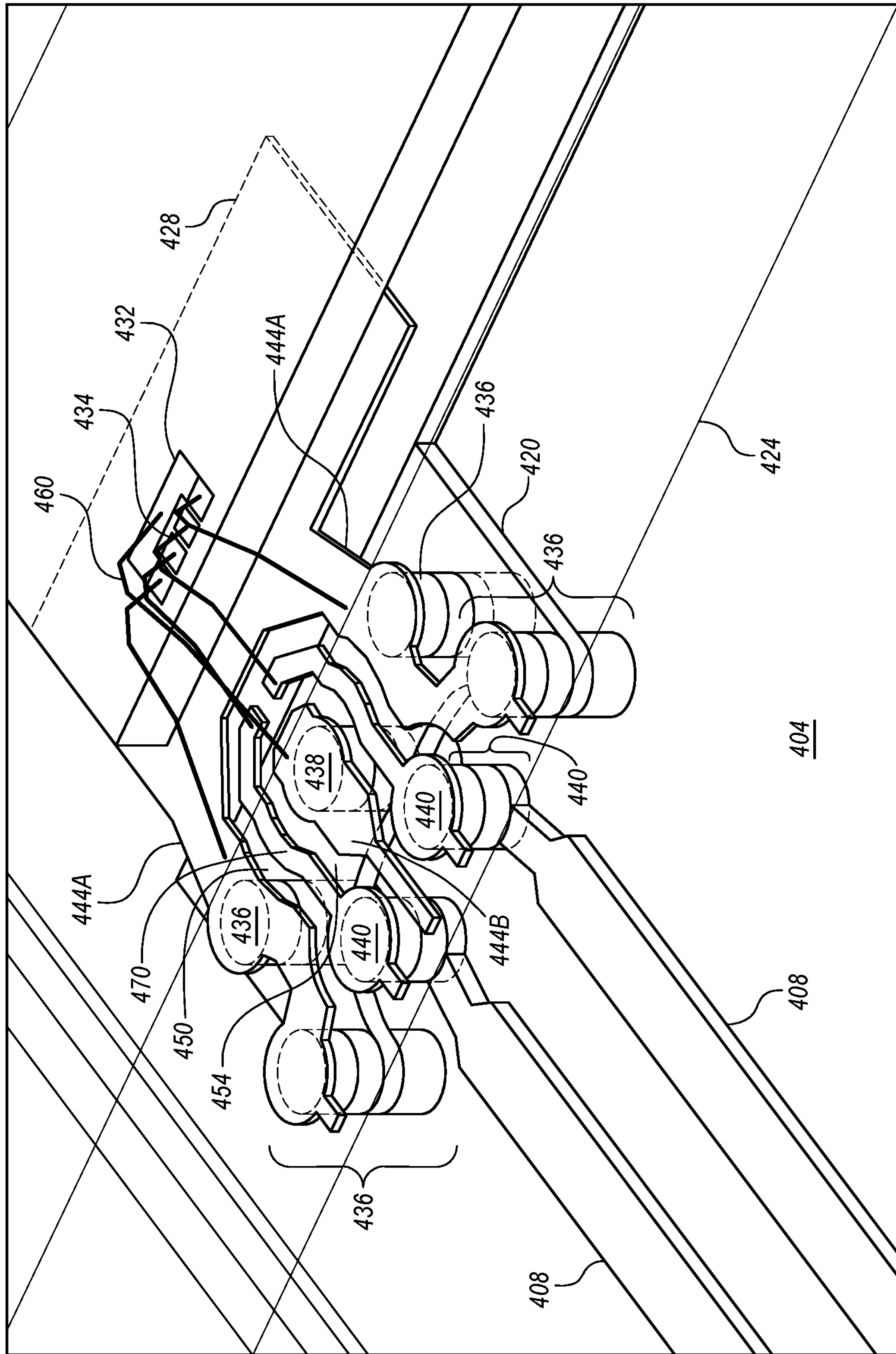


FIG. 6

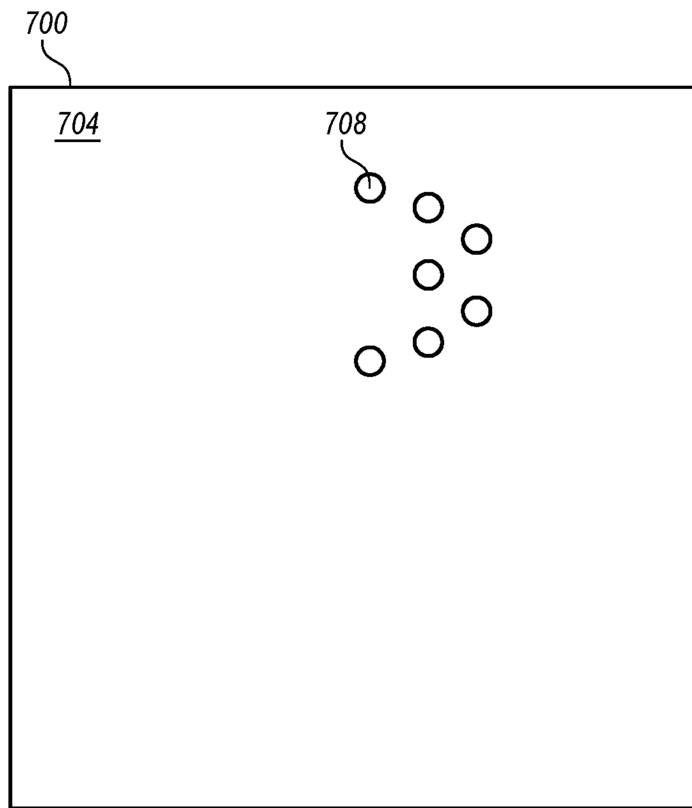


FIG. 7A

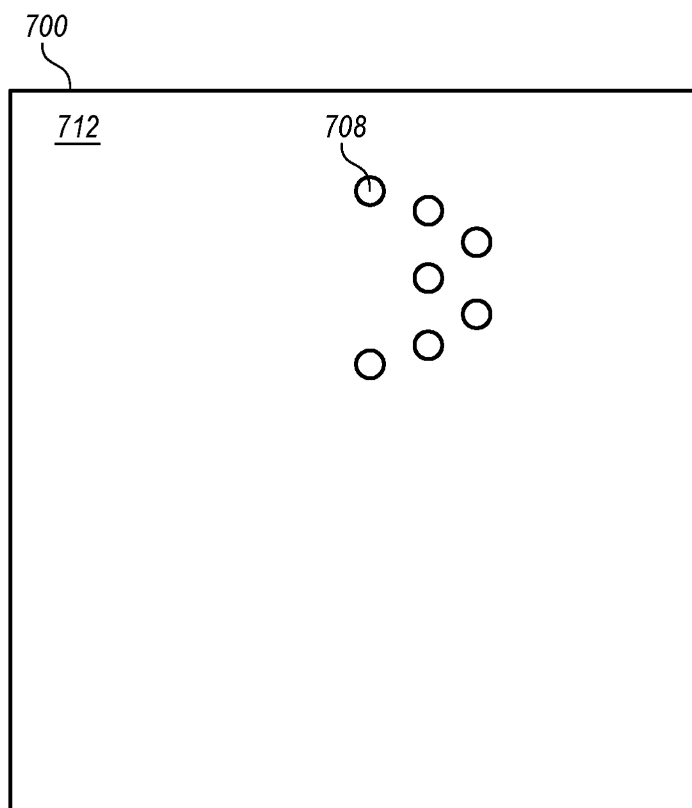


FIG. 7B

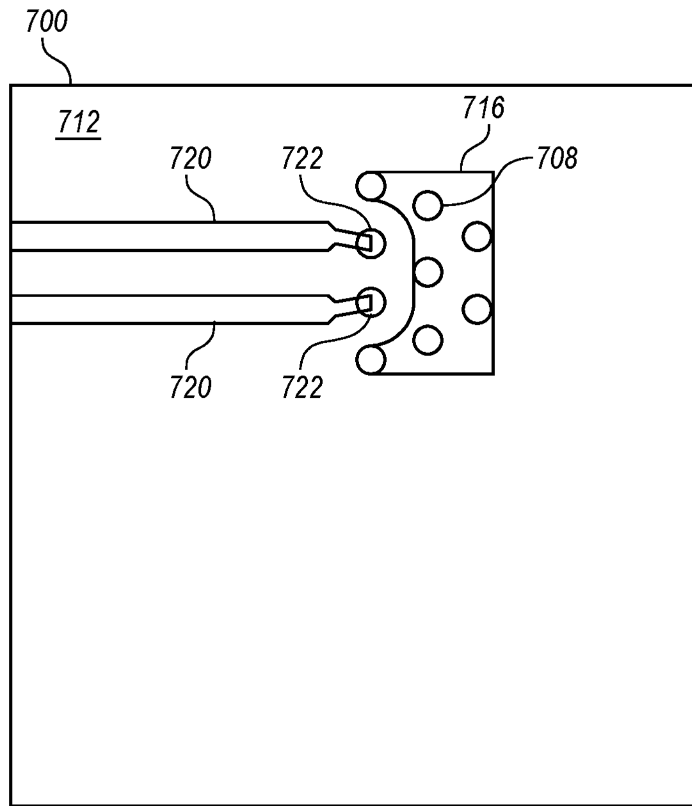


FIG. 7C

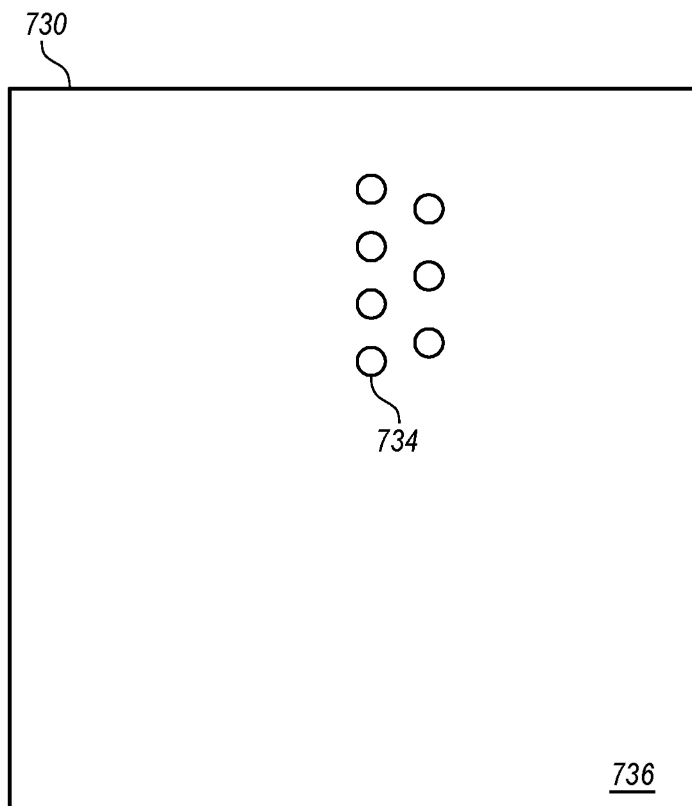


FIG. 7D

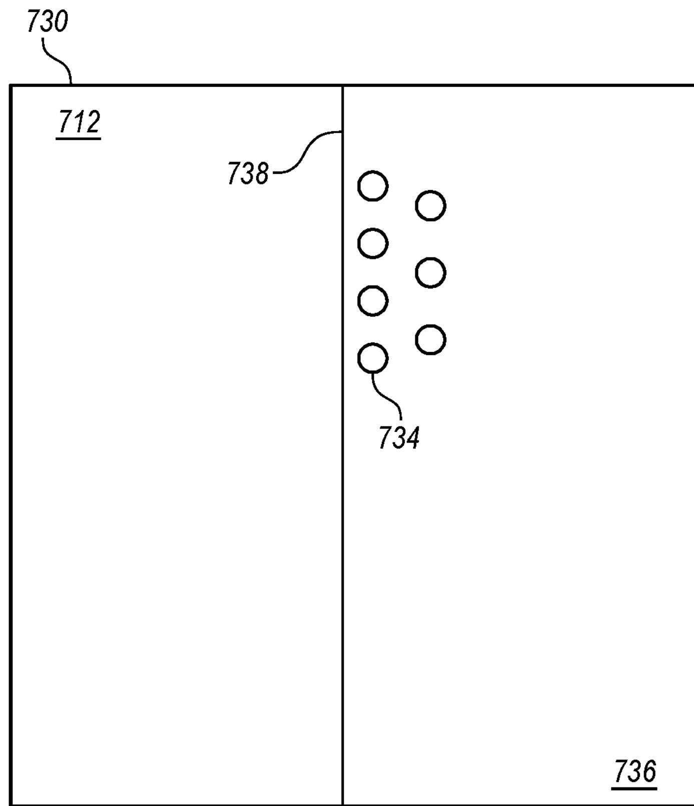


FIG. 7E

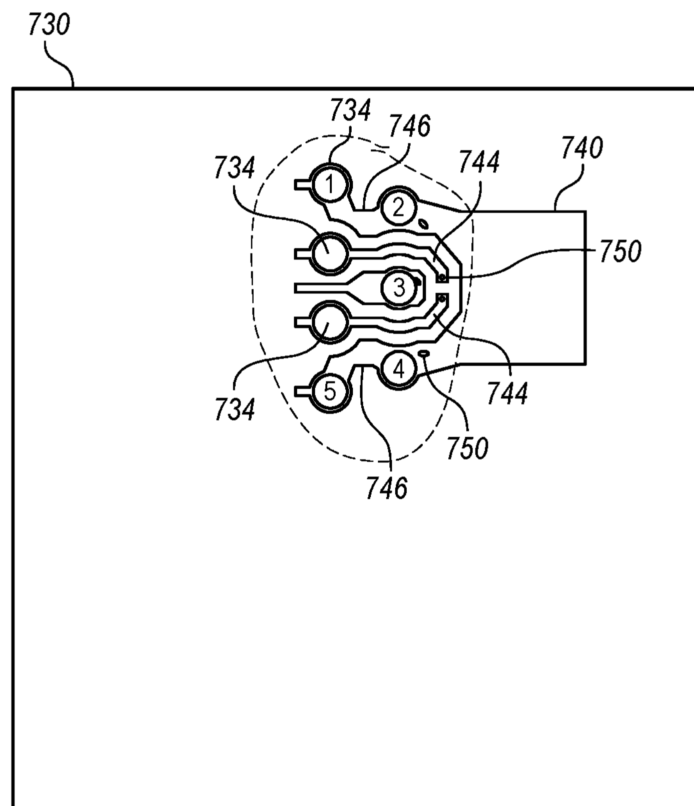


FIG. 7F

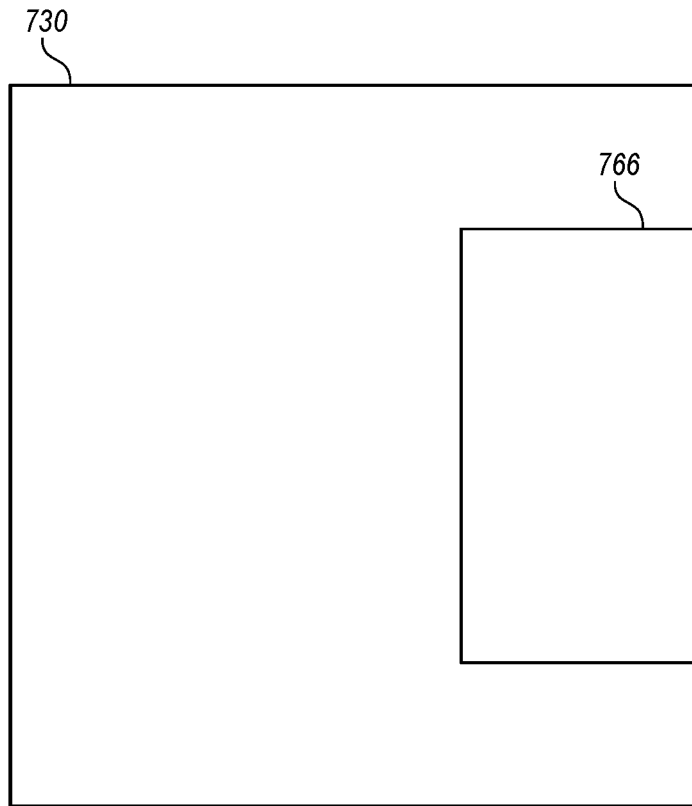


FIG. 7G

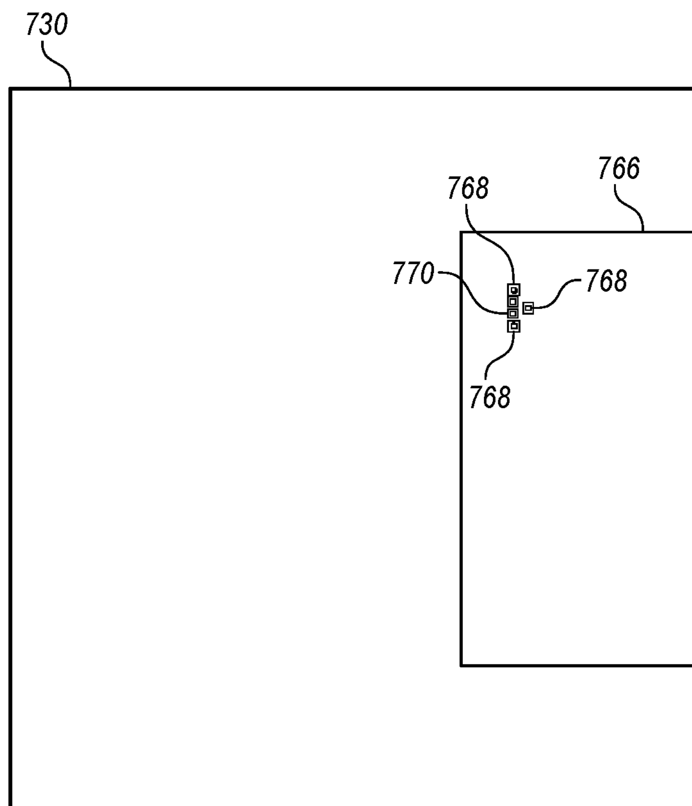


FIG. 7H

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/036861

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/522(2006.01)i, H01L 23/498(2006.01)i, H01L 23/48(2006.01)i, H01L 23/00(2006.01)i, H05K 1/11(2006.01)i, H05K 1/18(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/522; H05K 1/11; H05K 1/14; H05K 1/00; H05K 1/02; H01L 23/495; H01L 23/498; H01L 23/48; H01L 23/00; H05K 1/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: circuit board, die, package, ground, signal, pad, via, conductor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015-0195906 A1 (VIA ALLIANCE SEMICONDUCTOR CO., LTD.) 09 July 2015 See paragraphs [0022]-[0025] and figures 2-3.	15,17
Y		1-14,16,18-20
Y	US 2012-0120619 A1 (EIICHI KODERA) 17 May 2012 See paragraphs [0047]-[0077] and figure 4.	1-14,16,18-20
A	US 2012-0247825 A1 (MING WEI et al.) 04 October 2012 See paragraphs [0026]-[0030] and figures 7-10.	1-20
A	US 2012-0104588 A1 (NAN-JANG CHEN et al.) 03 May 2012 See paragraphs [0062]-[0066] and figure 18.	1-20
A	US 2005-0121752 A1 (SHENG-YUAN LEE) 09 June 2005 See paragraphs [0040]-[0047] and figures 4A-4C.	1-20

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 September 2017 (15.09.2017)	**15 September 2017 (15.09.2017)**

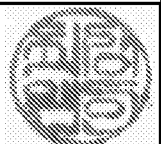
Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

CHOI, Sang Won



Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/036861

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015-0195906 A1	09/07/2015	TW 201528884 A	16/07/2015
		TW I572256 B	21/02/2017
		US 9198286 B2	24/11/2015
US 2012-0120619 A1	17/05/2012	JP 2012-104457 A	31/05/2012
		JP 5652145 B2	14/01/2015
		US 8817478 B2	26/08/2014
US 2012-0247825 A1	04/10/2012	CN 102711362 A	03/10/2012
		TW 201240531 A	01/10/2012
US 2012-0104588 A1	03/05/2012	CN 101211794 A	02/07/2008
		CN 101211794 C	02/07/2008
		CN 101471317 A	01/07/2009
		CN 101471317 B	15/01/2014
		EP 1944802 A2	16/07/2008
		EP 1944802 A3	11/03/2009
		TW 200828525 A	01/07/2008
		TW 200929494 A	01/07/2009
		TW I376019 B	01/11/2012
		TW I385774 B	11/02/2013
		US 2008-0211068 A1	04/09/2008
		US 2008-0290486 A1	27/11/2008
		US 7834435 B2	16/11/2010
		US 8124461 B2	28/02/2012
		US 8350380 B2	08/01/2013
US 2005-0121752 A1	09/06/2005	TW 200520173 A	16/06/2005
		TW I229422 B	11/03/2005
		US 7087993 B2	08/08/2006