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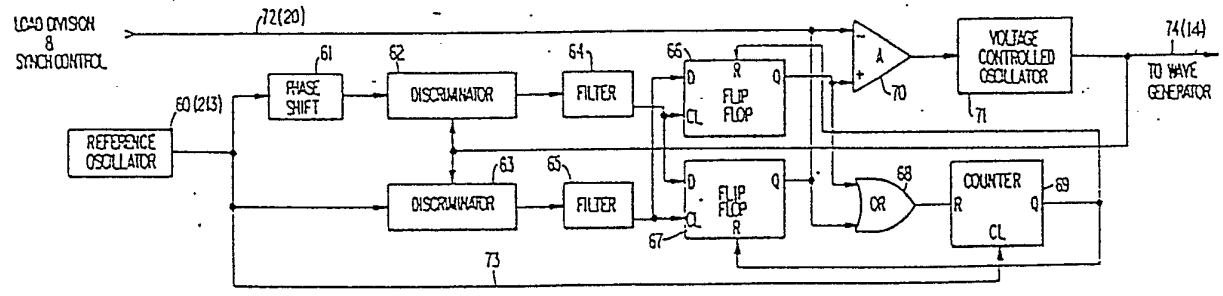

(57) Abstract

Frequency control apparatus, or simply frequency control, for an AC system, adapted to be connected in parallel with another system, with particular application to variable speed constant frequency (VSCF) systems. Each system has an individual frequency control which receives an input signal (72) that corresponds to the difference in operating frequency and/or phase, of the plural systems. Each individual frequency control contains a reference frequency oscillator (60) which operates at fixed frequency, a signal controlled oscillator (71), and a feedback loop (62-70) which compares the frequencies of the two oscillators (60, 71). When the input signal (72) is present, the frequency of the controlled oscillator (71) is varied accordingly, ultimately to a frequency which is the average of the natural frequencies of the plural systems. In the absence of input signal (72), the controlled oscillator (71) operates at the frequency of the reference oscillator (60).

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FREQUENCY CONTROL APPARATUS FOR AC MACHINE

BACKGROUND OF THE INVENTION

Field Of The Invention

The present invention relates generally to frequency control for AC machines and, more particularly, to frequency control of alternating current systems having individual reference oscillators. The present invention is applicable for matching the frequencies of parallel connected alternating current generators, and for adjusting the frequency of an AC motor in accordance with a frequency control signal.

The present invention has particular application in the field of variable speed constant frequency generator systems used in any aircraft environment. The present invention allows the generator systems to be connected in parallel so as to generate output signals having a frequency which is the average of all the individual frequencies of the generator systems. The present invention may also be used to control the prime mover speed in conventional generating systems so as to adjust frequency of the output of each machine when the outputs are connected in parallel.

Description Of The Prior Art

The phase lock loop is a commonly used method of frequency control. In such phase lock loop systems, a master oscillator sets the system frequency, and all individual machines are then phase shifted with respect to this master oscillator in order to share the load. In this conventional method, the system maintains the master frequency. Such phase lock loop master oscillator systems work well during normal operation of parallel generator systems.

A major disadvantage of phase lock loop master oscillator systems is that if for any reason the master oscillator malfunctions, the entire system frequency will be lost. If this malfunction should occur in generator systems generating in parallel, such as a variable speed constant frequency (VSCF) system, there must be some backup means for providing a new master oscillator signal. When the master oscillator fails, however, logic circuitry must be provided to decide which of the oscillators of the other parallel systems is to become the new master oscillator for controlling the frequency of the entire parallel connected system.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates in block diagram form two generator systems of the VSCF type connected in parallel in accordance with the present invention.

Figure 2 shows an embodiment of the circuitry of the load division and synchronization circuit 12 of Figure 1 which generates a control signal proportional to the circulating current present in the parallel connected systems.

Figure 3 presents a block diagram of a frequency control having a reference oscillator and signal controlled oscillator.

Figure 4 illustrates an embodiment of the frequency control circuit of Figure 3.

Figure 5 shows another embodiment of the frequency control circuit of Figure 3 and includes an additional counter start pulse circuit.

Figures 6A and 6B plot the wave forms which occur at the various stages of the circuit shown in Figure 4, with the vertical axis of each plot representing amplitude and with the horizontal axis of each plot representing time.

SUMMARY OF THE INVENTION

In order to control the frequency of each parallel AC system in accordance with the average of all individual systems, the frequency control of each system in accordance with the present invention is provided with a signal control oscillator in addition to its reference oscillator. When not in parallel, the signal controlled oscillator is forced to the same frequency as the reference oscillator. The output of the signal controlled oscillator is used to control the frequency of the AC system or generator.

When two or more systems are paralleled or synchronized, a control signal is provided to the signal controlled oscillator. A control loop is provided in accordance with the present invention to adjust the frequency of the signal controlled oscillator up or down in accordance with whether the signal controlled oscillator output is faster than or slower than the reference oscillator output.

The frequency control of the present invention can determine whether the signal controlled oscillator output is faster or slower than the reference oscillator output. The absolute frequency difference between these two signals is determined by means of a discriminator.

The frequency control of the present invention averages all of the natural frequencies of the individual systems. Since none of the oscillators of the paralleled systems act as a master oscillator, there is no need for the present invention to select a new master oscillator if one of these oscillators should fail. The parallel connected systems in accordance with the present invention will automatically average the frequencies of the remaining systems.

The present invention may also be used to adjust the frequency of motors. A reference oscillator maintains the nominal speed, and speed adjustment is accomplished using a second control signal applied to the frequency control loop.

The actual determination of whether the reference oscillator or the voltage controlled oscillator is faster or slower is determined in the preferred embodiments by phase shifting the output of the reference oscillator. The reference oscillator output and the phase shifted reference oscillator output are each discriminated with respect to the output of the signal controlled oscillator. Determination of which of these signals is leading determines which oscillator has a higher frequency.

DETAILED DESCRIPTION OF THE INVENTION

In Figure 1, there are shown two generators connected in parallel which utilize frequency controls in accordance with the present invention. In the system shown, the circulating currents between phase A of generator GEN 1 and phase A of generator GEN 2 are detected. These circulating currents along with the reference oscillator associated with each generator are then used to control the frequency of each generator. More specifically, with respect to generator GEN 1, there is shown a

current transformer 10a connected to the phase A output, and a similar current transformer 10b connected to the phase A output of generator 2. A differential arrangement D extracts from the transformer 10a and 10b a differential circulating current, and applies two voltages proportional to this circulating current to the load division and sync circuits 12a and 12b via respective lines 17a and 17b.

Each load division and sync circuit 12 generates a control signal, e.g., a voltage, which is proportional to a phasor portion of the circulating current, and this control signal is applied via a line 20 to a frequency control 13. For purposes of explanation, the control signal on line 20 is referred to as a control voltage signal, but this control signal could also be a control current signal. Each frequency control 13 has associated with it a reference oscillator(R-01,R-02) which is represented by a circuit block 213. The frequency control 13 adjusts the controlled frequency output on a line 14 in accordance with the reference oscillator 13 and the control voltage on line 20. A wave generator 15, such as that which is used on a variable speed constant frequency generator of the type shown in U.S. Patent No. 3,873,928, entitled "Reference Wave Generator Using Logic Circuitry for Providing Substantially Sinusoidal Output," to David L. Lafuze, and assigned to the General Electric Company, receives on line 14 the controlled frequency signal from frequency control 13.

In the case of a VSCF system, such as that shown in U.S. Patent No. 3,902,073, entitled "Starter Generator Electrical System utilizing Phase Controlled Rectifiers to Drive a Dynamo-Electric Machine as a Brushless DC Motor in the Starter Mode and to Provide Frequency Conversion for a Constant Frequency Output in the Generating Mode," to David L. Lafuze, and assigned to the General Electric Company, it is known that the impedance of the generator is at approximately 45° lagging or in the

inductive direction. In the instance of a VSCF generator, the wave generator, such as wave generator 15, will produce a substantially 45° leading signal along with many other signals necessary for generator control and operation. This 45° leading signal is the reference signal on a respective line 16 which is fed back to its load division and sync circuit 12. This reference signal enables each load division and sync circuit 12 to produce its control voltage signal on line 20 by selecting a phasor portion of the circulating current, the difference signal from the transformer control loop 17.

Also shown in Figure 1 are lines 18a and 18b, which feed back to the load division and sync circuits 12 the terminal voltages present at generator 1 phase A and generator 2 phase A, respectively. These terminal voltages are used in the initial synchronization of the two generators. Synchronization of the generators is initiated by closure of a control switch 201. This couples a SYNCH signal to, and activates a phase lock loop system within each load division and sync circuit 12. This generator synchronization is necessary to prevent high transient currents which would otherwise occur when the "paralleling" contactor 21 is closed. As has been done even up to this point, a recital of typically "frequency control 13" implies that the description applies to both the frequency controls 13a and 13b.

Thus an identical control system in accordance with the present invention to that used for phase A of generator 1 is shown in Figure 1 for phase A of generator 2. In structure, the two control systems are identical and, consequently, the just indicated convention for describing both systems, will be continued. In terms of operation, the circulating current signal derived by current transformers 10 is of opposite polarity for the two control systems. Thus, the control system for phase A of generator 2 operates inversely to the operation of the control system for phase A of generator 1. That is

to say, if the control system for phase A of generator 1 causes generator 1 to speed up, the control system for phase A of generator 2 causes generator 2 to slow down correspondingly, and vice versa. It should also be understood that any number of generator systems can be controlled by controlled systems of the present invention in an analogous fashion so as to operate all of these systems in parallel.

In Figure 2, there is shown in detail a load division and sync circuit 12 which may be used for initial synchronization, and the production of the control frequency signal for the frequency control 13. As stated above, there is a separate load division and sync circuit 12 associated with each of the generators of the AC systems connected in parallel. In operation, the generators are synchronized, and once the synchronization is complete, the polyphase contactors 21 are closed, causing the generators of the systems to be operating in parallel. Upon the closing of the contactor 21 (Figure 1), the terminal voltage on feedback lines 18 are identical because generators 1 and 2 are in parallel. Thus, the signals at inputs 30 and 31 of the load division and sync circuit 12 of Figure 2 are identical so that the comparison signal, which is a function of the difference between the signals at inputs 30 and 31 (18a and 18b of Fig.1), which are normally different during synchronization, goes to zero after closing of contactor 21. Thus, once contactor 21 is closed, the present invention controls the parallel-connected systems in accordance with the voltage signal for each phase of each generator, each voltage signal being proportional to the circulating component in that phase of the total parallel-connected system.

The top portion of Figure 2 shows the synchronization circuit of the load division and sync circuit 12 a used for initial synchronization of the two generators GEN 1

and GEN2. Applied to inputs 30 and 31 are the terminal voltages of phase A of generators 1 and 2, respectively, as these generators are operating independently of each other. With switch 201 (Fig. 1) closed, the SYNCH signal is applied via an amplifier 214 to the + input of a comparator amplifier 33, to enable for operation in the manner to be immediately described, the following: comparator amplifier 33, another comparator amplifier 32, a pair of flip-flops 34 and 35, and an operational amplifier 36. The amplifier 36 is enabled by the SYNCH signal additionally, in the sense of connecting its output to line 20a (Figs. 1 and 2), via an inverting amplifier 215 and a resistance 216. Were the SYNCH signal absent, i.e. switch 201 open -- this condition usually obtains upon initial start-up of the generators GEN1 and GEN2 --, the units 32 to 36 would be disabled.

The terminal voltage signals on inputs 30 and 31 are fed to the comparator amplifiers 32 and 33 which convert these two signals into square waves in accordance with their zero crossings. These square wave signals are supplied, respectively, to the flip-flops 34 and 35, which measure the phase difference between these two signals. When the square wave signal at the output of comparator 32 is leading the square wave signal at the input of comparator 33, the Q output of flip-flop 34 indicates this phase difference and is applied via a scaling resistor to the non-inverting input of the operational amplifier 36 connected as a differential amplifier. Conversely, when the square wave signal at the input of comparator 32 is lagging the square wave signal at the input of comparator 33, the Q output of flip-flop 35 indicates this phase difference and is applied via a scaling resistor to the inverting input of the operational amplifier 36. The output signal from operational amplifier 36 goes negative when generator 1 phase A leads generator 2 phase A (which effectively causes the frequency of generator 1 to be decreased) and goes positive when generator 1 phase A lags generator 2 phase A (which effectively causes the frequency of generator 1 to be increased).

The signal at the output of amplifier 36, which is the voltage control signal on line 20a of Figure 1, is the output of a phase discriminator of a phase lock loop made up of the voltage controlled oscillator of frequency control 13a, the wave generator 15a and generator 1. This phase lock loop brings the frequency and phase of phase A of generator 1 into alignment with the frequency and phase of phase A of generator 2. Once this frequency and phase synchronization is achieved, contactor 21 is closed, connecting generators 1 and 2 in

parallel. Once the generators are in parallel, the phase discriminator made up of comparators 32 and 33 and flip-flops 34 and 35 no longer provides a phase difference signal because the terminal voltage signals at the inputs of comparators 32 and 33 are the same. Thereafter, the load division circuit shown in the bottom part of Figure 2 takes control of the frequency and phase of the generators by generating the control signal on line 20a proportional to a component of the circulating current, which effectively adjusts the frequency and phase of generator 1.

The lower part of Figure 2 illustrates the load-division-circuit-parts of the blocks D, 12a and 12b of Figure 1. Of these parts, those associated with block D (identified by reference numerals 37 to 42) are shared by the blocks 12a and 12b. The block D includes the secondaries 37,38 of the current sensing transformers 10a and 10b, which are shunted by respective burden resistors 39 and 40, and also by respective primary windings 41 and 42 of isolation transformers 43a and 43b. The primaries 41 and 42 are "cross-coupled" in the manner shown. The secondaries 44a and 44b develop substantially equal voltages, each one proportional to the phasor-difference -- this term is explained below -- of the currents delivered by phase A of generator GEN 1 and phase A of generator GEN 2. Moreover the secondaries 44a and 44b are each center-tapped, and hence two pairs of outgoing lines 17a1, 17a2 and 17b1, 17b2 are shown. These pairs correspond respectively to the lines 17a and 17b of Figure 1. The pair of lines 17a1 and and 17a2 feed a system, applicable to the generator GEN 1, which is further described below, and the lines 17b1 and 17b2 feed a duplicate such system, applicable to the generator GEN 2.The individual system for the generator GEN 1 begins with the input line 16a, which carries the reference signal of the wave generator 15a of Fig. 1; that individual system includes components bearing reference numerals 45 and higher.

It should be understood at this point that only one load division

circuit (for generator 1) is shown in Figure 2 because it is assumed that generator 1 is a symmetrical, three-phase system with phases B and C being displaced 120° and 240°, respectively; therefore, if phase A of the total system is effectively controlled, then phases B and C will be correspondingly controlled. However, if improved load division between the parallel-connected generators is desired, each phase of the total system can be measured and controlled using a similar load division circuit as that shown in Figure 2.

The purpose of transmission gates 45 and 46 connected to the respective leads 17a1 and 17a2 of the secondary 44a is to provide the system with phase sensitivity. Transmission gates 45 and 46 essentially act as on/off switches, which are controlled by the reference signal 16a from the wave generator 15a. The purpose of the transmission gates or discriminators 45 and 46 is to provide that portion of the circulating current phasor which is used to control the frequency of phase A of the total system. In a conventional synchronous generator system, when two generators are connected in parallel and the generated voltages are equal in amplitude and frequency, but are slightly displaced in phase, the phasor difference voltage of the two generated voltages is substantially at 90° relative to the system terminal voltage. This phasor differences voltage applied to the inductive source impedance of the generators results in a circulating current in phase with the system terminal voltage. This circulating current signal is used by the present invention to control the speed of the generators and hence the frequency of the power produced thereby so as to reduce the circulating current to substantially zero.

In comparison, in a VSCF system, when two generators are connected in parallel and the generated voltages are equal in amplitude and frequency but slightly displaced in phase, the phasor difference voltage of the two generated voltages is substantially at 90° relative to the system terminal voltage. However, because the source impedance of the VSCF is only 45°

lagging, the circulating current is displaced from the phasor difference voltage by 45° as opposed to 90° in the conventional generator system. This circulating current signal is thus displaced 45° from the system terminal voltage and is used by the present invention to control the frequency of the power generated by the cycloconverters so as to reduce the circulating current to substantially zero.

Referring again to Figure 2, in the case of a VSCF system, the 45° leading signal from wave generator 15a is brought in on line 16a. If the proper desired 45° leading signal cannot be furnished by wave generator 15a, it may be generated by introducing a 45° phase lead to the phase A voltage from generator 1. In the case of a conventional generator system, the signal applied on line 16a would be merely in phase with the system terminal voltage for phase A. The explanation given below for the load division circuit is for the VSCF application, but is equally applicable to the conventional generator application if the signal on line 16a is in phase with the system terminal voltage.

The control signal on line 16a is essentially a square wave, and is used to switch the transmission gates 45 and 46. The transmission gates 45 and 46 in conjunction with secondary winding 44a can be thought of as operating similar to a full-wave rectifier controlled by the control signal on line 16a from the wave generator 15a.

It is through the selection of one phasor part of the total difference current signal of phase A that it is possible for the load division circuit effectively to adjust the frequency of the power generated by the cycloconverters. When two systems are connected in parallel (Figure 1), the frequency correction caused by the load division circuit in one system is in a first direction and the frequency correction produced in the

second system will be in the opposite direction. This frequency correction can be understood by assuming that the reference oscillators of the parallel-connected generator systems are different in frequency. If the reference oscillator 213a of generator 1 is lower in frequency than the reference oscillator 213b of generator 2, then the circulating current will tend to drive generator 1 to a greater frequency, while at the same time tending to drive lower the frequency of generator 2. Inverter 47 merely acts to provide the inversion of the square wave signal on input 16a applied to transmission gate 46 to produce the full-wave phase discrimination action of the two transmission gates 45 and 46.

Once the desired phasor portion of the circulating current has been derived at the commonly connected outputs of transmission gates 45 and 46, it is applied to an inverting input of an amplifier 49, which acts as a buffer stage. The output of amplifier 49 is supplied to the inverting input of amplifier 36 discussed above. The output of amplifier 36 constitutes the frequency control voltage applied to frequency control 13a to readjust the frequency of the electric power generated by the cycloconverter of generator 1 phase A in accordance with the selected phasor portion of the circulating current. The output of amplifier 36 is a DC signal having an amplitude proportional to the selected phasor portion.

Figure 3 shows in block diagram form a preferred embodiment of the frequency control 13a. This embodiment is equally applicable to frequency control 13b. Each frequency control 13 includes a reference oscillator 60 and a voltage controlled oscillator 71. (Reference oscillator 60 is designated as block 213 in Figure 1.) The signal supplied to a line 72 is the output signal from amplifier 36 of the load division and sync circuit 13, and this signal is applied to the inverting input of an amplifier 70. Line 72 corresponds to line 20 of Figure 1.

Within frequency control 13 is a control loop consisting of phase shift 62, discriminators 62 and 63, filters 64 and 65, flip-flops 66 and 67, amplifier 70, voltage controlled oscillator 71, and a line 73. This control loop in cooperation with the load division and sync circuit 12 loop produces averaging of the frequencies of the reference oscillator 60 and the corresponding reference oscillator of the other system connected in parallel. If the frequency control 13 is used in connection with a speed control of a motor, then a signal is applied to line 72 which causes a readjustment of the frequency control loop of this speed control.

The determination of any frequency difference between the voltage control oscillator 71 and the reference oscillator 60 is straightforward. This determination involves the use of a discriminator, such as discriminator 63, wherein the output of voltage controlled oscillator 71 is phase discriminated against the output of reference oscillator 60. The output of discriminator 63 is a series of pulses, the filtered average of which is indicative of any difference in frequency. For example, reference oscillator 60 produces a high frequency output signal having a fixed frequency in the 3 megahertz range.

There must be additional circuitry beyond that necessary to determine the frequency difference in order to determine whether the frequency of the output of voltage controlled oscillator frequency 71 is less than or greater than the output of reference oscillator 60. The relationship of the frequency of the output from voltage controlled oscillator 71 to the frequency of the output from reference oscillator 60 is determined by the present invention through the use of two discriminators as follows. The output of one of the oscillators, in this case that of voltage controlled oscillator 71, is applied as a direct input to both discriminators 62 and 63, while the other

oscillator, in this case reference oscillator 60, is not applied directly as an input to discriminator 63, but is phase shifted by a preselected amount by phase shift 61 before being supplied as an input to discriminator 62. The use of the phase shifting allows the determination of the frequency relationship between the two frequency signals. That is to say, the phase of one of the discriminator output envelopes reverses with respect to the other discriminator output envelope when the frequency of the voltage controlled oscillator goes from being greater than to less than the frequency of the reference oscillator. It should be noted that the phase shift produced by phase shift 61 may be any amount, so long as it is not close to zero or 180°. A phase shift of 90° is easily obtainable with digital techniques, and is used in the preferred embodiments.

The output from discriminator 62 and the output from discriminator 63 are filtered and converted to square waves, by filters 64 and 65, respectively. This filtering and squaring operation is necessary in order to obtain respective square wave signals indicative of both the frequency and the phase relationship of the envelope outputs of discriminators 62 and 63. That is to say, the cycle time of either of the square waves is indicative of the absolute frequency difference between the outputs of the two oscillators, and the phase relationship between the two square waves is indicative of the actual frequency relationship between the two oscillator outputs. This analysis of the square waves is performed by flip-flops 66 and 67.

Flip-flops 66 and 67 are used to compare the square wave signals at the outputs of filters 64 and 65 to establish the phase relationship between these two square wave signals. The flip-flop having the square wave from one of the filters applied to its data (D) input which goes positive prior to the other square wave

applied to its clock (CL) input is toggled and indicates that the square wave at its data input is leading the square wave at its clock input. The other flip-flop, however, is cross-connected and does not toggle because its data input is low when the square wave applied to its clock input goes high. Thus, the outputs of flip-flops 66 and 67 indicate the actual frequency relationship between the two oscillator outputs.

The output of the toggled flip-flop is applied either to the non-inverting or inverting terminal of amplifier 70, whose output drives voltage controlled oscillator 71 up or down in frequency depending on which of flip-flops 66 or 67 is toggled. For example, the output of flip-flop 66 is connected to the non-inverting input of amplifier 70, and the output of flip-flop 67 is connected to the inverting input of amplifier 70. When flip-flop 66 is toggled, the output of amplifier 70 goes positive, which indicates that the frequency of the reference oscillator 60 is greater than the frequency of the voltage controlled oscillator 71. The toggling of flip-flop 67 indicates the opposite condition.

As stated above, the toggling of either flip-flip 66 or 67 indicates only the direction of the frequency error and does not indicate the frequency difference, which must be known. Either of the flip-flops 66 or 67 is toggled for each cycle of the frequency difference. The outputs of flip-flops 66 and 67 are provided as inputs to an OR gate 68, whose output goes high for each toggle. This output signal is applied to the reset (R) input of a counter 69, and allows counter 69 to count when this output signal is high. Counter 69 also has applied to its clock (CL) input the output signal from the reference oscillator 60. Therefore, counter 69 will count a given number of reference oscillator cycles before the count is terminated by the output Q of counter 69 going high, which resets flip-flop 66 or 67.

The average voltage at the Q outputs of either of the flip-flops 66 or 67 is indicative of the frequency difference and is equal to the flip-flop high voltage times the ratio of the measured time divided by the period of the difference frequency. The gain of the frequency difference detector can be made as high as is desired by increasing the number of counts of counter 69. For example, if it is desired to control the output frequency to plus or minus 10% of the reference oscillator frequency, the following approach may be used. Counter 69 is set to count eight frequency reference periods. If the high state of the flip-flops is 12 volts, a 10% frequency error will be indicated by a 9.6-volt signal to the input of amplifier 70, which is eight times twelve divided by ten.

Reference oscillator 60 is set to a high frequency value, for example, 3 megahertz. By running reference oscillator 60 at a much higher frequency than the generator (GEN1, GEN2) output, the response of the frequency control loop is rapid. The frequency control will introduce negligible phase shift in the load division loop when, for example, the frequency of the generator output is 400 Hz.

Referring now to Figure 4, there is shown a detailed circuit of a first embodiment of frequency control 13 of the present invention. In this embodiment, the frequency of the output on line 74 (line 14 of Fig.1) from the voltage controlled oscillator is 3.06 megahertz when there is no control signal on line 72. The embodiment of Figure 4 is constructed using CMOS components. CMOS components have been found to be advantageous in VSCF aircraft applications because of their low power consumption and high noise immunity.

The reference oscillator consists of a 6.12 megahertz crystal 80, capacitors 81 and 82, resistors 83 and 84, and an inverter 85. The output of the oscillator appears on line 86 and is applied to the clock (CL)

terminal of a flip-flop 87. Flip-flop 87 produces at its Q output the logic state of its data (D) input when a clock input is received. Flip-flop 87 is a divide by two counter in that its D input is connected to its $\overline{Q}$ output. The Q and $\overline{Q}$ outputs of flip-flop 87 are consequently at 3.06 megahertz. Line 88 is connected to the $\overline{Q}$ output of flip-flop 87, and line 90 is connected to the Q output.

Figure 6A plots the waveforms present at various points in the frequency control circuit 13 of Figure 4, with the vertical axis of each trace representing amplitude and with the horizontal axis of each trace representing time. The horizontal axis of each trace is consistent.

A flip-flop 92 is connected as a divide by two counter and produces at its Q output connected to a line 89 a signal whose frequency is one-half of the frequency of the signal applied to its clock input from flip-flop 87. The waveform of the output signal on line 89 is shown on Figure 6A, and is a 1.53 megahertz square wave. This signal is applied to the D terminal of a flip-flop 93 and to an input of an exclusive OR gate 94. Exclusive OR gate 94 produces the same function as discriminator 63 of Figure 3.

The 90° phase shift necessary for determining whether the voltage controlled oscillator is faster or slower than the reference oscillator is produced by flip-flop 93. Line 90 is connected to its clock input. Flip-flop 93 produces at its Q output terminal a square wave signal that is lagging by 90° the signal on line 89. The output signal on the Q terminal is applied via a line 91 to an input of an exclusive OR gate 95. The waveform on line 91 is shown in Figure 6A. Exclusive OR gate 95 produces the same function as discriminator 62 of Figure 3.

Both exclusive OR gates 94 and 95 have applied to their other inputs a signal on a line 97 representative of the voltage controlled oscillator output. The frequency of the voltage controlled oscillator is 3.06 megahertz. A flip-flop 96 is connected as a divide by two counter and has its clock input connected to the output of the voltage controlled oscillator via a line 131. Hence, the frequency of the signal at the $\overline{Q}$ of flip-flop 96 is at 1.53 megahertz, and is applied via line 97 to exclusive OR gates 94 and 95.

For purposes of illustration, the signal on line 97 is first assumed to be slightly lagging the signal on line 89, the reference oscillator signal, as shown in Figure 6A. When this lag occurs, a series of relatively wide pulses appear on line 98, as labeled in Figure 6A as line 98 lag. Similar traces are shown for the state where the signal on line 97 is leading the signal on line 89. The pulses from discriminators 95 and 94 are of widths determined by the phase relationship between the voltage controlled oscillator signal 97 and the reference oscillator signals 91 and 89, respectively.

The pulse train shown in Figure 6B is representative of the outputs of discriminators 95 and 94 and shows the condition where the frequency difference is large, as shown by the fact that there are only a few pulses* per cycle of frequency difference. Figure 6B plots the envelopes of the pulse trains that appear on lines 98 and 99 during such a condition. The curve marked "frequency difference" represents the output that appears on line 99 since it is merely the voltage controlled oscillator output discriminated against the reference oscillator output. The curve labeled "VCO faster" is the envelope of the pulses that appear on line 98 when the frequency of the VCO signal is higher than the frequency of the reference oscillator. Similarly, the curve

*As the frequency difference approaches zero, the number of such pulses increases rapidly, but then suddenly collapses to zero at zero frequency difference

marked "VCO slower" is the envelope of the pulses that appear on line 98 when the frequency of the VCO is lower than the frequency of the reference oscillator. A comparison of the signals on lines 98 and 99 determine whether the frequency of the VCO is higher or lower than the frequency of the reference oscillator.

The transformation of the pulse trains at discriminator outputs 98 and 99 to corresponding square waves is accomplished by a filtering and Schmitt triggering operation, as shown in Figure 4. The filter, Schmitt trigger circuit which shapes the output signals on line 99 includes a resistor 101, a resistor 102, a capacitor 100, and an amplifier 103. Similarly, the output on line 99 is transformed to a corresponding square wave by the circuit comprising a resistor 105, a resistor 106, a capacitor 104, and an amplifier 107.

The waveform of the signal on line 109 is plotted in Figure 6B. The signal on line 109 represents the absolute frequency difference. The operation of flip-flops 110 and 111, which correspond respectively to flip-flops 66 and 67 of the embodiment of Figure 3, is understood best if it is assumed that the signal on line 108 is leading the signal on line 109, as is shown in Figure 6B. When this condition is present, the frequency of the VCO is higher than the frequency of the reference oscillator.

Referring again to Figure 4, when the signal on line 108 leads the signal on line 109, flip-flop 110 always remain low because its clock (line 108) goes high before its data input (line 109) goes high. Conversely, flip-flop 111 will trigger once each cycle, and will trigger on the leading edge of the pulses on line 109 because its data input (line 108) is high at that time.

The outputs of flip-flops 110 and 111, for the case of the signal on line 108 is leading the signal on line 109, are plotted in Figure 6B. Similarly, the outputs of flip- flops 110 and 111, for the case of the signal on line 108 lags the signal on line 109, are also plotted in Figure 6B.

Connected to $\overline{Q}$ output of flip-flop 110 and Q output of flip-flop 111 are the two inputs of an exclusive OR gate 112. Exclusive OR gate 112 is functionally equivalent to OR gate 68 of Figure 3. The output of exclusive OR gate 112 is high when either (but not both) the Q output of flip-flop 111 is high or the $\overline{Q}$ output of flip-flop 110 is high. The output of exclusive OR gate 112 is connected to the reset terminal of a counter 113. The clock input of counter 113 is connected by a lead 90 to the output signal from the reference oscillator. The output Q of counter 113 is fed back to the reset inputs of flip-flops 110 and 111. The number of counts of counter 113 specifies the periods that flip-flops 110 or 111 remains in the Q high state. The Q output of flip-flop 110 is supplied via a line 114 to one of the inputs of an amplifier 116, and the Q output of flip-flop 111 is furnished via line 115 to the other input of amplifier 116.

Also applied to the inverting input of amplifier 116 connected to line 114 is the control voltage signal supplied via line 72 from the load division and sync control circuit 12 of Figure 2. A capacitor 121 (connected between the output and the inverting input of amplifier 116), and a capacitor 120 (connected between the non-inverting input and ground), cause amplifier 116 to provide at its output a signal which is an integral of the pulse train signals being provided at its inputs. This output signal from amplifier 116 is used to drive the voltage controlled oscillator.

The voltage controlled oscillator comprises NAND gates 124 and 125 and buffer amplifiers 126, 127 and

128. The output of the voltage controlled oscillator appearing on line 74 has a center frequency of 3.06 megahertz when there is no signal on line 72, and this output signal is fed to the wave generator 15 of Figure 1 for frequency control of the system.

In Figure 5, another embodiment of the frequency control of the present invention is shown. The reference oscillator includes a multi-stage counter 150 which divides the frequency of the basic oscillator and provides at its Q2 and Q3 outputs frequency signals to the inputs of an exclusive OR gate 151. Exclusive OR gate 151 produces the phase shift required for determining whether the frequency of the voltage controlled oscillator is higher or lower than the reference oscillator frequency. Thus, exclusive OR gate 151 produces the same function as flip-flop 93 of Figure 4. The inputs of an exclusive OR gate 152 are connected to the output of exclusive OR gate 151 and the output of the voltage controlled oscillator 180 on line 74. Exclusive OR gate 152 performs the same function as exclusive OR gate 95 of Figure 4. The inputs of an exclusive OR gate 153 are connected to the Q3 output of counter 150 and the output of voltage controlled oscillator 180 and it performs the same function as exclusive OR gate 94 of Figure 4.

The filtering and squaring function is performed in the embodiment of Figure 5 by resistors 154 and 155, capacitors 156 and 157, and NAND gate 158. NAND 158 includes an internal Schmitt trigger. These components produce the same function as buffer amplifier 103 and its associated components in Figure 4.

Resistors 159 and 160, capacitors 161 and 162 and NAND gate 163 perform the same filtering and squaring function for the output signal of exclusive OR gate 153. These components thus produce the same function as do buffer amplifier 107 and its associated components in Figure 4.

Flip-flops 164 and 165 perform the same functions respectively as produced by flip-flops 110 and 111 of Figure 4. An exclusive OR gate 166 produces the inverse function as produced by exclusive OR gate 112 of Figure 4, but because of the inversion produced by NAND gate 168, the output of NAND gate 168 is analogous to the output produced by exclusive OR gate 112.

The embodiment of Figure 5 also includes additional circuitry used to eliminate any ambiguity which occurs when the period of the count time of the counter exceeds the period of the frequency difference between the reference oscillator output and the output of the voltage controlled oscillator. If the count time of the embodiment of Figure 4 exceeds the frequency difference time, counter 113 will continue to count into the next cycle. This interval overlap produces an ambiguity. As can be seen from the trace labeled flip-flop 111 (line 108 lead) of Figure 6B, if the period of counter 113 extends into the period of the next count, the flip-flop 111 will not return to its reset state until after its clock pulse is received. When flip-flop 111 returns to its reset state, it will go low and remain so until the next clock signal is received. Thus, when the period of the counter 113 exceeds the frequency difference, the output of flip-flop 111 will go low rather than remain at the proper high level. The same ambiguity problem exists with respect to flip-flop 110. In order to correct this ambiguity problem in the embodiment of Figure 4, additional circuitry has been added to the embodiment of Figure 5.

NAND gates 167 and 168 and a capacitor 169 and a resistor 170 are the additional circuitry added to the embodiment of Figure 5 to prevent the ambiguity condition. This circuit produces a negative-going transient* at the input of NAND gate 168 whenever the output of both NAND gates 158 and 163 goes high. NAND gate 168

* see the last waveshape in Figure 6B

inverts the negative-going transient at its input. In this way, a positive transient is always applied to the reset input of counter 171 to restart its counting cycle. Thus, when the frequency error is great, and the time period of counter 171 exceeds the time period of the frequency difference, the Q outputs of flip-flops 164 or 165 applied to the voltage control oscillator via amplifier 172 will remain at their high state rather than being reset to the low state for part of every other frequency difference cycle.

In the embodiment of Figure 5, amplifier 172 and its associated components perform the same function that is produced by amplifier 116 and its associated components of Figure 4.

The voltage controlled oscillator of the embodiment of Figure 5 is indicated by reference numeral 180.

CLAIMS

1. Apparatus for frequency adjusting an alternating current machine comprising:

a) a reference oscillator having an output (213,60)

b) a signal controlled oscillator (71) for producing a controlled output frequency signal (74), having an input and an output effectively connected to said alternating current machine;

c) first means (63,65,67) for producing a signal proportional to the frequency difference between said reference oscillator output and said controlled output frequency (74);

d) second means (61,62,64,66) for providing a signal indicative of whether said controlled output frequency is above or below the frequency of said reference oscillator output; and

e) means (68-70) for supplying a drive signal to said input of said signal controlled oscillator in response to said signal of said first means and said signal of said second means.

2. Apparatus according to Claim 1, wherein said first means comprises:

a) first discriminator means (63) for furnishing an output signal proportional to the phase difference between said reference oscillator output and said controlled output frequency signal; and

b) first filter means (65) for producing a filtered version of said output signal of said first discriminator means (63).

3. Apparatus according to Claim 2, wherein said second means comprises:

a) phase shift means (61) for introducing a desired phase shift to said reference oscillator (70) output;

b) second discriminator means (62) for supplying an output signal inputs connected proportional to the phase difference between said phase-shifted reference oscillator output and said controlled output frequency signal (74);

c) second filter means (64) for providing a filtered version of said output signal of said second discriminator means (62); and

d) means (66-69) for generating an output signal indicating the phase relationship between said output signal of said first filter means and said output signal of said second filter means (64).

4. Apparatus according to Claim 3, wherein said means for generating an output signal indicating the phase relationship comprises:

a) a first flip-flop (67) having a clock input effectively connected to said output signal of said first filter means, a data input effectively connected to said output of said second filter means, and an output; and

b) a second flip-flop (66) having a clock input effectively connected to said output of said second filter means, a data input effectively connected to said output of said first filter means, and an output.

5. Apparatus according to Claim 4, wherein said means for supplying a drive signal comprises:

a) an amplifier (70) having inputs effectively connected to said outputs of said first and second flip-flops, and an output effectively connected to said input of said signal controlled oscillator;

b) logic means (68) having inputs effectively connected to said outputs of said first and second flip-flops, and an output; and

c) counter means (69) having a reset input effectively connected to said output of said logic means, a clock input effectively connected to said reference oscillator output, and an output effectively connected to set or reset inputs of said flip-flops (66,67).

6. Apparatus for producing a controlled frequency output, for use for an AC machine, comprising:

a) a reference oscillator (60) having an output;

b) first discriminator means (63) for producing an output signal proportional to the phase difference between said reference oscillator (60) output and a signal present at an input;

c) phase shift means (61) for introducing a desired phase shift to said reference oscillator (60) output;

d) second discriminator means (62) for providing an output signal proportional to the phase difference between said output of said phase shift means and a signal present at an input;

e) first filter means (65) for furnishing a filtered version of said output of said first discriminator means (63);

f) second filter means (64) for supplying a filtered version of said output of said second discriminator means (62);

g) a first flip-flop (67) having a clock input effectively connected to said output of said first filter means and an input effectively connected to said output of said second filter means (64);

h) a second flip-flop (66) having a clock input effectively connected to said output of said first filter means and an input effectively connected to said output of said first filter means (65);

Claim 6 (continued)

i) logic means (68) having a first input effectively connected to said output of said first flip-flop (67), a second input effectively connected to said output of said second logic flip-flop (66), and an output;

j) counter means (69) having a reset input effectively connected to said output of said logic means, a clock input effectively connected to said reference oscillator output, and an output effectively connected to set or reset inputs of said first and second flip-flop (67,66);

k) an amplifier (70) having a first input effectively connected to said output of said first flip-flop (67), a second input effectively connected to said output of said second flip-flop (66) and an output;

l) control signal input means effectively connected to one of said inputs of said amplifier (70); and

m) a controlled oscillator (71) having an input effectively connected to said output of said amplifier (70) and having an output effectively connected to said inputs of said first discriminator means and second discriminator means, its output providing a controlled frequency signal (74).

7. Apparatus for connecting alternating current systems in parallel having individual frequency controls (13) with independent reference oscillators ($R\text{-}O_1$, $R\text{-}O_2$) comprising:

a) contactor means (21) for connecting the outputs of said alternating current systems in parallel;

b) means (10,11,D) for determining a desired circulating component of the current between the outputs of said parallel-connected systems; and

c) means (12) for adjusting the individual frequency control of each parallel-connected alternating current system in accordance with said desired circulating current component and in accordance with an output signal of said individual reference oscillator associated with said individual frequency control (13).

FIG 1

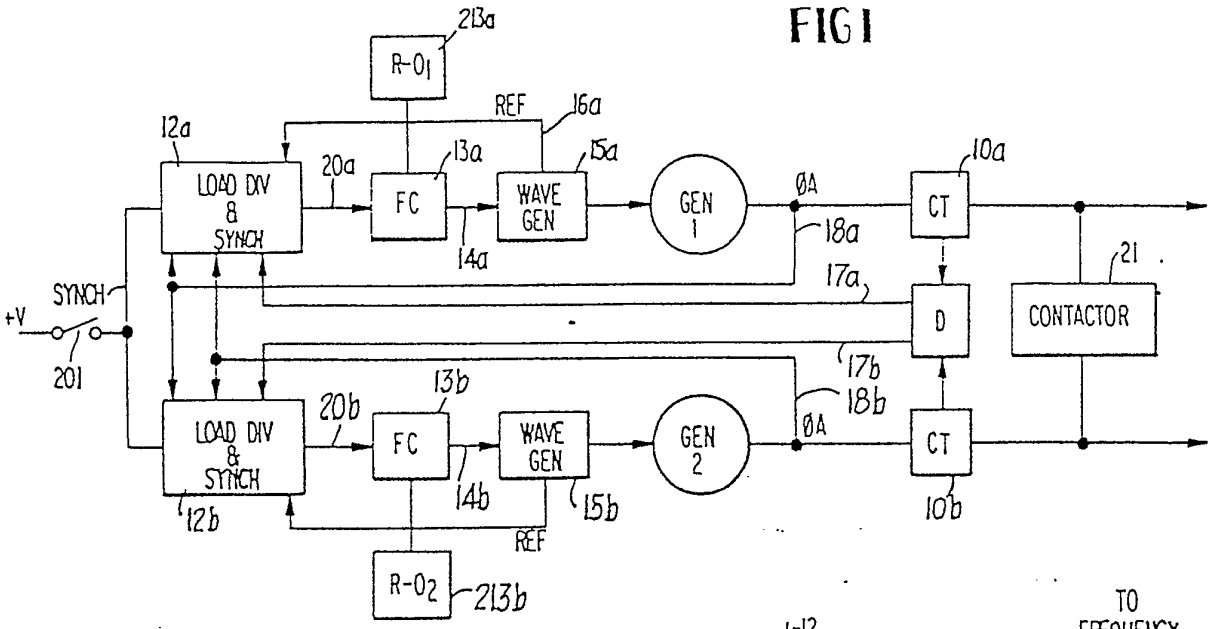
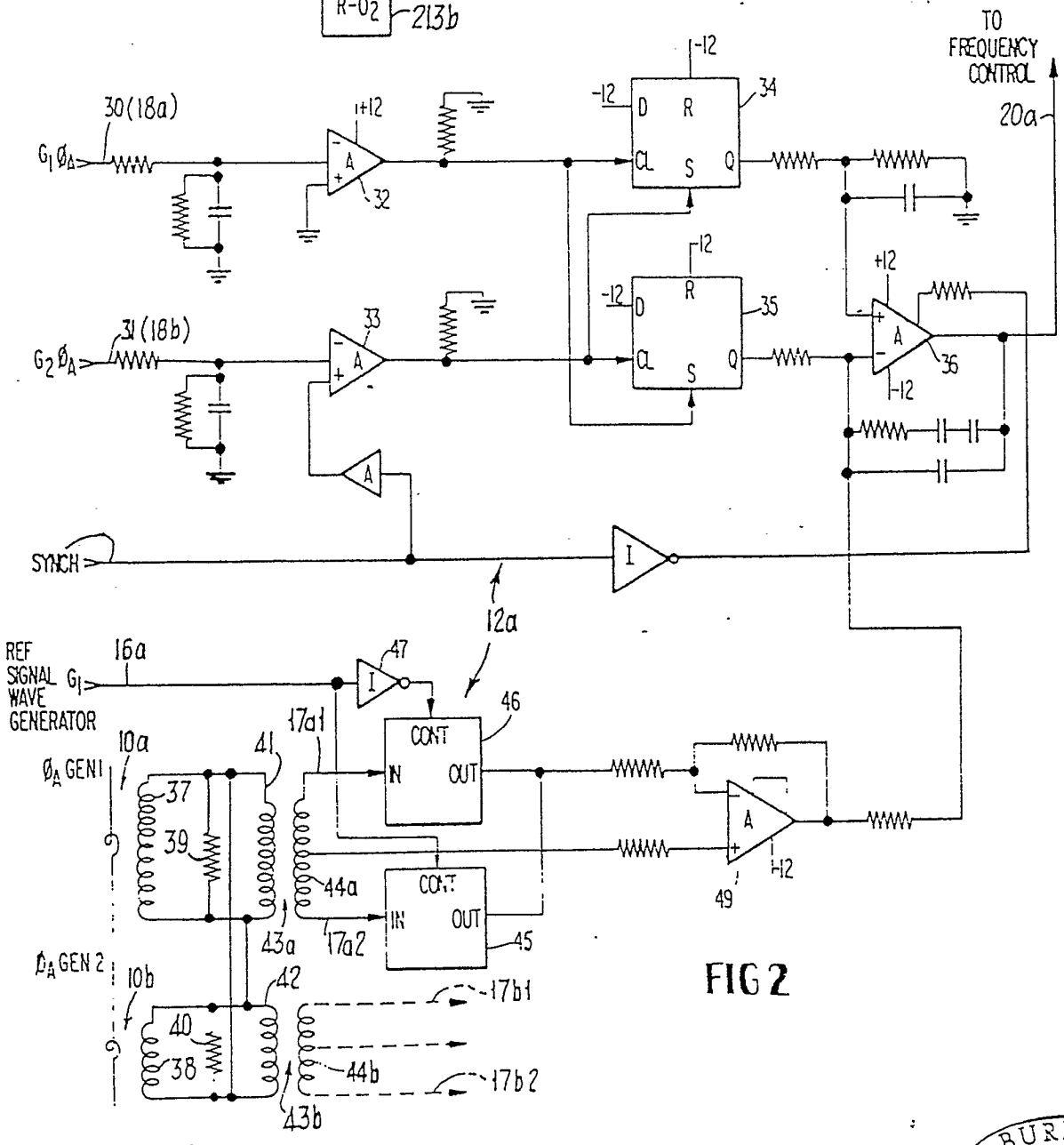


FIG 2



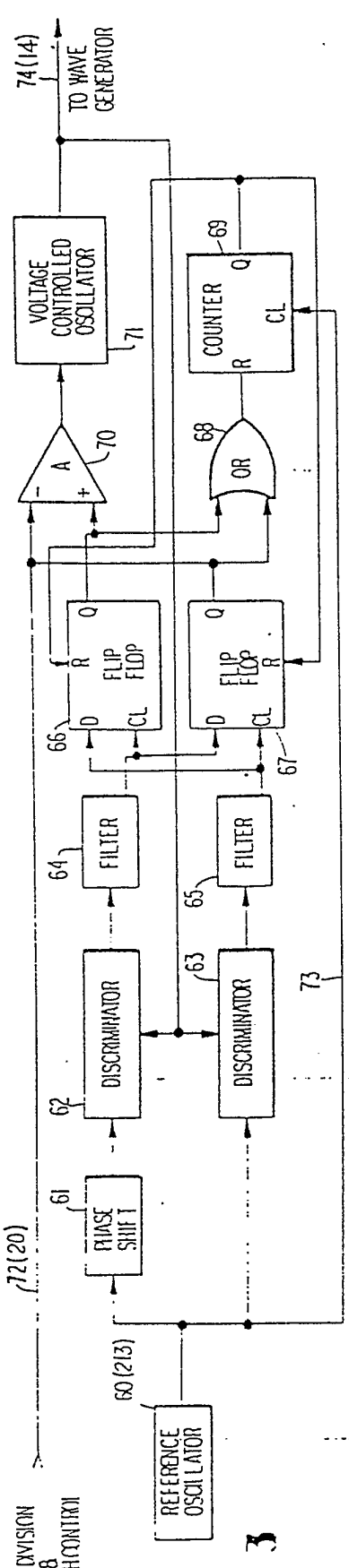


FIG 3

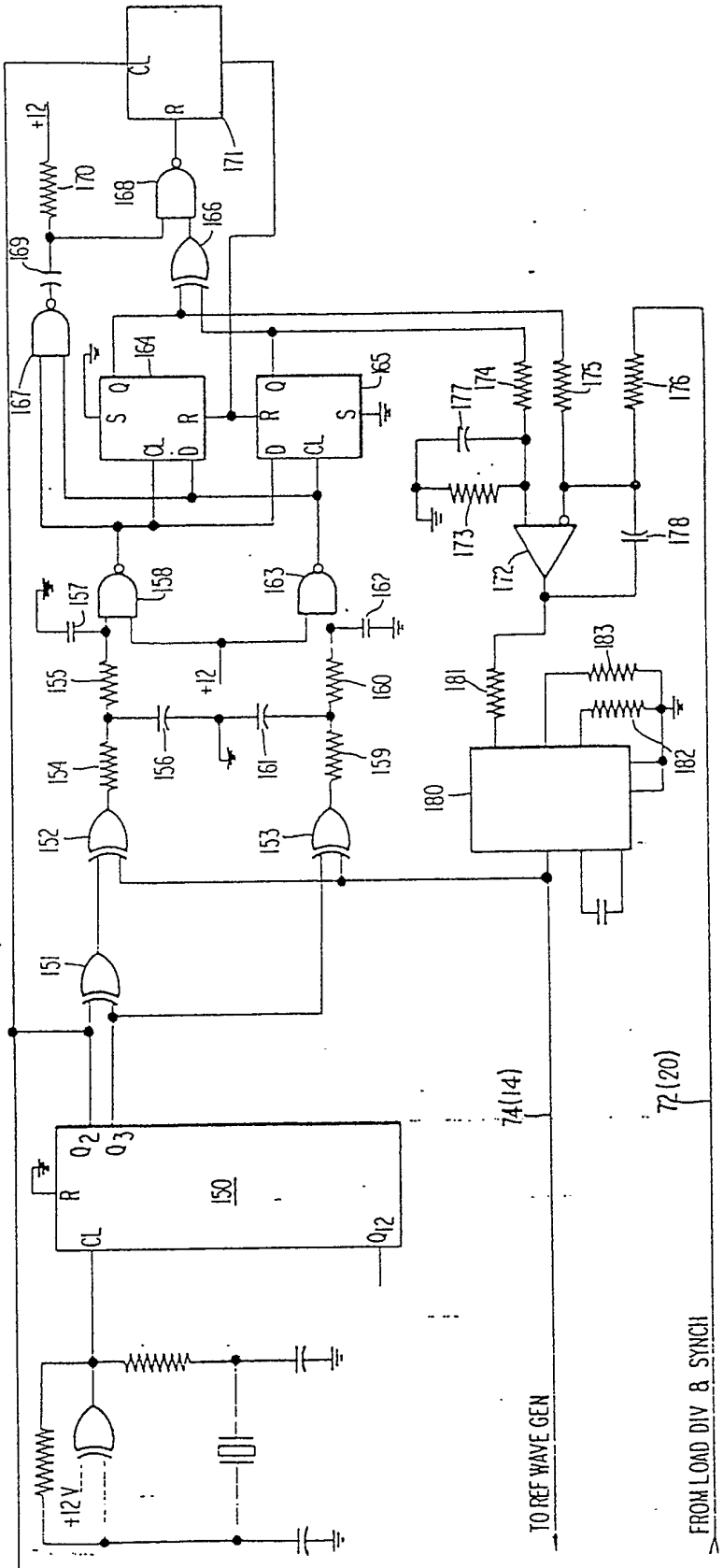


FIG 5

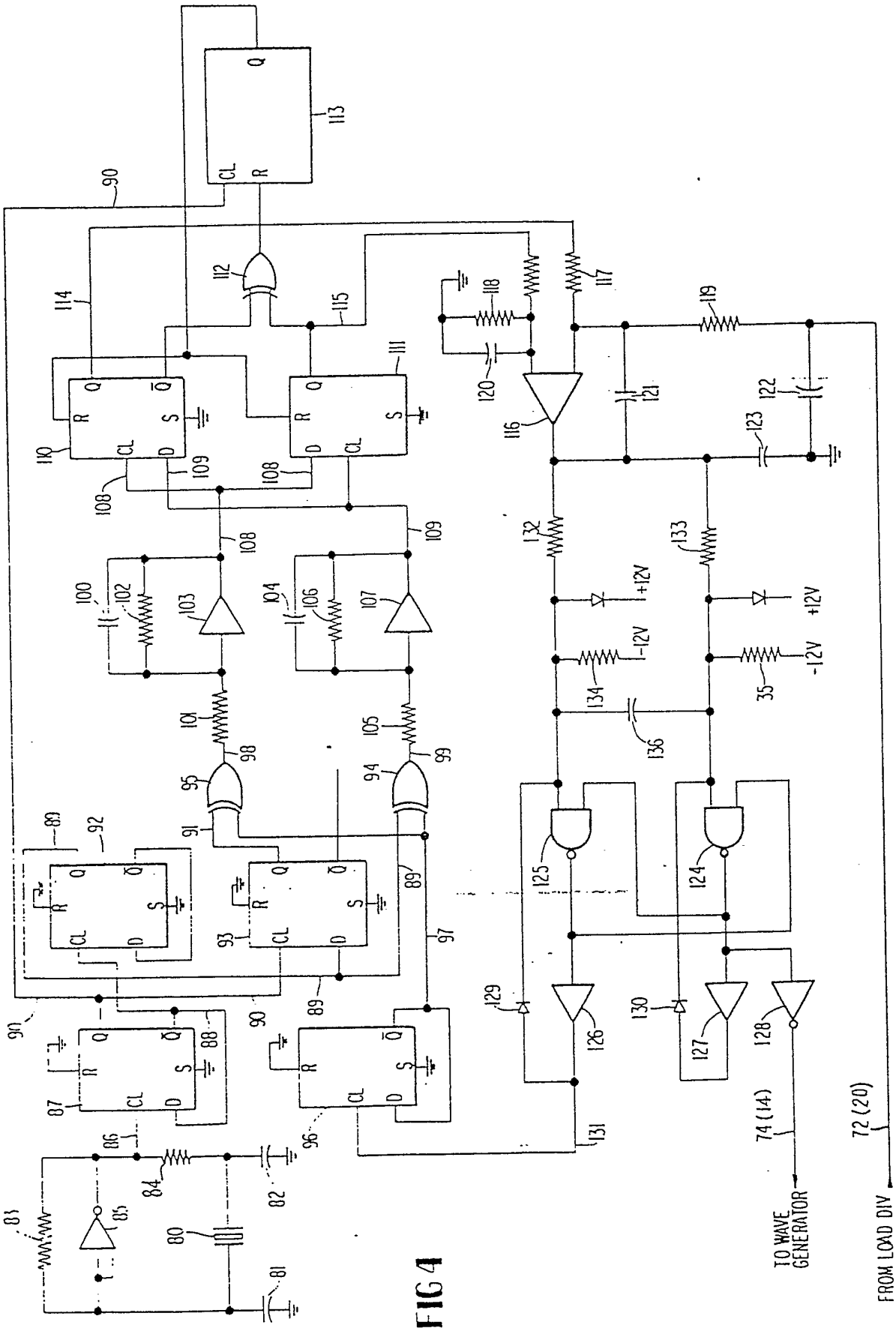


FIG 4

FIG 6a

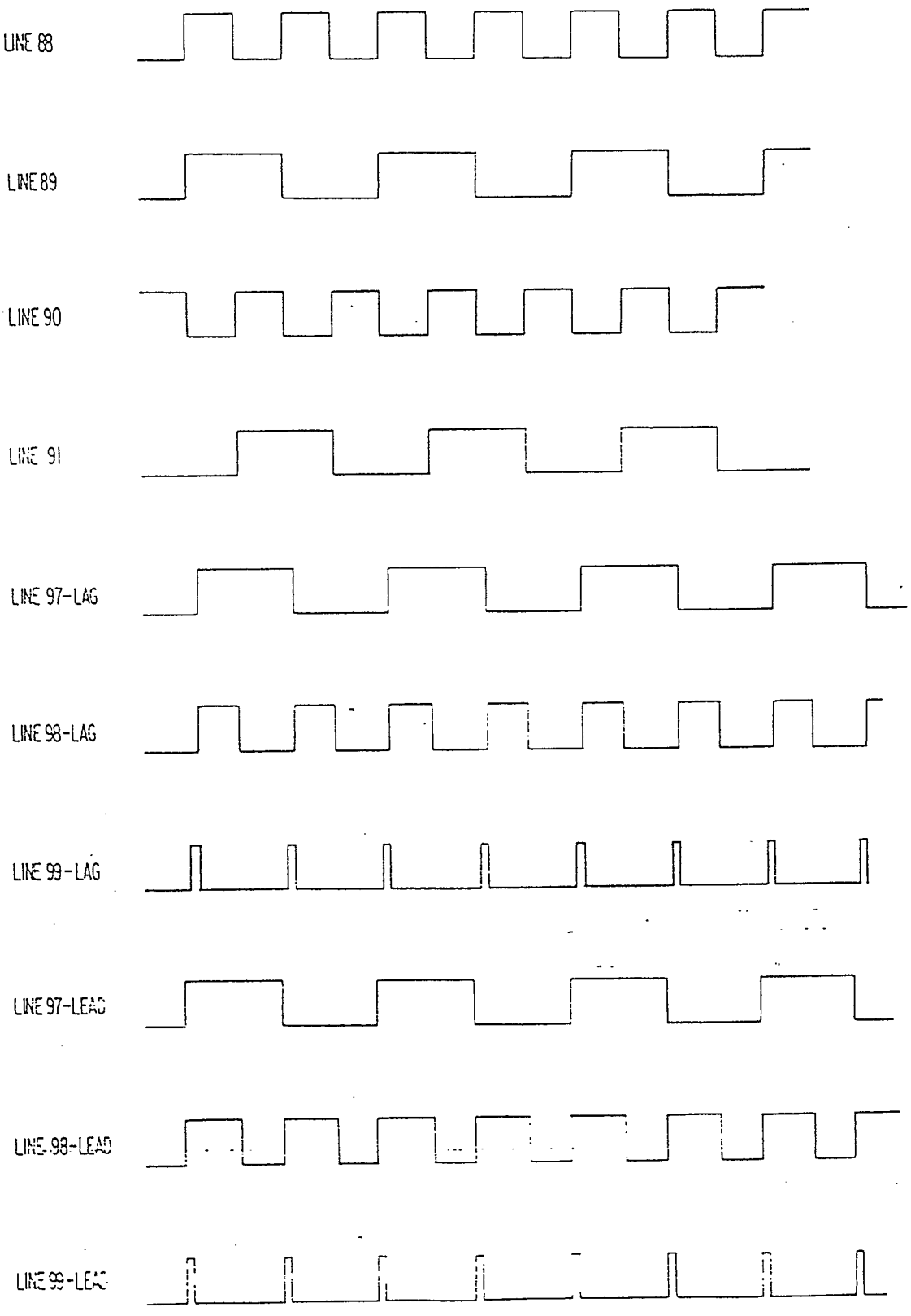
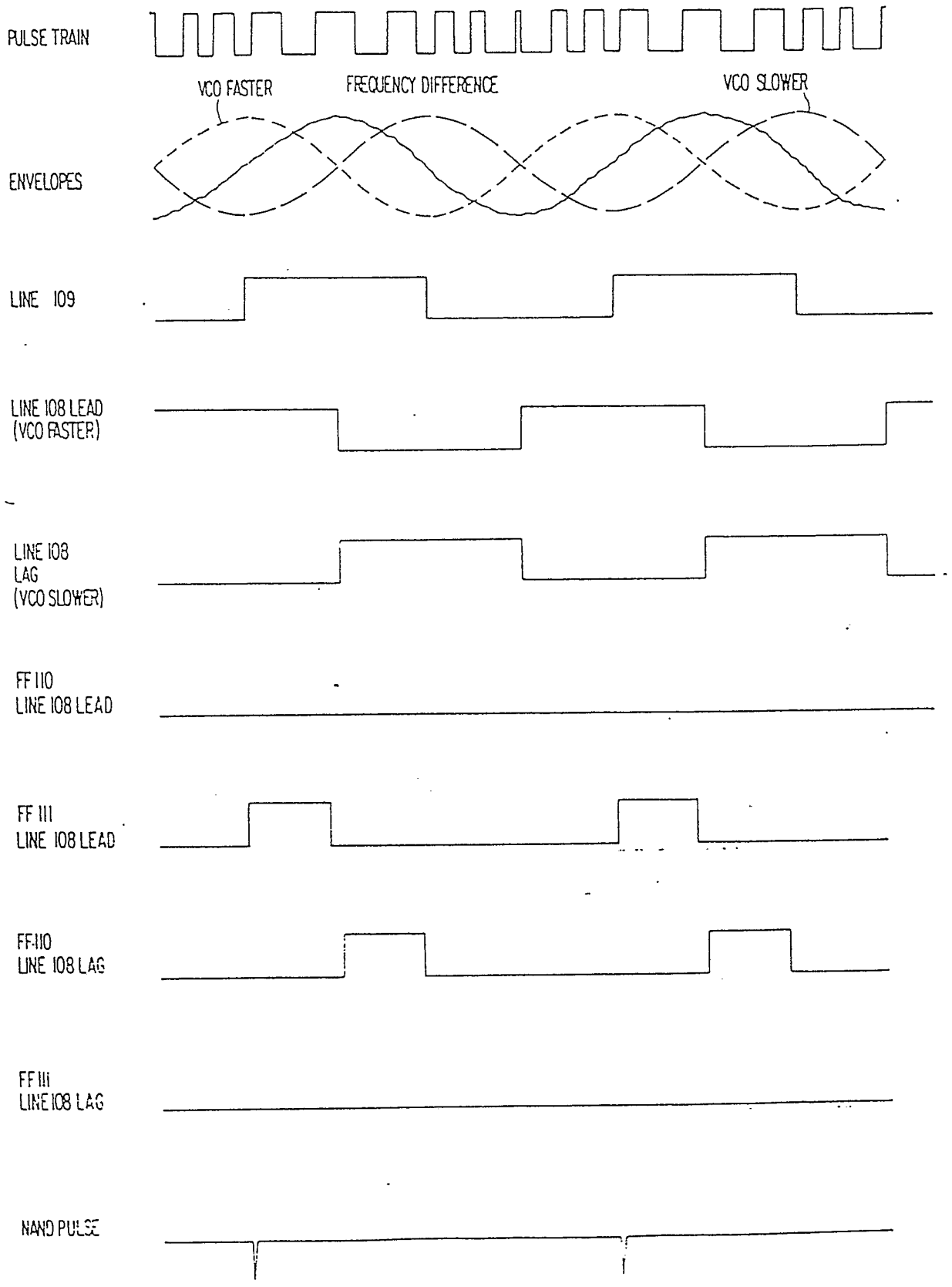


FIG 6b



INTERNATIONAL SEARCH REPORT

International Application No PCT/US80/00614

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[3] H02J 3/40; H02P 5/34
US. Cl. 307/87 ; 318/66

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	307/87,73,86,85,3,129,58,57,27 328/133,134 318/66

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	Bowlus & Nims; Parallel Operation of Aircraft Alternators Using Electronic Frequency Changers; ALEE Technical Paper 47-5; October 1946; New York	1- 7

* Special categories of cited documents: [15]

"A" document defining the general state of the art

"E" earlier document but published on or after the international filing date

"L" document cited for special reason other than those referred to in the other categories

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but on or after the priority date claimed

"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [1]	Date of Mailing of this International Search Report [2]
5-Aug. 1980	29 AUG 1980
International Searching Authority [1]	Signature of Authorized Officer [19]
ISA/US	Stafford D. Griffin

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PRIMARY EXAMINER
ART UNIT 211