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(54) Title: METHOD AND APPARATUS FOR ANTI-ISLANDING OF DISTRIBUTED POWER GENERATION SYSTEMS

(57) Abstract: A method and apparatus for anti-islanding of distributed power generation systems having an inverter comprising a phase locked loop (PLL), a phase shift generator for injecting a phase shift into the PLL during at least one sample period, and a phase error signature monitor for monitoring at least one phase error response of the PLL during the at least one sample period.

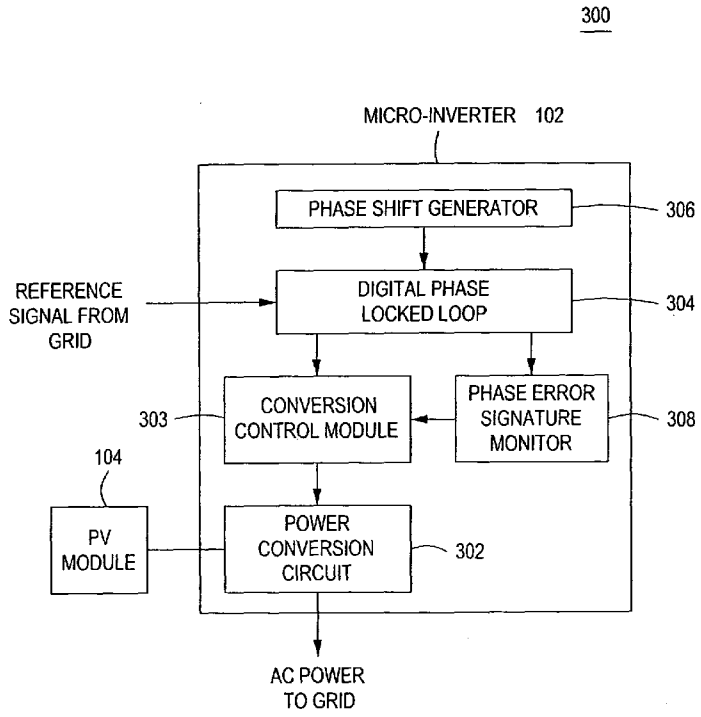

FIG. 3

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METHOD AND APPARATUS FOR ANTI-ISLANDING OF DISTRIBUTED POWER GENERATION SYSTEMS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of United States provisional patent application serial number 60/959,644, filed July 16, 2007, which is herein incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] Embodiments of the present disclosure generally relate to a method and apparatus for anti-islanding of distributed power generation systems.

Description of the Related Art

[0003] Solar panels have historically been deployed in mostly remote applications, such as remote cabins in the wilderness or satellites, where commercial power was not available. Due to the high cost of installation, solar panels were not an economical choice for generating power unless no other power options were available. However, the worldwide growth of energy demand is leading to a durable increase in energy cost. In addition, it is now well established that the fossil energy reserves currently being used to generate electricity are rapidly being depleted. These growing impediments to conventional commercial power generation make solar panels a more attractive option to pursue.

[0004] Solar panels, or photovoltaic (PV) modules, convert energy from sunlight received into direct current (DC). The PV modules cannot store the electrical energy they produce, so the energy must either be dispersed to an energy storage system, such as a battery or pumped hydroelectricity storage, or dispersed by a load. One option to use the energy produced is to employ inverters to convert the DC current into an alternating current (AC) and couple the AC current to the

commercial power grid. The power produced by such a distributed generation (DG) system can then be sold to the commercial power company.

[0005] Under some conditions, a grid-connected DG system may become disconnected from the utility grid, resulting in a potentially dangerous condition known as "islanding". During islanding, the utility cannot control voltage and frequency in the DG system island, creating the possibility of damage to customer equipment coupled to the island. Additionally, an island may create a hazard for utility line workers or the general public by causing a line to remain energized that is assumed to be disconnected from all energy sources. In order to mitigate the potential hazards of islanding, the IEEE standard 929-2000 requires inverters in a DG system detect the loss of the utility grid and shut down the inverter within two seconds. As such, all commercially available inverters, including each micro-inverter of a micro-inverter array, must be equipped with an inverter-based anti-islanding capability. Current techniques employed to meet such a standard require substantial power, thus reducing the efficiency of the inverter.

[0006] Therefore, there is a need in the art for a method and apparatus for fast detection of islanding in a grid-connected inverter.

SUMMARY OF THE INVENTION

[0007] Embodiments of the present invention generally relate to a method and apparatus for anti-islanding of distributed power generation systems having an inverter comprising a phase locked loop (PLL), a phase shift generator for injecting a phase shift into the PLL during at least one sample period, and a phase error signature monitor for monitoring at least one phase error response of the PLL during the at least one sample period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which

are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0009] Figure 1 is a block diagram of a system for distributed generation in accordance with one or more embodiments of the present invention;

[0010] Figure 2 is a block diagram of a control module in accordance with one or more embodiments of the present invention;

[0011] Figure 3 is a block diagram of a micro-inverter in accordance with one or more embodiments of the present invention;

[0012] Figure 4 is a block diagram of a Digital Phase Locked Loop in accordance with one or more embodiments of the present invention.

[0013] Figure 5 is a block diagram of a phase error signature monitor in accordance with one or more embodiments of the present invention;

[0014] Figure 6 is a graphical diagram of a phase error response in the presence of a connected grid in accordance with one or more embodiments of the present invention;

[0015] Figure 7 is a graphical diagram of a phase error response in the absence of a connected grid in accordance with one or more embodiments of the present invention;

[0016] Figure 8 is a flow diagram of a method for detecting an islanding state in a grid-connected inverter in accordance with one or more embodiments of the present invention; and

[0017] Figure 9 is a flow diagram of a method for synchronizing phase shift injection in a plurality of micro-inverters in accordance with one or more embodiments of the present invention.

DETAILED DESCRIPTION

[0018] Figure 1 is a block diagram of a system 100 for distributed generation (DG) in accordance with one or more embodiments of the present invention. This diagram only portrays one variation of the myriad of possible system configurations. The present invention can function in a variety of distributed power generation environments and systems.

[0019] The system 100 comprises a plurality of micro-inverters 102_1, 102_2 . . . 102_n, collectively referred to as micro-inverters 102, a plurality of PV modules 104_1 , 104_2. . . 104_n, collectively referred to as PV modules 104, an AC bus 106, a load center 108, and an array control module 110.

[0020] Each micro-inverter 102_1, 102_2 . . . 102_n is coupled to a PV module 104_1 , 104_2. . . 104_n, respectively. The micro-inverters 102 are further coupled to the AC bus 106, which in turn is coupled to the load center 108. The load center 108 houses connections between incoming power lines from a commercial power grid distribution system and the AC bus 106. The micro-inverters 102 convert DC power generated by the PV modules 104 into AC power, and meter out AC current that is in-phase with the AC commercial power grid voltage. The system 100 couples the generated AC power to the commercial power grid via the load center 108.

[0021] A control module 110 is coupled to the AC bus 106. The control module 110 is capable of issuing command and control signals to the micro-inverters 102 in order to control the functionality of the micro-inverters 102.

[0022] Figure 2 is a block diagram of a control module 110 in accordance with one or more embodiments of the present invention. The control module 110 comprises a transceiver 202 coupled to at least one central processing unit (CPU) 204. The CPU is additionally coupled to support circuits 206, and a memory 208. The CPU 204 may comprise one or more conventionally available microprocessors. Alternatively, the CPU 204 may include one or more application specific integrated circuits (ASIC). The support circuits 206 are well known circuits used to promote functionality of the central processing unit. Such circuits include, but are not limited

to, a cache, power supplies, clock circuits, buses, network cards, input/output (I/O) circuits, and the like.

[0023] The memory 208 may comprise random access memory, read only memory, removable disk memory, flash memory, and various combinations of these types of memory. The memory 208 is sometimes referred to as main memory and may, in part, be used as cache memory or buffer memory. The memory 208 generally stores the operating system 214 of the control module 110. The operating system 214 may be one of a number of commercially available operating systems such as, but not limited to, SOLARIS from SUN Microsystems, Inc., AIX from IBM Inc., HP-UX from Hewlett Packard Corporation, LINUX from Red Hat Software, Windows 2000 from Microsoft Corporation, and the like.

[0024] The memory 208 may store various forms of application software, such as micro-inverter control software 210. The transceiver 202 communicably couples the control module 110 to the micro-inverters 102 to facilitate command and control of the micro-inverters 102. The transceiver 202 may utilize wireless or wired communication techniques for such communication. In one embodiment, the micro-inverter control software 210 synchronizes the anti-islanding hardware and/or software of the micro-inverters 102, which is further described below.

[0025] Figure 3 is a block diagram of a micro-inverter 102 in accordance with one or more embodiments of the present invention. The micro-inverter 102 comprises a power conversion circuit 302, a conversion control module 303, a digital phase-locked loop (DPLL) 304, a phase shift generator 306, and a phase error signature monitor 308. The DPLL 304 is coupled to the conversion control module 303, the phase shift generator 306, and the phase error signature monitor 308. The conversion control module 303 is further coupled to the phase error signature monitor 308 and the power conversion circuit 302. The power conversion circuit 302 is coupled to the PV module 104 and acts to convert a DC current from the PV module 104 to an AC current; the conversion control module 303 provides operative control of the power conversion circuit 302. The DPLL 304 receives a grid voltage

reference signal and locks to the frequency of the grid voltage; additionally the DPLL receives a nominal cycle input that provides the nominal period of the grid system in order to prevent the DPLL 304 from changing when the nominal grid frequency changes. The DPLL 304 provides an input to the conversion control module 303 that drives the power conversion circuit 302 to inject the generated AC output current in phase with the grid as required by the relevant standards.

[0026] The phase shift injector 306 injects a small phase shift through the DPLL 304. In one embodiment, where the connected grid operates at a frequency of 60 Hz, a phase shift of magnitude 50 microseconds over a period of one cycle (i.e., 16.7 milliseconds) is injected at 0.5 second intervals; such an injected phase shift represents a phase shift of one degree and causes an insignificant distortion to the current injected into the grid and/or load. Alternative embodiments may utilize different phase shift magnitudes, durations, and/or injection intervals. While the micro-inverter 102 remains connected to the utility grid, the DPLL 304 produces a certain phase error response as a result of the injected phase shift. If the micro-inverter 102 becomes disconnected from the grid, the DPLL 304 produces a different phase error response as a result of the injected phase shift. Such phase error responses are shown in Figures 6 and 7 and further described below. The phase error signature monitor 308 monitors the phase error response of the DPLL 304 to determine when the micro-inverter 102 is no longer connected to the grid, creating an island. In the event of an island, the phase error signature monitor 308 provides a deactivation signal to the conversion control module 303 to shut down the power conversion circuit 302.

[0027] Figure 4 is a block diagram of a Digital Phase Locked Loop (DPLL) 304 in accordance with one or more embodiments of the present invention. Such a DPLL 304 can be implemented in hardware, software, or a combination of hardware and software. The DPLL 304 comprises a phase detector 402, an adder 404, a Proportional Integral Derivative (PID) controller 406, an adder 408, and a numerically controlled oscillator (NCO) 410. The phase detector 402 receives a first input from a reference signal of the grid voltage frequency as described above; the output of the

NCO 410 is coupled to the phase detector 402 and provides a second input. The output from the NCO 410 and the reference signal of the grid voltage frequency are compared by the phase detector 402 to produce a resulting phase error. This phase error output of the phase detector 402 is coupled to the adder 404 along with the output of the phase shift generator 306. The phase shift generator 306 injects a phase shift as described above. The resulting output of the adder 404 is coupled to the PID controller 406. In one embodiment, the PID controller 406 acts as the loop filter for the DPLL 304; alternative embodiments may comprise other forms of loop filter implementations. The PID controller 406 output comprises a phase error response that is coupled to the phase error signature monitor 308. Additionally, the PID controller 406 output is coupled to the adder 408 along with a nominal cycle time input. In one embodiment, the nominal cycle time is 1/60 seconds. The resulting output of the adder 408 is coupled to the NCO 410. The NCO 410 output, in addition to being coupled to the phase detector 402, is coupled to the conversion control module 303 to drive the generated AC current injection into the grid as described above.

[0028] Figure 5 is a block diagram of a phase error signature monitor 308 in accordance with one or more embodiments of the present invention. Such a phase error signature monitor 308 can be implemented in hardware, software, or a combination of hardware and software. The phase error signature monitor 308 comprises a resettable integrator 502 coupled to a sampler 504, and a resettable integrator 509 coupled to a sampler 510. The outputs of the samplers 504 and 510 are coupled to a subtractor 512. The output of the subtractor 512 is coupled to an input of a comparator 506. A reference threshold input is coupled to a second input of the comparator 506. The output of the comparator 506 is coupled to an islanding decision controller 508.

[0029] The phase error response at the output of the PID controller 406 is coupled to the resettable integrators 502 and 509. During a sample period, the resettable integrators 502 and 509 are both reset, and the resettable integrator 509 integrates a baseline phase error response over a baseline period. In one

embodiment, the sample period is 0.5 seconds and the baseline period is seven consecutive grid cycles (i.e., 116.667 milliseconds for a 60 Hz grid voltage). Following the baseline period, the sampler 510 samples the output of the integrator 509 and provides the resulting baseline integrated phase error response value to the subtractor 512. Also following the baseline period, a phase shift is injected; in one embodiment, the phase shift is injected during the grid cycle immediately following the baseline period. The resettable integrator 502 integrates the phase error response resulting from the injected phase shift over an integration period. In one embodiment, the integration period is seven consecutive grid voltage cycles immediately following the phase shift injection (e.g., 116.667 milliseconds for a 60 Hz grid voltage). After the integration period, the sampler 504 samples the output of the integrator 502 and provides the resulting integrated phase error response value to the subtractor 512. The subtractor 512 subtracts the baseline integrated phase error response value from the integrated phase error response value resulting from the phase shift injection; the output of the subtractor 512 is provided to an input of the comparator 506. In alternative embodiments where the grid voltage frequency remains stable, the baseline integrated phase error response is not required, and the phase error signature monitor 308 can thusly be implemented without the resettable integrator 509, the sampler 510, and the subtractor 512. In such alternative embodiments, the output of the sampler 504 is coupled to the input of the comparator 506.

[0030] The comparator 506 compares the resulting difference to a reference threshold. If the threshold is satisfied, the sample period containing the injected phase shift is considered indicative of a potential grid disconnection. The output of the comparator 506 is coupled to the islanding decision controller 508. The islanding decision controller 508 determines whether "n" out of the "p" most recent sample periods indicate a potential grid disconnection; if this condition is satisfied, an islanding state is declared and the islanding decision controller 508 issues a control signal to the conversion control module 303 to shut down the power conversion circuit 302.

[0031] Figure 6 is a graphical diagram of a phase error response 600 in the presence of a connected grid in accordance with one or more embodiments of the present invention. In the presence of a connected grid, the phase shift injected by the phase shift generator 306 causes an insignificant distortion to the current injected into the grid and produces no voltage impact on the grid. Thus, the grid voltage reference signal to the phase detector 402 does not change as a result of the injected phase shift, and the DPLL 304 compensates for the injected phase error such that the bipolar phase error response 600 is generated. Integrating the bipolar phase error response 600 over time results in a value of about zero. Thus, the reference threshold input to the comparator 506 can be set such it is not exceeded by the difference between the baseline integrated phase error response and the integrated phase error response resulting from the injected phase shift, and the output of the comparator 506 indicates a continued grid connection.

[0032] Figure 7 is a graphical diagram of a phase error response 700 in the absence of a connected grid in accordance with one or more embodiments of the present invention. When the grid becomes disconnected from the micro-inverter 102, the grid voltage reference signal is no longer provided to the phase detector 402 and is replaced by a reference signal that is a product of the inverter current and the impedance of a load coupled to the inverter. As a result, the DPLL 304 does not provide compensation for the injected phase error, resulting in the unipolar phase error response 700. Integrating the phase error response 700 over time results in an increasing integrated phase error response value. The difference between the baseline integrated phase error response and the increasing integrated phase error response resulting from the injected phase shift will at some point exceed the reference threshold input to the comparator 506, generating an output of the comparator 506 indicating a potential grid disconnection. The reference threshold can be set such that the loss of the grid connection is rapidly detected.

[0033] Figure 8 is a flow diagram of a method 800 for detecting an islanding state in a grid-connected inverter in accordance with one or more embodiments of the present invention. The method 800 begins at step 802 and proceeds to step 803. At

step 803, at the start of a sample period, a baseline phase error response of the DPLL of an inverter is accumulated over a baseline period. In one embodiment, a sample period of 0.5 seconds and a baseline period of 116.667 milliseconds (i.e., seven cycles for a 60 Hz grid voltage) are utilized. The method proceeds to step 804. At step 804, a small phase shift is injected through the DPLL of the inverter such that the phase shift causes an insignificant distortion to the current injected into the grid. In one embodiment, the phase shift has a magnitude of 50 microseconds over a duration of 16.7 milliseconds (i.e., one cycle for a 60 Hz grid voltage). In alternative embodiments, the phase shift is injected through the DPLL of a micro-inverter.

[0034] The method 800 proceeds to step 806. At step 806, a phase error response of the DPLL resulting from the injected phase shift is accumulated over an integration period; in one embodiment, an integration period of 116.667 milliseconds (i.e., seven cycles for a 60 Hz grid voltage) is utilized. At step 807, the accumulated baseline phase error response is subtracted from the accumulated phase error response resulting from the injected phase shift, and, at step 808, the resulting difference is compared to a threshold. If the resulting difference does not satisfy the threshold, the method 800 proceeds to step 810. If the current sample period has not elapsed, the method 800 waits at step 810; if the current sample period has elapsed, the method 800 returns to step 803.

[0035] If the resulting difference satisfies the threshold at step 808, the method 800 proceeds to step 812. At step 812, the current sample period is flagged as indicating a potential grid disconnection. At step 814, the method 800 determines whether "n" potential grid disconnections have occurred within the "p" most recent consecutive sample periods; in one embodiment, the method 800 determines whether two potential grid disconnections have occurred within the three most recent consecutive sample periods. If the n-out-of-p potential grid disconnections have not occurred, the method 800 proceeds to step 810. If the n-out-of-p potential grid disconnections have occurred, the method 800 proceeds to step 816, where an

islanding state is declared and the inverter is shut down. The method 800 then ends at step 818.

[0036] Figure 9 is a flow diagram of a method 900 for synchronizing phase shift injection in a plurality of micro-inverters in accordance with one or more embodiments of the present invention. The method 900 begins at step 902 and proceeds to step 904. At step 904, a control module coupled to a plurality of micro-inverters, such as the control module 110 coupled to micro-inverters 102 via the AC bus 106, broadcasts a message to the plurality of micro-inverters. In one embodiment, the message comprises a millisecond timestamp. The method proceeds to step 906. At step 906, each micro-inverter of the plurality of micro-inverters simultaneously injects a phase shift through its DPLL, such as in the method 800 described above. The method 900 then ends at step 908.

[0037] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims:

1. Apparatus for converting DC power to AC power, comprising:

a phase locked loop (PLL);

a phase shift generator for injecting a phase shift into the PLL during at least one sample period; and

a phase error signature monitor for monitoring at least one phase error response of the PLL during the at least one sample period.

2. The apparatus of claim 1, wherein the phase error signature monitor:

integrates the at least one phase error response over at least one integration period to obtain at least one integrated phase error response;

compares the at least one integrated phase error response to at least one threshold; and

flags the at least one sample period as indicative of a possible islanding state when the at least one integrated phase error response satisfies the at least one threshold.

3. The apparatus of claim 2, wherein the phase error signature monitor declares an islanding state when a first number of the at least one sample period within a second number of the at least one sample period are flagged as indicative of a possible islanding state.

4. The apparatus of claim 3, wherein the phase error signature monitor comprises at least one resettable integrator, a comparator, at least one sampler, a subtractor, and an islanding decision controller.

5. The apparatus of claim 4, wherein the islanding decision controller determines when the first number of the at least one sample period within the second number of the at least one sample period are flagged as indicative of a possible islanding state.

6. The apparatus of claim 5, wherein the second number of the at least one sample period are consecutive sample periods.

7. The apparatus of claim 6, wherein the phase shift is of a magnitude of 50 microseconds over a single cycle of a frequency of a commercial power grid, wherein the commercial power grid is coupled to the inverter.

8. The apparatus of claim 1, wherein the inverter is a micro-inverter.

9. The apparatus of claim 1, wherein the at least one phase error response comprises a first phase error response and a second phase error response, wherein the first phase error response occurs prior to an injected phase shift and the second phase error response occurs after the injected phase shift.

10. The apparatus of claim 9, wherein the phase error signature monitor:

integrates the first phase error response over a first integration period to obtain a first integrated phase response;

integrates the second phase error response over a second integration period to obtain a second integrated phase error response;

compares a difference between the first integrated phase error response and the second integrated phase error response to a threshold; and

flags the at least one sample period as indicative of a possible islanding state when the difference satisfies the threshold.

11. A system, comprising:

a plurality of inverters, wherein each inverter of the plurality of inverters comprises a phase locked loop (PLL), a phase shift generator for injecting a phase shift into the PLL during at least one sample period, and a phase error signature monitor for monitoring at least one phase error response of the PLL during the at least one sample period; and

a controller coupled to the plurality of inverters, wherein the controller communicates a message to the plurality of inverters that causes the phase shift

generator of each of the inverters of the plurality of inverters to inject the phase shift simultaneously into the plurality of inverters.

12. The system of claim 11, wherein the at least one phase error response comprises a first phase error response and a second phase error response, wherein the first phase error response occurs prior to an injected phase shift and the second phase error response occurs after the injected phase shift.

13. The system of claim 11, wherein the plurality of inverters is a plurality of micro-inverters.

14. A method, comprising:

injecting a phase shift into a phase locked loop (PLL) of an inverter, wherein the phase shift is injected during at least one sample period;

integrating at least one phase error response of the PLL over at least one integration period to obtain at least one integrated phase error response;

comparing the at least one integrated phase error response to at least one threshold; and

flagging the at least one sample period as indicative of a possible islanding state when the at least one integrated phase error response satisfies the at least one threshold.

15. The method of claim 14, further comprising declaring an islanding state when a first number of the at least one sample period within a second number of the at least one sample period are flagged as indicative of a possible islanding state.

16. The method of claim 15, wherein the second number of the at least one sample period are consecutive sample periods.

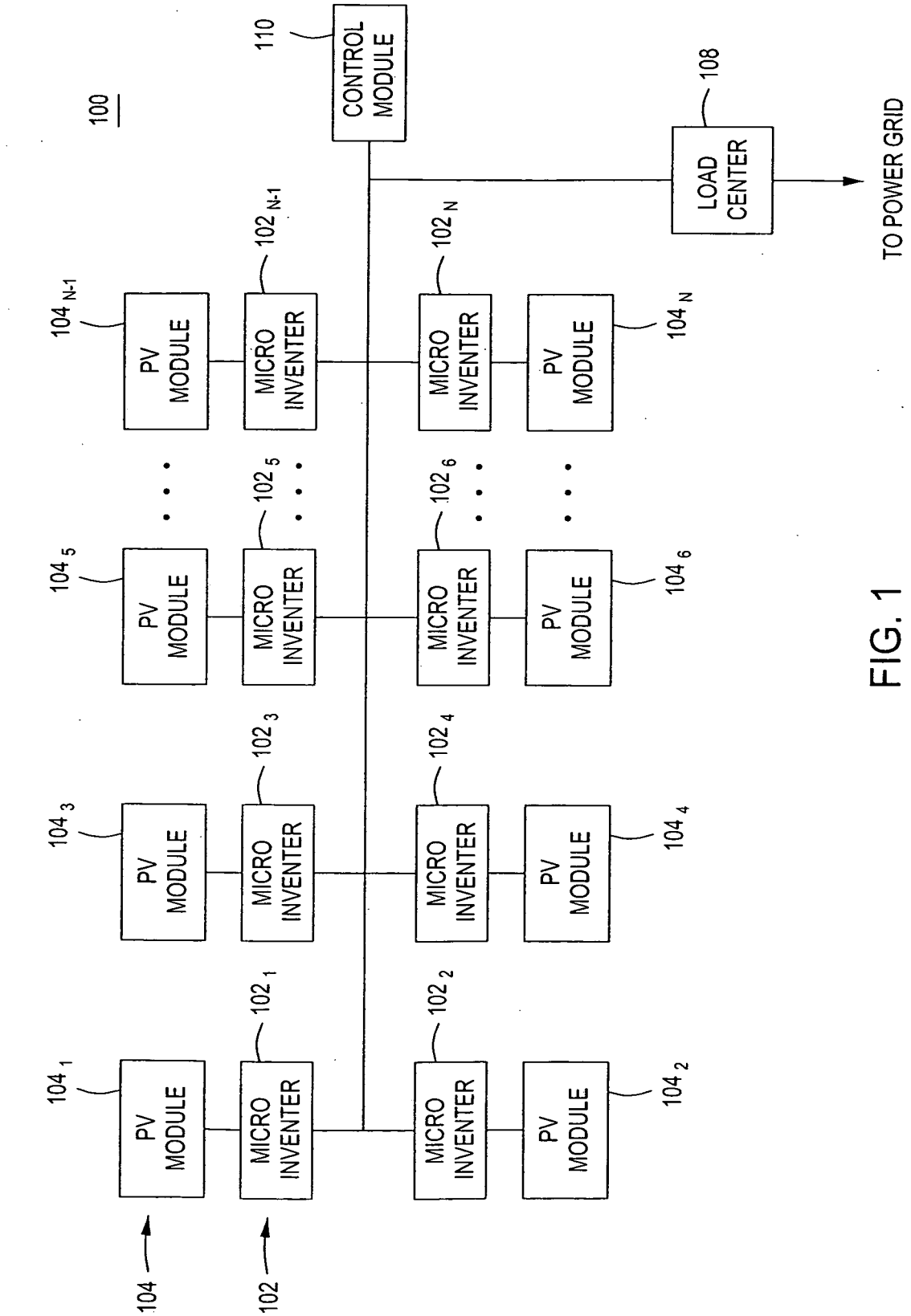
17. The method of claim 16, wherein the phase shift is of a magnitude of 50 microseconds over a single cycle of a frequency of a commercial power grid, wherein the commercial power grid is coupled to the inverter.

18. The method of claim 16, further comprising communicating a message to a plurality of inverters, wherein the message causes each inverter of the plurality of inverters to inject the phase shift simultaneously.

19. The method of claim 14, wherein the inverter is a micro-inverter.

20. The method of claim 19, wherein the inverter is a micro-inverter.

21. The method of claim 14, wherein the integrating step comprises integrating a first phase error response over a first integration period to obtain a first integrated phase error response and a second phase error response over a second integration period to obtain a second integrated phase error response, wherein the first phase error response occurs prior to the injecting step and the second phase error response occurs after the injecting step; and wherein the at least one integrated phase response of the comparing and the flagging steps comprises a difference between the first and the second integrated phase error responses.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108
LOAD CENTER
TO POWER GRID
PV MODULE
MICRO INVENTER
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104
102

FIG. 1

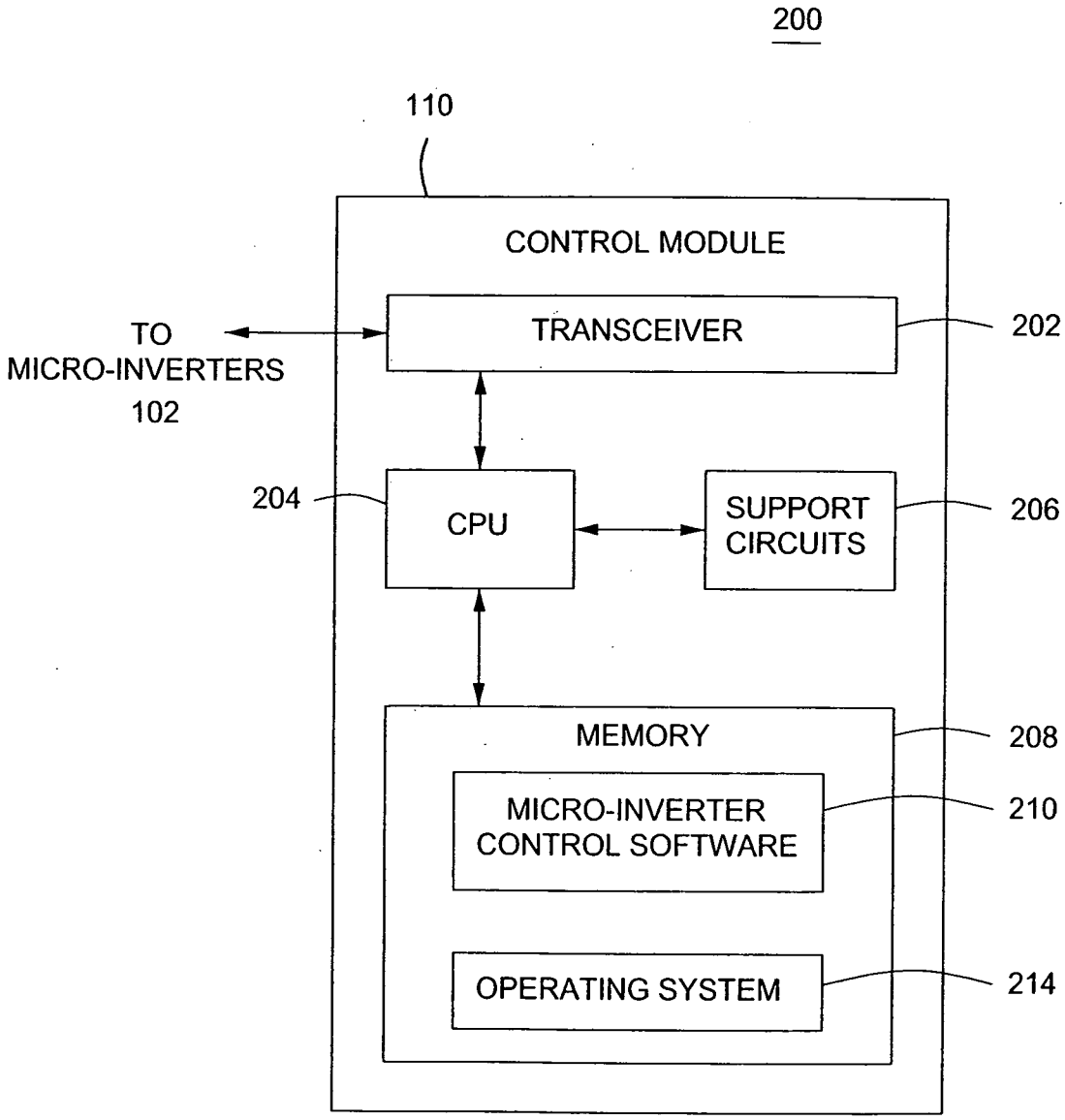
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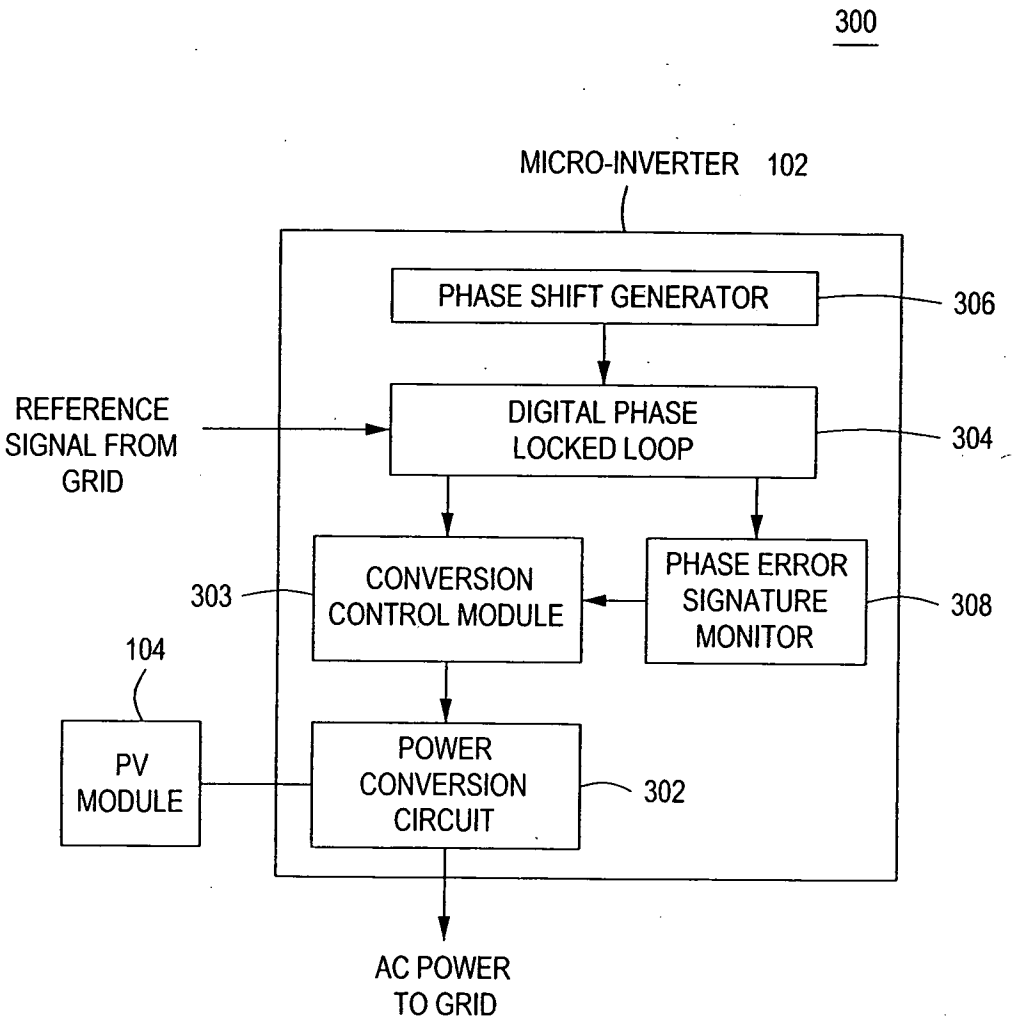
FIG. 2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PHASE ERROR SIGNATURE MONITOR
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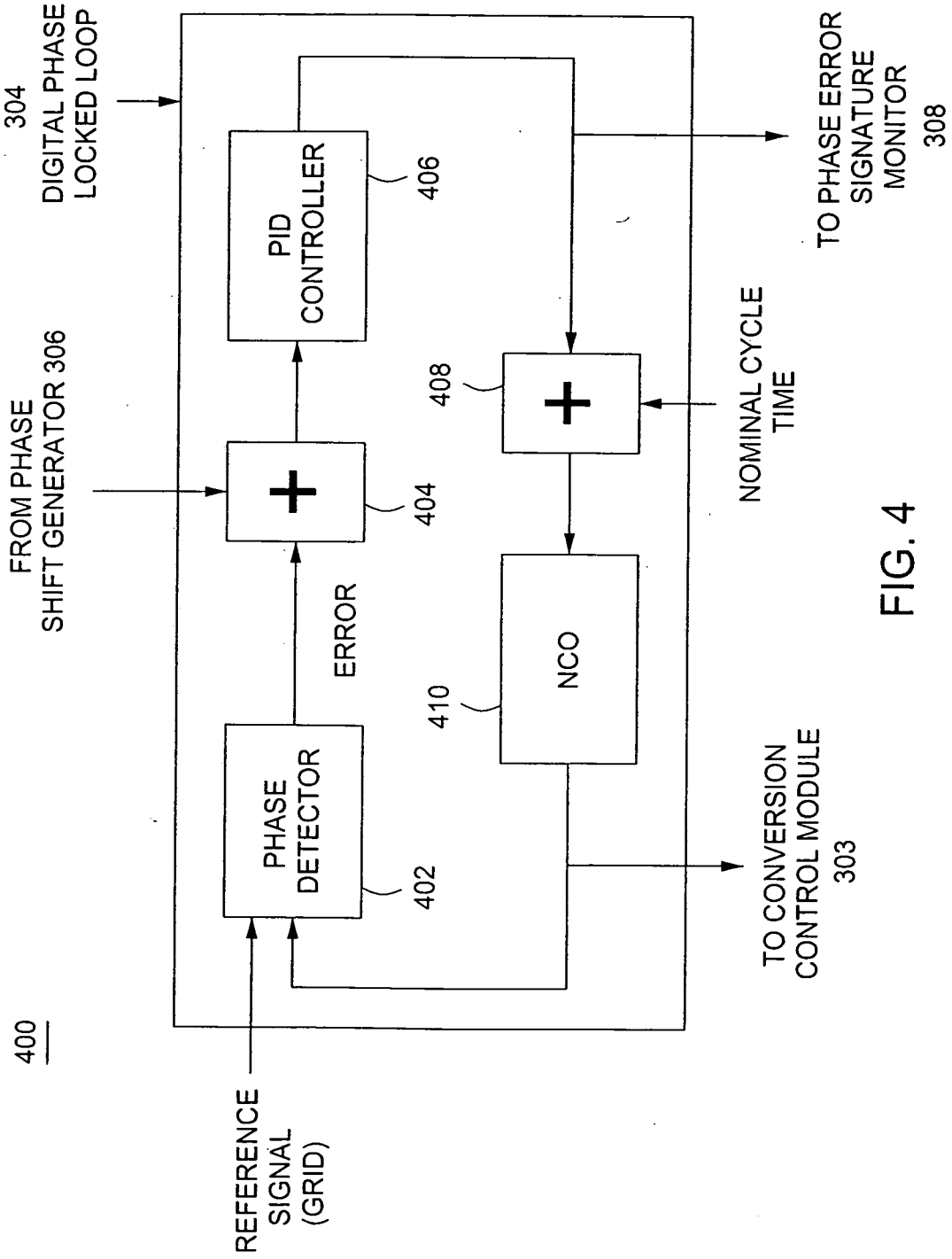
PV MODULE
POWER CONVERSION CIRCUIT
302
AC POWER TO GRID

FIG. 3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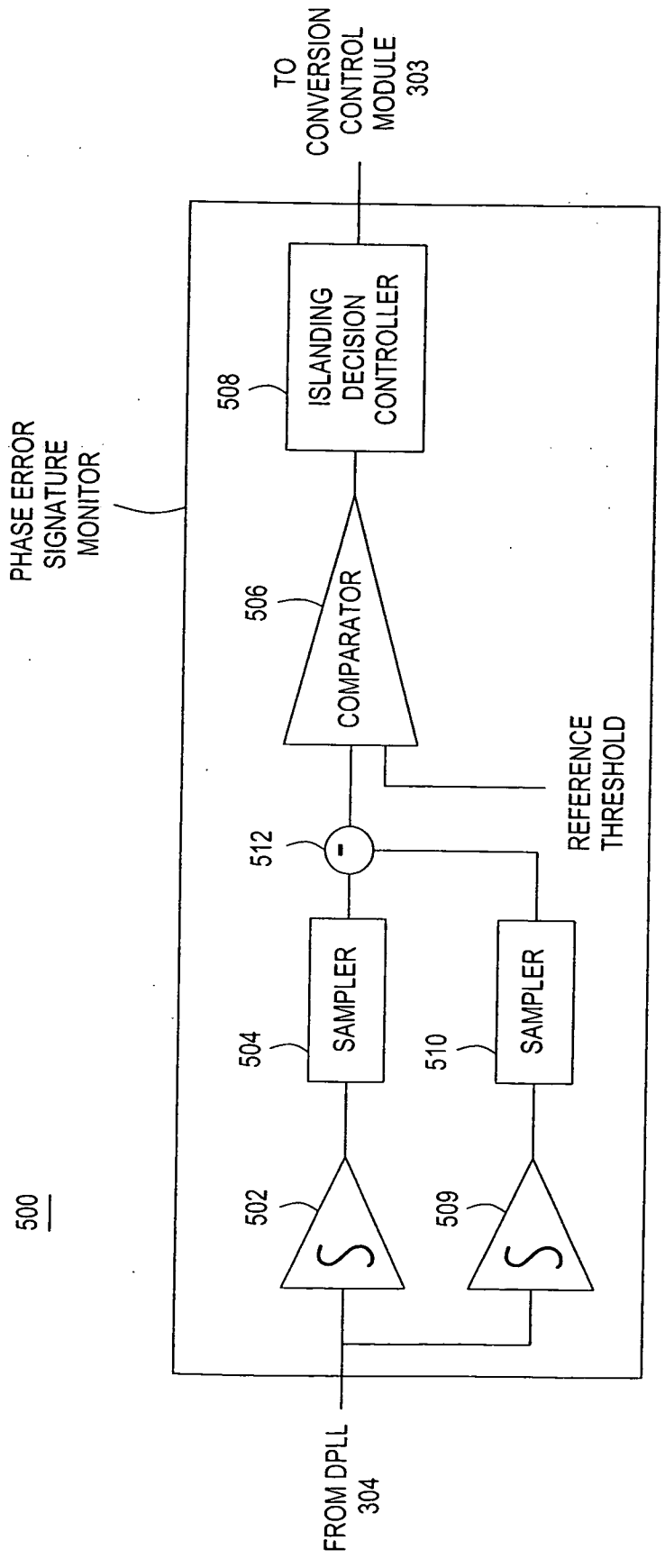
TO CONVERSION CONTROL MODULE 303

FIG. 4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ISLANDING
DECISION
CONTROLLER
506
COMPARATOR
REFERENCE
THRESHOLD
512
-
504
SAMPLER
510
SAMPLER
502
509
FROM DPLL
304

FIG. 5

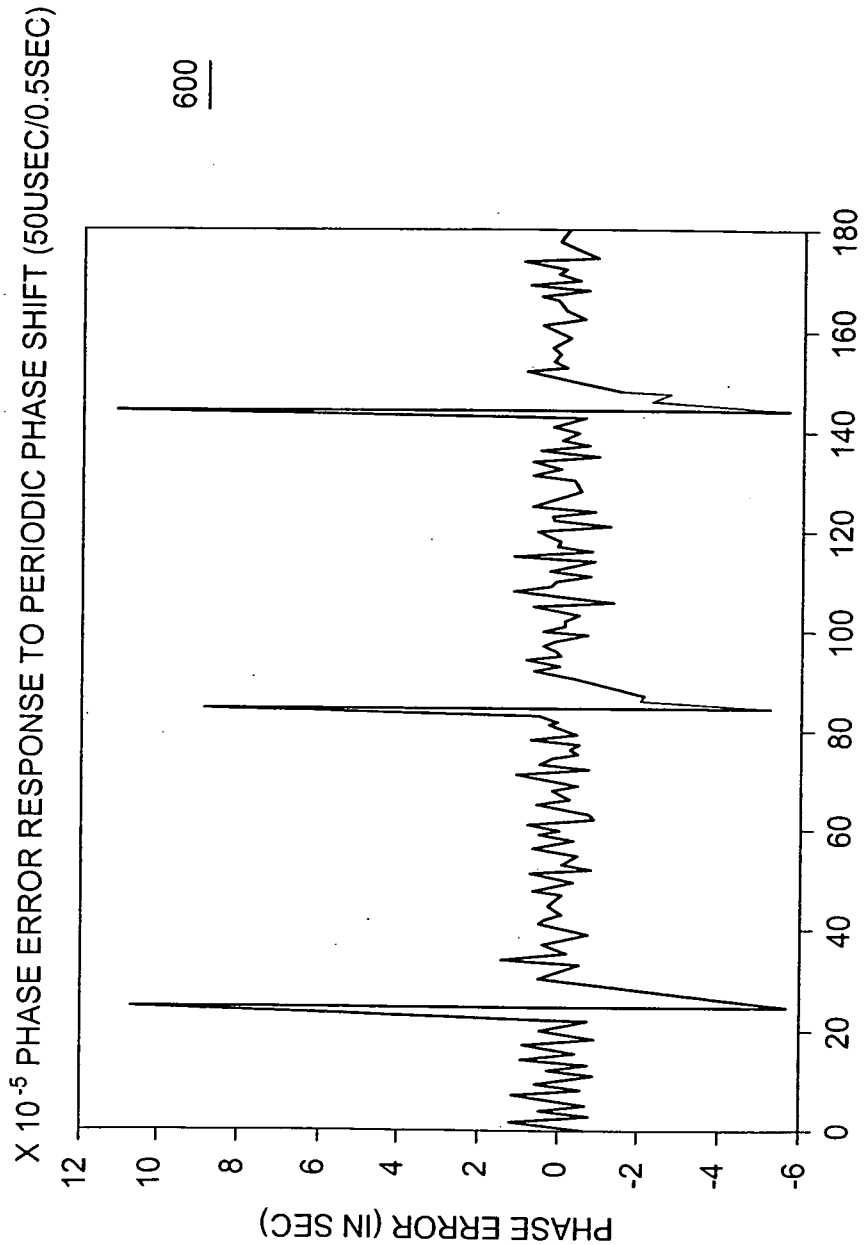
600
X 10-5 PHASE ERROR RESPONSE TO PERIODIC PHASE SHIFT (50USEC/0.5SEC)
PHASE ERROR (IN SEC)
12
10
8
6
4
2
0
-2
-4
-6
0
20
40
60
80
100
120
140
160
180
CYCLE#

FIG. 6

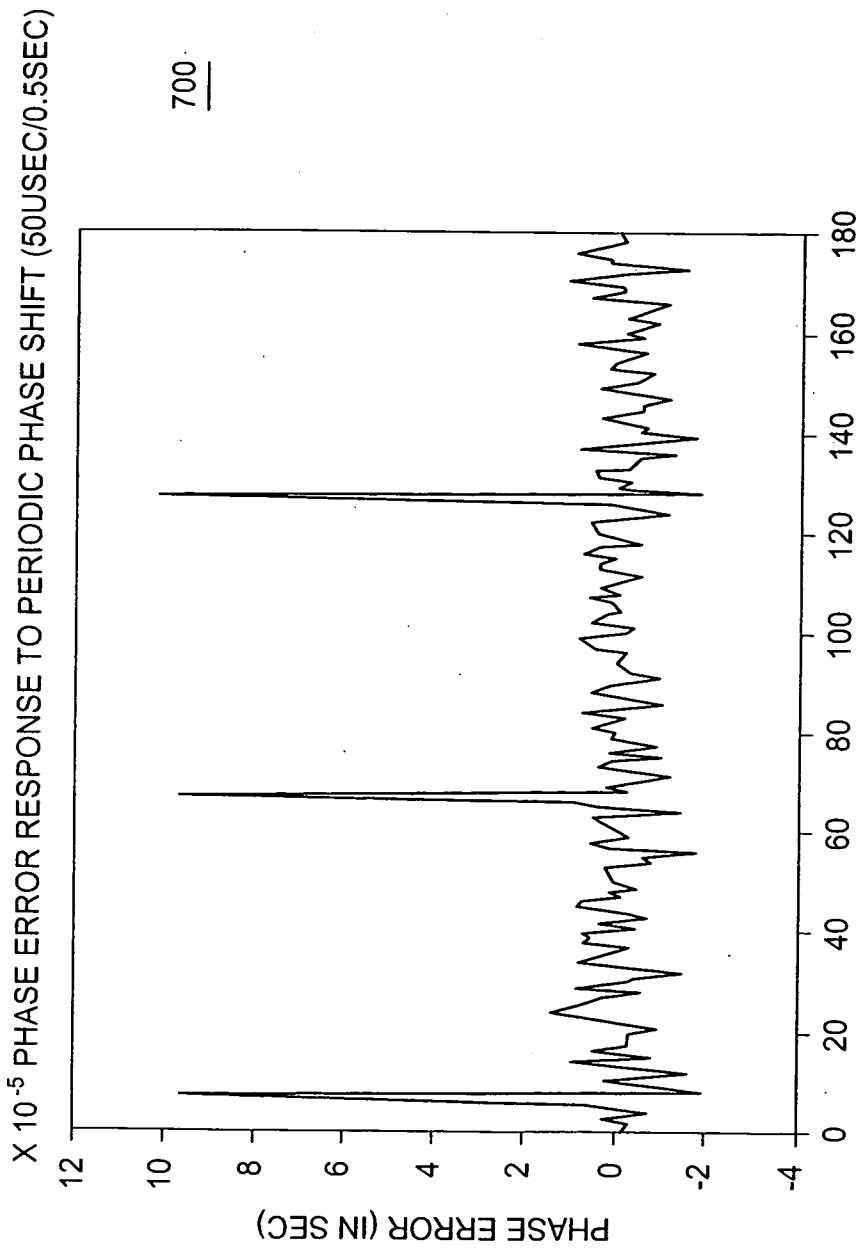
700
X 10-5 PHASE ERROR RESPONSE TO PERIODIC PHASE SHIFT (50USEC/0.5SEC)
PHASE ERROR (IN SEC)
12
10
8
6
4
2
0
-2
-4
0
20
40
60
80
100
120
140
160
180
CYCLE#

FIG. 7

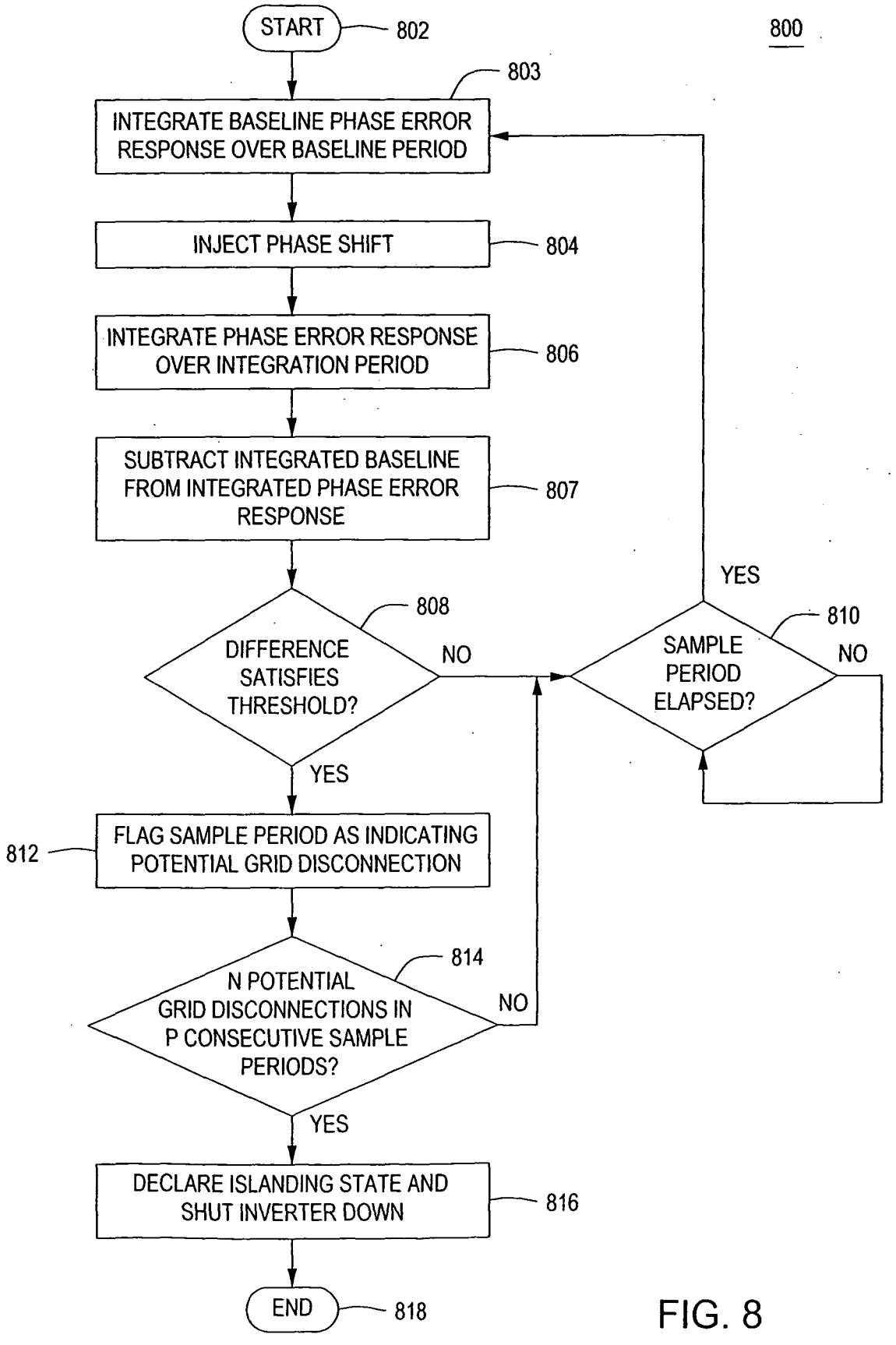
800
START
802
803
INTEGRATE BASELINE PHASE ERROR RESPONSE OVER BASELINE PERIOD
INJECT PHASE SHIFT
804
INTEGRATE PHASE ERROR RESPONSE OVER INTEGRATION PERIOD
806
SUBTRACT INTEGRATED BASELINE FROM INTEGRATED PHASE ERROR RESPONSE
807
DIFFERENCE SATISFIES THRESHOLD?
808
NO
YES
SAMPLE PERIOD ELAPSED?
810
NO
YES
FLAG SAMPLE PERIOD AS INDICATING POTENTIAL GRID DISCONNECTION
812
N POTENTIAL GRID DISCONNECTIONS IN P CONSECUTIVE SAMPLE PERIODS?
814
NO
YES
DECLARE ISLANDING STATE AND SHUT INVERTER DOWN
816
END
818

FIG. 8

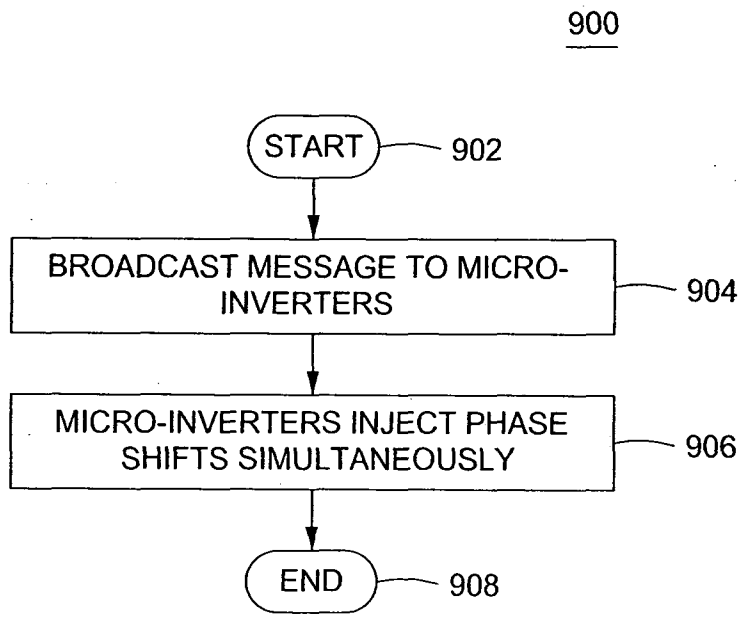
900
START
902
BROADCAST MESSAGE TO MICRO-INVERTERS
904
MICRO-INVERTERS INJECT PHASE SHIFTS SIMULTANEOUSLY
906
END
908

FIG. 9