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(54) **Information transmission systems**

(57) A multiplex information handling system has a plurality of receivers and transmitters connected by a signal bus and a power bus. Timing of transmitted data is controlled by issuing clock pulses CP at intervals and so that these clock pulses can be recognised they are made shorter in duration than any other pulses transmitted. A synchronising pulse (SP) fronts each transmission of data and so this can be recognised this pulse is made longer than any other pulse in the transmission. After a transmission, the signal bus is held high for a period to prevent further transmission so that switching of loads consequent upon the first transmission does not affect these further transmissions. Noise suppression circuitry is also provided.

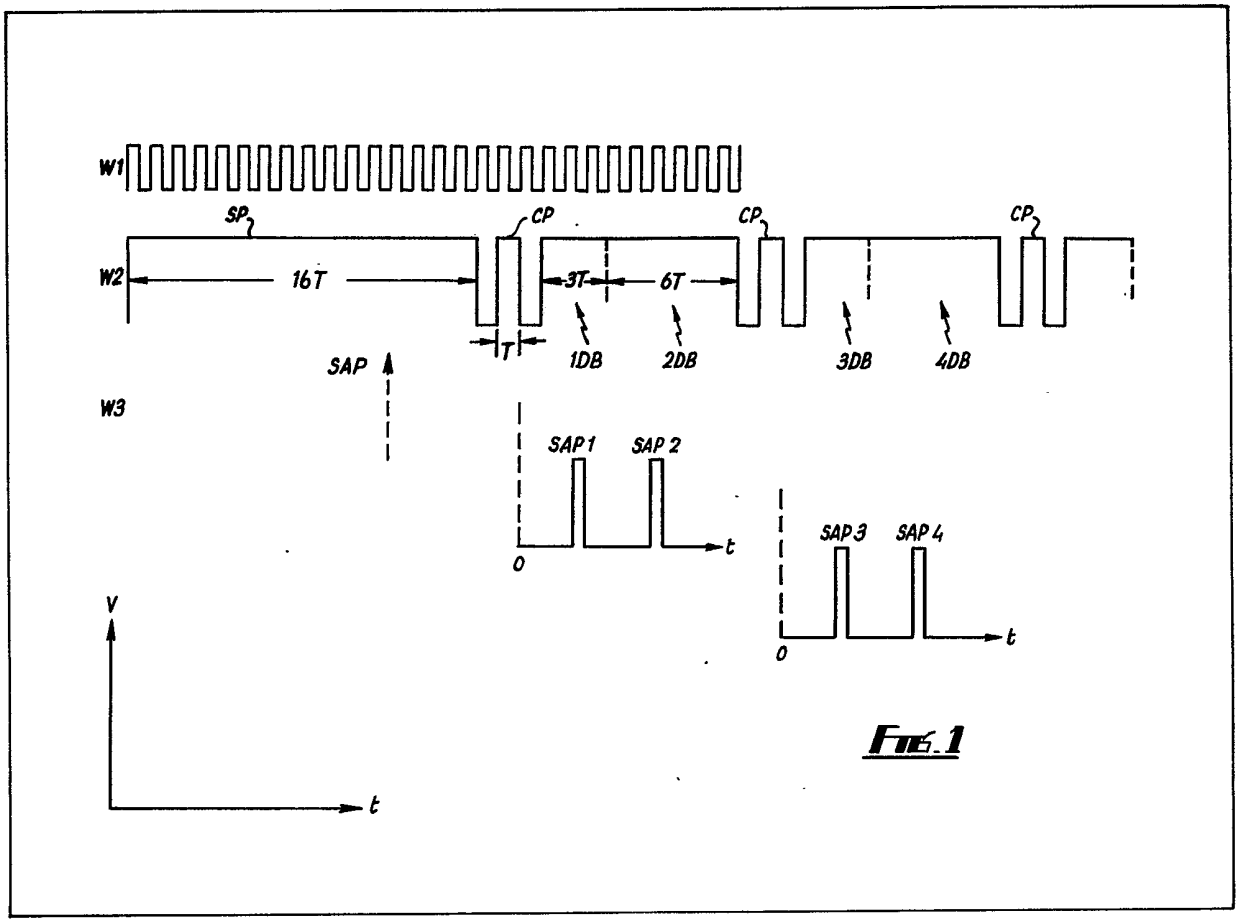

FIG. 1

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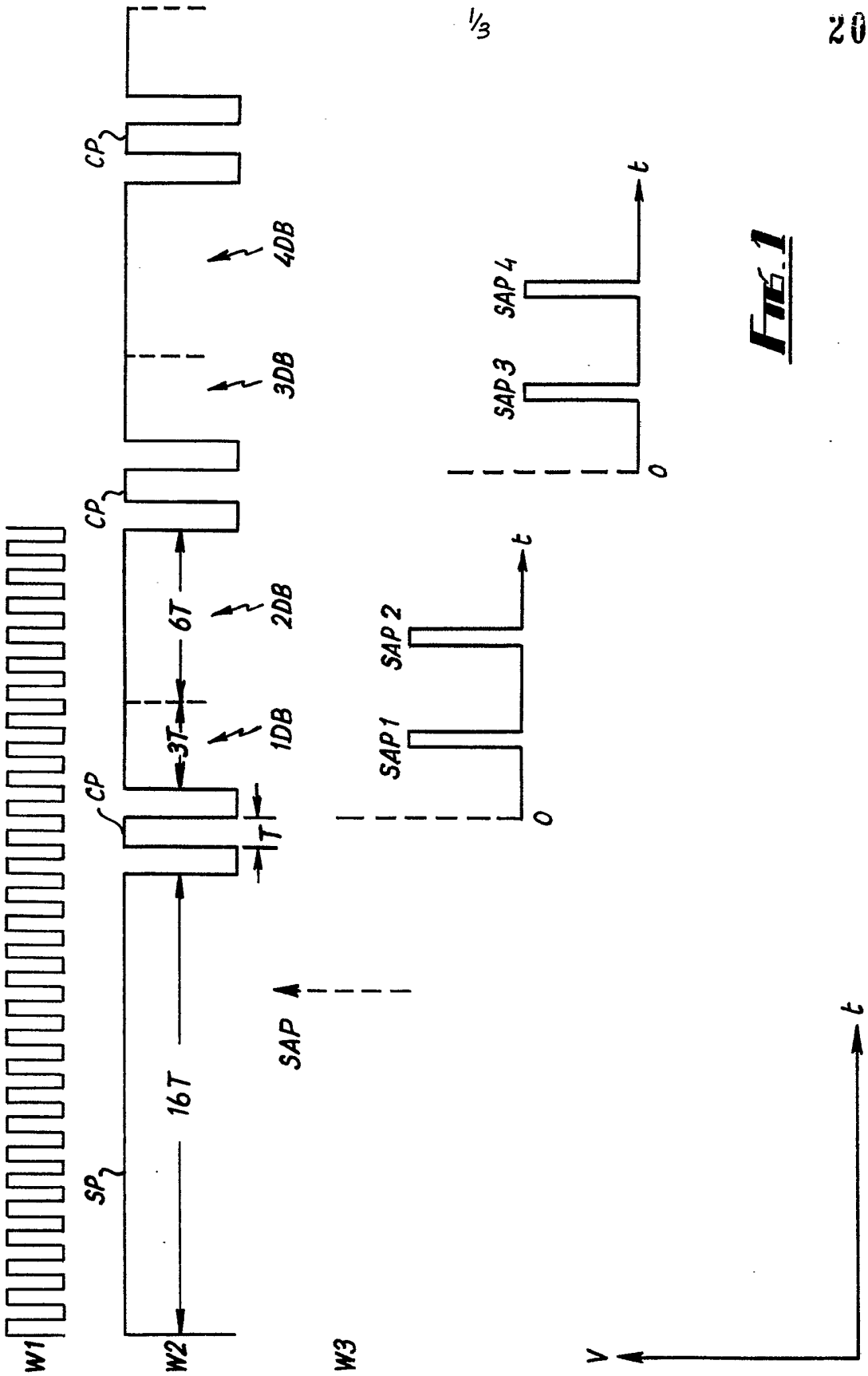
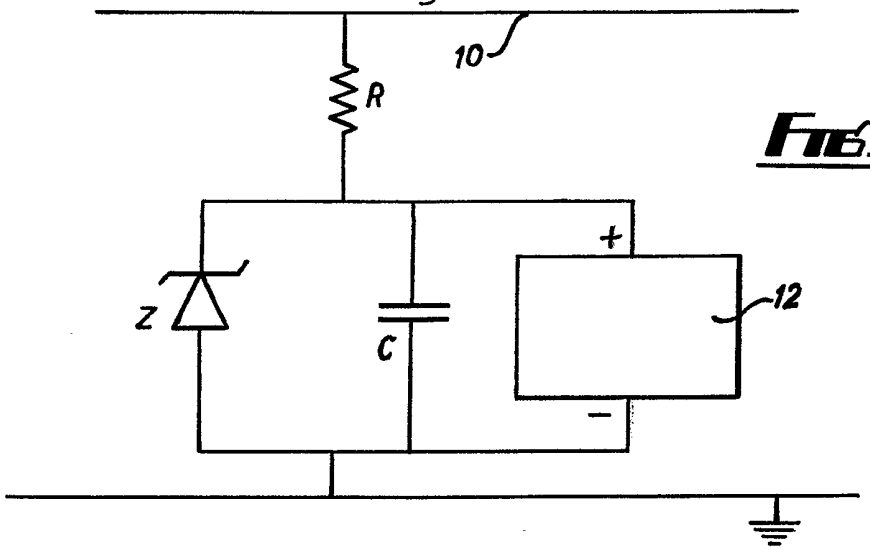


FIG.1



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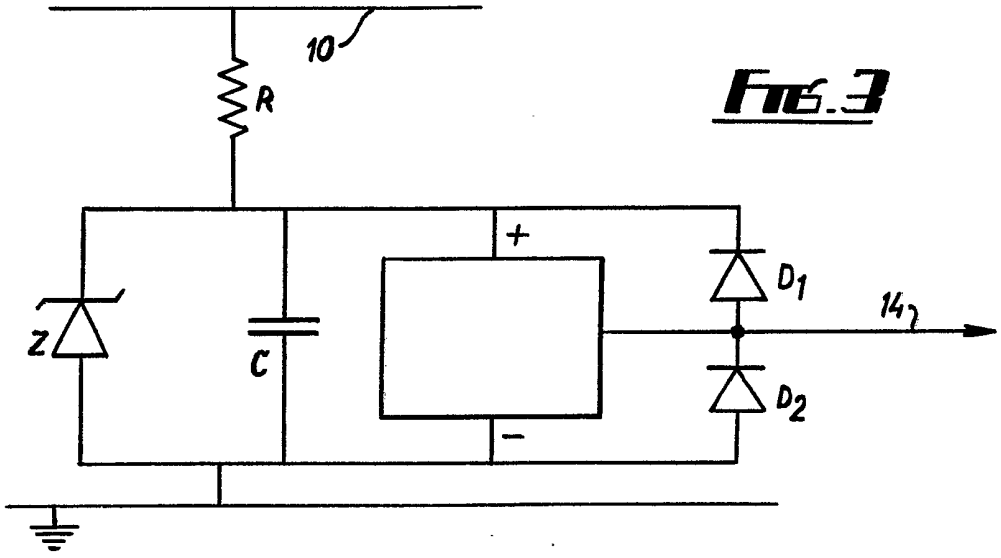

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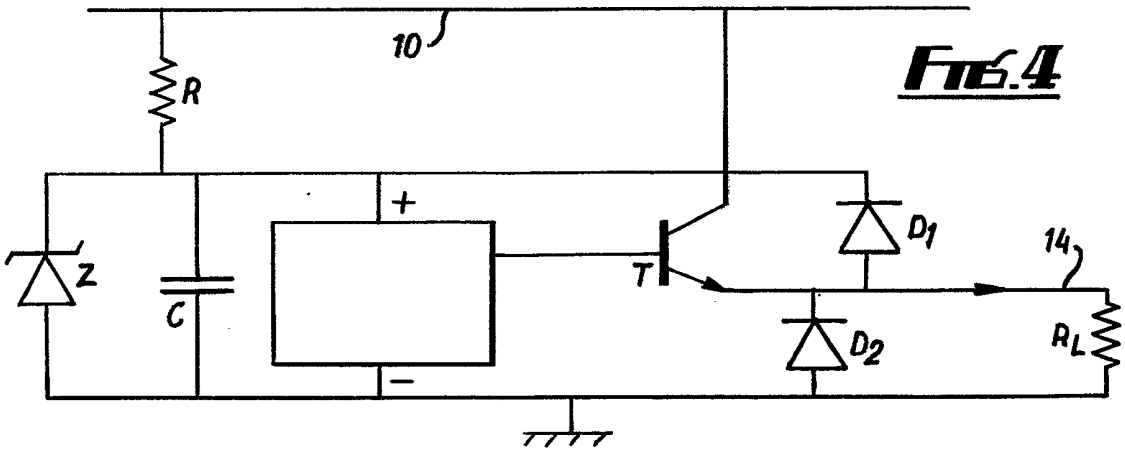

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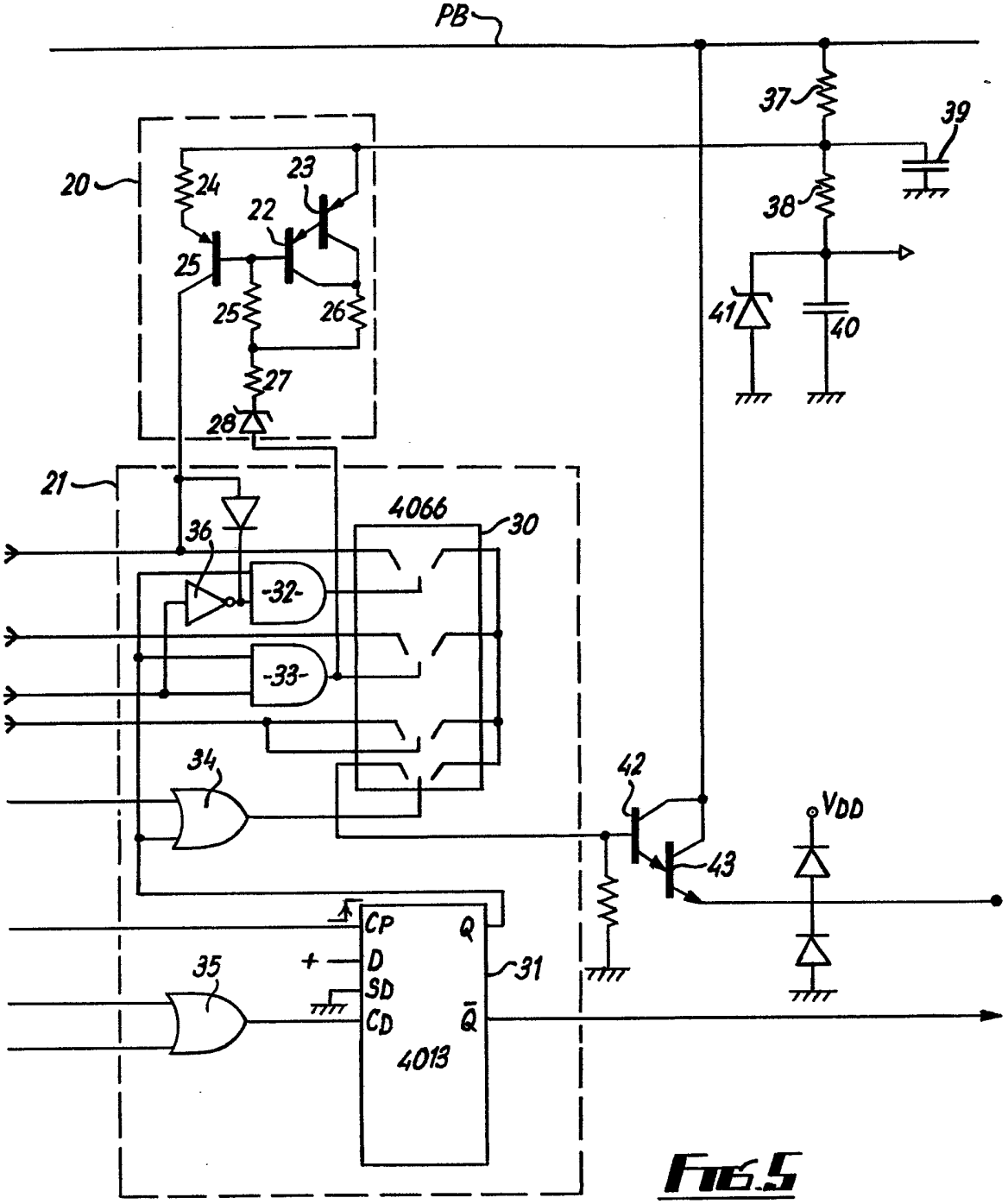
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CD
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FIG.5

SPECIFICATION

A multiplex information handling system

This invention relates to an improvement in multiplex information handling systems and more particularly to an improvement in efficiency for a system containing more than one oscillator, and to an improvement in the immunity to noise.

A multiplex information system consists of a plurality of interconnected processing units between which a signal containing digital and/or analogue data usually in the form of electrical or optical pulses is transmitted. If the system is organised so that the transmission is timed from one unit, such as an oscillator, not synchronised with the first such unit, then it is advantageous to ensure that the system does not malfunction unless the frequency of the two oscillators is significantly different, for example in excess of 25%. At the same time, bandwidth must be efficiently used so that the maximum transmitted frequency is as low as possible in order to minimise the radiation of radio interference.

According to the present invention, there is provided a multiplex information handling system comprising a plurality of transmitters and a plurality of receivers all interconnected by a signal bus pieces of control equipment associated with the transmitters and receivers responsive to signals received by an associated receiver along the signal bus characterised in that timing means are provided operative to produce a clock pulse which is as short or shorter than any other pulse transmitted as to assist the pulse to be recognised as such by the or each receiver receiving it.

In order that the invention may be more clearly understood several embodiments of the invention will now be described, by way of example, with reference to the accompanying drawing in which:—

Figure 1 shows a timing diagram for a multiplex information handling system having a single signal bus,

Figures 2, 3 and 4 respectively show circuit diagrams of three noise suppression systems for a multiplex information handling system, and

Figure 5 shows a circuit diagram of an output stage for a transmitter of the multiplex information handling system of Figure 1.

Referring to Figure 1, the uppermost waveform W1 represents the repetitive pulses of the oscillator of a transmitter. Time (t) is plotted on the abscissa against voltage V on the ordinate. The oscillator frequency is 1/T and T is the duration of each of the clock pulses forming part of the next waveform W2. This transmission waveform W2 begins with a synchronising pulse SP which is 16T in duration and exceeds in length the length on any other pulse transmitted along the signal bus of the system. This synchronising pulse is followed by a clock pulse CP. The clock pulse itself is a logic high and is preceded and succeeded by a logic low each of T duration to minimize radio interference. The complete clock format is therefore low for T, high for T and then low for T again. First and second data bits 1DB and 2DB follow the first clock pulse, the first bit being of 3T duration and the second being of 6T duration. A further clock pulse format follows itself followed by third and fourth data bits 3DB and 4DB respectively.

Waveforms W3, W4 and W5 respectively indicate the time at which the length of the synchronising pulse is tested, the times the first and second data bits are sampled and the times the third and fourth data bits are sampled by appropriate sampling pulses SAP to SAP4 in the receivers receiving the transmission. Zero time for the sample pulses starts on the falling edge of corresponding clock pulses.

Thus with the above described transmission format the length of the synchronising pulse sent once at the start of the transmission from a transmitter is greater than the longest continuous pulse possible arising from a combination of data bits by sufficient margin to enable it to be recognised by a receiver which has an oscillator the frequency of which is within the desired tolerance, of for example 25%, providing the oscillator in the transmitter also satisfies the desired tolerance. The synchronising pulse clears all counters in the receiver. The length of the synchronising pulse may also be used to identify the transmitter type it issues from, different length pulses being used for different transmitter types. The clock pulse is as short as possible again to facilitate recognition. The relative positions of the various pulses also assists in enabling them to be identified.

No time is allowed between the falling edge of the first data bit and the rising edge of the second data bit following the clock pulse and as the timing of the second data bit after a clock pulse requires a greater restraint on the tolerance between the oscillator frequencies than the first bit, the second bit is made longer in duration.

Because the two oscillators, one in the transmitter and the other in the receiver, are not synchronised the timing may fluctuate by up to one oscillator bit, even if they were of the same frequency. Taking this into account, if the first data bit is three oscillator bits and the second data bit is six oscillator bits as described above, then the 25% tolerance on timing is easily achieved.

Following the receipt of a transmission various items of operational equipment forming part of, or controled by, the multiplex information handling system can be expected to be switched to change their operational state. Such switching can cause a noisy environment which could result in a following transmission being adversely affected. To avoid this happening further transmission or reception is inhibited by generating a post transmission high on the signal bus for a limited period when any output of any receiver is about to change state. It may also be advantageous to reset the timing means of each receiver to precisely initiate the timing of an event. This may be done, for example, by making the resetting coincident with a selected change in the logic state on the signal bus.

Analogue data is transmitted by means of the height of the voltage pulses. Corruption of data transmitted in this way may result from variation in the power supply voltage on the power bus. This may be prevented by providing each transmitter with an output driver stage and supply filter which incorporates a constant current source. Such a circuit is shown in Figure 5. Referring to Figure 5, the output driver stage and supply filter T7 of the transmitter comprises a current generator 20 and logic circuitry 21. The current generator comprises two PNP transistors 22 and 23 connected in cascade and a further PNP transistor 24a connected with associated resistors 24, 25, 26 and 27 and zener diode 28. The logic circuitry 21 comprises two integrated circuits 30 and 31. The pins of logic circuits 30 and 31 are fed through a selection of logic gates comprising two AND gates 32 and 33, two OR gates 34 and 35 and a NOT gate 36. The current generator is fed from the power bus PB through a supply filter comprising two resistors 37 and 38, two capacitors 39 and 40 and a zener diode 41. The output from the circuit is through two cascaded PNP transistors 42 and 43 to the signal bus SB.

The above described multiplex information handling systems are particularly suitable for use in vehicles.

The power rail in vehicles is very susceptible to electrical noise arising from surges of current and back emfs when switching loads. Any electronic circuit fed from this power rail must withstand this noisy voltage fluctuation of the power rail without malfunction.

Figures 2, 3 and 4 shows the circuit diagrams of three possible noise suppression systems. Equivalent elements on these figures have been given the same reference numerals. Referring to Figure 2 a power bus 10 is fed to an electronic circuit 12 through a resistor R. A capacitor C and zener diode Z are connected in parallel with the positive and ground terminals of the electronic circuit. The circuit is designed so that the mean current consumption is small which is easily done using complementary electronics such as CMOS thereby ensuring that the resistor R can be significantly large without dropping too great a voltage. The capacitor C must be large enough to provide high transient currents to the electronic circuit with minimal voltage change across the capacitor terminals. The capacitor also supplies power to the circuit in the event that the voltage of the power bus momentarily drops due to the presence of noise. If the power bus 10 carries a large positive pulse arising from the breaking of an inductive circuit, the the zener diode Z clamps the voltage across the electronic circuit to the zener voltage. In practice the zener diode will have a finite slope resistance, r, and a positive noise voltage will be attenuated by r/(r+R). Again using a resistor R with a significantly large value provides a good circuit protection.

Other parts of the electronic circuit can be diode clamped to the positive and negative terminals of the electronic circuit which have been isolated from noise on the power bus 10 as outlined above. If electrical signals are to be transmitted along a signal bus as used in an electronic multiplexing wiring system, for example, then the signal bus will be susceptible to noise by capacitative coupling to the power bus. If the signal bus 14 is connected to the positive and negative terminals of the noise protected electronic circuit by two diodes D1 and D2 as shown in Figure 3, then D1 will conduct if the signal bus potential rises significantly above the potential of the positive terminal, and D2 will conduct if the signal bus potential falls significantly below that of the negative terminal. By these means the potential of the signal bus 14 is prevented from passing significantly outside the voltage range set by the value of potentials at the positive and negative terminals.

Figure 4 illustrates the driving of an electrical output from the electronic circuit 12. If the output, by way of example, is considered as a signal bus of a multiplexed wiring system then the signal bus can be driven by a transistor T in an emitter follower output stage. The collector of the transistor T can be taken directly to the power bus 10, but the signal to the base is derived from the electronic circuit 12 which is noise protected as described with reference to Figure 1. The potential of the emitter of transistor and hence of the signal bus 12 follows that of the base which is noise protected, and consequently noise voltages on the power bus 12 and hence on the collector are of minimal significance. Using an emitter follower gives a single ended drive, and it is necessary to provide a pull down resistor or emitter load, R_L. This load R_L can have a very low value, because the current through it does not pass through the resistor R. If R_L is very low then noise potentials induced on the signal bus by capacitative coupling with the power bus 10 is greatly minimised.

The signal bus 14 is susceptible to pick-up from sources of radiative noise such as sparks, for example, especially if the impedance defined by the pull down resistor R_L, referred to in the embodiment of Figure 4 is large. If the power bus 10 and signal bus 14 are combined in one co-axial cable such that the outer carries the power whilst the inner carries the signal, then the signal bus will be screened from radiative pick up by the power bus. A further advantage of a co-axial construction is that the voltage pulses on the signal bus will be prevented from radiating radio interference by the presence of the outer screen which is clamped at very low impedance to the d.c. power supply of the vehicle.

CLAIMS

1. A multiplex information handling system comprising a plurality of transmitters and a plurality of receivers all interconnected by a signal bus pieces of control equipment associated with the transmitters and receivers responsive to signals received by an associated receiver along the signal bus characterised in that timing means are provided operative to produce a clock pulse which is as short or shorter than any other pulse transmitted to assist the pulse to be recognised as such by the of each receiver receiving it.

2. A multiplex information handling system as claimed in Claim 1, characterised in that the timing means are operative to produce opposite logic levels to the clock pulse itself immediately preceding and

succeeding it, each opposite logic level being for a duration equal to the duration of the clock pulse.

3. A multiplex information handling system as claimed in Claim 1 or 2, characterised in that two or more data bits are transmitted after each clock pulse, the bits progressively increasing in duration the further they are from the clock pulse.

4. A multiplex information handling system as claimed in Claim 1, 2 or 3, characterised in that each transmitter is operative to produce a synchronising pulse at the beginning of each transmission which is longer than any other combination of directly adjacent data pulses in the transmission so that it can be recognised as such by a receiver receiving the transmission.

5. A multiplex information handling system as claimed in Claim 4, characterised in that each transmitter is operative to produce a synchronisation pulse having a length which is dependent upon the transmitter type from which it issues whereby a receiver receiving a transmission can identify that type.

6. A multiplex information handling system as claimed in any preceding claim, characterised in that the timing means are adapted to be reset in the event of a selected transition in the logic state on the signal bus.

7. A multiplex information handling system as claimed in any preceding claim, characterised in that means are provided for applying a signal to the signal bus to inhibit transmission or reception.

8. A multiplex information handling system as claimed in any preceding claim, characterised in that a power bus is provided interconnecting the receivers and transmitters, each transmitter incorporates means for protecting the transmission of analogue data against variation in the voltage on the power bus.

9. A multiplex information handling system as claimed in Claim 8, characterised in that the means for protecting incorporates a constant current source.

10. A multiplex information handling system as claimed in any preceding claim, characterised in that each transmitter or receiver is fed from the power bus via a resistor and a capacitor and zener diode are connected in parallel with the circuit.

11. A multiplex information handling system as claimed in Claim 10, characterised in that the signal bus is clamped to the positive and negative terminals of the transmitter or receiver by respective diodes.

12. A multiplex information handling system as claimed in Claim 11, characterised in that the base emitter junction of a transistor is connected in the signal bus, the emitter of the transistor being connected to the junction of the two diodes and the collector to the power bus.

New claims or amendments to claims filed on 29 Nov. 1979
New Claim:—

16. A multiplex information handling system substantially as hereinbefore described with reference to Figure 1 of the accompanying drawings or to this figure when modified in accordance with any of Figures 2-5 of the accompanying drawings.

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