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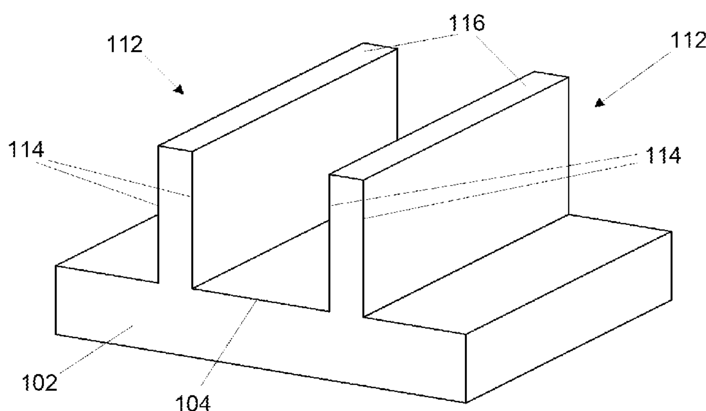

FIG. 1

(57) Abstract: Transistor devices having a buffer between an active channel and a substrate, which may include the active channel comprising a low band-gap material on a sub-structure, e.g. a buffer, between the active channel and the substrate. The sub-structure may comprise a high band-gap material having a desired conduction band offset, such that leakage may be arrested without significant impact on electronic mobility within the active channel. In an embodiment, the active channel and the sub-structure may be formed in a narrow trench, such that defects due to lattice mismatch between the active channel and the sub-structure are terminated in the sub-structure. In a further embodiment, the sub-structure may be removed to form either a void between the active channel and the substrate, or an insulative material may be disposed between the active channel and the substrate, such that the void or the insulative material form an insulative buffer.

WO 2016/043770 A1

APPARATUS AND METHODS TO CREATE A BUFFER TO REDUCE LEAKAGE IN MICROELECTRONIC TRANSISTORS

TECHNICAL FIELD

5 Embodiments of the present description generally relate to the field of microelectronic devices, and, more particularly, to forming a buffer adjacent to an active channel in a microelectronic transistor to reduce current leakage.

BACKGROUND

Higher performance, lower cost, increased miniaturization of integrated circuit 10 components, and greater packaging density of integrated circuits are ongoing goals of the microelectronic industry for the fabrication of microelectronic devices. To achieve these goals, transistors within the microelectronic devices must scale down, i.e. become smaller. Along with the reduction in the size of transistors, there has also been a drive to improve their efficiency with improvement in their designs, materials used, and/or in their fabrication processes. Such 15 design improvements include the development of unique structures, such as non-planar transistors, including tri-gate transistors, FinFETs, TFETS, omega-FETs, and double-gate transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly 20 claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be 25 described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIGs. 1-8 are oblique sectional views of the fabrication of forming a high band-gap buffer for a non-planar transistor, according to an embodiment of the present description.

FIGs. 9-16 are oblique sectional and side cross-sectional views of forming an insulative 30 buffer for a non-planar transistor, according to an embodiment of the present description.

FIG. 17 illustrates a computing device in accordance with one implementation of the present description.

DESCRIPTION OF EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings that

show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present description. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

The terms "over", "to", "between" and "on" as used herein may refer to a relative position of one layer with respect to other layers. One layer "over" or "on" another layer or bonded "to" another layer may be directly in contact with the other layer or may have one or more intervening layers. One layer "between" layers may be directly in contact with the layers or may have one or more intervening layers.

As will be understood to those skilled in the art, controlling the source to drain leakage through the sub-substructures below active channels is an important consideration in any transistor design. In non-planar transistor devices, such III-V NMOS TFET devices, sub-structure leakage presents more of a challenge. This challenge stems from the high mobility materials which are required for the formation of active channel in order to achieve high electron mobility, which inherently have low band gap and, hence, high conductivity. Non-planar transistors may utilize low band-gap materials, such as indium gallium arsenide, in the formation of active channels, which has a band-gap lower than a typical silicon substrate over which active channels are formed. If the sub-structure is composed of these high conductivity materials, then

leakage would be considerable, as the sub-structure material would form a conductive path between the source and drain.

Embodiments of the present description relate to the fabrication of transistor devices having a buffer between an active channel and a substrate. In at least one embodiment of the
5 present description, an active channel comprising a low band-gap III-V material may be epitaxially grown on a sub-structure, e.g. a buffer, between the active channel and the substrate. The sub-structure may comprise a high band-gap III-V material, which may have a desired conduction band offset, such that leakage may be arrested without having a significant impact on electronic mobility within the active channel. With the embodiments of the present description,
10 leakage may be decreased by at least three orders of magnitude compared with forming an active channel without such a buffer. In an embodiment of the present description, the active channel and the sub-structure may be formed in a narrow trench, such that defects due to lattice mismatch between the active channel and the sub-structure are terminated by defect trapping in the sub-structure below the active channel region. In a further embodiment, the sub-structure may be
15 removed to form either a void between the active channel and the substrate, or an insulative material may be disposed between the active channel and the substrate, such that the void or the insulative material form an insulative buffer.

As shown in FIG. 1, at least one fin 112 may be formed on a substrate 102, wherein the fins 112 may include opposing sidewalls 114 extending from a first surface 104 of the substrate
20 102 and which terminate in an upper surface 116. For the clarity and brevity, only two fins 112 are illustrated in FIG. 1; however, it is understood that any appropriate number of fins 112 could be fabricated. In one embodiment, an etch mask (not shown) may be patterned on the substrate 102 followed by the etching of the substrate 102, wherein the portions of the substrate 102 protected by etch mask (not shown) become the fins 112, and the etch mask (not shown) may be
25 thereafter removed, as will be understood to those skilled in the art. In an embodiment of the present disclosure, the substrate 102 and the fins 112 may be any appropriate material, including, but not limited to, a silicon-containing material, such as monocrystalline silicon. The substrate 102 and the fins 112, however, need not necessarily be fabricated from silicon-containing materials, and can be other types of materials known in the art. In a further embodiment, the
30 substrate 102 may comprise a silicon-on-insulator (SOI) substrate, a silicon-on-nothing (SON), a germanium substrate, a germanium-on-insulator (GeOI) substrate, or a germanium-on-nothing (GeON).

As shown in FIG. 2, a dielectric material may be deposited, by any appropriate deposition process, over the substrate 102 and the fins 112, and the dielectric material may be planarized to

exposed the fin upper surface 116, thereby forming isolation structures 122, known as shallow trench isolation structures, abutting the opposing fin sidewalls 114. The isolation structures 122 may be formed from any appropriate dielectric material, including but not limited to, silicon oxide (SiO_2).

5 As shown in FIG. 3, the fins 112 may be removed, thereby forming a trench 124. The fins 112 may be removed by any known etching techniques, including, but not limited to, dry etching, wet etching, or combinations thereof. In one embodiment, a portion of the each trench 124 may be formed to extend into the substrate 102 either during the removal of the fins 112 or thereafter. This portion of the trench 124 will hereinafter be referred to as a 10 nucleation trench 132. In one embodiment, the nucleation trench 132 may have a (111) faceting, which may facilitate the growth of a III-V material, as will be discussed. It is understood that alternate geometries of the nucleation trench 132 may be utilized.

As shown in FIG. 4, a nucleation layer 142 may be formed in the nucleation trench 132. The nucleation layer 142 may be formed by any formation process and may be any appropriate 15 material, such as a III-V epitaxial material, including but not limited to, indium phosphide, gallium phosphide, gallium arsenide, and like.

As further shown in FIG. 4, a sub-structure 144 may be formed on the nucleation layer 142 within the trench 124 (see FIG. 3). The sub-structure 144 may be formed by any known formation process, and may be any appropriate material, such as a high band-gap III-V material, 20 including, but not limited to, indium aluminum arsenide, indium phosphide, gallium phosphide, gallium arsenide, gallium arsenide antimonide, aluminium arsenide antimonide, indium aluminum gallium arsenide, indium aluminum gallium phosphide, aluminum gallium arsenide, and the like. For the purpose of the present description, a high band-gap material may be defined to be a material that has a band-gap greater than silicon. In one embodiment, the sub-structure 25 144 may be the same material as the nucleation layer 142. In other embodiments, the nucleation layer 142 may be graded into the sub-structure 144 or the material compositions thereof may be stepped in concentration from one to the other, as will be understood to those skilled in the art.

As yet further shown in FIG. 4, an active channel 146 may be formed on the sub-structure 144 within the trench 124 (see FIG. 3). The active channel 146 may be formed by any known 30 formation process, and may be any appropriate material, such as a low band-gap III-V epitaxial material, including, but not limited to indium gallium arsenide, indium arsenide, indium antimonide, and the like. For the purpose of the present description, a low band-gap material may be defined to be a material that has a band-gap less than silicon. In one embodiment, the active channel 146 may be undoped (electrically neutral or doped with less than 5E17 carriers of

either p-type or n-type dopants).

In some example embodiments, the nucleation layer 142, the sub-structure 144 and/or the active channel 146 may be epitaxially deposited. The thickness T_s (see FIG. 5) of the sub-structure 144 (see FIG. 5) and the thickness T_a of the active channel 146 may be in the range, for example, of about 500 to 5000 Å, in accordance with some specific example embodiments, although other embodiments may have other layer thicknesses, as will be apparent in light of this disclosure. In particular trench-fill embodiments will be in this thickness range while blanket deposition and subsequent patterning embodiments can have thickness values up to 100 times higher. In some embodiments, a chemical vapor deposition (CVD) process or other suitable deposition technique may be used for the depositing or otherwise forming the nucleation layer 142, the sub-structure 144 and/or the active channel. For example, the deposition may be carried out by CVD, or rapid thermal CVD (RT-CVD), or low pressure CVD (LP-CVD), or ultra-high vacuum CVD (UHV-CVD), or gas source molecular beam epitaxy (GS-MBE) tools using III-V material compounds, such as combinations of indium, aluminum, arsenic, phosphorus, gallium, antimony, and/or precursors thereof. In one specific such example embodiment, the active channel 146 may be indium gallium arsenide, and the nucleation layer 142 and the sub-structure 144 may be indium phosphide. In any such embodiments, there may be a precursor bubbler with a carrier gas such as, for instance, hydrogen, nitrogen, or a noble gas (e.g., precursor may be diluted at about 0.1-20% concentration with the balance being carrier gas). In some example cases, there may be an arsenic precursor such as arsine or tertiary butyl arsine, a phosphorous precursor such as tertiary butylphosphine, a gallium precursor such as trimethylgallium, and/or an indium precursor such as trimethylindium. There may also be an etchant gas such as, for example, halogen-based gas such as hydrogen chloride (HCl), chlorine (Cl), or, hydrogen bromide (HBr). The basic deposition of the nucleation layer 142, the sub-structure 144, and/or the active channel 146 may be possible over a wide range of conditions using a deposition temperature in the range, for example, from between about 300°C and 650°C, or in a more specific example, from between about 400 and 500°C) and reactor pressure, for instance, in the range of between about 1 Torr and 760 Torr. Each of the carrier and etchants can have a flow in the range of between about 10 and 300 SCCM (typically, no more than 100 SCCM of flow is required, but some embodiments may benefit from higher flow rates). In one specific example embodiment, the deposition of the nucleation layer 142, the sub-structure 144, and/or the active channel 146 may be carried out at a flow rate that ranges between about 100 and 1000 SCCM.

The material utilized for the sub-structure 144 may be selected to have the desired

conduction band offset with the active channel 146 which will be effective in excluding electrons from the sub-structure 144, thereby reducing leakage. Furthermore, as the formation of the nucleation layer 142, the sub-structure 144, and the active channel 146 occurs in a relatively narrow trench 124. In one embodiment, the narrow trench 124 may have a height H (see FIG. 3) in the range of about 50 to 500nm and a width W (see FIG. 3) of less than about 25nm (preferably less than 10nm). Lattice mismatch between the substrate 102 and the nucleation layer 142/sub-structure 144 can be larger than that which allows for substantially defect free formation, as the nucleation layer 142/sub-structure 144 may be formed to have a sufficient depth D to trap defects, such as stacking faults, dislocations, and the like, away from the active channel 146, as will be understood to those skilled in the art. Thus, electron mobility in the active channel 146 may not be significantly impaired thereby. While the active channel 146 may not achieve theoretical maximum mobility values, it nevertheless provides a compelling performance advantage relative to silicon based n-MOS transistors. In one embodiment the sub-structure 144 may have a depth D (e.g. the distance between the substrate 102 and the active channel 146) of greater than about 50nm and a width of less than about 25nm (i.e. the trench width W).

As still further shown in FIG. 4, a portion 148 of active channel 146 may extend out of the trench (see FIG. 3), particularly when epitaxial growth processes are utilized. Thus, as shown in FIG. 5, the portion 148 of the active channel 146 may be removed, such as by chemical mechanical planarization. As shown in FIG. 6, the isolation structures 122 may be recessed, such as by an etching process, such that at least a portion of the active channel 146 extends above an upper plane 126 of the isolation structures 122. In one embodiment, the height F_h of the active channel 146 extending about the isolation structure upper plane 126 may be about 45nm . An intersection I between the active channel 146 and the sub-structure 144 may occur at a depth F_d relative to the isolation structure upper plane 126. In an embodiment, the intersection I may be slightly above or slightly below the isolation structure upper plane 126, such as about 10nm above or below.

As shown in FIG. 7, at least one gate 150 may be form over the portion of the active channel 146 extending above the isolation structures 122. The gate 150 may be fabricated by forming a gate dielectric layer 152 on or adjacent to the fin upper surface 116 and on or adjacent to the pair of laterally opposing fin sidewalls 114, and forming a gate electrode 154 on or adjacent the gate dielectric layer 152, either by a gate first or a gate last process flow, as will be understood to those skilled in the art.

The gate dielectric layer 152 may be formed from any well-known gate dielectric material,

including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium
5 oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate dielectric layer 152 can be formed by well-known techniques, such as by depositing a gate electrode material, such as chemical vapor deposition ("CVD"), physical vapor deposition ("PVD"), atomic layer deposition ("ALD"), and then patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in
10 the art.

The gate electrode 154 can be formed of any suitable gate electrode material. In an embodiment of the present disclosure, the gate electrode 154 may be formed from materials that include, but are not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide,
15 tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. The gate electrode 154 can be formed by well-known techniques, such as by blanket depositing a gate electrode material and then patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

20 As shown in FIG. 8, a gate spacer 156 may be deposited and patterned on the gate electrode 154 with well-known deposition and etching techniques. The gate spacer 156 may be formed from any appropriate dielectric material, including, but not limited to, silicon oxide, silicon nitride, and the like.

It is understood that a source region and a drain region (not shown) may be formed in the
25 active channel 146 on opposite sides of the gate 150 or a portions of the active channel 146 may be removed on opposite sides of the gate 150 and the source region and the drain region formed in place thereof. The source and drain regions may be formed of the same conductivity type, such as p-type conductivity. In some implementations of an embodiment of the present disclosure, the source and drain regions may have the substantially the same doping
30 concentration and profile while in other implementations they may vary. It is understood that only n-MOS are shown, p-MOS regions would be patterned and processed separately.

FIGs. 9-15 illustrate additional embodiments of the present description. Beginning with FIG. 7, a replacement gate process may be followed, wherein the gate dielectric 152 and the gate electrode 154 may be formed from sacrificial materials. A dielectric layer 162 may deposited

over the structure of FIG. 8 and planarized to expose the sacrificial gate electrode 154, as shown in FIG. 9. The sacrificial gate electrode 154 and the gate dielectric 152 may be removed to expose the active channel 146 between the remaining portions of the gate spacer 156 forming a exposed active channel region 146, as shown in FIGs. 10 and 11(cross-sectional view along line 5 11-11 of FIG. 10 with only cross-sectioned structures shown).

As shown in FIG. 12, the isolation structures 122 may be recessed within the exposed active channel region 146, such as by etching, to expose a portion of the sub-structure 144, such that a selective etch (e.g. wet etch, dry etch, or a combination thereof) may penetrate into the sub-structure 144 and remove the same including the nucleation layer 142, as shown in FIG. 13.

10 A dielectric material 166 may be deposited to fill the space left from the removal for the sub-structure 144 (see FIG. 12) and the nucleation layer 142 (see FIG. 12), as shown in FIG. 14, or to form a void 168, as shown in FIG. 15. Thereafter, the remaining components of a transistor may be formed following a known processing flow, such as a tri-gate processing flow, as will be understood to those skilled in the art. In another embodiment, as shown in FIG. 16, a gate oxide 15 layer 172 may be formed to surround the exposed active channel 146 and a gate electrode layer 174 may be formed to surround the gate oxide layer 172 and the remaining components of a transistor may be following a known gate all-around processing flow in single or multiple wire configurations, as will also be understood to those skilled in the art.

It is noted that although the detailed description describes non-planar transistors, the 20 present subject matter may be implemented in non-planar transistors, as will be understood to those skilled in the art.

FIG. 17 illustrates a computing device 200 in accordance with one implementation of the present description. The computing device 200 houses a board 202. The board 202 may include a number of components, including but not limited to a processor 204 and at least one 25 communication chip 206A, 206B. The processor 204 is physically and electrically coupled to the board 202. In some implementations the at least one communication chip 206A, 206B is also physically and electrically coupled to the board 202. In further implementations, the communication chip 206A, 206B is part of the processor 204.

Depending on its applications, the computing device 200 may include other components 30 that may or may not be physically and electrically coupled to the board 202. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass,

an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 206A, 206B enables wireless communications for the transfer of data to and from the computing device 200. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 206 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 200 may include a plurality of communication chips 206A, 206B. For instance, a first communication chip 206A may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 206B may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 204 of the computing device 200 may include microelectronic transistors as described above. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. Furthermore, the communication chip 206A, 206B may include microelectronic transistors fabricated as described above.

In various implementations, the computing device 200 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 200 may be any other electronic device that processes data.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-17. The subject matter may be applied to other microelectronic device and assembly applications, as well as any other appropriate transistor applications, as will be understood to those skilled in the art.

The following examples pertain to further embodiments, wherein Example 1 is a

microelectronic structure, comprising a substrate, a low band-gap active channel, and a high band-gap sub-structure disposed between the substrate and the low band-gap active channel, wherein the high band-gap sub-structure abuts the low band-gap active channel.

In Example 2, the subject matter of Example 1 can optionally include the high band-gap sub-structure comprising a material selected from the group consisting of indium aluminum arsenide, indium phosphide, gallium phosphide, gallium arsenide, gallium arsenide antimonide, aluminum arsenide antimonide, indium aluminum gallium arsenide, indium aluminum gallium phosphide, and aluminum gallium arsenide.

In Example 3, the subject matter of any of Examples 1 and 2 can optionally include the low band-gap active channel comprising a material selected from the group consisting of indium gallium arsenide, indium arsenide, and indium antimonide.

In Example 4, the subject matter of any of Examples 1 to 3 can optionally include a nucleation trench extending into the substrate and a nucleation layer abutting the nucleation trench.

In Example 5, the subject matter of Example 4 can optionally include the nucleation trench comprises a nucleation trench having (111) faceting.

In Example 6, the subject matter of any of Examples 4 and 5 can optionally include the nucleation layer comprising a material selected from the group consisting of indium phosphide, gallium phosphide, and gallium arsenide.

In Example 7, the subject matter of any of Examples 1 to 6 can optionally include a portion of the active channel extending above the isolation structures and a gate formed over the portion of the active channel extending above the isolation structures.

In Example 8, the subject matter of any of Examples 1 to 7 can optionally include the high band-gap sub-structure having a depth greater than about 50nm and a width of less than about 25nm.

The following examples pertain to further embodiments, wherein Example 9 is a microelectronic structure, comprising a substrate including a nucleation trench therein, a low band-gap active channel over the nucleation trench, and an insulative buffer disposed between the nucleation trench and the low band-gap active channel.

In Example 10, the subject matter of Example 9 can optionally include the insulative buffer comprising an insulative material.

In Example 11, the subject matter of Example 9 can optionally include the insulative buffer comprising a void.

In Example 12, the subject matter of any of Examples 9 to 11 can optionally include the

low band-gap active channel comprising a material selected from the group consisting of indium gallium arsenide, indium arsenide, and indium antimonide.

In Example 13, the subject matter of Example 12 can optionally include the nucleation trench comprising a nucleation trench having (111) faceting.

5 In Example 14, the subject matter of any of Examples 9 to 13, can optionally include a gate surrounding the active channel.

The following examples pertain to further embodiments, wherein Example 15 is a microelectronic structure, comprising forming at least one fin on a substrate, wherein the at least one fin comprises a pair of opposing sidewalls extending from the substrate; forming isolation

10 structures abutting each of the fin sidewalls; forming a trench by removing the at least one fin; forming a high band-gap sub-structure in the trench; and forming a low band-gap active channel in the trench, which abuts the high band-gap substructure.

In Example 16, the subject matter of Example 15 can optionally include forming the high band-gap sub-structure comprises forming a high band-gap sub-structure having a depth greater

15 than about 50nm and a width of less than about 25nm.

In Example 17, the subject matter of any of Examples 15 and 16 can optionally include forming the high band-gap sub-structure from a material selected from the group consisting of indium aluminum arsenide, indium phosphide, gallium phosphide, gallium arsenide, gallium arsenide antimonide, aluminum arsenide antimonide, indium aluminum gallium arsenide, indium

20 aluminum gallium phosphide, and aluminum gallium arsenide.

In Example 18, the subject matter of any of Examples 15 to 17 can optionally include forming the low band-gap active channel from a material selected from the group consisting of indium gallium arsenide, indium arsenide, and indium antimonide.

In Example 19, the subject matter of any of Examples 15 to 18 can optionally include

25 forming a nucleation trench extending into the substrate.

In Example 20, the subject matter of Example 19 can optionally include forming the nucleation trench comprising forming a nucleation trench having (111) faceting.

In Example 21, the subject matter of any of Examples 15 and 19 can optionally include forming a nucleation layer abutting the nucleation trench.

30 In Example 22, the subject matter of Example 21 can optionally include forming the nucleation layer from a material selected from the group consisting of indium phosphide, gallium phosphide, and gallium arsenide.

In Example 23, the subject matter of any of Examples 15 to 22 can optionally include recessing the isolation structure, such that at least a portion of the active channel extends above

the isolation structures.

In Example 24, the subject matter of any of Examples 15 to 23 can optionally include forming a gate over the portion of the active channel extending above the isolation structures.

In Example 25, the subject matter of any of Examples 15 to 24 can optionally include removing the high band-gap sub-structure to from a void between the low band-gap active channel and the substrate.

In Example 26, the subject matter of Example 25 can optionally include forming a gate to surround the low band-gap active channel.

In Example 27, the subject matter of any of Examples 25 and 26 can optionally include depositing an insulative material within the void.

Having thus described in detail embodiments of the present description, it is understood that the present description defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

Claimed:

1. A microelectronic structure, comprising:

a substrate;

5 a low band-gap active channel; and

a high band-gap sub-structure disposed between the substrate and the low band-gap active channel, wherein the high band-gap sub-structure abuts the low band-gap active channel.

2. The microelectronic structure of claim 1, wherein the high band-gap sub-structure comprises a material selected from the group consisting of indium aluminum arsenide, indium
10 phosphdide, gallium phosphide, gallium arsenide, gallium arsenide antimonide, aluminium arsenide antimonide, indium aluminum gallium arsenide, indium aluminum gallium phosphide, and aluminum gallium arsenide.

3. The microelectronic structure of either claim 1 or 2, wherein the low band-gap active channel comprises a material selected from the group consisting of indium gallium arsenide,
15 indium arsenide, and indium antimonide.

4. The microelectronic structure of claim 1, further including a nucleation trench extending into the substrate and a nucleation layer abutting the nucleation trench.

5. The microelectronic structure of claim 4, wherein the nucleation trench comprises a nucleation trench having (111) faceting.

20 6. The microelectronic structure of either claim 4 or 5, wherein the nucleation layer comprises a material selected from the group consisting of indium phosphide, gallium phosphide, and gallium arsenide.

7. The microelectronic structure of claim 1, further comprising a portion of the active channel extending above the isolation structures and a gate formed over the portion of the active
25 channel extending above the isolation structures.

8. The microelectronic structure of claim 1, wherein the high band-gap sub-structure has a depth greater than about 50nm and a width of less than about 25nm.

9. A microelectronic structure, comprising:

a substrate including a nucleation trench therein;

30 a low band-gap active channel over the nucleation trench; and

an insulative buffer disposed between the nucleation trench and the low band-gap active channel.

10. The microelectronic structure of claim 9, wherein the insulative buffer comprises an insulative material.

11. The microelectronic structure of claim 9, wherein the insulative buffer comprises a void.

12. The microelectronic structure of claims 9, wherein the low band-gap active channel comprises a material selected from the group consisting of indium gallium arsenide, indium
5 arsenide, and indium antimonide.

13. The microelectronic structure of any of claims 9 to 12, further comprising a gate surrounding the active channel.

14. A method of fabricating a microelectronic structure, comprising:

forming at least one fin on a substrate, wherein the at least one fin comprises a pair of
10 opposing sidewalls extending from the substrate;

forming isolation structures abutting each of the fin sidewalls;

forming a trench by removing the at least one fin;

forming a high band-gap sub-structure in the trench; and

forming a low band-gap active channel in the trench, which abuts the high band-gap
15 substructure.

15. The method of claim 14, wherein forming the high band-gap sub-structure comprises forming a high band-gap sub-structure having a depth greater than about 50nm and a width of less than about 25nm.

16. The method of claim 14, wherein forming the high band-gap sub-structure comprises
20 forming the high band-gap sub-structure from a material selected from the group consisting of indium aluminum arsenide, indium phosphide, gallium phosphide, gallium arsenide, gallium arsenide antimonide, aluminium arsenide antimonide, indium aluminum gallium arsenide, indium aluminum gallium phosphide, and aluminum gallium arsenide.

17. The method of any of claims 14 to 16, wherein forming the low band-gap active
25 channel comprises forming the low band-gap active channel from a material selected from the group consisting of indium gallium arsenide, indium arsenide, and indium antimonide.

18. The method of claim 14, wherein forming the trench further includes forming a nucleation trench extending into the substrate.

19. The method of claim 18, wherein forming the nucleation trench comprises forming a
30 nucleation trench having (111) faceting.

20. The method of claim 14, further comprising forming a nucleation layer abutting the nucleation trench.

21. The method of claim 20, wherein forming the nucleation layer comprises forming the nucleation layer from a material selected from the group consisting of indium phosphide, gallium

phosphide, and gallium arsenide.

22. The method of claim 14, further comprising recessing the isolation structure, such that at least a portion of the active channel extends above the isolation structures.

23. The method of claim 22, further comprising forming a gate over the portion of the
5 active channel extending above the isolation structures.

24. The method of claim 14, further comprising removing the high band-gap sub-structure to from a void between the low band-gap active channel and the substrate.

25. The method of claim 24, further comprising depositing an insulative material within the void.

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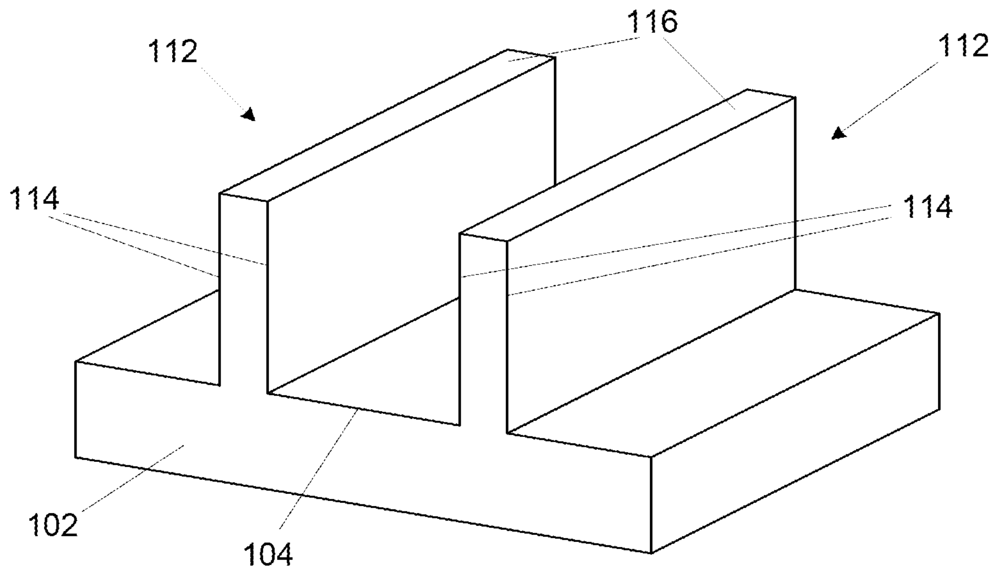

FIG. 1

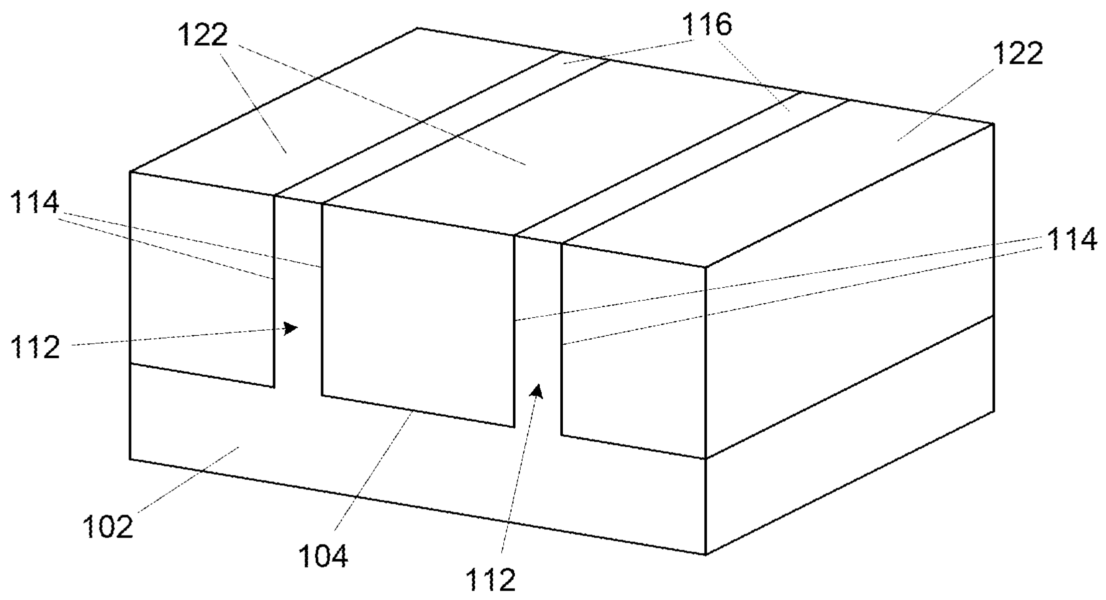

FIG. 2

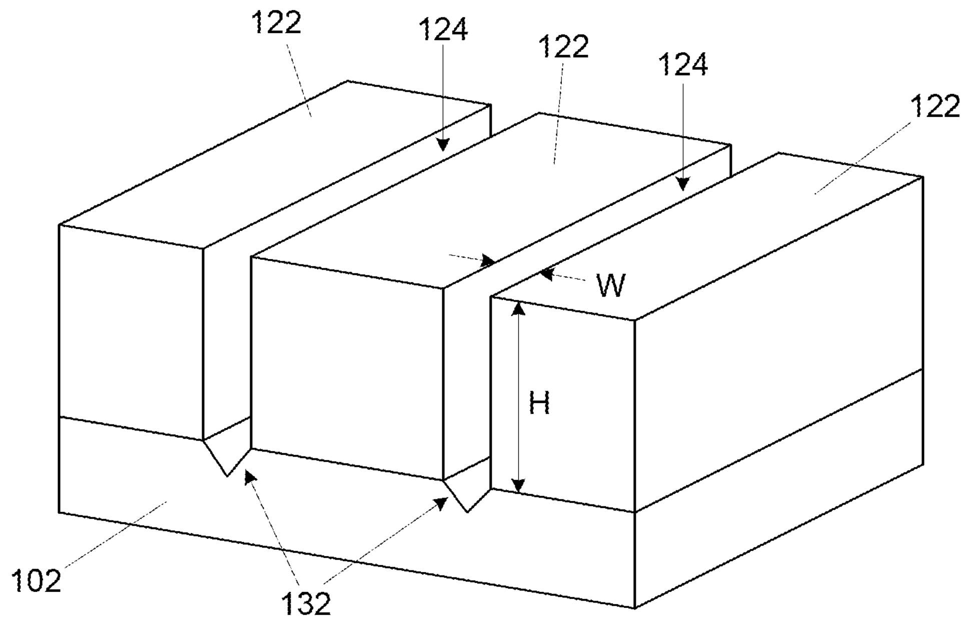

FIG. 3

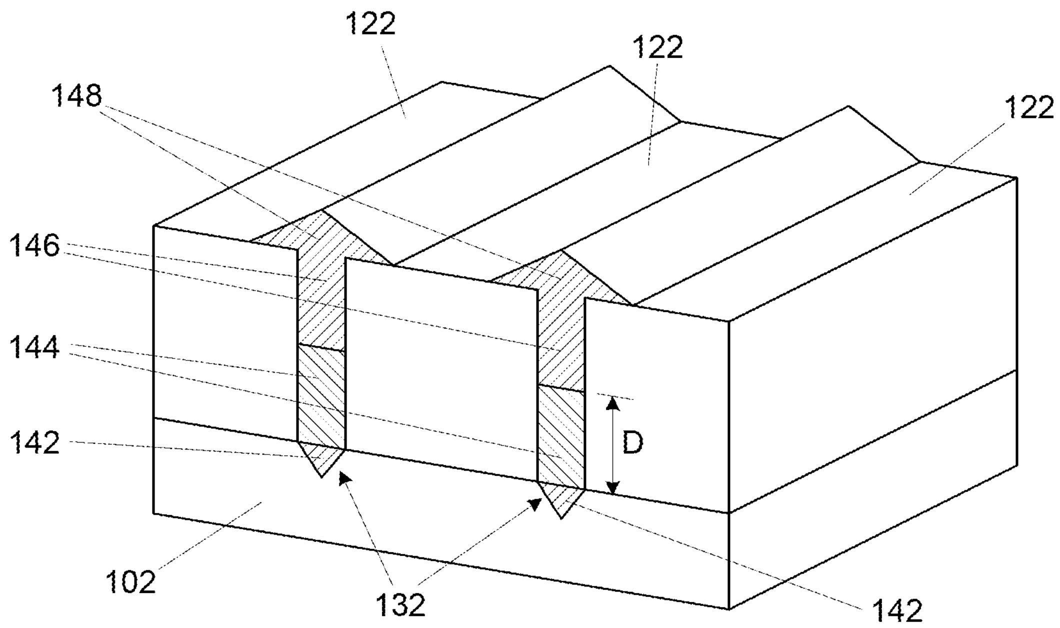

FIG. 4

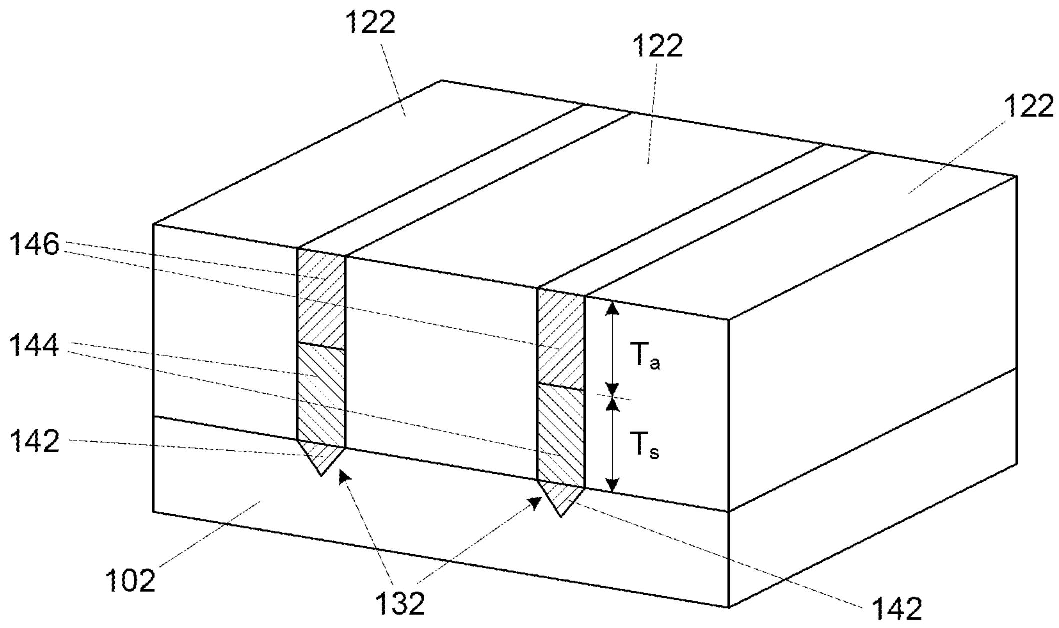

FIG. 5

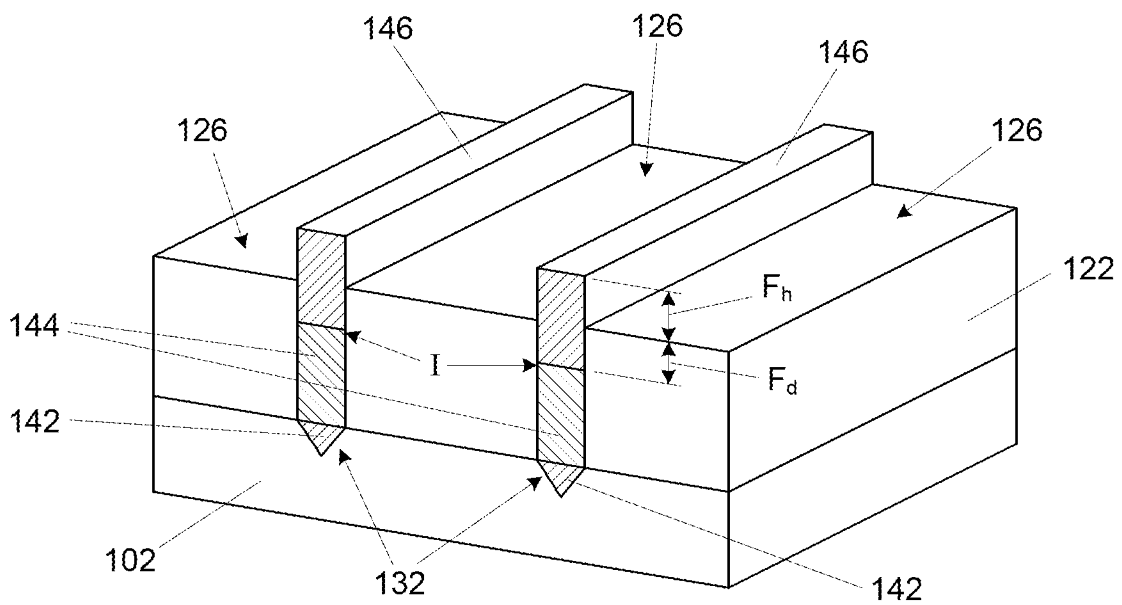

FIG. 6

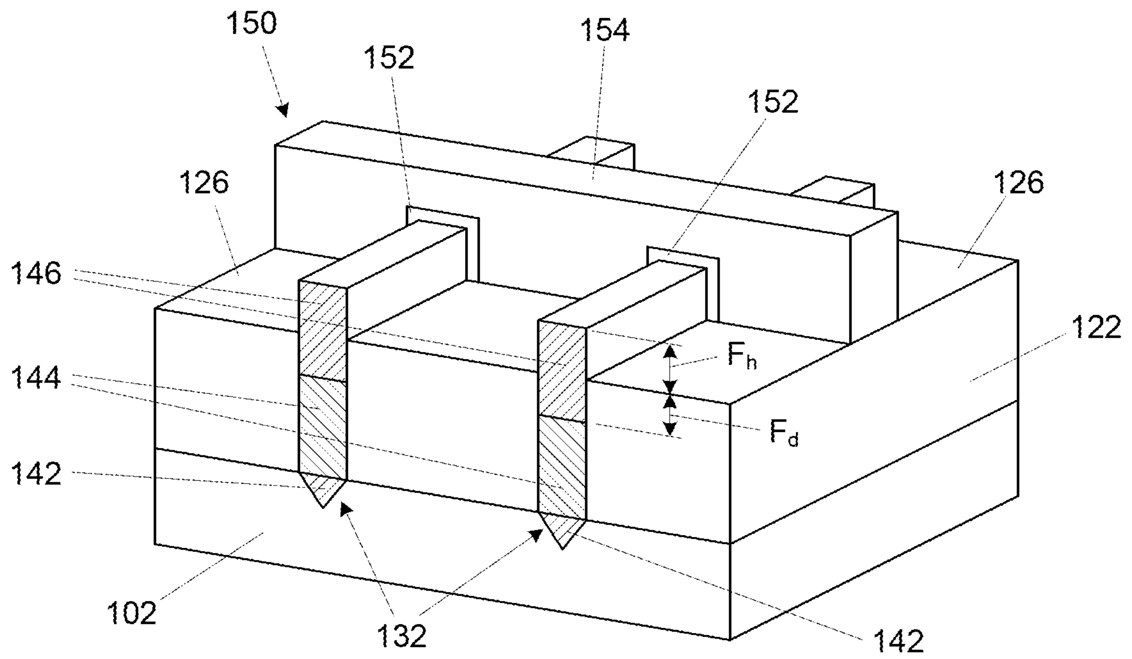

FIG. 7

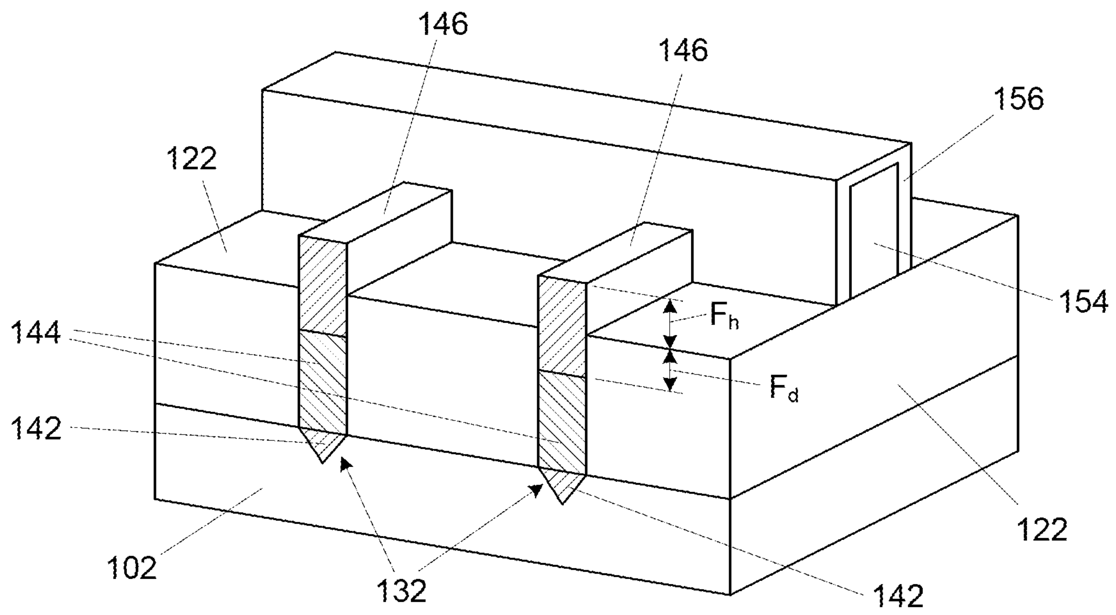

FIG. 8

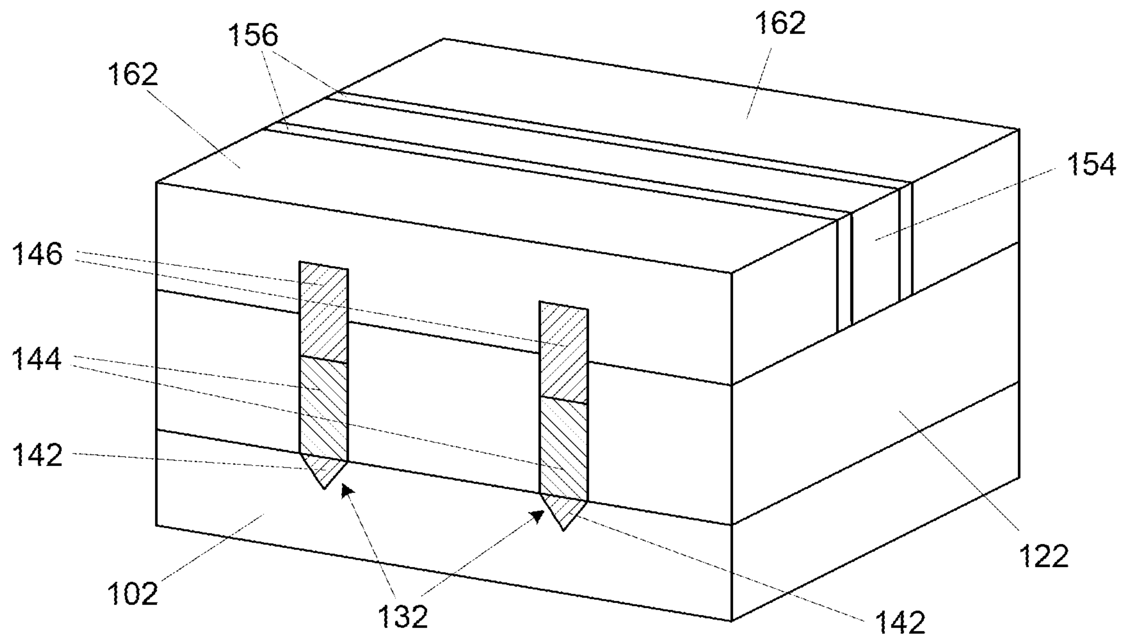

FIG. 9

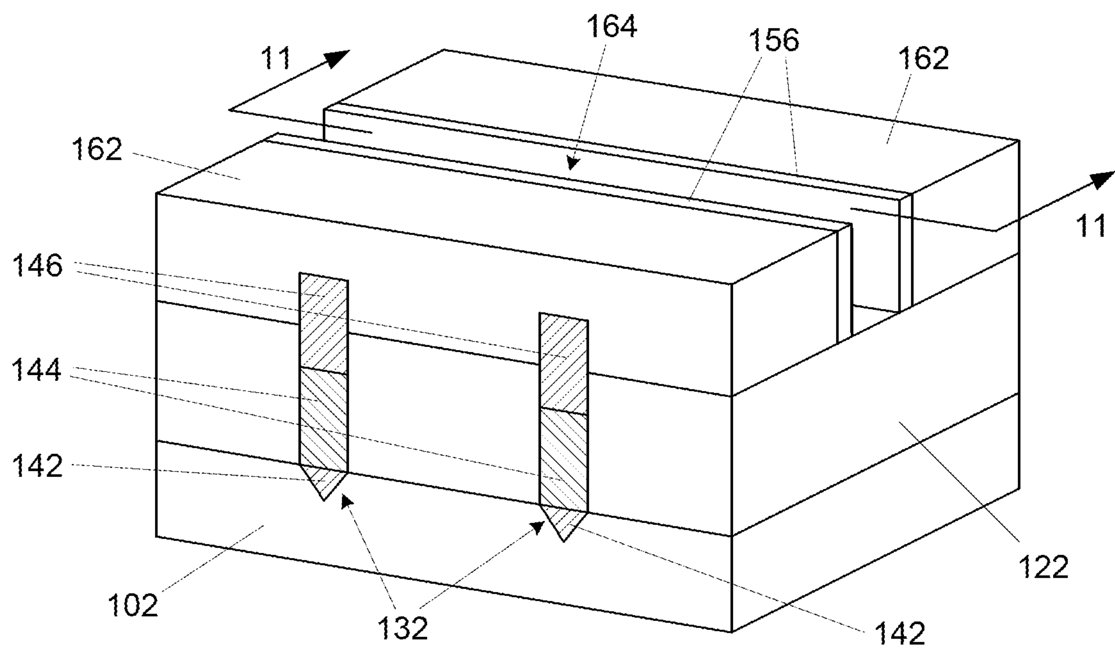

FIG. 10

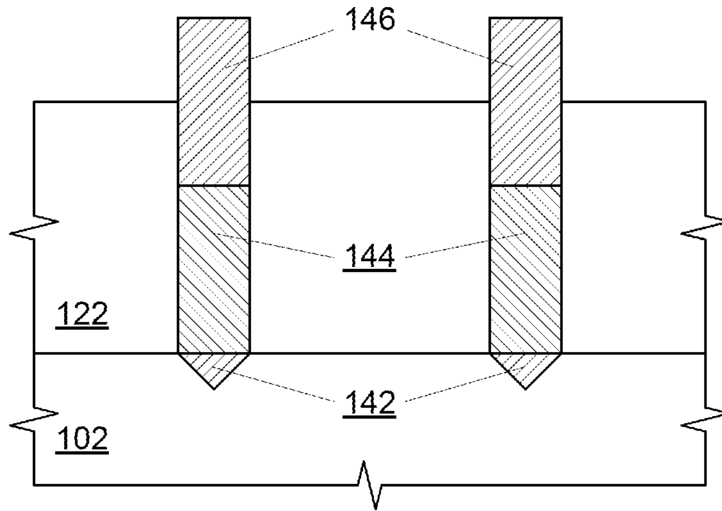

FIG. 11

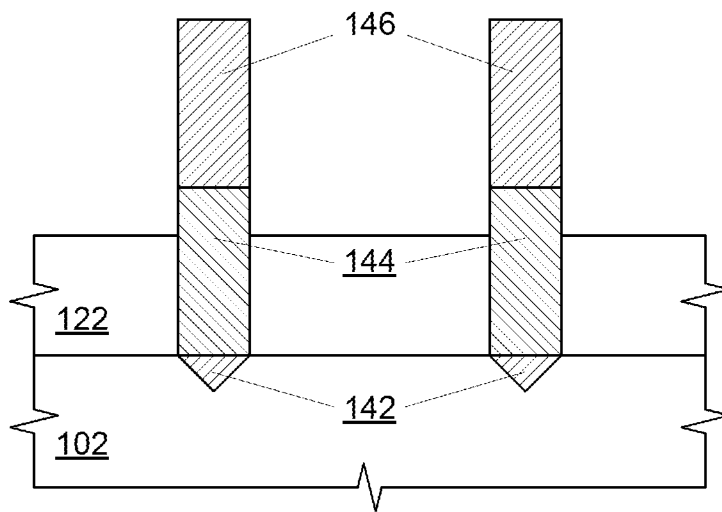

FIG. 12

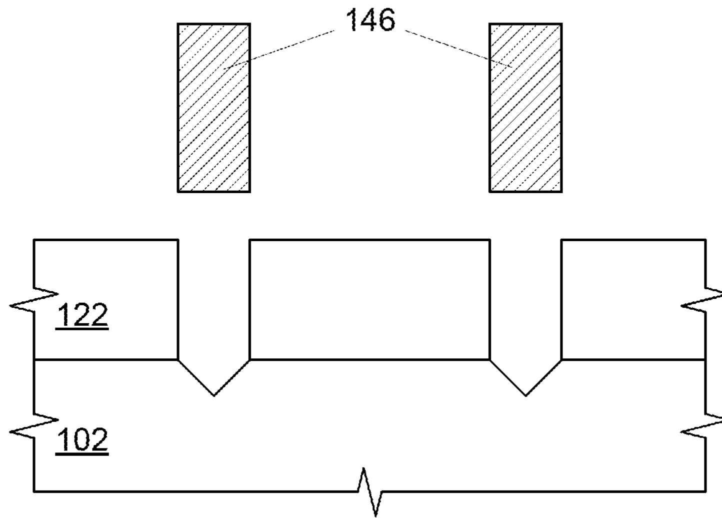

FIG. 13

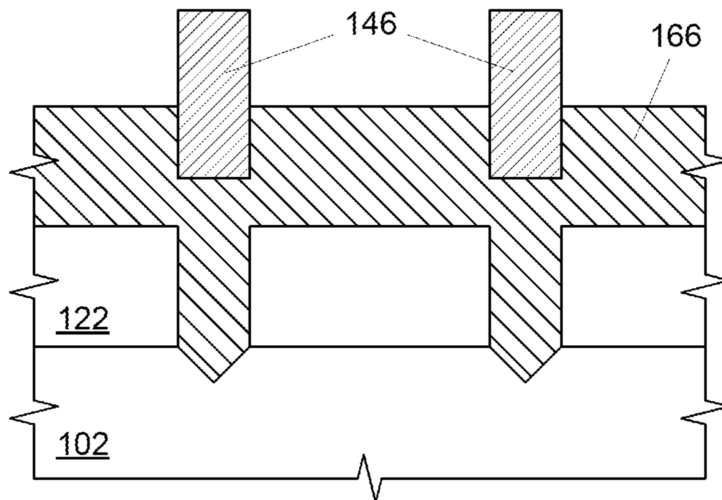

FIG.14

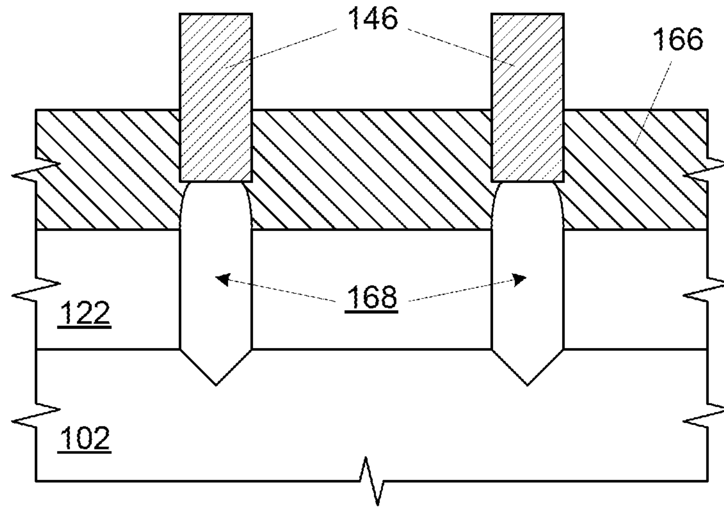

FIG. 15

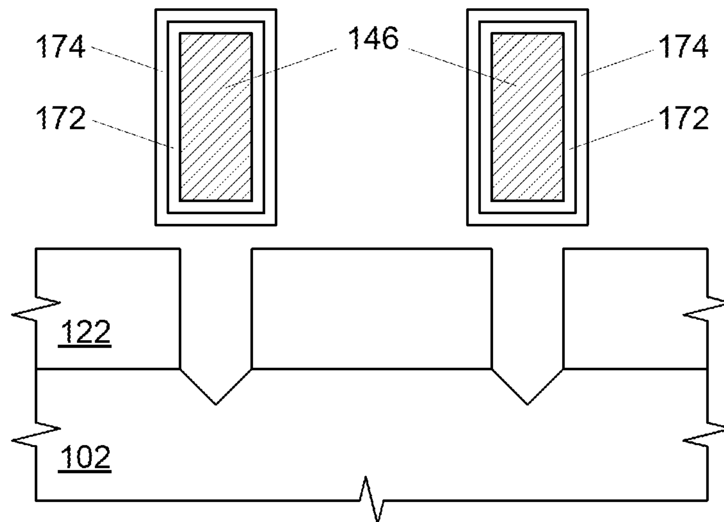

FIG. 16

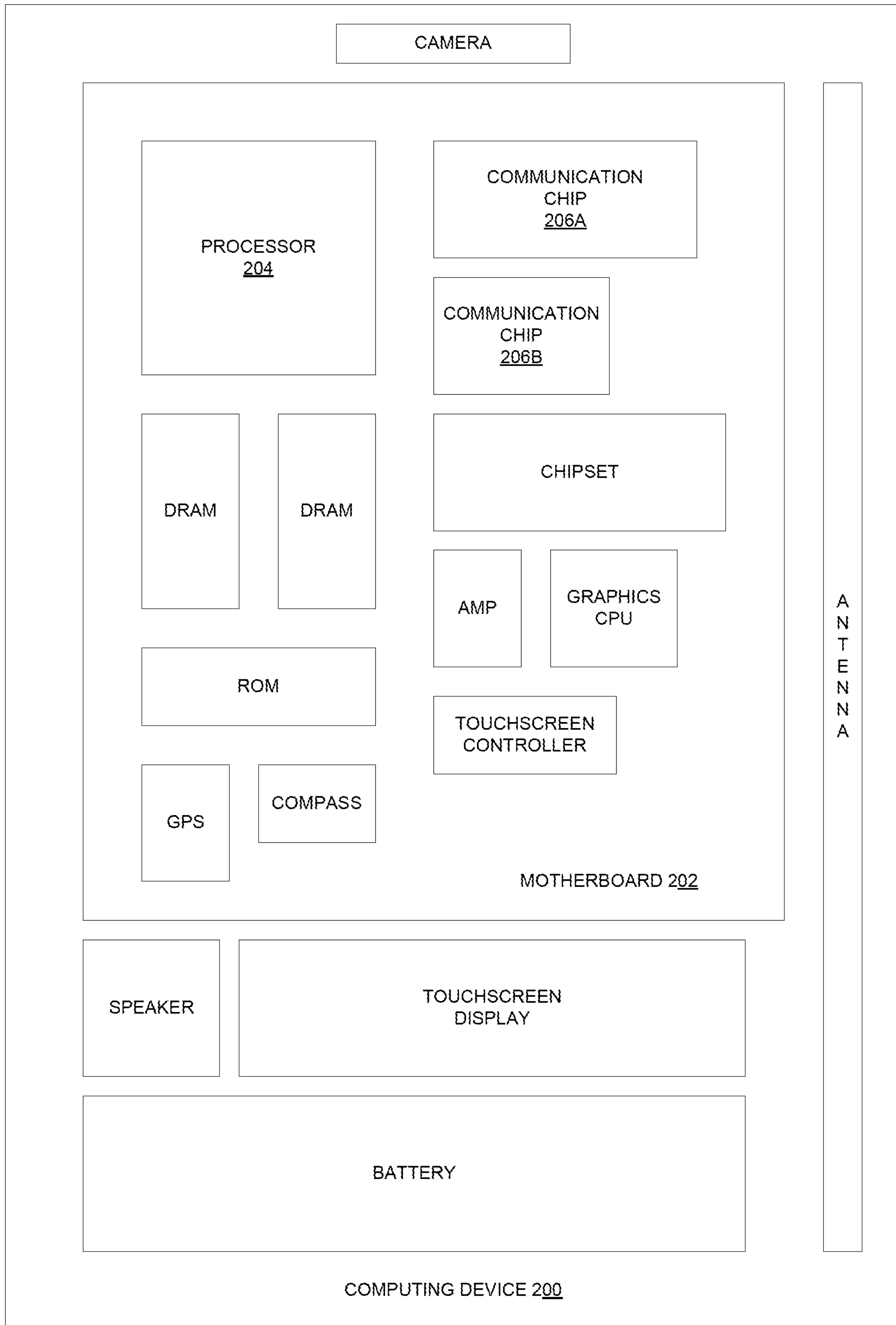

FIG. 17

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 21/336; H01L 29/205; H01L 21/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: fin, channel, indium, gallium, arsenide, band gap, nucleation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0264438 A1 (MARTIN CHRISTOPHER HOLLAND et al.) 18 September 2014 See abstract, paragraphs [0024]-[0046], [0071], [0075] and figures 3, 10-17.	1-3,7,8,14-17,22-25
Y		4-6,12,13,18-21
A		9-11
X	US 2013-0105860 A1 (ANTHONY J. LOCHTEFELD et al.) 02 May 2013 See abstract, paragraphs [0115]-[0117], [0121], [0127] and figures 5A, 14B, 15A.	9-11
Y		4-6,12,13,18-21
A	US 2013-0034943 A1 (ANTHONY J. LOCHTEFELD) 07 February 2013 See abstract, paragraphs [0029]-[0054] and figures 1-7.	1-25
A	US 2013-0270607 A1 (GERBEN DOORNBOS et al.) 17 October 2013 See abstract, paragraphs [0017]-[0048] and figures 1-8B.	1-25
A	WO 2014-133293 A1 (INDUSTRY-ACADEMIC COOPERATION, YONSEI UNIVERSITY et al.) 04 September 2014 See abstract, paragraphs [0047]-[0060] and figures 2-8.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
18 June 2015 (18.06.2015)

Date of mailing of the international search report
19 June 2015 (19.06.2015)

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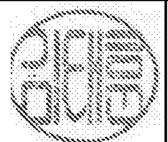

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2014/056528

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