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(54) **PROCESS OF VERTICALLY STACKING MULTIPLE WAFERS SUPPORTING DIFFERENT ACTIVE INTEGRATED CIRCUIT (IC) DEVICES**

division of application No. 10/077,967, filed on Feb. 20, 2002, now Pat. No. 6,762,076.

Publication Classification

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(57) **ABSTRACT**

A method of vertically stacking wafers is provided to form three-dimensional (3D) wafer stack. Such method comprising: selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers; bonding the adjacent wafers, via the metallic lines, to establish electrical connections between active devices on vertically stacked wafers; and forming one or more vias to establish electrical connections between the active devices on the vertically stacked wafers and an external interconnect. Metal bonding areas on opposing surfaces of the adjacent wafers can be increased by using one or more dummy vias, tapered vias, or incorporating an existing copper (Cu) dual damascene process.

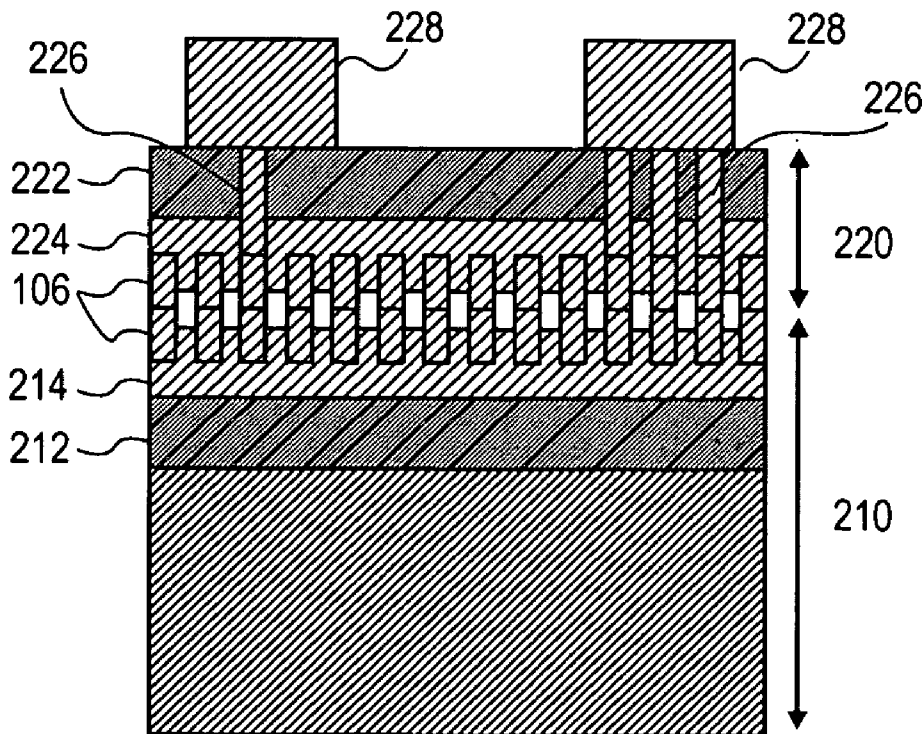
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Related U.S. Application Data

(60) Continuation of application No. 10/855,032, filed on May 26, 2004, now Pat. No. 7,157,787, which is a

200



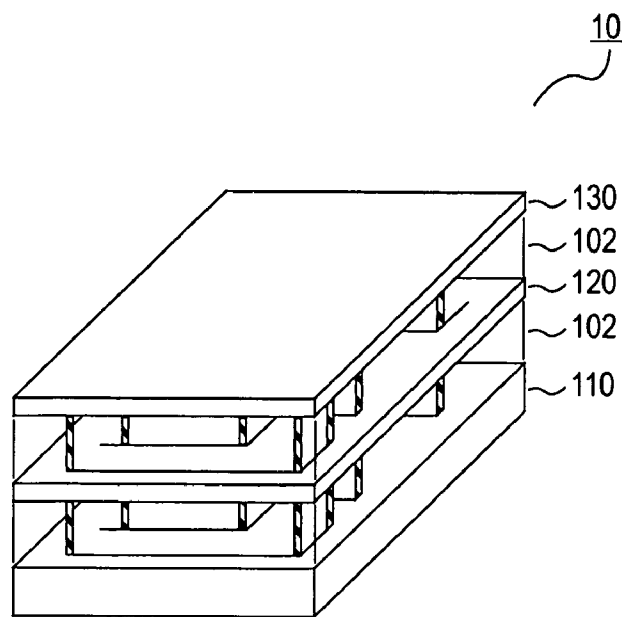


FIG. 1

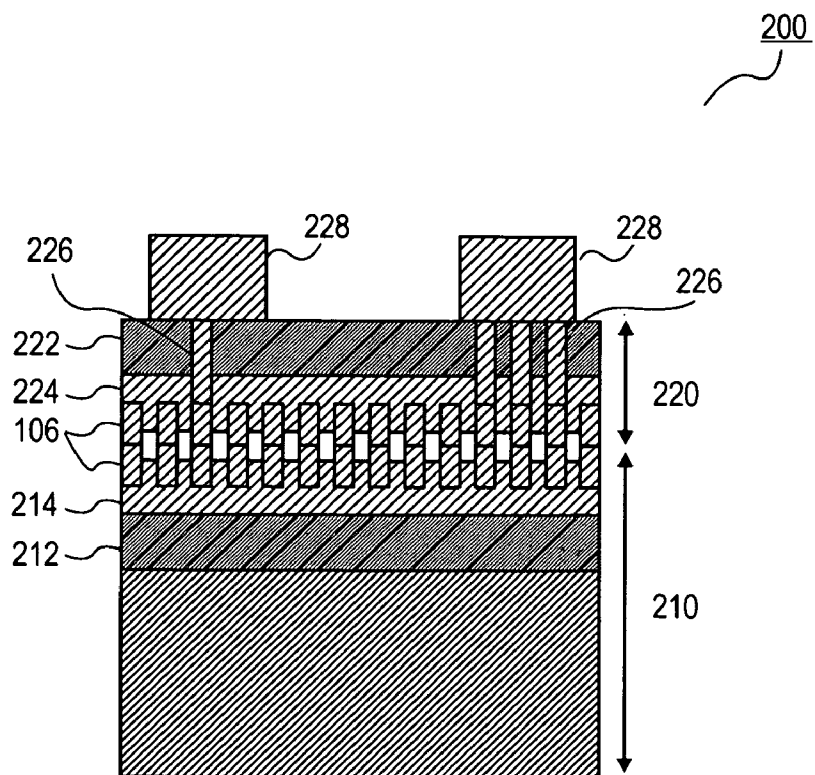


FIG. 2

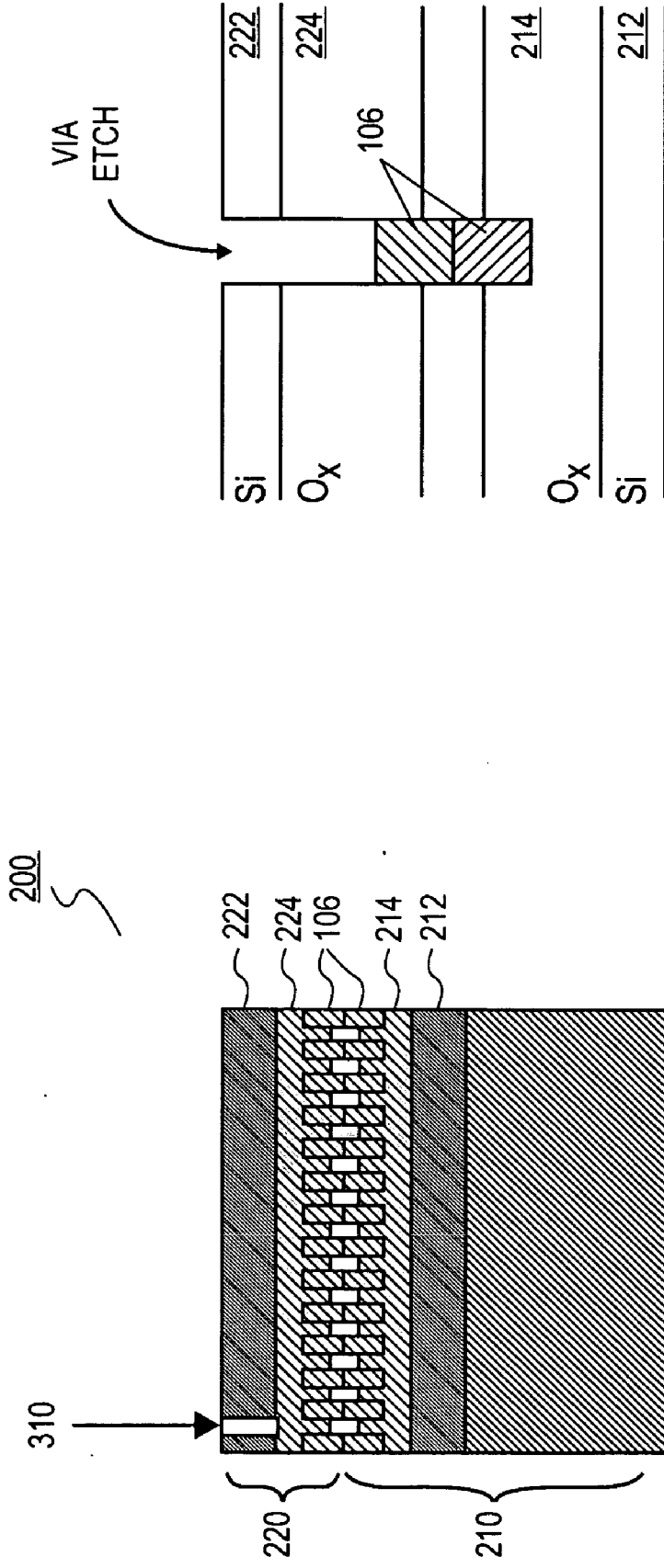


FIG. 3B

FIG. 3A

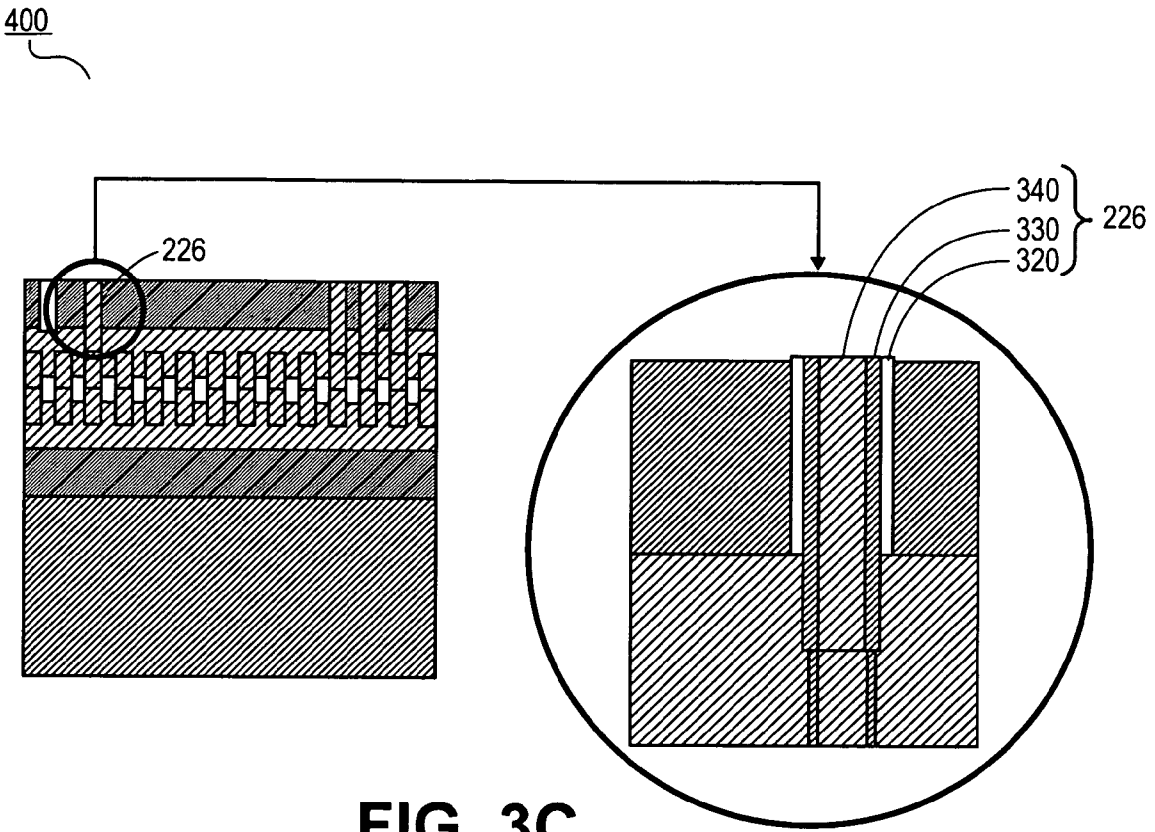


FIG. 3C

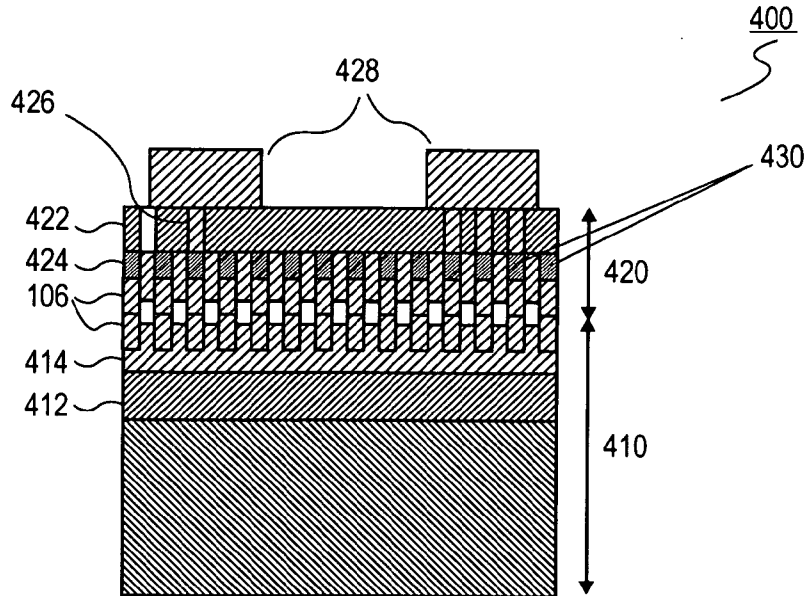


FIG. 4

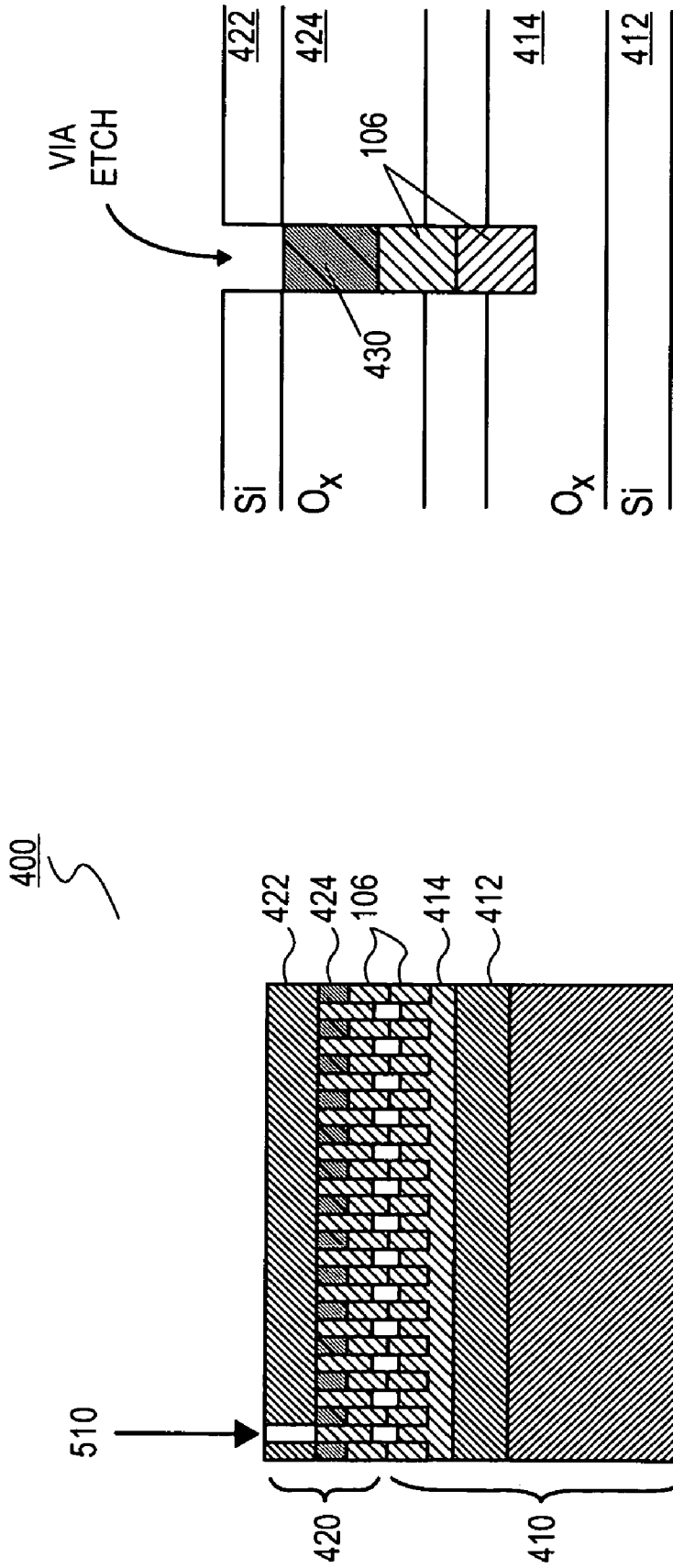


FIG. 5A

FIG. 5B

400

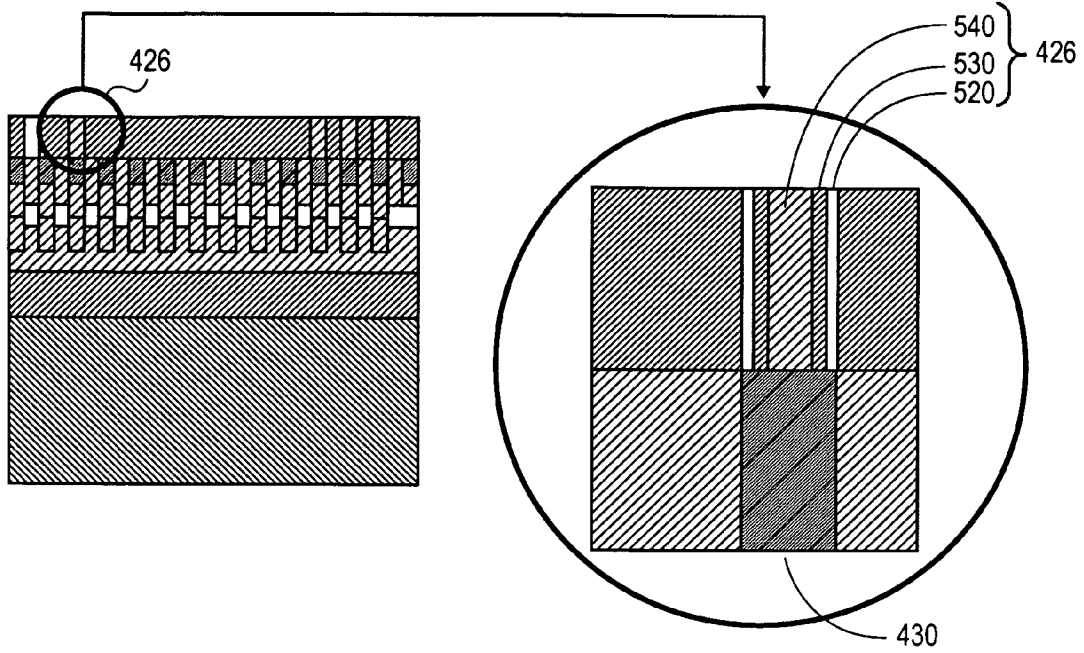


FIG. 5C

Si Via that processed during STI steps

200

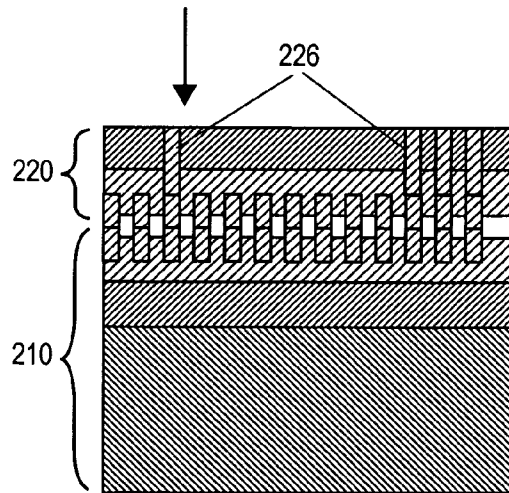


FIG. 6

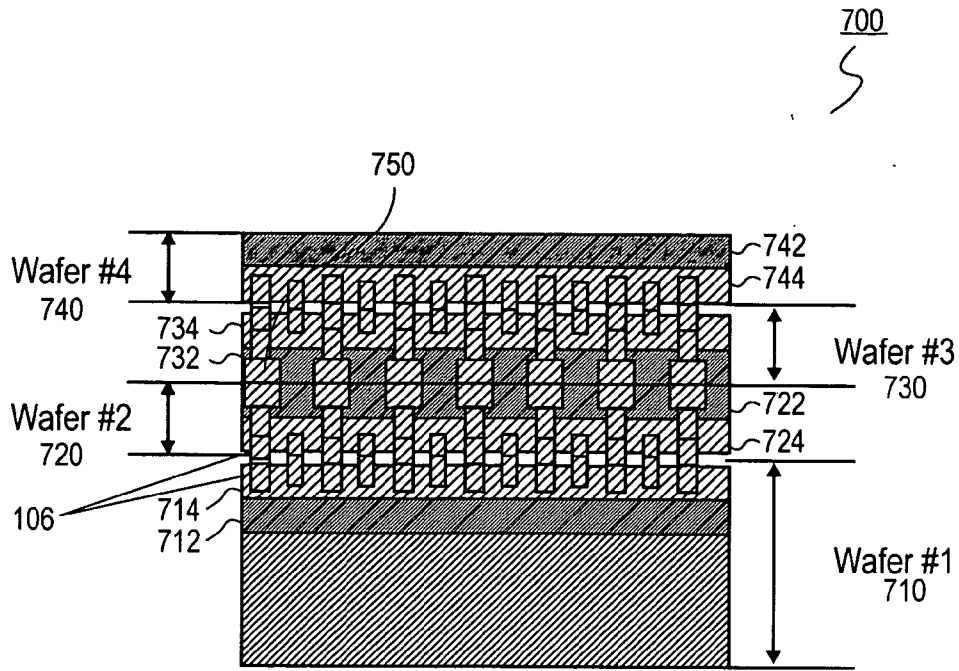


FIG. 7A

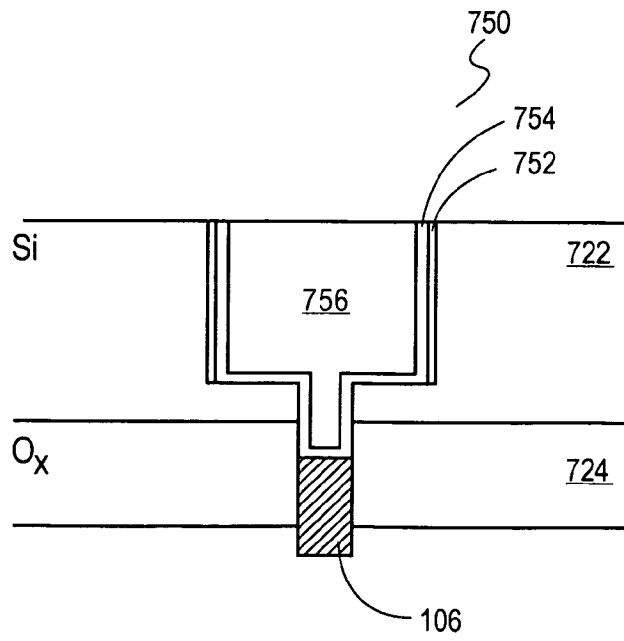


FIG. 7B

800
S

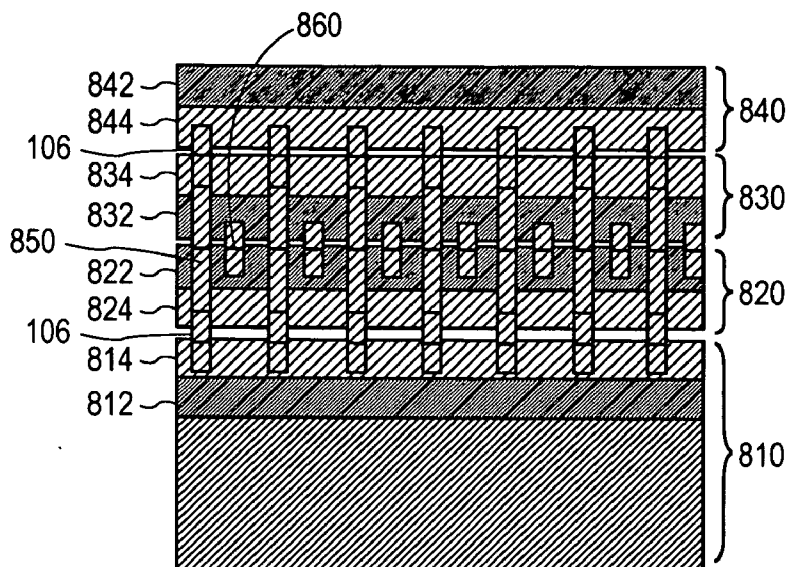


FIG. 8

900
S

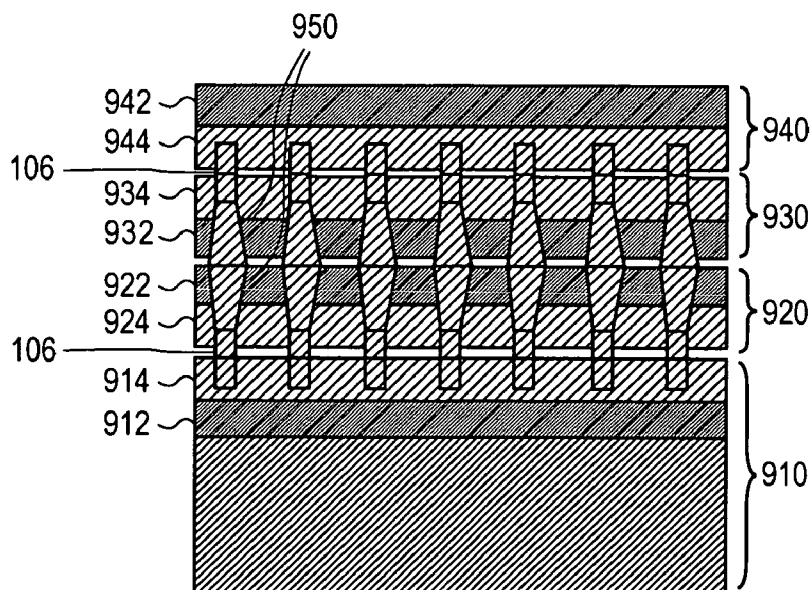


FIG. 9

**PROCESS OF VERTICALLY STACKING
MULTIPLE WAFERS SUPPORTING DIFFERENT
ACTIVE INTEGRATED CIRCUIT (IC) DEVICES**

CROSS-REFERENCE TO RELATED
APPLICATIONS

[0001] The present patent application is a Continuation Application of, and claims priority to, Ser. No. 10/855,032, filed on May 26, 2004, which is a Divisional Application of, and claims priority to, Ser. No. 10/077,967, filed Feb. 20, 2002, which issued as U.S. Pat. No. 6,762,076 on Jul. 13, 2004.

[0002] This application is related to the following patents and pending applications, which are assigned to the assignee of this application: U.S. Pat. No. 6,661,085, filed on Feb. 6, 2002 and issued on Dec. 9, 2003; U.S. patent application Ser. No. 10/066,643, filed on Feb. 6, 2002 and issued as U.S. Pat. No. 6,975,016 on Dec. 13, 2005; U.S. patent application Ser. No. 10/066,645, filed on Feb. 6, 2002 and issued as U.S. Pat. No. 6,887,769 on May 3, 2005; U.S. patent application Ser. No. 10/613,006, filed on Jul. 7, 2003 and which has been allowed; and U.S. patent application Ser. No. 10/695,328, filed on Oct. 27, 2003 and issued as U.S. Pat. No. 7,037,804 on May 2, 2006.

TECHNICAL-FIELD

[0003] The present invention relates to a semiconductor process and, more specifically, relates to a process of vertically stacking multiple wafers supporting different active IC devices on a single die with low cost and high via density with optimum metal bonding areas.

BACKGROUND

[0004] Integrated circuits (ICs) form the basis for many electronic systems. Essentially, an integrated circuit (IC) includes a vast number of transistors and other circuit elements that are formed on a single semiconductor wafer or chip and are interconnected to implement a desired function. The complexity of these integrated circuits (ICs) requires the use of an ever increasing number of linked transistors and other circuit elements.

[0005] Many modern electronic systems are created through the use of a variety of different integrated circuits; each integrated circuit (IC) performing one or more specific functions. For example, computer systems include at least one microprocessor and a number of memory chips. Conventionally, each of these integrated circuits (ICs) is formed on a separate chip, packaged independently and interconnected on, for example, a printed circuit board (PCB).

[0006] As integrated circuit (IC) technology progresses, there is a growing desire for a "system on a chip" in which the functionality of all of the IC devices of the system are packaged together without a conventional PCB. Ideally, a computing system should be fabricated with all the necessary IC devices on a single chip. In practice, however, it is very difficult to implement a truly high-performance "system on a chip" because of vastly different fabrication processes and different manufacturing yields for the logic and memory circuits.

[0007] As a compromise, various "system modules" have been introduced that electrically connect and package inte-

grated circuit (IC) devices which are fabricated on the same or on different semiconductor wafers. Initially, system modules have been created by simply stacking two chips, e.g., a logic and memory chip, one on top of the other in an arrangement commonly referred to as chip-on-chip structure. Subsequently, multi-chip module (MCM) technology has been utilized to stack a number of chips on a common substrate to reduce the overall size and weight of the package, which directly translates into reduced system size.

[0008] Existing multi-chip module (MCM) technology is known to provide performance enhancements over single chip or chip-on-chip (COC) packaging approaches. For example, when several semiconductor chips are mounted and interconnected on a common substrate through very high density interconnects, higher silicon packaging density and shorter chip-to-chip interconnections can be achieved. In addition, low dielectric constant materials and higher wiring density can also be obtained which lead to the increased system speed and reliability, and the reduced weight, volume, power consumption and heat to be dissipated for the same level of performance. However, MCM approaches still suffer from additional problems, such as bulky package, wire length and wire bonding that gives rise to stray inductances that interfere with the operation of the system module.

[0009] An advanced three-dimensional (3D) wafer-to-wafer vertical stack technology has been recently proposed by researchers to realize the ideal high-performance "system on a chip" as described in "Face To Face Wafer Bonding For 3D Chip Stack Fabrication To Shorten Wire Lengths" by J. F. McDonald et al., Rensselaer Polytechnic Institute (RPI) presented on Jun. 27-29, 2000 VMIC Conference, and "Copper Wafer Bonding" by A. Fan et al., Massachusetts Institute of Technology (MIT), Electrochemical and Solid-State Letters, 2 (10) 534-536 (1999). In contrast to the existing multi-chip module (MCM) technology which seeks to stack multiple chips on a common substrate, 3-D wafer-to-wafer vertical stack technology seeks to achieve the long-awaited goal of vertically stacking many layers of active IC devices such as processors, programmable devices and memory devices inside a single chip to shorten average wire lengths, thereby reducing interconnect RC delay and increasing system performance.

[0010] One major challenge of 3-D wafer-to-wafer vertical stack integration technology is the bonding between wafers and between die in a single chip. In the RPI publication, polymer glue is used to bond the vertically stacked wafers. In the MIT publication, copper (Cu) is used to bond the vertically stacked wafers; however, a handle (carrier wafer) is required to transport thinly stacked wafers and a polymer glue is also used to affix the handle on the top wafer during the vertically stacked wafer processing. As a result, there is a need for a simpler but more efficient process of vertically stacking multiple wafers supporting different active IC devices on a single die with low cost and high via density with optimum metal bonding areas.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] A more complete appreciation of exemplary embodiments of the present invention, and many of the attendant advantages of the present invention, will become readily apparent as the same becomes better understood by

reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

[0012] FIG. 1 illustrates an example three-dimensional (3-D) wafer-to-wafer vertical stack forming a single chip;

[0013] FIG. 2 illustrates an example 2-wafer vertical stack according to an embodiment of the present invention;

[0014] FIGS. 3A-3C illustrate an example wafer bond and via etch in an example 2-wafer vertical stack as shown in FIG. 2;

[0015] FIG. 4 illustrates an example 2-wafer vertical stack according to another embodiment of the present invention;

[0016] FIGS. 5A-5C illustrate an example wafer bond and via etch in an example 2-wafer vertical stack as shown in FIG. 4;

[0017] FIG. 6 illustrates an example wafer bond and via etch during STI process steps in an example 2-wafer vertical stack shown in FIG. 2;

[0018] FIGS. 7A-7B illustrate an example 4-wafer vertical stack with increased metal bonding areas for multiple wafer-to-wafer bonding according to an embodiment of the present invention;

[0019] FIG. 8 illustrates example 4-wafer vertical stack with increased metal bonding areas for multiple wafer-to-wafer bonding according to another embodiment of the present invention; and

[0020] FIG. 9 illustrates an example 4-wafer vertical stack with increased metal bonding areas for multiple wafer-to-wafer bonding according to yet another embodiment of the present invention.

DETAILED DESCRIPTION

[0021] The present invention is applicable for use with all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, MOS transistors, CMOS devices, MOSFETs, and new memory devices and communication devices such as smart cards, cellular phones, electronic tags, and gaming devices which may become available as semiconductor technology develops in the future. However, for the sake of simplicity, discussions will concentrate mainly on exemplary use a three-dimensional (3-D) wafer-to-wafer vertical stack, although the scope of the present invention is not limited thereto.

[0022] Attention now is directed to the drawings and particularly to FIG. 1, an example three-dimensional (3-D) wafer-to-wafer vertical stack is illustrated. As shown in FIG. 1, the 3-D vertical stack (chip) 100 may comprise any number of active device polysilicon (Si) wafers, such as wafer #1110 including, for example, one or more microprocessors; wafer #2120 including one or more memory devices; and wafer #3130 including one or more radio-frequency (RF) or optical communication devices. Typically, a dielectric layer 102 is used to bond the active device wafers 110, 120 and 130.

[0023] According to one aspect of the present invention, however, a metal to metal bond can be used to stack wafers 110, 120 and 130 to form the vertical stack 100. This metal

to metal bond method may serve not only as electrical connections to active IC devices on the vertically stacked wafers 110, 120 and 130 on a 3-D wafer-to-wafer vertical stack 100 but also bond adjacent wafers 110, 120 and 130. Dummy metal, bonding pads can also be made to increase the surface area for wafer to wafer bonding and serve as auxiliary structures such as ground planes or heat conduits for the active IC devices. In addition, improved etch stop layers for the Si via etch can be used in vertically stacked wafer processing (i.e., 3-D interconnect processing) which provide more efficient electrical conductivity between vertically stacked wafers 110, 120 and 130.

[0024] Turning now to FIG. 2, an example three-dimensional (3-D) wafer-to-wafer vertical stack according to an embodiment of the present invention is illustrated. Specifically, FIG. 2 illustrates an example 2-wafers vertical stack 200. However, the number of wafers in a vertical stack is not limited hereto. Through 3-D interconnect structure, wiring between vertically stacked wafers can be shortened resulting a faster signal and minimal interconnect RC delays. In addition, the vertical stack can effectively integrate diverse process technologies on a single wafer process, such as, for example, logic/memory stacking, processor stacking, optical interconnect, system-on-chip, and RF interconnect.

[0025] As shown in FIG. 2, the bottom silicon (Si) wafer 210 may include an active silicon (Si) layer 212 supporting one or more active IC devices (not shown), and an interlayer dielectric (ILD) layer 214. Likewise, the top Si wafer 220 may also include an active silicon (Si) layer 222 supporting one or more active IC devices (not shown), and an interlayer dielectric (ILD) layer 224. In both wafers 210 and 220, the ILD layers 214 and 224 are shown as a single layer respectively for purposes of simplification. In practice, the ILD layers 214 and 224 may comprise a stack or composite of dielectric material. Typically, the ILD layers 214 and 224 may be oxide deposited on the respective active silicon (Si) layers 212 and 222. In addition, the bottom wafer 210 can be made thick to support the stacking of the top wafer 220, while the top wafer 220 can be made thinned to minimize interconnection lengths between vertically stacked wafers 210 and 220. The wafers 210 and 220 can also be aligned using a standard alignment tool and bonded, via a metal bonding layer 106 deposited on opposing surfaces of the bottom wafer 210 and the top wafer 220 at designated bonding areas to establish electrical connections between active IC devices on vertically stacked wafers 210 and 220 and to bond adjacent wafers 210 and 220, while maintaining electrical isolation between bonding areas via ILD layers 214 and 224.

[0026] In the example 2-wafer vertical stack 200 shown in FIG. 2, the metal bonding process between adjacent wafers 210 and 220 may be performed in a vacuum or an inert gas environment, and a dielectric recess can be made surrounding the metal bonding areas, e.g., the metal bonding layer 106 to facilitate direct metal bonding between adjacent wafers 210 and 220 to ensure that the adjacent wafers 210 and 220 are bonded, while maintaining electrical isolation between the metal bonding areas. The metal bonding layer 106 may include a plurality of interconnect metallic lines deposited on opposing surfaces of the vertically stacked wafers 210 and 220 that can be used for metal diffusion bonding while serving as electrical contacts between active IC devices on the vertically stacked wafers 210 and 220.

Copper (Cu) or Cu alloy may be selected because of its low electrical resistivity, high electro-migration resistance and high diffusivity. However, other metallic materials can also be used, including, for example, tin, indium, gold, nickel, silver, palladium, palladium-nickel alloy, titanium, or any combination thereof.

[0027] After the wafer bonding process is completed, the top wafer **220** can also be thinned for a subsequent silicon (Si) via process. Thereafter, one or more interwafer (interconnect) vias (or via holes) **226** can be etched, via the top wafer **220**, to establish electrical connections between active IC devices on the vertically stacked wafers **210** and **220** and an external interconnect (not shown), via a C4 bump **228**. Interwafer vias **226** can be formed employing damascene technology, that is, forming an opening, e.g., a damascene opening in the ILD layer **224** through the active layer **222**, depositing a diffusion barrier layer, typically tantalum (Ta), titanium (Ti), or tungsten (W), and filling the opening with copper (Cu) or a Cu alloy. The opening in the ILD layer **224** can be filled by initially depositing a seed layer and then electroplating the copper (Cu) or Cu alloy layer. The seed layer typically comprises copper (Cu), though other materials such as refractory metals have been suggested. Both the seed layer and barrier layer are typically deposited by a Physical Vapor Deposition (PVD) process and, for purposes of simplification, can be referred to as a single barrier/seed layer. Chemical Mechanical Polish (CMP) can then be performed such that the upper surface of the Cu or Cu alloy layer is substantially coplanar with the upper surface of the active Si layer **222**.

[0028] FIGS. 3A-3C illustrate an example process of vertically stacking multiple wafers in an example three-dimensional (3-D) wafer-to-wafer vertical stack shown in FIG. 2. Each of the adjacent wafers **210** and **220** contains an active Si layer (**212** and **222**) for supporting one or more active IC devices (not shown), an oxide layer (**214** and **224**) and an identical set of metallic lines formed by the metal bonding layer **106** to dispose in the oxide layer (**214** and **224**) of the adjacent wafers **210** and **220** for serving not only as electrical connections to active IC devices on adjacent wafers **210** and **220** but also for bonding the adjacent wafers **210** and **220**. Metallic lines on the oxide layer **214** and **224** of the adjacent wafers **210** and **220** can be formed by etching the oxide layer **214** and **224** using an etch mask and then filling etched areas (trenches) on the oxide layer **214** and **224** with copper (Cu), Cu alloy or other selected metallic materials as described with reference to FIG. 2.

[0029] As shown in FIG. 3A, an alignment mark **310** may be used to facilitate the face to face alignment between the top wafer **220** and the bottom wafer **210** before the wafers **210** and **220** are ready for bonding. If the alignment mark **310** is needed, an oxide trench alignment mark can be processed on the top wafer **220**. When both wafers **210** and **220** are ready for bonding, the wafers **210** and **220** are aligned using a standard alignment tool and bonded using metal to metal bond, via a metal bonding layer **106**. After the wafers **210** and **220** are bonded, the top wafer **220** may be thinned by a Chemical Mechanical Polish (CMP), grinding, or Silicon (Si) wet etch process so as to minimize the wiring length between the vertically stacked wafers **210** and **220**. For example, the top wafer **220** is typically 700-760 .mu.m of silicon (Si). After the wafer-to-wafer bonding and silicon (Si) thinning processes are completed, one or more inter-

wafer vias (or via holes) **226** can be formed at designated locations to establish electrical connections between active IC devices on the vertically stacked wafers **210** and **220** and an external interconnect (not shown). The interwafer vias **226** can be patterned by conventional lithography and the active silicon (Si) on the top wafer **220** can be etched using an etch mask.

[0030] As shown in FIG. 3B, the active silicon (Si) layer **222** of the top wafer **220** is etched using an etch mask to pattern one or more vias **226**. Via etch can be performed by several techniques. For example, the silicon (Si) layer **222** of the top wafer **220** can be etched first stopping at the oxide layer **224**. A thin layer of oxide **320** can then be deposited in the Si vias **226**, as shown in FIG. 3C, so as to protect and insulate the sidewall of the Si vias **226**. Then oxide via (oxide layer **320** and ILD **224**) can be etched using an etch mask, stopping on a barrier/seed layer **330**. In other words, a silicon (Si) via etch is first performed stopping at the oxide layer **224** to form Si vias **226**. Oxide is then deposited in the Si vias **226** and an oxide via etch is performed, leaving behind a thin layer of oxide **320** deposited on a sidewall of the interwafer vias **226**.

[0031] In another example technique, the silicon (Si) layer **222** and the oxide layer **224** of the top wafer **220** can be etched in the same step. A thin layer of oxide **320** can then be deposited on the interwafer vias **226** so as to protect and insulate the sidewall of the interwafer vias **226**. Then anisotropic oxide etch can be performed to remove the thin layer of oxide **320** at the bottom of the interwafer vias **226**. In other words, the silicon (Si) via etch and the oxide via etch are performed at the same time. Oxide is then deposited in the interwafer vias **226** and anisotropic oxide via etch is performed to clear a thin layer of oxide at the bottom of the interwafer vias **226**.

[0032] After the oxide etch or the anisotropic oxide etch, a barrier/seed layer **330** can then be deposited inside the oxide via. Such a barrier/seed layer **330** contains a barrier layer deposited on the oxide layer **320** and a seed layer deposited on the barrier layer using, for example, a Chemical Vapor Deposition (CVD) process. The barrier layer can be a single or a stack of materials selected from the groups of tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W). The seed layer can be a few layers of copper (Cu) atoms deposited on the barrier layer by a Chemical Vapor Deposition (CVD) process.

[0033] After the barrier/seed layer **330**, copper (Cu) **340** can then be deposited in the interwafer vias **226**, via electroplating and Chemical Mechanical Polish (CMP), to establish electrical connections of active IC devices between vertically stacked wafers **210** and **220** to an external interconnect, via the C4 bump **228** shown in FIG. 2.

[0034] FIG. 4 illustrates an example 3-D wafer-to-wafer vertical stack **400** according to another embodiment of the present invention. As shown in FIG. 4, the bottom silicon (Si) wafer **410** may include an active silicon (Si) layer **412** supporting one or more active IC devices (not shown), and an interlayer dielectric (ILD) layer **414**. Likewise, the top Si wafer **420** may also include an active silicon (Si) layer **422** supporting one or more active IC devices (not shown), and an interlayer dielectric (ILD) layer **424**. In both wafers **410** and **420**, the ILD layer **414** and **424** are oxide deposited on the respective active silicon (Si) layer **412** and **422**. The

wafers **410** and **420** can then be aligned and bonded, via a metal bonding layer **106** deposited on opposing surfaces of the bottom wafer **410** and the top wafer **420** at designated bonding areas to establish electrical connections between active IC devices on vertically stacked wafers **410** and **420** and to bond adjacent wafers **410** and **420**, while maintaining electrical isolation between bonding areas via an ILD layer **414** and **424**. One or more interwafer vias **426** can be etched, via the top wafer **420**, to establish electrical connections between active IC devices on the vertically stacked wafers **410** and **420** and an external interconnect (not shown), via a C4 bump **448**.

[0035] However, in the example 2-wafer vertical stack **400** shown in FIG. 4, a conductive plug **430** filling a via hole (or hole like via) is formed during a standard W contact process to serve as an etch stop to stop the silicon (Si) via etch before the wafers **410** and **420** are bonded so as to establish electrical contact with an active region, via the copper (Cu) lines (the metal bonding layer **106**) of the vertically stacked wafers **410** and **420**. Such a conductive plug **430** filling a via hole (trench) is typically formed by forming an opening through the dielectric oxide by conventional photolithographic and etching techniques, and filling the opening with a conductive material such as tungsten "W". Copper (Cu) lines are then used for metal diffusion bonding and serve as electrical contacts between active IC devices on the vertically stacked wafers **410** and **420**. Tungsten "W" conductive plug **430** serves as an etch stop to stop the silicon (Si) via etch in order to avoid the requirement of a high selectivity etch process to stop at a thin barrier layer as described with reference to FIGS. 3A-3C.

[0036] FIGS. 5A-5C illustrate an example wafer bond and via etch in an example 3-D wafer-to-wafer vertical stack **400** as shown in FIG. 4. As shown in FIG. 5A, an alignment mark **510** may be used to facilitate the face to face alignment between the top wafer **420** and the bottom wafer **410** before the wafers **410** and **420** are ready for bonding. If the alignment mark **510** is needed, an oxide trench alignment mark can be processed on the top wafer **420**. When both wafers **410** and **420** are ready for bonding, the wafers **410** and **420** are aligned using a standard alignment tool and bonded using metal to metal bond, via a metal bonding layer **106**. After the wafers **410** and **420** are bonded, the top wafer **420** may be thinned by a Chemical Mechanical Polish (CMP), grinding, or Silicon (Si) wet etch process so as to minimize the wiring length between the vertically stacked wafers **410** and **420**. After the wafer-to-wafer bonding and silicon (Si) thinning processes are completed, one or more interwafer vias **426** can be formed at designated locations to establish electrical connections between active IC devices on the vertically stacked wafers **410** and **420** and an external interconnect (not shown). The interwafer vias **426** can be patterned by conventional lithography and the active silicon (Si) on the top wafer **420** can be etched using an etch mask.

[0037] As shown in FIG. 5B, the active silicon (Si) layer **422** of the top wafer **420** is etched using an etch mask to pattern one or more interwafer vias **426**. The silicon (Si) layer **422** of the top wafer **420** is etched stopping at the tungsten "W" conductive plug **430**. A thin layer of oxide **520** can then be deposited on the interwafer vias **426** so as to protect and insulate the sidewall of the interwafer vias **426**. Then anisotropic oxide etch can be performed to remove the thin layer of oxide **520** at the bottom of the interwafer vias

426. In other words, the silicon (Si) via etch is performed stopping at the tungsten "W" conductive plug **430**. Oxide is then deposited in the interwafer vias **426** and anisotropic oxide via etch is performed to clear a thin layer of oxide **520** at the bottom of the interwafer vias **426**. There is no need for oxide via etch since the tungsten "W" plug **430** serves as electrical connection.

[0038] After the anisotropic oxide etch, a barrier/seed layer **530** can then be deposited on the oxide layer **520** and the bottom of the interwafer vias **426**. After the barrier/seed layer **530**, copper (Cu) **540** can then be deposited in the interwafer vias **426**, via electroplating and Chemical Mechanical Polish (CMP), to establish electrical connections between active IC devices on the vertically stacked wafers **410** and **420** and an external interconnect (not shown), via the C4 bump **428** shown in FIG. 4.

[0039] In both the example 2-wafer vertical stack **200** shown in FIG. 2 and the example 2-wafer vertical stack **400** shown in FIG. 4, silicon (Si) via pattern/etch/oxide deposition steps used to protect silicon (Si) sidewall are required for electrical isolation between vias. However, these steps (Si via pattern/etch/oxide deposition) can be completed during Shallow Trench Isolation (STI) process steps in the wafer that is placed on the top (i.e., top wafer **220** shown in FIG. 2 or **420** shown in FIG. 4).

[0040] For example, FIG. 6 illustrates an example via etch during STI process steps in the example 2-wafer vertical stack **200** shown in FIG. 2. During STI process steps, Si vias **226** can be patterned, etched, and STI oxide can then be deposited in all vias **226**. When both wafers **210** and **220** are ready for bonding, the wafers **210** and **220** are aligned and bonded using metal to metal bond, via a metal bonding layer **106**. After the wafers **210** and **220** are bonded, the top wafer **220** may be thinned by a Chemical Mechanical Polish (CMP), grinding, or Silicon (Si) wet etch process so as to minimize the wiring length between the vertically stacked wafers **210** and **220**. After the wafer-to-wafer bonding and silicon (Si) thinning processes are completed, one or more STI oxide vias **226** can be patterned by conventional lithography and the active silicon (Si) on the top wafer **220** can be etched using an etch mask stopping at the barrier/seed or tungsten "W" contact plug. Copper (Cu) can then be deposited in the interwafer vias **226**, via electroplating and Chemical Mechanical Polish (CMP), to establish electrical connections between active IC devices on the vertically stacked wafers **210** and **220** and an external interconnect (not shown), via the C4 bump **228** shown in FIG. 2.

[0041] In the example 3-D wafer-to-wafer vertical stacks as described with reference to FIGS. 2-6, two (2) wafers are bonded face to face, and only the top wafer needs silicon (Si) vias to establish electrical connections of active IC devices between vertically stacked wafers to an external interconnect, via C4 bumps. However, when one or more additional wafers are bonded back to back on the second (top) wafer in the example 3-D wafer-to-wafer vertical stacks as described with reference to FIGS. 2-6, a large metal bonding area for wafer to wafer bonding process is required.

[0042] According to another aspect of the present invention, effective metal bonding areas on opposing surfaces of vertically stacked wafers can be made increased without consuming active silicon (Si) area by using one or more dummy Si vias, tapered Si vias, or incorporating an existing

copper (Cu) dual damascene process. FIGS. 7A-7B and FIGS. 8-9 illustrate an example 4-wafer vertical stack and various techniques of increasing metal bonding areas for multiple (>2) wafer to wafer bonding process according to an embodiment of the present invention.

[0043] For example, FIGS. 7A-7B illustrate an example 4-wafer vertical stack with increased metal bonding areas for multiple wafer-to-wafer bonding according to an embodiment of the present invention. As shown in FIG. 7A, the multiple vertical stack 700 contains wafer #1710 including an active layer 712 which supports one or more IC devices such as microprocessors, and an ILD (oxide) layer 714; wafer #2720 including an active layer 722 which supports one or more IC devices such as memory devices, and an ILD (oxide) layer 724; wafer #3730 including an active layer 732 which supports one or more IC devices such as programmable devices, and an ILD (oxide) layer 734; and wafer #4740 including an active layer 742 which supports one or more IC devices such as radio-frequency (RF) or optical communication devices, and an ILD (oxide) layer 744. The bottom wafer 710 may be sufficiently thick to support the stacking of the top wafers 720, 730 and 740, while the top wafers 720, 730 and 740 may be thinned to minimize interconnection lengths between vertically stacked wafers 710, 720, 730 and 740.

[0044] After the first two wafers are bonded in the same manner as described with reference to FIG. 2, that is, after wafer #1710 and wafer #2720, and wafer #3730 and wafer #4740 are bonded separately, via the metal bonding layer 106, the opposing surfaces of wafer #2720 and wafer #3730 can be separately thinned by a Chemical Mechanical Polish (CMP), grinding, or Silicon (Si) wet etch process so as to minimize the wiring length between the vertically stacked wafers 710 and 720 and the vertically stacked wafers 730 and 740. After the wafer-to-wafer bonding and silicon (Si) thinning processes are completed, interwafer vias 750 can be formed at designated locations to establish electrical connections of active IC devices between the vertically stacked wafers 710 and 720 and the vertically stacked wafers 730 and 740. Interwafer vias 750 can be patterned with a dual damascene process. A dual damascene process involves the formation of an opening comprising a lower contact or via hole section in communication with an upper trench section, which opening is filled with a conductive material, typically a metal, to simultaneously form a conductive plug in electrical contact with a conductive line (metal bonding layer 106).

[0045] FIG. 7B illustrates a cross section of an example via 750 formed on wafer #720, for example, employing copper (Cu) dual damascene technology according to an embodiment of the present invention. As shown in FIG. 7B, the active Si layer 722 of wafer #2720 is etched to form an upper trench section of vias. A thin layer of oxide 752 can then be deposited on the Si vias 750 so as to protect and insulate the sidewall of the Si vias 750. The oxide layer 752 as deposited on the Si vias 750 is again etched to form a lower trench section (or via contact section) of vias in the ILD layer 724 for planned dual damascene interconnects with the lower level metalization, e.g., metallic line (metal bonding layer 106). A barrier/seed layer 754 is then deposited overlying the active layer 722 and the ILD 724 in the vias and trenches. Copper (Cu) 756 is then deposited by electroplating or any other Cu deposition techniques such as

metal-organic chemical vapor deposition (CVD) or plasma-enhanced metal-organic CVD.

[0046] The barrier/seed layer 754 can comprise a barrier layer deposited overlying the active layer 722 and the ILD 724 and a copper (Cu) seed layer deposited overlying the barrier layer. The barrier layer is typically comprised of a material that can eliminate out-diffusion of copper (Cu) ions from the dual damascene interconnect into the ILD layer 724, and serve as a catalyst for the copper (Cu) deposition reaction. The barrier layer preferably comprises one of the group containing: tantalum, titanium, and tungsten. The copper (Cu) seed layer deposited on the barrier layer can be made very thin while still exhibiting excellent step coverage or conformity. The copper (Cu) dual damascene process advantageously increases (Cu) metal bonding areas for multiple wafer to-wafer bonding in an example 3-D wafer-to-wafer vertical stack 700 shown in FIG. 7A.

[0047] FIG. 8 illustrates example 4-wafer vertical stack with increased metal bonding areas for multiple wafer-to-wafer bonding according to another embodiment of the present invention. As shown in FIG. 8, the multiple vertical stack 800 contains the same number of wafers as described with reference to FIGS. 7A-7B, comprising, for example, wafer #1810 including an active layer 812 which supports one or more IC devices, and an ILD (oxide) layer 814; wafer #2820 including an active layer 822 which supports one or more IC devices, and an ILD (oxide) layer 824; wafer #3830 including an active layer 832 which supports one or more IC devices, and an ILD (oxide) layer 834; and wafer #4840 including an active layer 842 which supports one or more IC devices, and an ILD (oxide) layer 844.

[0048] After the first two wafers are bonded in the same manner as described with reference to FIG. 2, that is, after wafer #1810 and wafer #2820, and wafer #3830 and wafer #4840 are bonded separately, via the metal bonding layer 106, the opposing surfaces of wafer #2820 and wafer #3830 can be separately thinned by a Chemical Mechanical Polish (CMP), grinding, or Silicon (Si) wet etch process so as to minimize the wiring length between the vertically stacked wafers 810 and 820 and the vertically stacked wafers 830 and 840. After the wafer-to-wafer bonding and silicon (Si) thinning processes are completed, interwafer (interconnect) vias 850 can be formed at designated locations to establish electrical connections of active IC devices between the vertically stacked wafers 810 and 820 and the vertically stacked wafers 830 and 840. Interwafer vias 850 and additional dummy vias 860 can be patterned with the same damascene process as described with reference to FIG. 2. However, dummy via size can be made smaller in diameter than interwafer vias 850.

[0049] For example, the active Si layer 824 of wafer #2820 can be etched to form Si vias 850 and dummy vias 860. An oxide layer (not shown) can then be deposited only on the Si vias 850 so as to protect and insulate the sidewall of the Si vias 850. The oxide layer (not shown) deposited on the Si vias 850 can again be patterned and etched to form a lower contact or via hole (trench) section in the ILD layer 824 with the lower level metalization, e.g., metallic line (metal bonding layer 106). A barrier/seed layer (not shown) can then be deposited overlying the active layer 822 and the ILD 824 in the vias and trenches. Copper (Cu) is then deposited by electroplating or any other Cu deposition

techniques such as metal-organic chemical vapor deposition (CVD) or plasma-enhanced metal-organic CVD. As a result, dummy vias **860** can serve as additional metal bonding pads to increase the surface of (Cu) metal bonding areas for multiple (>2) wafer to-wafer bonding in an example 3-D wafer-to-wafer vertical stack **800**, as shown in FIG. **8**, while providing auxiliary structures such as ground planes or heat conduits for the active IC devices in the vertically stacked wafers **810**, **820**, **830** and **840**.

[**0050**] FIG. **9** illustrates an example 4-wafer vertical stack with increased metal bonding areas for multiple wafer-to-wafer bonding according to yet another embodiment of the present invention. As shown in FIG. **9**, the multiple vertical stack **900** contains the same number of wafers as described with reference to FIGS. **7A-7B** and FIG. **8**, comprising, for example, wafer #**1910** including an active layer **912** and an ILD (oxide) layer **914**; wafer #**2920** including an active layer **922** and an ILD (oxide) layer **924**; wafer #**3930** including an active layer **932** and an ILD (oxide) layer **934**; and wafer #**4940** including an active layer **942** and an ILD (oxide) layer **944**.

[**0051**] After the first two wafers are bonded in the same manner as described with reference to FIG. **2**, that is, after wafer #**1910** and wafer #**2920**, and wafer #**3930** and wafer #**4940** are bonded separately, via the metal bonding layer **106**, the opposing surfaces of wafer #**2920** and wafer #**3930** can be separately thinned by a Chemical Mechanical Polish (CMP), grinding, or Silicon (Si) wet etch process so as to minimize the wiring length between the vertically stacked wafers **910** and **920** and the vertically stacked wafers **930** and **940**. After the wafer-to-wafer bonding and silicon (Si) thinning processes are completed, interwafer vias **950** can be formed at designated locations to establish electrical connections of active IC devices between the vertically stacked wafers **910** and **920** and the vertically stacked wafers **930** and **940**. Interwafer vias **950** can be patterned with the same damascene process as described with reference to FIG. **2**. However, the etching process of Si vias **950** can be controlled such that the Si vias **950** can be tapered from the top to the bottom via hole. As a result, tapered vias **950** can have a larger surface area so as to increase the (Cu) metal bonding areas for multiple wafer to-wafer bonding in an example 3-D wafer-to-wafer vertical stack **900**.

[**0052**] The example Si via process can be described as follows: The active Si layer **924** of wafer #**2920** can first be patterned and etched at a predetermined angle to form tapered vias **950**. An oxide layer (not shown) can then be deposited only on the tapered vias **950** so as to protect and insulate the sidewall of the tapered vias **950**. The oxide layer (not shown) deposited on the tapered vias **950** can again be patterned and etched to form a lower contact or via hole section in the ILD layer **924** with the lower level metalization, e.g., metallic line (metal bonding layer **106**). A barrier/seed layer (not shown) can then be deposited overlying the active layer **922** and the ILD **924** in the tapered vias **950**. Copper (Cu) is then deposited by electroplating or any other Cu deposition techniques such as metal-organic chemical vapor deposition (CVD) or plasma-enhanced metal-organic CVD.

[**0053**] As described in this invention, there are several processes of vertically stacking multiple wafers supporting different active IC devices with low cost and high via

density. Metal bonding areas on wafers can be increased by using either a copper (Cu) dual damascene process, dummy vias, or tapered vias to effectively bond vertically stacked wafers and establish electrical connections between active IC devices on the vertically stacked wafers and an external interconnect (not shown), via C4 bumps.

[**0054**] While there have been illustrated and described what are considered to be exemplary embodiments of the present invention, it will be understood by those skilled in the art and as technology develops that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the present invention. Many modifications may be made to adapt the teachings of the present invention to a particular situation without departing from the scope thereof. Therefore, it is intended that the present invention not be limited to the various exemplary embodiments disclosed, but that the present invention includes all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A method of metal bonding vertically stacked wafer pairs comprising:

forming a first wafer pair, including bonding a metallic line disposed on an ILD on a front side of a first wafer to a corresponding metallic line disposed on an ILD on a front side of a second wafer;

forming a second wafer pair, including bonding a metallic line disposed on an ILD on a front side of a third wafer to a corresponding metallic line disposed on an ILD on a front side of a fourth wafer;

providing a first metal bonding area at a back side of the second wafer and a second metal bonding area at a back side of the third wafer, said providing including forming an Si via through an active layer at a back side of the second wafer, wherein a first end of the Si via connects to the metallic line of the second wafer and a second end of the Si via is exposed at the back side of the second wafer;

increasing the first and second metal bonding areas; and

bonding the increased first metal bonding area to the increased second metal bonding area.

2. The method of claim 1, wherein increasing the metal bonding areas comprises:

increasing a horizontal cross-sectional area of the second end of the Si via.

3. The method of claim 2, wherein increasing the horizontal cross-sectional area comprises:

forming an upper trench section in the back side of the second wafer, the upper trench section filled with a conductive material and connected to the Si via.

4. The method of claim 2, wherein increasing the horizontal cross-sectional area comprises:

etching the first Si via to form a tapered via.

5. The method of claim 1, wherein increasing the metal bonding areas comprises:

forming a dummy Si via in the active layer of the second wafer and a corresponding dummy Si via in the active layer of the third wafer.

6. The method of claim 5, wherein forming each dummy Si via comprises forming each dummy Si via to have a diameter smaller than a diameter of the first Si via.

7. The method of claim 1, further comprising:

thinning the back side of the second wafer.

8. The method of claim 1, further comprising:

forming a microprocessor in the first wafer;

forming a memory device in the second wafer; and

forming a communication device in the third or fourth wafer.

9. A method of metal bonding multiple vertically stacked wafers comprising:

depositing a first metallic line on an ILD of a front side of a first wafer;

depositing a second metallic line on an ILD of a front side of a second wafer;

bonding the first metallic line to the second metallic line;

depositing a third metallic line on an ILD of a front side of a third wafer;

depositing a fourth metallic line on an ILD of a front side of a fourth wafer;

bonding the third metallic line to the fourth metallic line;

forming a first Si via through an active layer at a back side of the second wafer, the first Si via having an internal end connected to the second metallic line and an external end exposed at the back side of the second wafer;

forming a second Si via through an active layer at a back side of the third wafer, the second Si via having an internal end connected to the third metallic line and an external end exposed at the back side of the third wafer;

increasing areas of the external ends of the first and second Si vias; and

bonding the areas.

10. The method of claim 9, wherein increasing the areas comprises:

forming a trench section in the back side of the second wafer, the trench section filled with a conductive material and connected to the first Si via; and

forming a corresponding trench section in the back side of the third wafer, the corresponding trench section filled with the conductive material and connected to the second Si via.

11. The method of claim 9, wherein increasing the areas comprises:

etching the active layer at the back side of the second wafer at an angle, such that the first Si via is tapered and has a larger cross-sectional area at the external end than at the corresponding internal end.

12. The method of claim 11, further comprising:

forming a third Si via through an active layer at a back side of the fourth wafer, the third Si via connecting to the fourth metallic line of the fourth wafer.

13. The method of claim 12, wherein forming the third Si via comprises:

etching the active layer at the back side of the fourth wafer to form a hole;

depositing oxide on surfaces of the hole;

removing oxide at a bottom surface of the hole using an anisotropic oxide etch;

depositing a barrier layer on oxide on sidewalls of the hole;

depositing a seed layer on the barrier layer; and

filling the hole with a conductive material.

14. The method of claim 13, wherein the barrier layer is composed of a material selected from the group consisting of: tantalum (Ta), tantalum nitride (Ta₂N₅), titanium (Ti), and tungsten (W).

15. The method of claim 13, wherein the seed layer comprises a layer of copper atoms deposited by CVD.

16. The method of claim 12, further comprising:

forming a C4 bump on the fourth wafer, the C4 bump physically connecting to the third Si via and electrically connecting to an active layer at a back side of the first wafer.

17. A method of metal bonding back sides of two wafers comprising:

forming a first Si via through an active layer at a back side of a first wafer, wherein a first end of the first Si via is exposed;

forming a second Si via through an active layer at a back side of a second wafer, wherein a second end of the second Si via is exposed;

increasing areas of the first end and second end; and

bonding the increased areas.

18. The method of claim 12, wherein forming the first Si via comprises:

etching a part of the active layer at the back side of the first wafer, said etching stopping a tungsten etch stop disposed at an interface between the active layer at the back side of the first wafer and an ILD layer at a front side of the first wafer.

19. The method of claim 17, wherein increasing the areas comprises:

forming a first trench section in the back side of the first wafer, the first trench section filled with a conductive material and connected to the first Si via; and

forming a second trench section in the back side of the second wafer, the second trench section filled with the conductive material and connected to the second Si via.

20. The method of claim 17, further comprising:

forming a first dummy via in the active layer of the first wafer;

forming a second dummy via in the active layer of the second wafer; and

bonding the first and second dummy vias.