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(54) **INCORPORATING HIGH-PURITY COPPER DEPOSIT AS SMOOTHING STEP AFTER DIRECT ON-BARRIER PLATING TO IMPROVE QUALITY OF DEPOSITED NUCLEATION METAL IN MICROSCALE FEATURES**

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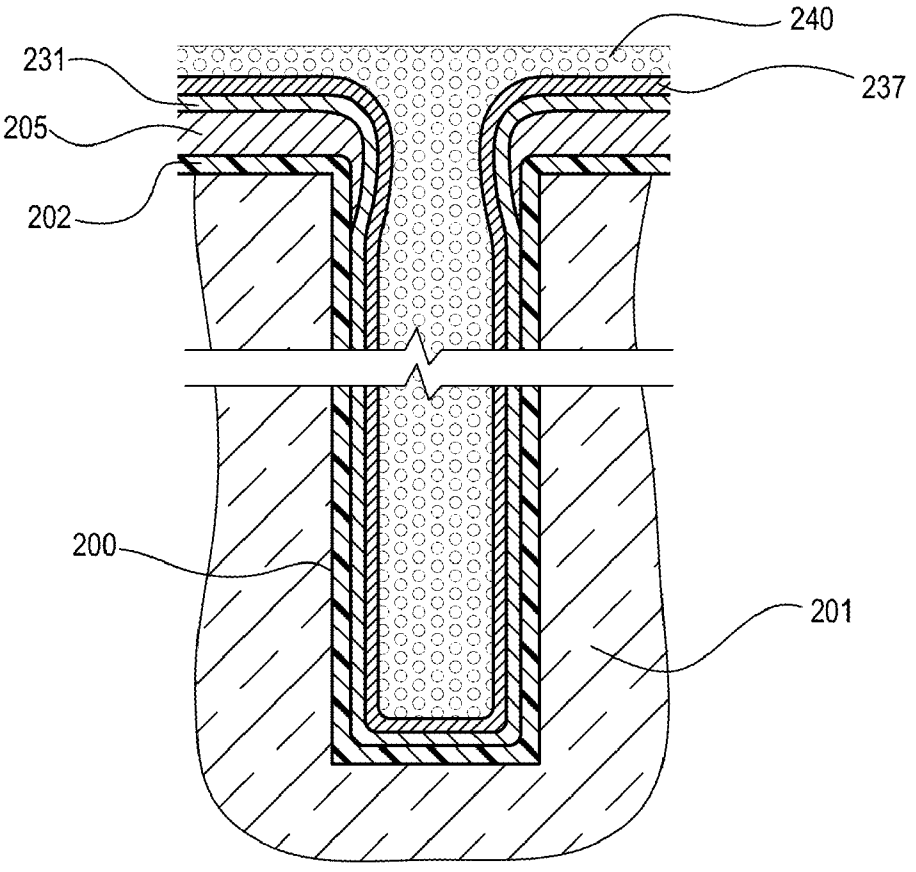
USPC ..... **205/123**; 204/269

(57) **ABSTRACT**

Techniques disclosed herein a method and system for coating the interior surfaces of microscale hole features fabricated into the substantially planar surface of a substrate. Techniques include creating a separation or smoothing layer between a nucleation layer process and a metallization or gapfill process. The addition of such a separation layer avoids dissolving a seed layer and gapfill complications from remnant organic material. Techniques include adding a conformal copper smoothing layer step after applying a direct on-barrier nucleation layer. The smoothing layer adds a sufficient thickness so that the gapfill chemistry does not erode the nucleation layer. The smoothing layer can also provide a high-purity copper film that will not detrimentally interact with the TSV gapfill chemistry. This smoothing layer can also provide a surface with consistent roughness to allow uniform adhesion of the organic additives in the TSV gapfill chemistry to create a filling profile that is void-free.



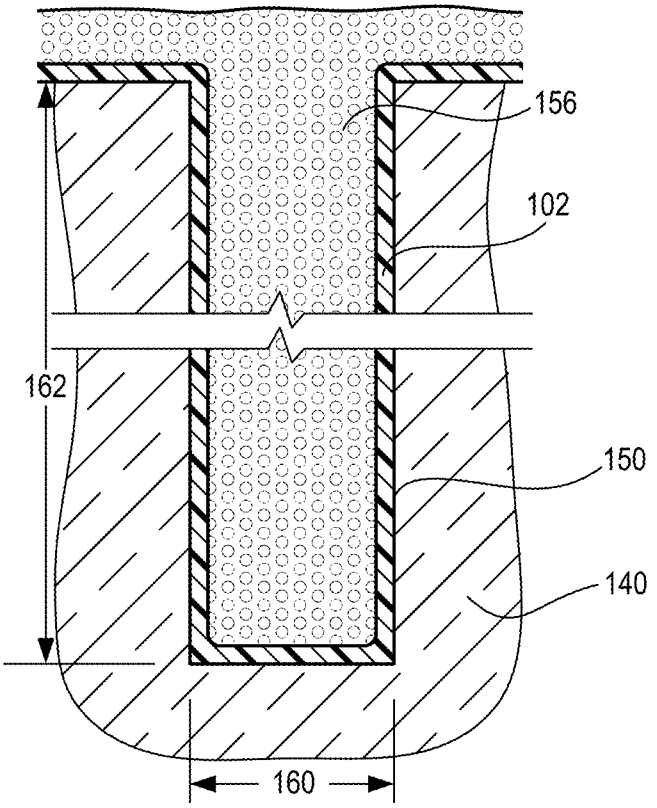



FIG. 1

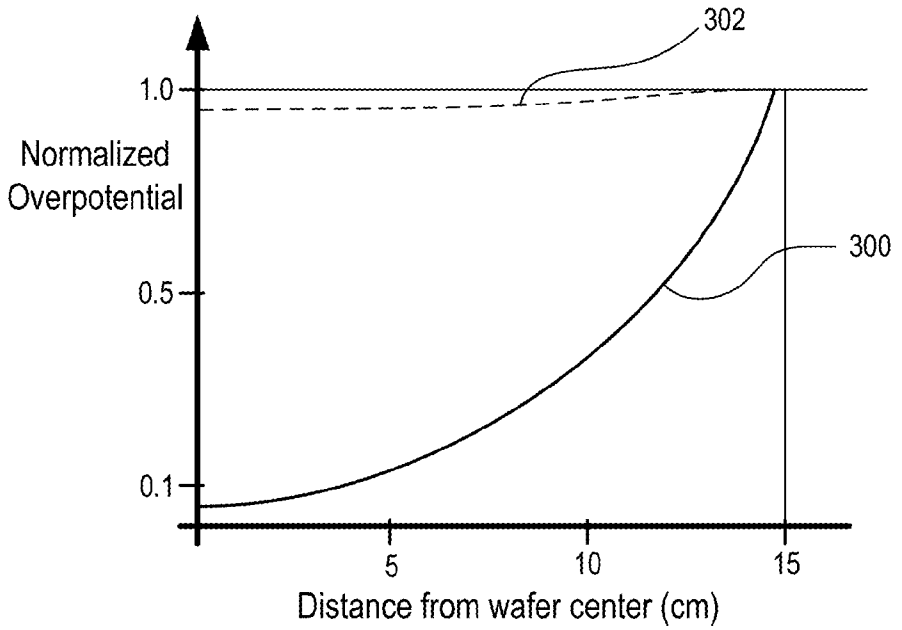

302
1.0
Normalized
Overpotential
300
0.5
0.1
5
10
15
Distance from wafer center (cm)

FIG. 2

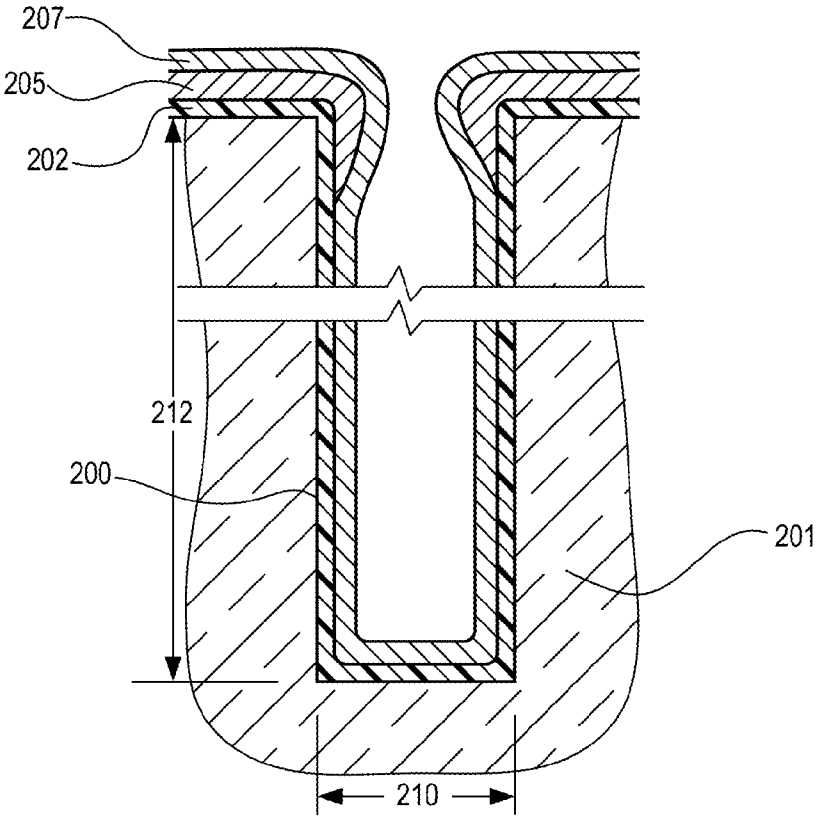

207
205
202
212
200
201
210

FIG. 3

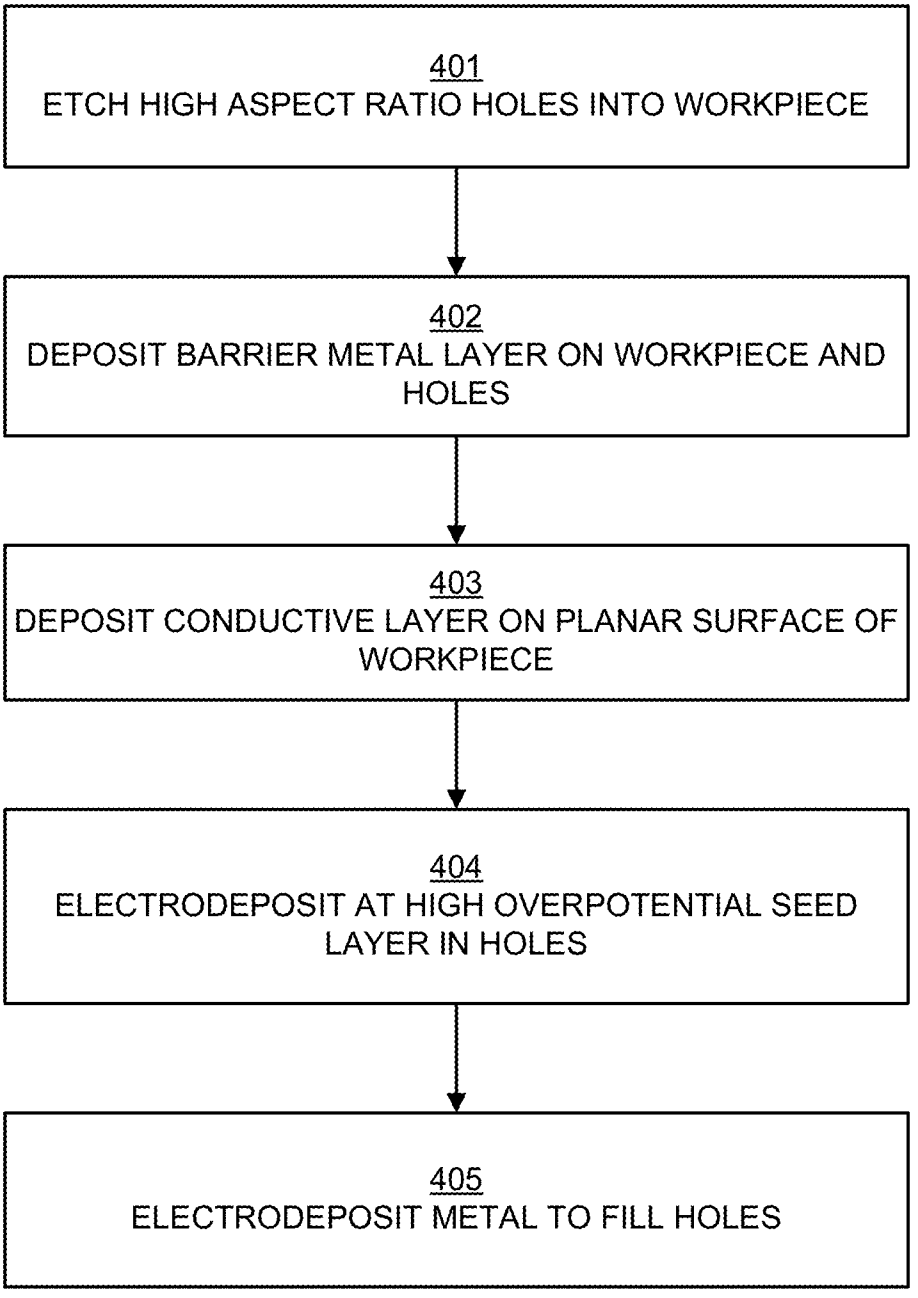

401
ETCH HIGH ASPECT RATIO HOLES INTO WORKPIECE
402
DEPOSIT BARRIER METAL LAYER ON WORKPIECE AND HOLES
403
DEPOSIT CONDUCTIVE LAYER ON PLANAR SURFACE OF WORKPIECE
404
ELECTRODEPOSIT AT HIGH OVERPOTENTIAL SEED LAYER IN HOLES
405
ELECTRODEPOSIT METAL TO FILL HOLES

FIG. 4

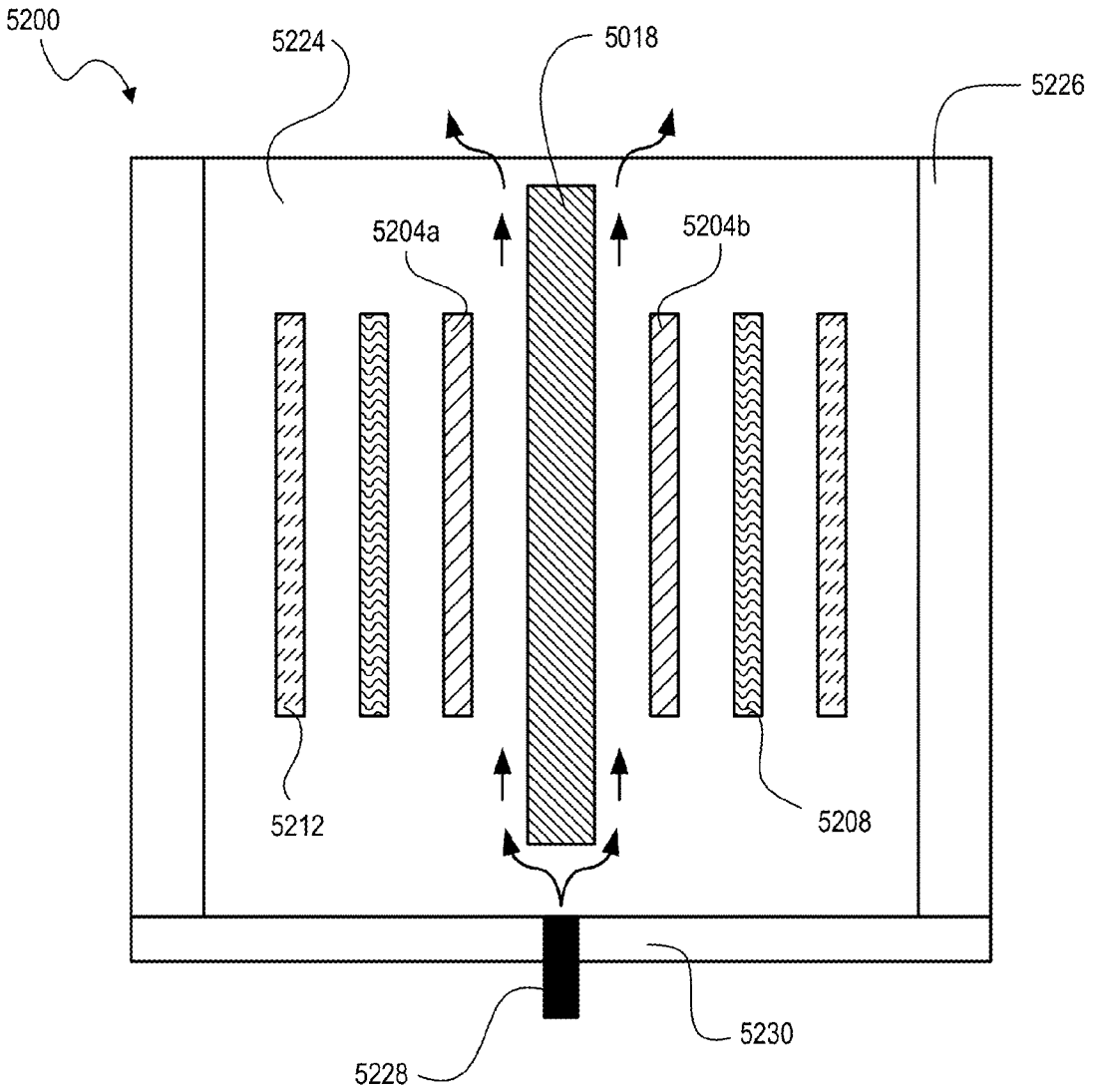



FIG. 5

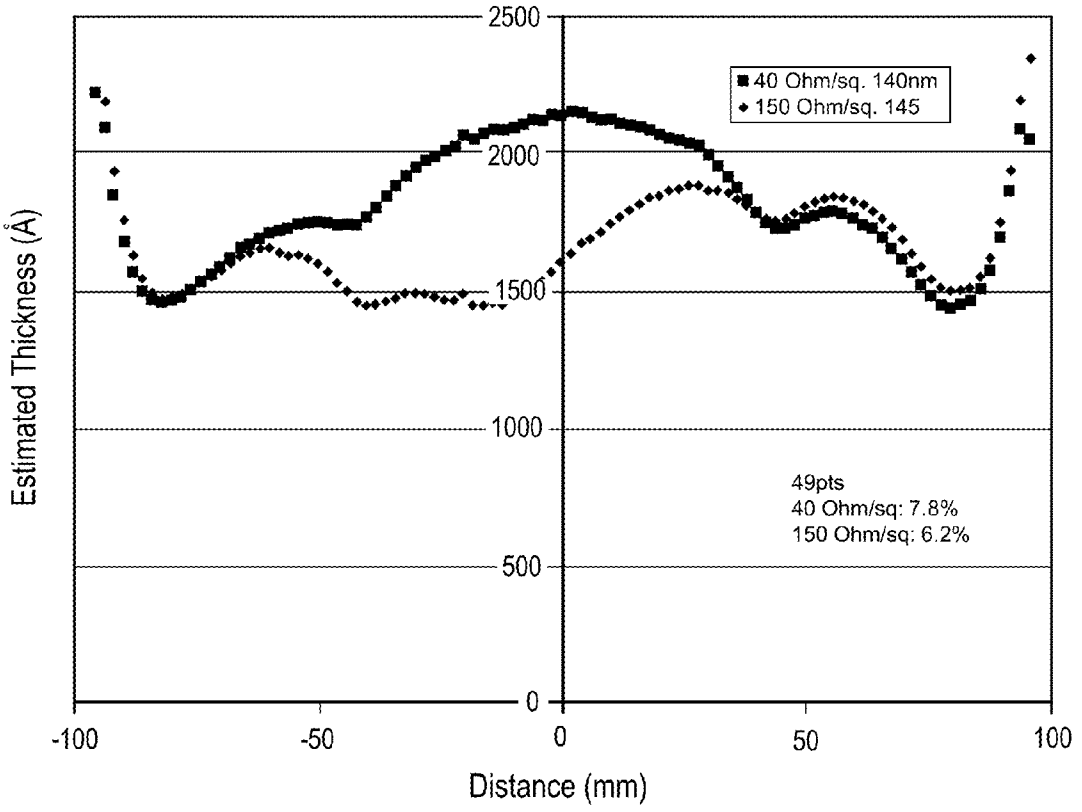

2500
2000
1500
1000
500
0
-100
-50
0
50
100
Estimated Thickness (Å)
Distance (mm)
40 Ohm/sq. 140nm
150 Ohm/sq. 145
49pts
40 Ohm/sq: 7.8%
150 Ohm/sq: 6.2%

FIG. 6

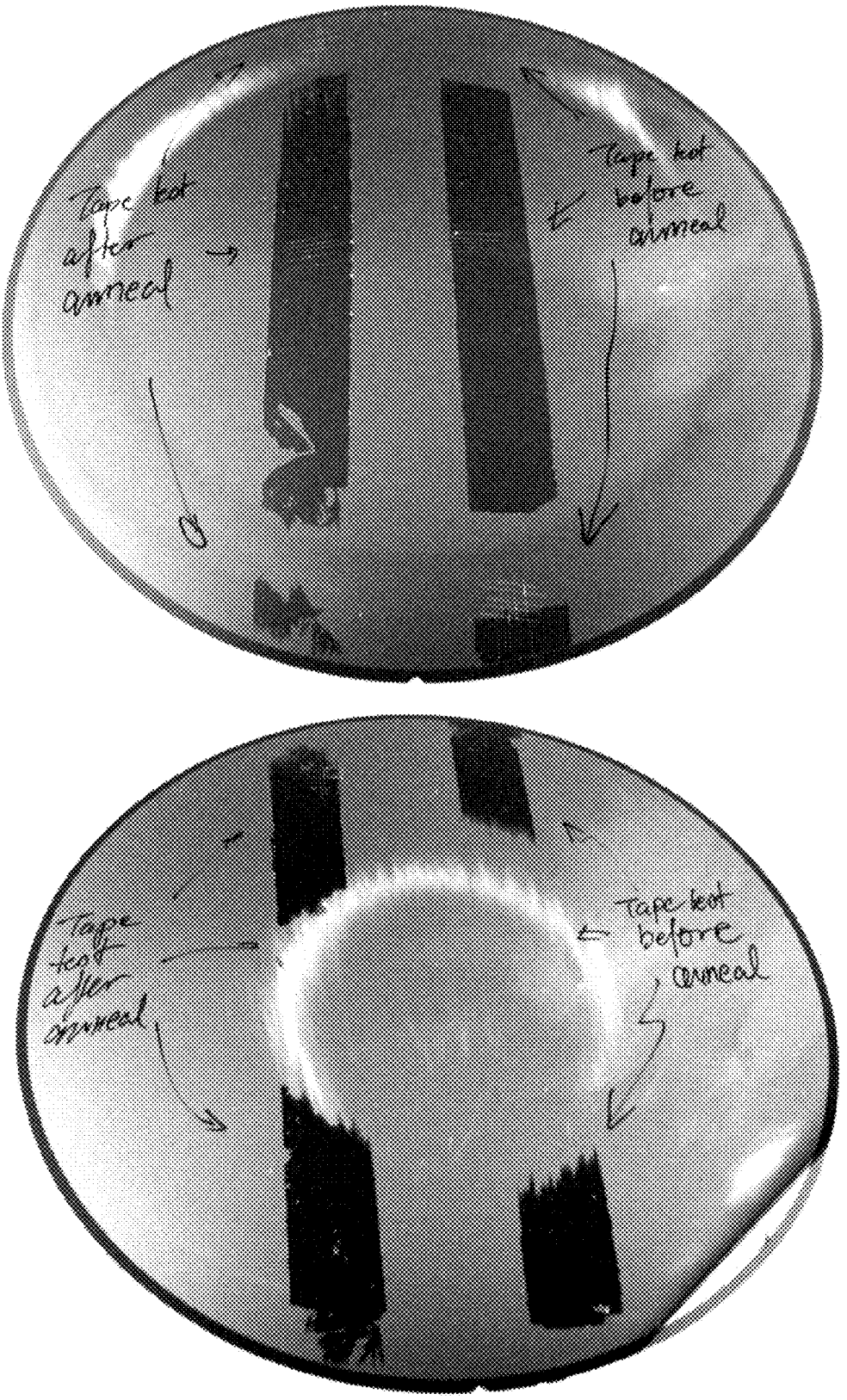

Tape hot after anneal
Tape hot before anneal
Tape hot after anneal
Tape hot before anneal

FIG. 7

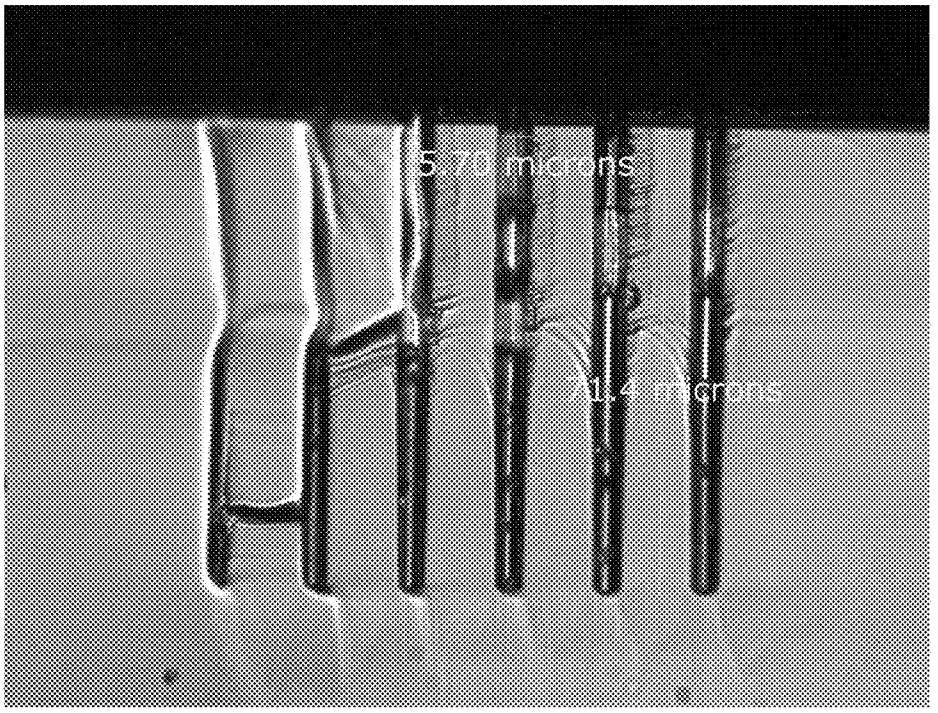



FIG. 8A

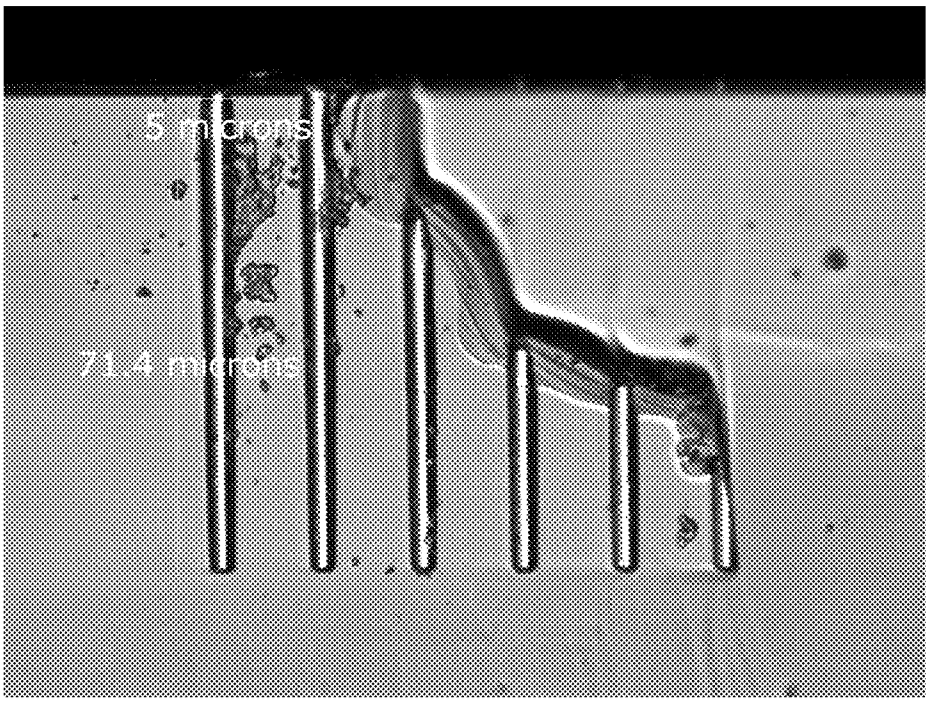



FIG. 8B

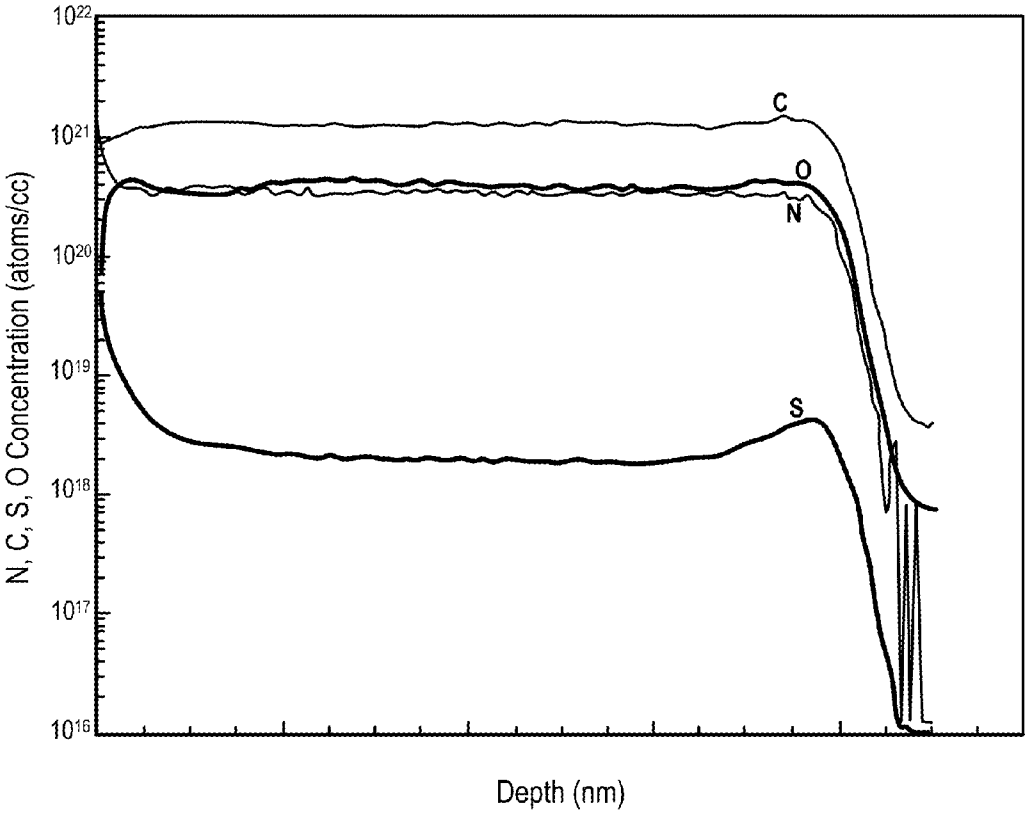

$10^{22}$
$10^{21}$
$10^{20}$
$10^{19}$
$10^{18}$
$10^{17}$
$10^{16}$
N, C, S, O Concentration (atoms/cc)
C
O
N
S
Depth (nm)

*FIG. 9*

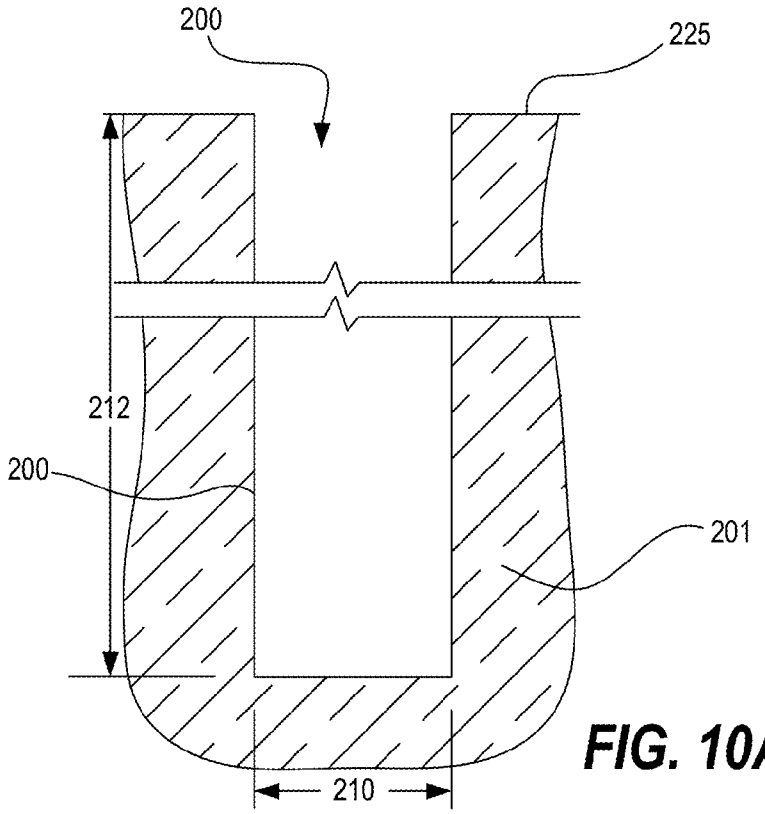



FIG. 10A

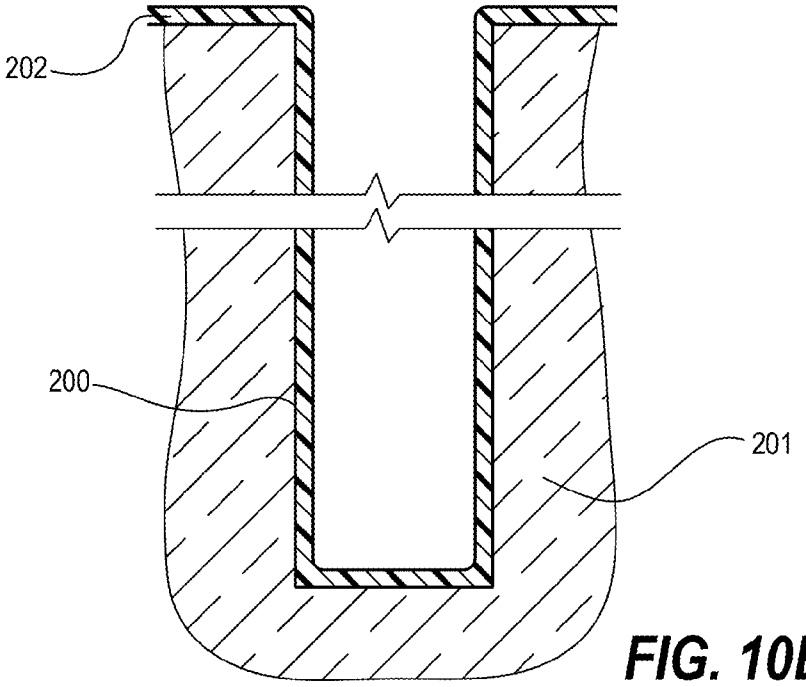



FIG. 10B

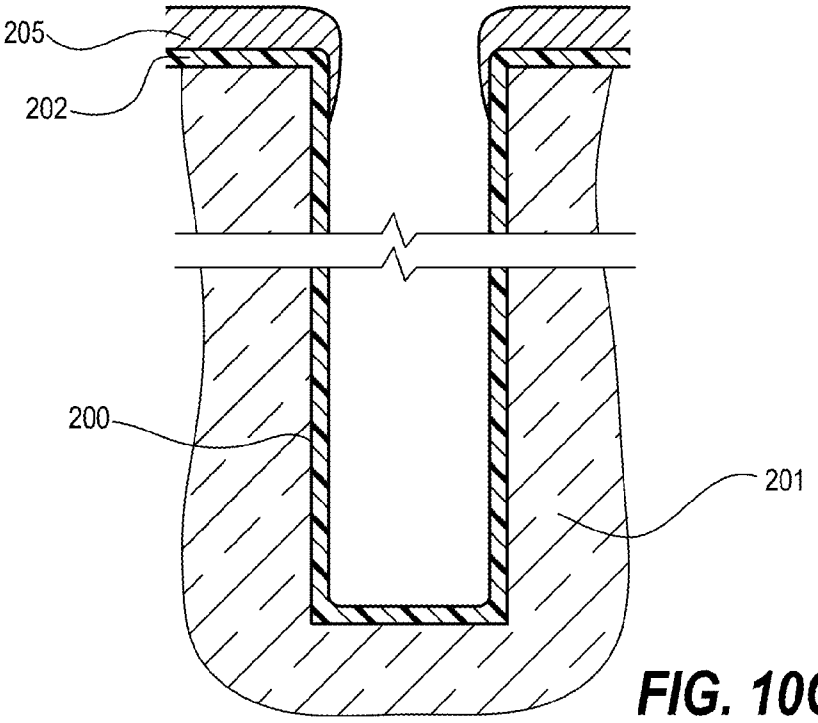



FIG. 10C

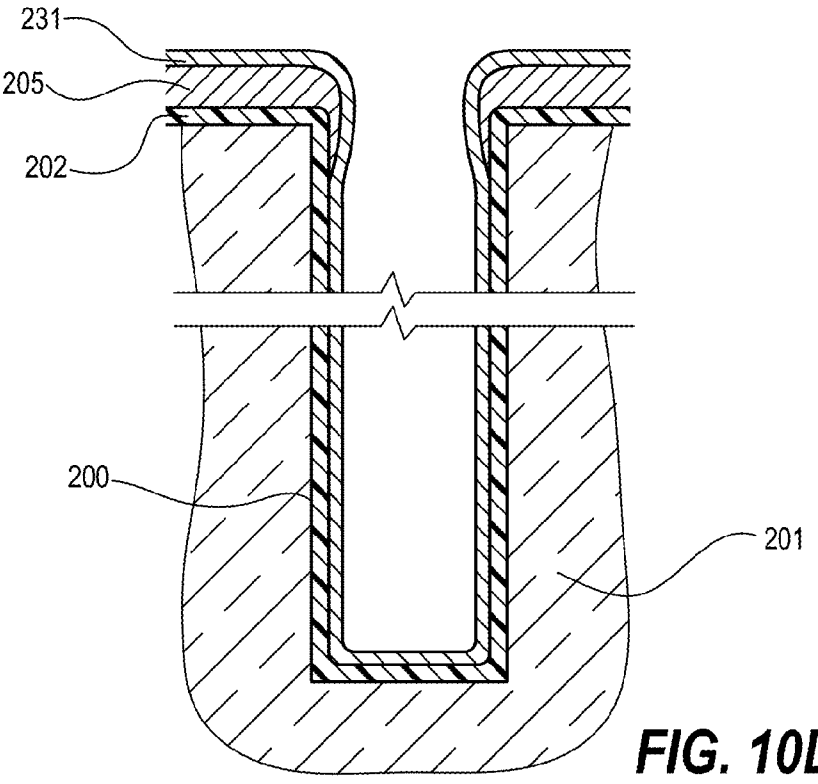



FIG. 10D

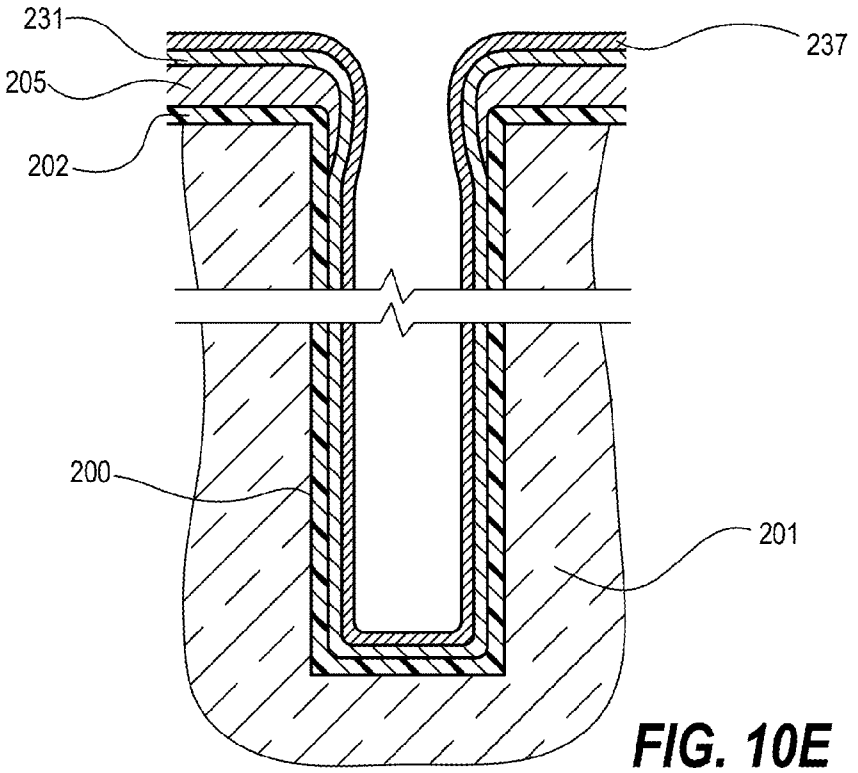



FIG. 10E

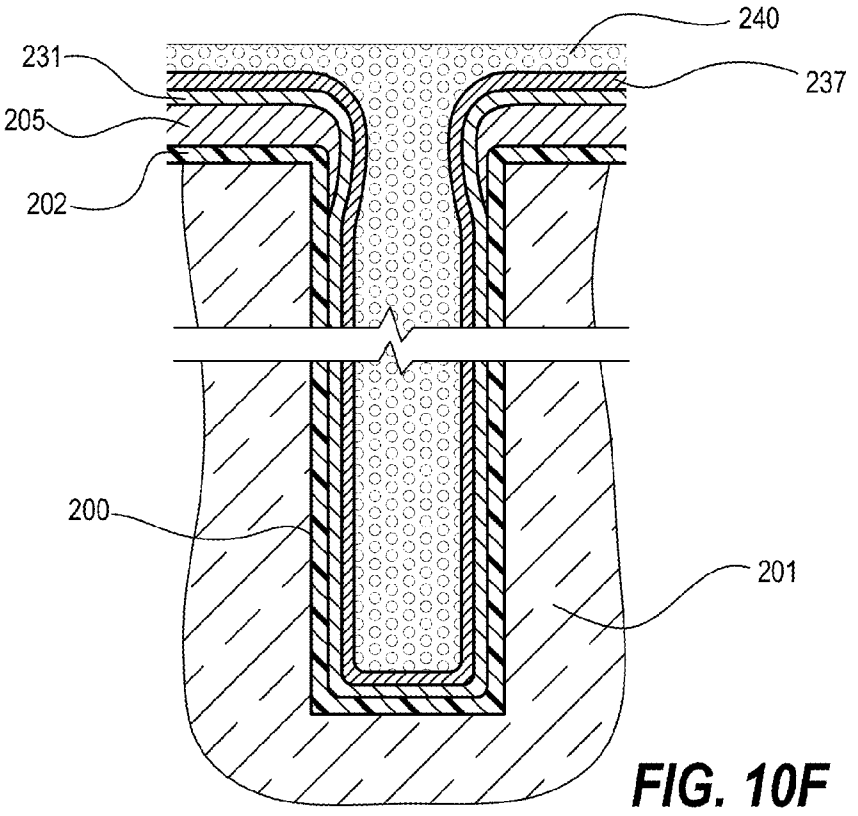



FIG. 10F

# INCORPORATING HIGH-PURITY COPPER DEPOSIT AS SMOOTHING STEP AFTER DIRECT ON-BARRIER PLATING TO IMPROVE QUALITY OF DEPOSITED NUCLEATION METAL IN MICROSCALE FEATURES

## CROSS REFERENCE TO RELATED APPLICATIONS

**[0001]** This application is a continuation-in-part of U.S. application Ser. No. 12/755,198, filed on Apr. 6, 2010, titled "Seed Layer Deposition in Microscale Features." The entire content of which is herein incorporated by reference.

## BACKGROUND OF THE INVENTION

**[0002]** Techniques disclosed herein relate to semiconductor fabrication, and more particularly to depositing metal into microscale recesses in the surface of a workpiece or substrate. This includes surfaces coated with high resistivity metal film coated within trenches, holes, and through-silicon-vias (TSV).

**[0003]** Through silicon via (TSV) structures have recently been developed as a method to produce three dimensional (3D) electronic integrated devices. These TSV structures entail forming a metal plug inside a small hole in the silicon or other substrate material, wherein the typical hole size may be from about 1 to 30 microns in diameter and from 10 to 250 microns in depth. FIG. **1** illustrates an example desired result from a metal filling process. To fabricate a TSV structure, holes, such as hole **150**, are first etched into the silicon or substrate material **140**. The hole(s) are coated with an insulating material, silicon dioxide for example, which is then covered with a barrier material **102**, such as titanium, tantalum, or their nitrides, titanium nitride or tantalum nitride, for example, and the hole is then filled with a conductive material **156**, copper for example. A conventional means of filling the TSV with copper is to employ electroplating using one of various means to cause the electroplating to deposit copper preferentially near the bottom of the hole and cause the copper to deposit more inside the via then on the flat surface, or field, of the silicon substrate. This is known as a bottom-up copper damascene filling electroplating process method.

## SUMMARY

**[0004]** To enable this bottom-up copper filling method, it is necessary to form a plating seed layer on which to grow the electroplated film. Lack of a seed layer results in a fill with insufficient adhesion. Typically the seed layer is of the same material as the electroplated filling step material, typically both are copper, and the copper plating seed layer is conventionally formed by physical vapor deposition (PVD). A difficulty in conventional methods using PVD metal layers in the case of high aspect ratio TSV structures (compared to damascene structures) is that very little if any of the physical vapor deposited metal coats the interior surfaces of the TSV hole, and therefore an incomplete and inadequate barrier and seed metal layers form in those regions. This disadvantage of PVD increases as the depth to diameter (i.e., aspect) ratio of the TSV increases because of the ballistic transport nature of PVD.

**[0005]** To achieve the commercial and reliability benefits of three dimensional IC fabrication, it is advantageous to fabricate the TSV holes with a high ratio of depth (**162**) to diameter (**160**), aspect ratios of 10 or more are advantageous. Alternate means of conventionally depositing the metal layers into the high aspect ratio TSV feature are atomic layer deposition (ALD) or chemical vapor deposition (CVD). ALD deposits metal films one atomic layer after another through a series of surface limited reactions, which are virtually independent of the microscale geometry of a surface and hence provides a technically ideal means of coating TSV interior features with metal layers. The ALD process, however, is slow and therefore commercially too uneconomical for many production TSV applications.

**[0006]** CVD is a well-known and commercially economical means of depositing TiN, TaN, or W barrier metals into high aspect ratio holes. CVD, however, has been found to be uneconomical for copper, or other seed layer metals, due to the instability and expense of the metal-organic precursor materials. Conventional wet processes, such as electrochemical deposition (ECD) and electroless metal deposition have also shown to be deficient in commercial fabrication of microscale structures. In the case of electroless metal deposition, a chemical potential may be caused by reaction of the fluid borne reactants and catalytic species on the TSV interior surface. Electroless metal deposition requires a series of chemical pre-treatments in order to set-up the reaction potential between the barrier metal and the seed metal reactants, and the chemical constituents of the pretreatment and deposition chemical baths must be tightly controlled, all of which can make the electroless metal process expensive and difficult to operate.

**[0007]** The alternative conventional wet process method, conventional ECD, suffers from other deficiencies that render it also not production worthy. For example, a significant difficulty of using conventional means for ECD to deposit seed metal on the interior surfaces of TSV features of a substrate coated with highly resistive barrier metal, for example a TiN with resistivity of 10 to 100 ohms/square, is the large radial electrical potential drop that occurs within the barrier metal as current flows from the substrate perimeter to the substrate center, this large potential drop causes an undesirable difference in the available driving electrical potential between edge and center regions of the substrate. Electrical contact to the substrate is formed at the substrate edge and the circuit is completed through the barrier metal and into the electrochemical bath. Consequently a highly resistive metal layer causes a significant voltage drop from edge to center of substrate.

**[0008]** A family of chemistry exists for the purpose of plating Copper (Cu) seed on a liner or barrier for a high aspect ratio, such as those encountered in Through Silicon Vias (TSV) and damascene trench-via structures. These direct on-barrier chemistries rely on complexing agents to increase the plating potential in order to achieve better nucleation and adhesion. These complexers (complexing agents) usually consist of organic components that could plate into the deposited metal film under certain conditions. One approach in terms of integration is to plate as thin of a layer as possible, and then continue the plating in the, for example, TSV gapfill chemistry. Two problems, however, can arise. One problem is that the acid in the gapfill chemistry attacks the thin seed and dissolves it before plating can commence. A second problem occurs when remnant organics from the direct on-barrier chemistry interact with organic additives in the, for example, TSV gapfill chemistry in a detrimental way, either prolonging the filling process, or completely disrupting it.

**[0009]** Techniques disclosed herein provide a separation layer between the seed layer process and the metallization or gapfill process. The addition of such a separation layer avoids the plating problems described above. Techniques include adding a conformal copper smoothing layer step after applying a direct on-barrier nucleation layer. The smoothing layer adds a sufficient thickness such that the TSV gapfill chemistry does not erode the nucleation layer. The smoothing layer can provide a high-purity copper film that will not detrimentally interact with the TSV gapfill chemistry. This smoothing layer can also provide a surface with consistent roughness to allow uniform adhesion of the organic additives in the TSV gapfill chemistry to create a filling profile that is void-free. In contrast, conventional attempts try to deposit a seed layer in one step, but contain additional organic additives that add impurities to the plated copper.

**[0010]** Techniques can include using one chemistry for applying the on-barrier nucleation layer, while using a different chemistry designed to provide a high quality Cu deposit with sufficient thickness, without eroding the nucleation layer. Separating this surface preparation into two separate process steps provides better adhesion than direct on-barrier chemistry alone. With conventional on-barrier chemistry alone, this conventional chemistry contains organic additives in an attempt to achieve a desired effect, but this adds impurities to the plated copper. In other words, techniques herein include separating on barrier chemistry application into two distinct process steps, with one chemistry created to provide good nucleation, while another chemistry is created to provide a high quality Cu deposit with sufficient thickness to enable a subsequent gapfill process. The combined result of using two separate chemistries can provide better adhesion than a direct on barrier chemistry alone.

**[0011]** One embodiment includes a method for coating surfaces of microscale features fabricated into a substantially planar upper surface of a substrate. This method can include several process steps. A substrate can be provided having a barrier layer that conforms to both an upper planar surface of the substrate, and conforms to surfaces of microscale features fabricated into the upper planar surface of the substrate. This barrier layer can include a metal-containing film that inhibits metal diffusion into the substrate. A nucleation layer is plated directly onto the barrier layer on the surfaces of the microscale features by exposing the substrate to a first liquid-phase plating chemistry containing a metal for metal plating, and causing the first liquid-phase plating chemistry to fully contact the surfaces of the microscale features. The first liquid-phase plating chemistry causes deposition and adhesion of the metal directly onto the barrier layer within the microscale features. This deposition and adhesion yields a first film thickness of deposited metal on the barrier layer within the microscale features. A smoothing layer is plated onto the nucleation layer on the surfaces of the microscale features by exposing the substrate to a second liquid-phase plating chemistry containing a second metal for metal plating, and causing the second liquid-phase plating chemistry to fully contact the nucleation layer. The second liquid-phase plating chemistry causes deposition of metal onto the nucleation layer. The deposition and adhesion yields a second film thickness of deposited metal on the barrier layer within the microscale features such that the smoothing layer defines an opening in the microscale features.

**[0012]** Another embodiment includes a substrate processing system for manufacturing microscale structures in a substrate. The system can include a first electrochemical cell containing a first chemical bath having metal ions suitable for electrodeposition. The first electrochemical cell is configured to immerse a substrate, having microscale features formed in an upper planar surface thereof and having a barrier layer conformally deposited thereon, in the first chemical bath. The first electrochemical cell is configured to cause the first chemical bath to fully contact surfaces of the microscale features. The first electrochemical cell is configured to apply a first electric potential at a perimeter of the substrate such that electrodeposition of metal ions onto the surfaces of the microscale features occurs and yields a nucleation layer when the substrate is immersed in the first chemical bath and when the first electric potential is applied. A first chemical supply system is coupled to the first electrochemical cell and configured to supply the first chemical bath with a metal-containing compound, for supplying first metal ions, and a first complexing agent.

**[0013]** A second electrochemical cell contains a second chemical bath having metal ions suitable for electrodeposition. The second electrochemical cell is configured to immerse the substrate, having the microscale features, in the second chemical bath. The second electrochemical cell is configured to cause the second chemical bath to fully contact surfaces of the microscale features. The second electrochemical cell is configured to apply a second electric potential at the perimeter of the substrate such that electrodeposition of metal ions onto the nucleation layer within the microscale features occurs and yields a smoothing layer when the substrate is immersed in the second chemical bath and when the second electric potential is applied. A second chemical supply system is coupled to the second electrochemical cell and configured to supply the second chemical bath with a second metal-containing compound that supplies second metal ions, and an acid. A controller can be coupled to the first chemical supply system and the second chemical supply system, and be configured to controllably supply the first chemical bath and the second chemical bath with chemical constituents to form a nucleation layer directly on the barrier layer within the microscale features in the first chemical bath and the smoothing layer on the nucleation layer with the microscale features in the second chemical bath without filling the microscale features. Alternative embodiments can include a system with a single bath cell that supplies and removes multiple different chemistries. Other embodiments include an apparatus having two or more cells, with each cell having a different chemistry bath.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0014]** The advantages of the technology described above, together with further advantages, may be better understood by referring to the following description taken in conjunction with the accompanying drawings. In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the technology.

**[0015]** FIG. **1** depicts cross sectional view of a microscale feature with metal fill.

**[0016]** FIG. **2** depicts the normalized deposition over potential as a function of position on a wafer or workpiece.

**[0017]** FIG. **3** depicts cross sectional view of the present disclosed embodiments.

**[0018]** FIG. **4** is a flow diagram of the present disclosed embodiments.

**[0019]** FIG. **5** is a schematic of an electroplating process cell suitable for use in the present disclosed embodiments.

**[0020]** FIG. **6** shows the resistance profile of Cu plated directly on a TiN barrier of varying resistance where not only is the overall uniformity hard to control, but there is also always a center edge difference that gets increasingly worse at higher barrier resistance.

**[0021]** FIG. **7** is a photograph that shows the results of tape pull tests the plated Cu on bare barrier wafer, a tape pull test was applied to check adhesion where given the varying center to edge over-potential of conventional means, (only a portion of the wafer can be optimized for good adhesion in this case either the center region or the wafer edge region, but not the entire wafer).

**[0022]** FIG. **8** (*a*) is a photograph that shows a via filled without having a conductive Cu PVD layer (the nucleation failed to reach towards the via bottom). FIG. **8** (*b*) is another photograph that shows results of a via filled using a system and process flow according to the exemplary embodiments, in this case resulting from the use of a conductive Cu PVD layer, generated in accordance with the disclosed embodiments, and where good Cu nucleation exists as evident from a solid fill can be observed throughout the via.

**[0023]** FIG. **9** is a graph showing a profile of organic complexers deposited on a film.

**[0024]** FIGS. **10**A-**10**F shows cross-sectional views of a microscale structures and progression of a copper deposition and gapfill process.

## DETAILED DESCRIPTION

**[0025]** Although the present invention will be described with reference to the embodiments shown in the drawings, it should be understood that the present invention can be embodied in many alternate forms of embodiments. In addition, any suitable size, shape or type of elements or materials could be used. For example, while TSV structures are described, the method and apparatus described herein may be applicable to other microscale features, including damascene trench-via structures.

**[0026]** Wet processing provides an attractive means for transporting reactants to the interior surfaces of TSV structures because the fluid transport at this feature scale is primarily through diffusion and is therefore significantly less restricted by the high aspect ratio geometry than is PVD. In order to effect wet processing of the TSV structures, it is desirable to provide a means for completely wetting the interior TSV surfaces, in other words providing a means for replacing the barrier metal/air interface with a barrier metal/fluid interface. After fluid is fully in contact with all elements of the interior TSV surface it is possible to transfer reactants to these surfaces via diffusive transport. By also providing a suitable electrical driving potential it is possible to cause an electrochemical reaction and transform reactants in the fluid into a metal deposit layer metal on the TSV interior surface. As noted before, however, a significant difficulty of using conventional ECD to deposit seed metal on the interior surfaces of TSV features of a substrate coated with highly resistive barrier metal (e.g., TiN with resistivity of about 10-100 ohms/square) is the large radial electrical potential drop that occurs within the barrier metal as current flows from the substrate perimeter to the substrate center. The large potential drop causes an undesirable difference in the available driving electrical potential between edge and center regions of the substrate. The disclosed embodiments overcome the problems of conventional deposition means, as will be described further below, to provide locally on the TSV interior surface an adequate electrical potential to cause suitable electrodeposition of metal to locally form a plating seed layer.

**[0027]** A desired characteristic of a seed or conductivity layer to be used, as will be described further below, for subsequent filling of TSV structures, is that said layer is adhered sufficiently well to the planar surface of the substrate to endure the applied stress of a relatively thick, 1 to 5 micron, copper layer which is formed on the planar surface during the TSV filling process, and which must endure the mechanical stresses of chemical mechanical polishing which is typically done after the TSV filling step. Adhesion of an electrodeposited metal film is strongly dependent on the nucleation density which depends on the local deposition overpotential as well as plating chemistry characteristics. Conventional methods for "direct on barrier" or "seed layer repair" electrodeposition involve costly complex equipment for electrodeposition to provide a minimum of overpotential variation across the substrate and may require an anneal step after the seed layer electrodeposition to improve the adhesion prior to the filling step. In contrast to conventional methods, the exemplary embodiments produce an economical method to provide reliable adhesion of seed layer without recourse to an anneal step and to provide better overpotential uniformity across the substrate to achieve repeatable adhesion and grain structure among all TSVs on the substrate as will be described in greater detail below.

**[0028]** The exemplary embodiments, as will be described below in various aspects, provide a method, systems and components for processing one or more workpieces by the formation of metal seed layers in the interior surfaces of through silicon via features on the surfaces of the workpiece (s). A workpiece can be planar or substantially planar, and can be thin or ultra-thin. Suitable workpieces include, but are not limited to, semiconductor wafers, silicon workpieces, interconnection substrates, and printed circuit boards.

**[0029]** First, microscale holes are formed in the workpiece by known etching processes, and suitable isolation and barrier films are applied to the workpiece, both on the planar surface as well as the interior surfaces of the micro-scale vias, in particular a tungsten, titanium-nitride or tantalum nitride barrier layer of from 200 to 500 angstroms in thickness is applied with chemical vapor deposition, this barrier film providing the substrate with a surface conductivity of between 10 and 200 ohms/square. Other barrier materials may include W, Re, Ru, Rh, and Ni. The disclosed embodiments provide a means of electrically connecting the plurality of microscale via features to the perimeter of the wafer by then applying with physical vapor deposition (PVD) a combined layer of adhesion promoting film such as titanium in the range of 200 to 500 angstroms in thickness followed by a substantially conductive layer film such as copper in the range of 1000 to 3000 angstroms in thickness (e.g. what may be referred to as a thick layer). In the exemplary embodiments the PVD process may not cause substantial or appreciable seed metal deposition within the microscale via feature. However the PVD process does provide reliable adhesion between the Ti/Cu layer and the planar surface of the substrate, thereby anchoring the conductive layer to the barrier layer and the substrate surface. This well adhered substantially conductive

Ti/Cu layer provides a path to apply electric potential to the interior surfaces of all the microscale vias.

**[0030]** The substrate with microscale vias may be immersed in a processing fluid using a means to ensure complete elimination of air to metal surface interfaces within said micro-scale via and their replacement with fluid to metal surface interfaces, such as be using a vacuum pre-wet method. Fluid may be de-ionized and de-aerated water, or it may be a water containing 0.5% by weight hydrofluoric acid. The wetting fluid may be removed and replaced with a copper electroplating solution. This may be accomplished while maintaining the wafer within a substantially oxygen free environment. This may be accomplished, for example, by pushing the fluid from the vacuum pre-wet vessel using an oxygen free gas such as nitrogen and replacing the new fluid by pumping out the nitrogen and resuming the vacuum environment. At this point the microscale vias contain copper electroplating solution. The top most portion of the sidewall of the microscale vias may be electrically connected to the wafer perimeter via the PVD Ti/Cu conductive layer that is connected to a power supply and an anode disposed substantially parallel to the wafer surface. A series of short pulses of negative electrical potential may be applied between the interconnected microscale via array and the anode. The duration of each pulse causes the copper ions immediately adjacent to the wafer surface interface to electro-deposit, within the microscale via, copper deposits on the metal barrier surface and on the planar field region copper deposits on the PVD copper surface. A delay between pulses may be provided to allow diffusion of copper ions from the bulk solution and replace those removed from the near surface region. By way of example, a ratio of about 2:10 between the off/on times has been found to be advantageous though any other suitable off/on cycle ratios may be used.

**[0031]** The presently disclosed embodiments overcome the problems of conventional means for example, by using what may be referred to as a relatively thick, substantially uniform and conductive PVD copper layer rather than a conventional ultra-thin discontinuous PVD copper seed layer. This substantially uniform and continuous conductive layer may interconnect substantially all the micro-scale vias (and more specifically the topmost portion of the via side walls). Copper may be directly deposited in the exemplary embodiments, on the barrier metal exposed on the walls of the microscale vias, which eliminates problems encountered by conventional means in repairing a thin PVD copper layer or depositing copper directly on barrier metal covering the full wafer surface. The presently disclosed embodiments further eliminate the difficulty encountered by conventional means (using an ultra-thin seed layer) of electro-depositing onto a highly resistive substrate, the need for costly ionized PVD deposition equipment, and minimize the uncertainty about achieving void free filing among all vias on the substrate.

**[0032]** In greater detail now, the presently disclosed embodiments provide a novel system and method of producing an electroplating seed layer on the high resistivity barrier layer interior surfaces of a plurality of microscale holes on a workpiece. In particular, the system and method of the exemplary embodiments provide the seed layer inside a high aspect ratio through-silicon-via (TSV) and then electrofill the TSV with copper.

**[0033]** In FIG. **2**, the curve **302** illustrates that an particular level of substrate resistivity can cause a substantial difference in deposition overpotential between wafer perimeter and wafer center. There can be as much as a 100 fold reduction in deposition over potential from perimeter to center. As disclosed herein, applying a relatively thick conductive metal coating to the planar surface of the substrate can yield a substantially uniform overpotential. Referring also to FIG. **3**., the presently disclosed embodiment is depicted in cross section as a microscale feature hole **200** fabricated into substrate **201** with the hole for example being in the range of diameter or width **210** of from about 1 to 10 microns (about 10,000 to 100,000 angstroms) and depth **212** of from about 10 to 100 microns (about 100,000 to 1,000,000 angstroms), an exemplary microscale feature being circular with a diameter of 5 microns (50,000 angstroms) and a depth of from 50 to 75 microns (500,000 to 750,000 angstroms). As may be realized, the microscale feature **200** shown in FIG. **3** is representative, and features similar to feature **200** may be located as desired anywhere on the substrate **201**. The substrate, along with the microscale features, may be coated with an insulating film (not shown) and may then be coated with a metal barrier film **202** by a process providing coverage that is substantially independent of the microscale geometry, exemplary processes being chemical vapor deposition (CVD) of titanium nitride, tantalum nitride, ruthenium or tungsten, or electroless chemical deposition of nickel, said barrier film having for example an electrical resistivity of from about 1 ohms/square to 200 ohms/square, exemplary process being from about 5 to 50 ohms/square.

**[0034]** The exemplary embodiments, as will be described further below provide for deposition of a well adhered and electrically conductive coating **205**, for example, using physical vapor deposition (PVD) of copper in the range of about 0.1 to 0.5 microns (1000 angstroms to 5000 angstroms) thick. The PVD copper layer may be deposited in the same machine (not shown) as the CVD barrier if said machine is capable of moving the substrate from the CVD chamber to the PVD chamber without causing oxide growth on the barrier which would degrade the adhesion of copper to barrier. In alternate embodiments, the PVD copper layer may be deposited in a separate machine using known methods of a plasma pre-clean etch to remove oxides from the barrier layer and providing a PVD sputtered adhesion layer followed by a thick PVD sputtered copper layer, (for example, in an embodiment being about 1000 angstroms of titanium and about 2000 angstroms of copper) though in alternate embodiments the barrier and connecting layer may have other respective suitable thicknesses. As depicted in FIG. **3** the PVD conductive layer **205** is substantially uniform and continuous and does not substantially or appreciably coat the interior surfaces of the microscale features **200** of high aspect ratio (e.g. AR>5). In the exemplary embodiments, microscale features **200** may have depth to diameter aspect ratios of from about 5 to 15. It is noted that conventional ionized PVD systems are capable of coating interior surfaces of microscale features up to aspect ratio of 10, however these conventional systems are very expensive to operate. In contrast, the exemplary embodiments may provide an economical alternative to the ionized PVD method, and may operate effectively to include microscale features with aspect ratio substantially greater than 10.

**[0035]** Referring now to FIG. **4**, there is shown a flow chart graphically illustrating a method in accordance with the exemplary embodiments disclosed herein for effecting electrodeposition of an adherent seed layer **207** (see also FIG. **3**) by virtue of the conductive layer providing microscale uniformity of the deposition overpotential applied to each of the

microscale features. Accordingly, a feature **200** at the center of the substrate is supplied with a similar overpotential to a feature **200** at the substrate perimeter. This may be achieved with commercially available single anode electroplating equipment such as the "Stratus" from NEXX Systems Incorporated.

**[0036]** FIG. **5** is a schematic cross-sectional view of an exemplary apparatus for effecting at least part of the process illustrated in the chart of FIG. **4**. This embodiment can be used, for example, to process two workpieces simultaneously, for instance held by dual sided workpiece holder(s) **5018**, though in alternate embodiments, the apparatus may be configured to process but a single workpiece. Generally, the apparatus may have a housing **5200** that includes a side wall **5224** and end walls **5226**, and the relative positioning of agitation members **5204***a* and **5204***b* (e.g. shear plates), plates **5208** and anodes **5212** is shown. These elements or the distances are not shown to scale. Although the members **5204***a* and **5204***b* are shown as two separate structures, they can form a single assembly.

**[0037]** In the embodiment shown, fluid enters the housing **5200** through at least one port **5228** in a bottom wall of the housing **5200**. The port **5228** can, in some embodiments, be located in a center portion of the bottom wall **5230** of the housing **5200**. In one embodiment, the port **5228** can be positioned in a bottom portion of a side wall **5224**. The fluid flows up along the surfaces of the one or more workpieces. The fluid can flow between the workpiece holder **5018** and the respective member **5204**, **5204***a*, or **5204***b* or between the workpiece holder **5018** and the plate **5208**. In various embodiments, the fluid exits the housing **5200'** through the top of the housing, through a top portion of a side wall **5224**, or through a top portion of an end wall **5226**. Arrows show the general direction of flow.

**[0038]** In the exemplary embodiment, the anode **5212** may form the outer wall of the housing **5200**. In one embodiment, the anode **5212** can be a component of an anode assembly, which forms the outer wall of the housing **5200**. In various embodiments, the housing **5200** has an outer wall and either the anode **5212** or the anode assembly are removably attached the wall or spaced from the wall.

**[0039]** In the exemplary embodiments, the anode **5212** may be a copper disk. In one embodiment, the exposed surface area of the anode **5212** is about 300 cm2. In one embodiment, the anode **5212** is consumed during electrodeposition (or another fluid process such as copper or solder deposition). One feature of the anode **5212** is that it can be removed and replaced with little effort, minimizing lost production time.

**[0040]** As may be realized, in the exemplary embodiments using an anode **5212**, the workpiece surface serves as the cathode. Referring again to FIG. **4**, it may be understood that in the exemplary embodiment etching of the high sheet ratio holes (TSV) into the workpiece **201** (see also FIG. **3**) as identified in block **401** of FIG. **4** may be performed outside or prior to placement of the workpiece in the electroplating apparatus. Similarly, the deposition as described previously of the barrier layer **202** and thick conductive layer **205**, respectively identified in blocks **402**-**403** of FIG. **4**, may be performed outside or prior to placement of the workpiece in the electroplating apparatus. As noted before and seen best in FIG. **3**, the thick conductive layer **205** deposited on the workpiece surface, is substantially uniform in thickness across the surface of the workpiece where the conductive layer **205** is deposited. The conductive layer **205** is also substantially continuous, where deposited, with no appreciable voids or discontinuities interrupting the conductive layer (e.g. no appreciable portions of the deposited conductive layer **205** are isolated from other portions of the conductive layer). As seen best in FIG. **3**, in the exemplary embodiment, but for a small (scale comparable to coating thickness itself) portion of the hole inner wall surface, at the topmost opening, the hole wall surface remains uncoated (has no appreciable conductive layer deposits) with the conductive layer.

**[0041]** Electrodeposition of the adherent seed or finish layer **207**, block **404** in FIG. **4**, may be performed as noted before with the electrodeposition apparatus illustrated in FIG. **5**, fully coating the workpiece surface, including that of the TSV(s) inner walls that lack any appreciable coating or deposits of a Cu PVD conduction layer. As noted before, the seed or finish layer **207** is coated, per block **404** in FIG. **4**, directly onto the barrier layer **202** on the inner walls of the TSV. In the exemplary embodiments, the finish or seed layer **207** may be formed (from the surface on which the seed layer is being deposited) to a desired final thickness of the seed layer in substantially one (deposition) step. As seen in FIG. **3**, the finish coat **207** is but one layer providing the finish surface upon which the fill process may be applied, block **405** of FIG. **4**. As may be realized, the apparatus in the exemplary embodiment shown in FIG. **5**, may also include a suitable controller (not shown) connected to the described components and adapted to operate the apparatus and effect the corresponding portions of the process show in FIG. **4** and described herein.

**[0042]** As has been described previously, in the exemplary embodiments, the thick copper layer removes the highly resistive characteristic of the substrate, as otherwise would exist for either a "direct on barrier" or "ultra-thin seed layer" type of substrate and provides a substantially uniform electrical conduction capability to all the microscale features located throughout and across the workpiece. Hence, it is possible to use a method that may be referred to as a so called "strike" process, wherein use of a chemical bath dilute in ions is combined with application of a high electrical overpotential to generate dense nucleation thereby providing an adherent deposit. The strike process may use an alkaline solution containing about 96 grams per liter of citric acid, 20 grams per liter of $CuCO_3Cu(OH)_2$, with pH adjusted to about 11.6 by addition of NaOH operating at a current density of 4 amperes per decimeter.

**[0043]** FIG. **7** is a photograph that shows the results of a tape test of such Cu plated on a blanket TiN barrier wafer. As may be realized from FIG. **7**, the system may be adjusted to maintain either good center or edge adhesion. The plating tool geometry may otherwise be modified to provide a non-uniform applied electric field to compensate for the spatially non-uniform overpotential, or by a means such as disposing a highly resistive porous plate between the anode and the substrate such as the Ebara Corporation "EREX" system. The deposition overpotential strongly influences the adhesion of the deposited film, primarily due to the influence of the overpotential on the deposit nucleation density. Where uniform deposition can be achieved for a particular sheet resistance wafer, it may need to be re-adjusted when there is a change in the barrier resistance. FIG. **6** shows the same process applied to two different barrier resistances.

**[0044]** Referring also to FIGS. **8**A-**8**B there is shown optical images of a cross-section of actual plated vias with and without the Cu PVD conduction layer. The sample was cleaved to expose the Cu-barrier interface of the via to the

wafer. FIG. **8**A shows similar process on a TiN barrier only, versus FIG. **8**B which includes the addition of the Cu PVD conduction layer in accordance with the exemplary embodiments as described herein. As may be seen, the plated Cu failed to reach all the way to the via bottom in FIG. **8**(*a*). Adhesion test using a tape pull procedure revealed that the sample in FIG. **8**(*a*) could easily be lifted-off, whereas the sample in FIG. **8**(*b*) had no such problems.

**[0045]** The disclosed embodiments provide a wide process operating window that facilitates an economical manufacturing process. Referring also to FIG. **6**, there is shown an illustration of the thickness profile of copper films plated directly on high resistance substrate using a multi-zone anode electroplating configuration. Although thickness uniformity is better than that achieved without anode zone control, there is metal thickness variation which is also indicative of variation in the nucleation and consequent adhesion of the copper film. As noted before, FIG. **7** illustrates conventionally plated Cu wafers directly on barrier after being subjected to a tape-pull test to test for adhesion. As shown, in conventional systems employing anode zone control, consistent and uniformly adherent plating is difficult to achieve resulting in either the center or edge region deposit in a condition that provided adequate adhesion (while the other portions of the substrate as shown were deposited in a low adhesion condition). The exemplary embodiments circumvent this problem by limiting the required control of nucleation and adhesion of copper on the barrier to the geometrical scale of the through silicon via itself. In other words the disclosed embodiments reduce the problem from controlling potential across the 300 mm surface of a typical silicon substrate to controlling the potential across the depth of a 0.1 mm deep microscale feature, thereby simplifying the problem by several orders of magnitude.

**[0046]** After the one layer finish or seed layer **207** has been deposited to a sufficient thickness inside the microscale feature, for example a minimum thickness of about 200 to 500 angstroms, the substrate may be moved to a conventional "bottoms-up" type of electroplating bath (block **405** in FIG. **4**), for example DVF200 by Enthone Incorporated. Copper is then electrochemically filled into the microscale feature by conventional methods. In the exemplary embodiment, the workpiece may not be annealed between the seed layer deposition and the subsequent filling deposition because the present disclosed embodiments advantageously assures reliable adhesion between barrier and seed on the planar surface of the substrate due to the well-known adhesive properties of the PVD applied conductive layer. Adhesion between barrier and seed layers on surfaces inside the TSV may be improved for example during annealing after filling the TSV. The compressive stress generated across the interface by the thermal expansion of the copper inside the microscale feature hole relative to the substrate expansion serves to improve the adhesion between the microstrike applied copper and the barrier material (e.g. substrate may be silicon which has a thermal expansion coefficient of approximately 4 ppm/C compared to that of copper which is 18 ppm/C).

**[0047]** In the exemplary embodiment(s) the grain structure and adhesion of the seed layer deposition inside the microscale feature during the strike bath may be influenced by applying the deposition potential in pulses. Specifically a positive voltage is applied to the substrate, or cathode, for a time period of from 10 to 100 milliseconds which is followed by an off period, with no voltage applied, of from 20 to 1000 milliseconds. For example, the off/on period ratio may be about 2:10, more specifically an off/on time period ratio of 1:4 may be used. In the exemplary embodiment(s), once a continuous Cu layer is formed all the way to the bottom of the via, the current is then reduced to optimize the grain structure of the Cu layer to support growth of a fine grain structure of the electrodeposited Cu filling material in the next step.

**[0048]** In one embodiment, a method for coating the interior surfaces of microscale hole features fabricated into the substantially planar surface of the workpiece is provided. The method comprises providing a workpiece with a barrier metal coating that is substantially continuous and uniform both along the planar surface of the workpiece and the inner surfaces of the microscale hole features wherein said barrier metal coating is applied by a substantially surface reaction limited process, providing the workpiece with a coating, on the planar surface of the workpiece, of a thick metal layer anchored to the barrier metal coat and disposed to provide substantially uniform electrical conduction capability to the microscale features located throughout and across the workpiece, providing an electrical contact path to the electrically conductive coating at the perimeter of the workpiece, immersing the workpiece in a chemical bath and causing said chemical bath to fully contact the interior surfaces of the microscale hole features, said chemical bath containing metal ions suitable for electrodeposition, and applying electric potential at the perimeter of the workpiece to cause electrodeposition of metal ions onto all surfaces of the workpiece including the interior surfaces of the microscale hole features forming a predetermined finish coat in one electrodeposition step.

**[0049]** In another embodiment, a semiconductor workpiece processing apparatus for manufacturing microscale hole structures in workpieces is described. The work piece has a barrier film applied to a planar surface and interior surfaces of microscale hole structures of the workpiece and has a metal layer deposited over and anchored to the barrier film. The apparatus has a housing defining a process chamber for the workpiece. The chamber is configured for pre-wetting the workpiece with a processing fluid that forms a fluid to metal surface interface between the processing fluid and the planar surface and interior surfaces of each microscale hole structures of the workpiece. An anode is located inside the chamber for electroplating the workpiece, the anode being arranged so that an electroplating overpotential is generated between the workpiece and anode that is substantially uniform across the workpiece which effects electrodeposition of metal on the planar surface and interior surfaces of each microscale hole structure of the workpiece so that the interior surfaces of each microscale hole structure have a finish coat that is a one layer coat.

**[0050]** Techniques herein include processes for producing a gapfill with good deposition and adhesion using on-barrier chemistries instead of PVD or iPVD (ionized PVD) steps. These techniques involve separating the liquid-phase plating chemistries into distinct process steps. Current direct on barrier chemistries use organic complexers that could readily deposit into the plated Cu film. A SIMS (secondary ion mass spectrometry) profile is shown in FIG. **9**. This SIMS profile shows such a film deposited using conventional chemistry. Here, high incorporation of oxygen and carbon can be observed. In addition, the resulting resistivity is much higher relative to plated Cu alone, indicating a very loosely packed structure. For a conventional process to be integrated with a

subsequent TSV gapfill step, a Cu seed ranging from 50 nm to 200 nm is desired. Techniques herein, however, replace this deposit with direct on barrier seed that is less than 10 nm thick, followed by a high purity Cu deposit to make-up or complete the remaining desired thickness. In this case, the direct on barrier only deposits sufficient thickness to provide good nucleation on the barrier surface. The chemistry for the smoothing step can include Cu-containing, low acid chemistry. The low acid in this chemistry reduces the dissolution of the direct on barrier seed when immersed in this high purity Cu solution, while the high Cu concentration improves the deposition rate as well as conformality. Copper plating using this step generally produces better adhesion as compared to using the direct on barrier chemistry alone.

**[0051]** Embodiments can include integration of the direct on barrier process (also used for microstrike or M-strike process) with the TSV gapfill chemistry. Addition of the smoothing step herein yields better TSV fills. For example, without such a smoothing step, center (seam) voids can result in holes that were attempted to be filled. Since most gapfill chemistries have been developed using PVD Cu seed as a development vehicle, the high purity ECD Cu deposit resembles the PVD seed most closely. Thus, integration of these two steps is convenient with the addition of the high purity Cu smoothing step, and can be readily incorporated into gapfill process systems.

**[0052]** For a CVD TiN/W barrier, the addition of the smoothing step reduces the number of voids with no seed present. This is believed to be due to the nucleation properties of this chemistry on a W barrier. Nucleation on W compared to TiN results in larger grain sizes, which are more loosely packed together. By adding the high purity Cu deposit as an intermediate layer, this deficiency is covered up and thus reduces or eliminates center voiding in conjunction with additional gapfill plating steps.

**[0053]** FIGS. **10**A-**10**F show cross-sectional views of a hole defined by a substrate, as well as progression of an example copper deposition and fill process. In one coating process, a substrate is provided having a barrier layer that conforms to both an upper planar surface of said substrate and conforms to surfaces of microscale features fabricated into said upper planar surface of said substrate. FIG. **10**A shows an example substrate **201** having an upper planar surface **225**. Substrate **201** defines a microscale feature **200**. The microscale feature can be a hole, a trench, a TSV, or feature defined by the substrate. Such microscale features can be created by known etching and patterning processes. The microscale feature **200** can have an aspect ratio that is its depth **212** to width **210** ratio. In some embodiments, the microscale features can comprise at least one through-silicon via (TSV). Note that cross-sectional views are not drawn to scale in that holes can be substantially deeper than they are wide. FIG. **10**B shows a barrier layer **202** that is substantially, continuously, and conformally applied to the upper planar surface **225** and the microscale feature **200**. The barrier layer comprises a metal-containing film that inhibits metal diffusion into said substrate. That is, relative to the properties of the substrate material, the barrier layer reduces diffusion of copper into the substrate. In some embodiments, the barrier layer can include one or more sub-layers containing one or more metals selected from the group consisting of Ti, Ta, W, Re, Ru, Rh, and Ni.

**[0054]** The coating process includes plating a nucleation layer **231** directly onto the barrier layer **202** on the surfaces of the microscale features by exposing the substrate to a first liquid-phase plating chemistry containing a metal for metal plating. The metal can be selected from any metal having properties that enable plating. Typically copper is the selected metal because of copper's high conductivity. The first liquid-phase plating chemistry is caused to fully contact the surfaces of the microscale features. The first liquid-phase plating chemistry causes deposition and adhesion of the metal directly onto the barrier layer within the microscale features. This deposition and adhesion yields a first film thickness of deposited metal on the barrier layer within the microscale features, such as within TSVs. FIG. **10**D shows an example result after the nucleation layer **231** has been plated.

**[0055]** Next a smoothing layer **237** is plated onto the nucleation layer on the surfaces of the microscale features by exposing the substrate to a second liquid-phase plating chemistry containing a second metal for metal plating. The second liquid-phase plating chemistry is caused to fully contact the nucleation layer. The second liquid-phase plating chemistry causes deposition of metal onto the nucleation layer. The deposition and adhesion yields a second film thickness of deposited metal on the barrier layer within the microscale features such that the smoothing layer defines an opening in the microscale features. In other words, the smoothing layer does not completely fill the hole, but can provide a substantially thicker layer as compared to the nucleation layer. FIG. **10**E shows an example result after the smoothing layer **237** has been plated.

**[0056]** By way of some example dimensions for given embodiments, the first film thickness exceeds **20** Angstroms, and the second film thickness is less than 1 micron. The first film thickness can exceed 100 Angstroms while the second film thickness is less than 600 nm. The first film thickness can exceed 100 Angstroms while the second film thickness is less than 20 nm. The first film thickness can range from 100 Angstroms to 100 nm, or from 100 Angstroms to 20 nm.

**[0057]** In some embodiments, an optional electrical contact path **205** can be provided at the upper planar surface **225** of the substrate **201**, as shown in FIG. **100**. This electrical contact path **205** can extend from a perimeter of the substrate to a center of the substrate. The electrical contact path permits generating an electrical potential at an entry to the microscale features. For example, some barrier materials can have too high a resistance and/or the substrate can have a surface area sufficiently large to reduce conductivity to the center of the substrate. In a more specific example, a sheet resistance of the barrier layer that is more than about 30 ohm/sq of the substrate has a resistance that is too high for uniform center-edge plating. In such scenarios the electrical contact path **205** is beneficial to conduct an electrical potential evenly to all microscale features in the substrate. The electrical contact path can be deposited as an electrically conductive coating on the upper planar surface of the substrate via vapor deposition. This electrically conductive coating is a metal layer adhered to the barrier layer on the upper planar surface and provides electrical conduction to the microscale features located throughout and across the substrate. Note that because this electrically conductive coating is deposited isotropically and because microscale features have a high aspect ratio, relatively little of this conductive coating adheres to surfaces of the microscale features because they are largely shadowed. For example, aspect ratios of the microscale features can be equal to, or greater than, 10-to-1. The electrically conductive coating can be a copper layer deposited using physical vapor

deposition (PVD) to a thickness of between about 2000 and 5000 angstroms. In most embodiments, the physical vapor deposition (PVD) excludes ionized PVD such that the electrically conductive coating applied by the physical vapor deposition is at most sparsely applied and discontinuous on the surfaces within the microscale features.

**[0058]** Plating the nucleation layer directly onto the barrier layer on the surfaces of the microscale features can comprise immersing the substrate in a first chemical bath containing the first liquid-phase plating chemistry that includes metal ions suitable for electrodeposition. Such immersion causes the first liquid-phase plating chemistry in the first chemical bath to fully contact the surfaces of the microscale features. A first electric potential can then be applied at the perimeter of the substrate. This first electric potential causes electrodeposition of metal ions onto the barrier layer within the microscale features. The first liquid-phase plating chemistry can include a metal ion source (that providing metal ions) and a complexing agent that bonds with and causes adhesion of the metal ions directly onto the barrier layer on the surfaces of the microscale features. A complexing agent is a compound that independently assists molecules or ions of a non-metal to form coordinate bonds with a metal atom or ion. A chelating agent is a compound that coordinates with a metal ion to form a chelate. The complexing agent can be selected to include a citrate, a tartrate, a sulfate, an acetate, or a fluoroborate, or any combination of two or more thereof.

**[0059]** By way of a non-limiting example, there are various techniques for applying the nucleation layer. Various complexing agents for use with a metal ion source to improve direct adhesion of metal to a metal barrier are commercially available or under development, and for example, may be made available by various chemical suppliers, such as Enthone, Inc. (West Haven, Conn.). In this bath, a first electric potential of about 9.5 $mA/cm^2$ is applied for about 20 seconds, followed by 3.5 $mA/cm^2$ for about 100-250 seconds. In another process for applying the nucleation layer, a conventional Cu citrate chemistry can be used. With this conventional chemistry, the first liquid-phase plating chemistry can have $Cu^{2+}$ ions at about 0.04 mol/L, $(NH_4)_2HC_6H_5O_7$ at about 0.04 mol/L, and have a pH of about 7.54. The ratio of $Cu^{2+}$ to ammonium citrate can be about 1:1. In this bath, a first electric potential of about 2.0-2.3 $mA/cm^2$ is applied for about 100 seconds.

**[0060]** Plating the smoothing layer onto the nucleation layer can comprise immersing the substrate in a second chemical bath containing the second liquid-phase plating chemistry that includes metal ions suitable for electrodeposition. Such immersion (and optional agitation) causes the second liquid-phase plating chemistry in the second chemical bath to fully contact the nucleation layer. A second electric potential is applied the perimeter of the substrate. This second electric potential causes electrodeposition of metal ions onto the nucleation layer within the microscale features. The second electric potential is less than the first electric potential. The second liquid-phase plating chemistry can include a metal ion source (that provides metal ions) and an acid. Note that the second liquid-phase plating chemistry can exclude a complexing agent.

**[0061]** In one specific example for plating the smoothing layer, the second bath can include $Cu^{2+}$ ions at about 0.79 mol/L, $H_2SO_4$ at about 0.20 mol/L, and $Cl^-$ at about 0.001 mol/L. In this bath, a second electric potential of about 0.5 $mA/cm^2$ is applied for about 300 seconds.

**[0062]** Some embodiments can include plating a metal layer **240** onto the smoothing layer applied to the surfaces of the microscale features by immersing the substrate in a third chemical bath containing a third liquid-phase chemistry that includes metal ions suitable for electrodeposition. Such immersion causes the third liquid-phase plating chemistry in the third chemical bath to fully contact the smoothing layer. A third electric potential can be applied at the perimeter of the substrate. This third electric potential causes electrodeposition of metal ions onto the smoothing layer and fills the microscale features, wherein the third electric potential is less than the first electric potential. FIG. **10**F shows an example result after the metal layer **240** has been plated. Note that metal layer **240** fills hole **200** in substrate **201**. Plating this metal layer onto the smoothing layer, and thus being applied to the surfaces of the microscale features, is executed by exposing the substrate to a third liquid-phase plating chemistry containing a metal suitable for metal plating, and causing the third liquid-phase plating chemistry to fully contact the smoothing layer. The third liquid-phase plating chemistry deposits metal onto the smoothing layer and fills the microscale features. The third liquid-phase plating chemistry includes a metal ion source (that provides metal ions) and an acid. The third liquid-phase plating chemistry excludes a complexing agent. The third liquid-phase plating chemistry can also include one or more plating additives selected from the group consisting of a plating leveler, a plating accelerator, and a plating suppressor. In some embodiments, when an acid is added to both the second liquid-phase plating chemistry and the third liquid-phase plating chemistry, the acid concentration of the acid in the third liquid-phase plating chemistry is greater than an acid concentration of the acid in the second liquid-phase plating chemistry.

**[0063]** In one specific example for gapfill plating, the third bath can include $Cu^{2+}$ ions at about 0.79-0.95 mol/L, $H_2SO_4$ at about 0.51-0.82 mol/L, and $Cl^-$ at about 0.001 mol/L. Note that additive concentrations can differ from varying commercial products. In this bath, a second electric potential of about 0.5 $mA/cm^2$ is applied initially, and can be optionally ramped up to about 3 $mA/cm^2$ for a period of time sufficient to fill a corresponding microscale feature.

**[0064]** Other embodiments include a substrate processing system for manufacturing microscale structures in a substrate, such as a plating apparatus. Such processing systems can include one or more cells. One system includes a first electrochemical cell containing a first chemical bath having metal ions suitable for electrodeposition. This first electrochemical cell is configured to immerse a substrate, having microscale features formed in an upper planar surface thereof and having a barrier layer conformally deposited thereon, in the first chemical bath. The first electrochemical cell is configured to cause the first chemical bath to fully contact surfaces of the microscale features. The first electrochemical cell is also configured to apply a first electric potential at a perimeter of the substrate such that electrodeposition of metal ions onto the surfaces of the microscale features occurs and yields a nucleation layer when the substrate is immersed in the first chemical bath and when the first electric potential is applied. A first chemical supply system can be coupled to the first electrochemical cell and be configured to supply the first chemical bath with a metal-containing compound (that supplies first metal ions) and a first complexing agent.

**[0065]** A second electrochemical cell contains a second chemical bath having metal ions suitable for electrodeposi-

tion. The second electrochemical cell is configured to immerse the substrate, having the microscale features, in the second chemical bath. The second electrochemical cell is also configured to cause the second chemical bath to fully contact surfaces of the microscale features. The second electrochemical cell is configured to apply a second electric potential at the perimeter of the substrate such that electrodeposition of metal ions onto the nucleation layer within the microscale features occurs and yields a smoothing layer when the substrate is immersed in the second chemical bath and when the second electric potential is applied. A second chemical supply system is coupled to the second electrochemical cell and is configured to supply the second chemical bath with a second metal-containing compound (that supplies second metal ions) and an acid. The processing system can include a controller coupled to the first chemical supply system and the second chemical supply system. The controller is configured to controllably supply the first chemical bath and the second chemical bath with chemical constituents to form a nucleation layer directly on the barrier layer within the microscale features in the first chemical bath and to form the smoothing layer on the nucleation layer within the microscale features in the second chemical bath without filling the microscale features.

**[0066]** The processing system can include a third electrochemical cell containing a third chemical bath having metal ions suitable for electrodeposition. The third electrochemical cell is configured to immerse the substrate, having the microscale features, in the third chemical bath. The third electrochemical cell is configured to cause the third chemical bath to fully contact surfaces of the microscale features. The third electrochemical cell is configured to apply a third electric potential at the perimeter of the substrate such that electrodeposition of metal ions onto the smoothing layer of the surfaces of the microscale features occurs and yields a metal layer that fills the microscale features when the substrate is immersed in the third chemical bath and when the third electric potential is applied. A third chemical supply system can be coupled to the third electrochemical cell and configured to supply the third chemical bath with a third metal-containing compound (that supplies third metal ions). The controller can also be coupled to the third chemical supply system and configured to controllably supply the third chemical bath with chemical constituents for filling the microscale features with metal.

**[0067]** It should be understood that the foregoing description is only illustrative of the invention. Various alternatives and modifications can be devised by those skilled in the art without departing from the invention. Accordingly, the present invention is intended to embrace all such alternatives, modifications and variances that fall within the scope of the appended claims.

**1**. A method for coating surfaces of microscale features fabricated into a substantially planar upper surface of a substrate, the method comprising:

providing a substrate having a barrier layer that conforms to both an upper planar surface of said substrate and conforms to surfaces of microscale features fabricated into said upper planar surface of said substrate, wherein said barrier layer comprises a metal-containing film that inhibits metal diffusion into said substrate;

plating a nucleation layer directly onto said barrier layer on said surfaces of said microscale features by exposing said substrate to a first liquid-phase plating chemistry containing a metal for metal plating, and causing said first liquid-phase plating chemistry to fully contact said surfaces of said microscale features, said first liquid-phase plating chemistry causing deposition and adhesion of the metal directly onto said barrier layer within said microscale features, the deposition and adhesion yielding a first film thickness of deposited metal on said barrier layer within said microscale features; and

plating a smoothing layer onto said nucleation layer on said surfaces of said microscale features by exposing said substrate to a second liquid-phase plating chemistry containing a second metal for metal plating, and causing said second liquid-phase plating chemistry to fully contact said nucleation layer, said second liquid-phase plating chemistry causing deposition of metal onto said nucleation layer, the deposition and adhesion yielding a second film thickness of deposited metal on said barrier layer within said microscale features such that said smoothing layer defines an opening in said microscale features.

**2**. The method of claim **1**, further comprising:

providing an electrical contact path at said upper planar surface of said substrate that extends from a perimeter of said substrate to a center of said substrate, said electrical contact path permits generating an electrical potential at an entry to said microscale features.

**3**. The method of claim **2**, wherein said plating a nucleation layer directly onto said barrier layer on said surfaces of said microscale features comprises:

immersing said substrate in a first chemical bath containing said first liquid-phase plating chemistry that includes metal ions suitable for electrodeposition, causing said first liquid-phase plating chemistry in said first chemical bath to fully contact said surfaces of said microscale features, and applying a first electric potential at said perimeter of said substrate that causes electrodeposition of metal ions onto said barrier layer within said microscale features.

**4**. The method of claim **3**, wherein said plating a smoothing layer onto said nucleation layer comprises:

immersing said substrate in a second chemical bath containing said second liquid-phase plating chemistry that includes metal ions suitable for electrodeposition, causing said second liquid-phase plating chemistry in said second chemical bath to fully contact said nucleation layer, and applying a second electric potential at said perimeter of said substrate that causes electrodeposition of metal ions onto said nucleation layer within said microscale features, wherein said second electric potential is less than said first electric potential.

**5**. The method of claim **4**, further comprising:

plating a metal layer onto said smoothing layer applied to said surfaces of said microscale features by immersing said substrate in a third chemical bath containing a third liquid-phase chemistry that includes metal ions suitable for electrodeposition, causing said third liquid-phase plating chemistry in said third chemical bath to fully contact said smoothing layer, and applying a third electric potential at said perimeter of said substrate that causes electrodeposition of metal ions onto said smoothing layer and that fills said microscale features, wherein said third electric potential is less than said first electric potential.

**6**. The method of claim **2**, wherein said providing an electrical contact path comprises: depositing an electrically con-

ductive coating on said upper planar surface of said substrate via vapor deposition, said electrically conductive coating being a metal layer adhered to said barrier layer on said upper planar surface and providing electrical conduction to said microscale features located throughout and across said substrate.

**7**. The method of claim **6**, wherein said electrically conductive coating is a copper layer deposited using physical vapor deposition (PVD) to a thickness of between about 2000 and 5000 angstroms.

**8**. The method of claim **7**, wherein said physical vapor deposition (PVD) excludes ionized PVD, and wherein said electrically conductive coating applied by said physical vapor deposition is at most sparsely applied and discontinuous on said surfaces within said microscale features.

**9**. The method of claim **8**, wherein an aspect ratio of said microscale features is equal to or greater than 10-to-1.

**10**. The method of claim **1**, wherein said first liquid-phase plating chemistry includes a metal ion source for providing metal ions, and a complexing agent that bonds with and causes adhesion of said metal ions directly onto said barrier layer on said surfaces of said microscale features.

**11**. The method of claim **10**, wherein said complexing agent includes a citrate, a tartrate, a sulfate, an acetate, or a fluoroborate, or any combination of two or more thereof.

**12**. The method of claim **1**, wherein said second liquid-phase plating chemistry includes a metal ion source, that provides metal ions, and an acid.

**13**. The method of claim **12**, wherein said second liquid-phase plating chemistry excludes a complexing agent.

**14**. The method of claim **1**, further comprising:

plating a metal layer onto said smoothing layer applied to said surfaces of said microscale features by exposing said substrate to a third liquid-phase plating chemistry containing metal suitable for metal plating, and causing said third liquid-phase plating chemistry to fully contact said smoothing layer, said third liquid-phase plating chemistry depositing metal onto said smoothing layer and filling said microscale features.

**15**. The method of claim **14**, wherein said third liquid-phase plating chemistry includes a metal ion source, that provides metal ions, and an acid.

**16**. The method of claim **15**, wherein said third liquid-phase plating chemistry excludes a complexing agent.

**17**. The method of claim **15**, wherein said third liquid-phase plating chemistry further includes one or more plating additives selected from the group consisting of a plating leveler, a plating accelerator, and a plating suppressor.

**18**. The method of claim **14**, wherein an acid is added to both said second liquid-phase plating chemistry and said third liquid-phase plating chemistry, and wherein an acid concentration of said acid in said third liquid-phase plating chemistry is greater than an acid concentration of said acid in said second liquid-phase plating chemistry.

**19**. The method of claim **1**, wherein a resistance of the barrier layer is more than about 30 ohm/sq for said substrate.

**20**. The method of claim **1**, wherein said barrier layer includes one or more sub-layers containing one or more metals selected from the group consisting of Ti, Ta, W, Re, Ru, Rh, and Ni.

**21**. The method of claim **1**, wherein said first film thickness exceeds 20 Angstroms, and said second film thickness is less than 1 micron.

**22**. The method of claim **1**, wherein said first film thickness exceeds 100 Angstroms, and said second film thickness is less than 600 nm.

**23**. The method of claim **1**, wherein said first film thickness exceeds 100 Angstroms, and said second film thickness is less than 20 nm.

**24**. The method of claim **1**, wherein said first film thickness ranges from 100 Angstroms to 100 nm.

**25**. The method of claim **1**, wherein said first film thickness ranges from 100 Angstroms to 20 nm.

**26**. The method of claim **1**, wherein said microscale features comprise at least one through-silicon via (TSV).

**27**. A substrate processing system for manufacturing microscale structures in a substrate, comprising:

a first electrochemical cell containing a first chemical bath having metal ions suitable for electrodeposition, said first electrochemical cell being configured to immerse a substrate, having microscale features formed in an upper planar surface thereof and having a barrier layer conformally deposited thereon, in said first chemical bath, said first electrochemical cell configured to cause said first chemical bath to fully contact surfaces of said microscale features, said first electrochemical cell configured to apply a first electric potential at a perimeter of said substrate such that electrodeposition of metal ions onto said surfaces of said microscale features occurs and yields a nucleation layer when said substrate is immersed in said first chemical bath and when said first electric potential is applied;

a first chemical supply system coupled to said first electrochemical cell and configured to supply said first chemical bath with a metal-containing compound, for supplying first metal ions, and a first complexing agent;

a second electrochemical cell containing a second chemical bath having metal ions suitable for electrodeposition, said second electrochemical cell being configured to immerse said substrate, having said microscale features, in said second chemical bath, said second electrochemical cell configured to cause said second chemical bath to fully contact surfaces of said microscale features, said second electrochemical cell configured to apply a second electric potential at said perimeter of said substrate such that electrodeposition of metal ions onto said nucleation layer within said microscale features occurs and yields a smoothing layer when said substrate is immersed in said second chemical bath and when said second electric potential is applied;

a second chemical supply system coupled to said second electrochemical cell and configured to supply said second chemical bath with a second metal-containing compound, for supplying second metal ions, and an acid; and

a controller coupled to said first chemical supply system and said second chemical supply system, and configured to controllably supply said first chemical bath and said second chemical bath with chemical constituents to form a nucleation layer directly on said barrier layer within said microscale features in said first chemical bath and said smoothing layer on said nucleation layer within said microscale features in said second chemical bath without filling said microscale features.

**28**. The substrate processing system of claim **27**, further comprising:

a third electrochemical cell containing a third chemical bath having metal ions suitable for electrodeposition,

said third electrochemical cell being configured to immerse said substrate, having said microscale features, in said third chemical bath, said third electrochemical cell configured to cause said third chemical bath to fully contact surfaces of said microscale features, said third electrochemical cell configured to apply a third electric potential at said perimeter of said substrate such that electrodeposition of metal ions onto said smoothing layer of said surfaces of said microscale features occurs and yields a metal layer that fills said microscale features when said substrate is immersed in said third chemical bath and when said third electric potential is applied; and

a third chemical supply system coupled to said third electrochemical cell, and configured to supply said third chemical bath with a third metal-containing compound for supplying third metal ions, wherein said controller is further coupled to said third chemical supply system, and configured to controllably supply said third chemical bath with chemical constituents for filling said microscale features with metal.

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