Jan. 23, 1962 H. L. GOLDSTEIN 3,018,431

ALTERNATING CURRENT VOLTAGE REGULATOR

Filed Jan. 4, 1960 4 Sheets-Sheet 1

FIG. 1

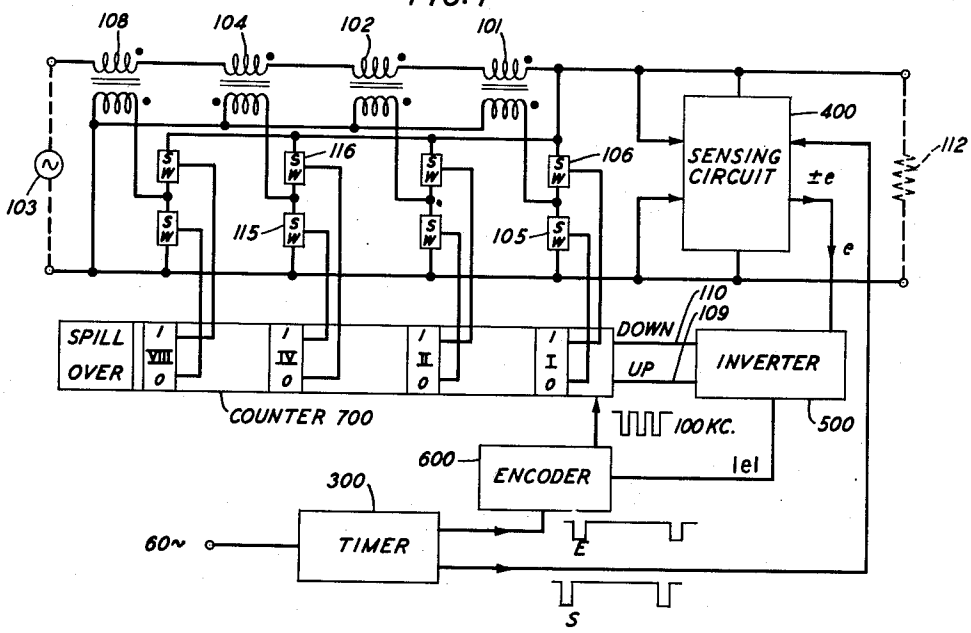
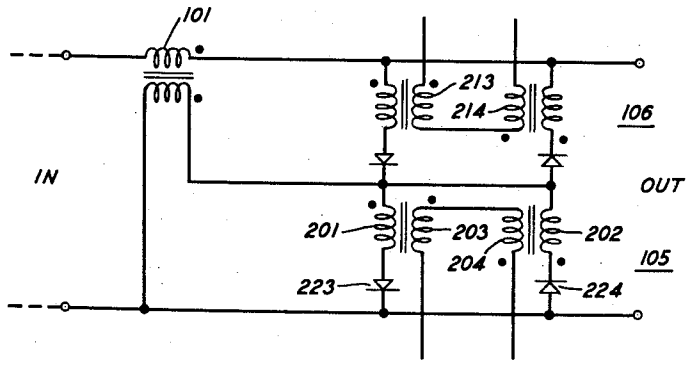


FIG. 2



INVENTOR
H. L. GOLDSTEIN
BY George C. Ford
ATTORNEY

Jan. 23, 1962 H. L. GOLDSTEIN 3,018,431

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Filed Jan. 4, 1960 4 Sheets-Sheet 2

FIG. 3

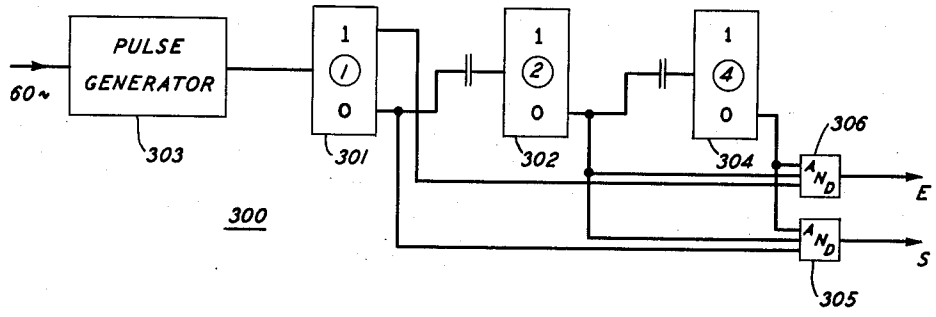
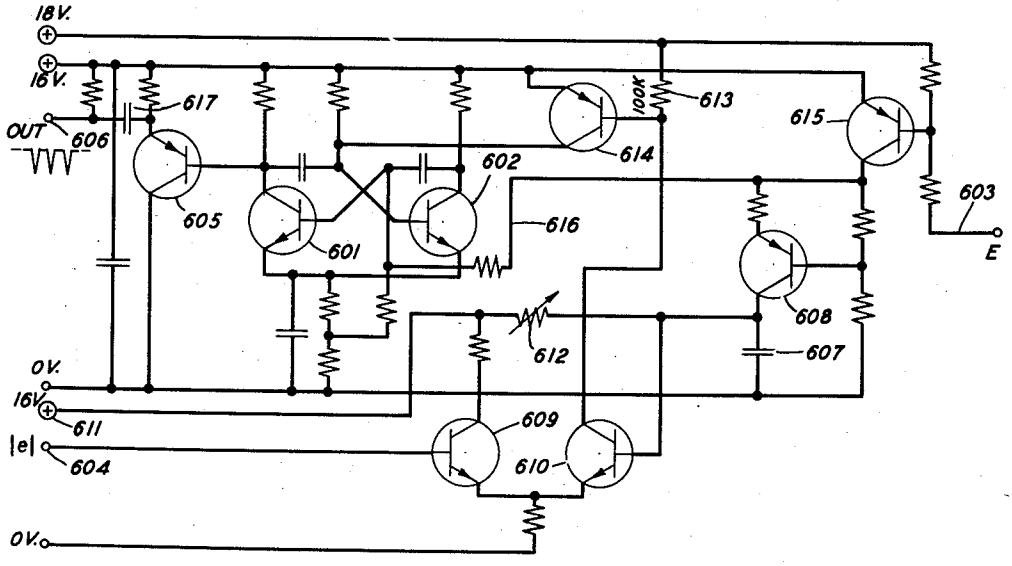


FIG. 6



INVENTOR
H. L. GOLDSTEIN
BY George C. Ford
ATTORNEY

ALTERNATING CURRENT VOLTAGE REGULATOR

Filed Jan. 4, 1960 4 Sheets-Sheet 3

FIG. 4

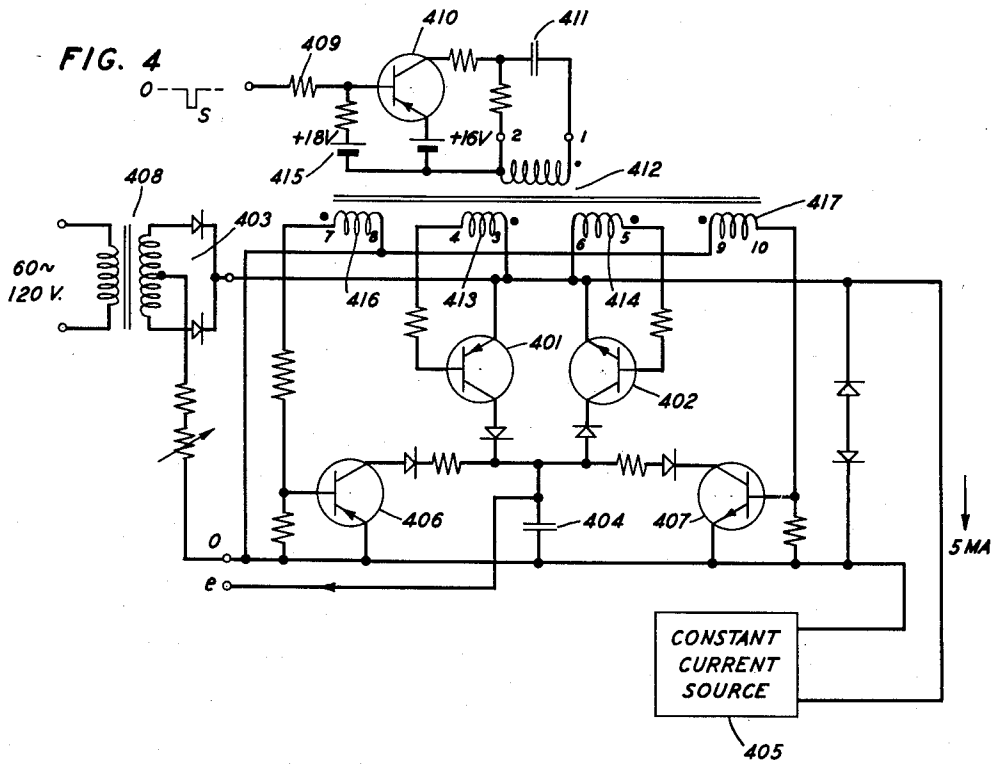
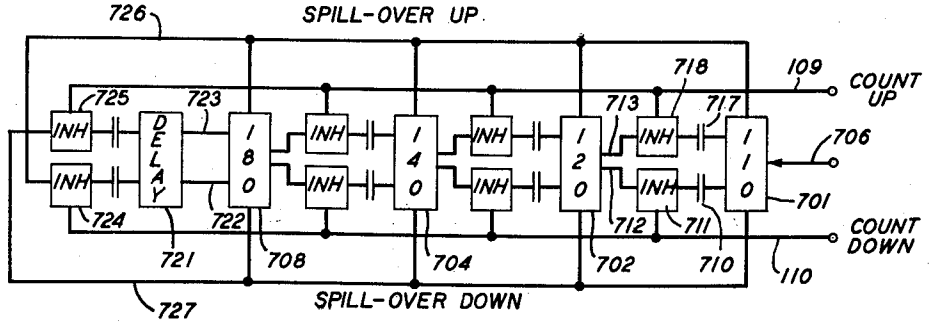


FIG. 7



INVENTOR
H. L. GOLDSTEIN
BY
George C. Tolk
ATTORNEY

Jan. 23, 1962 H. L. GOLDSTEIN 3,018,431

ALTERNATING CURRENT VOLTAGE REGULATOR

Filed Jan. 4, 1960 4 Sheets-Sheet 4

FIG. 8

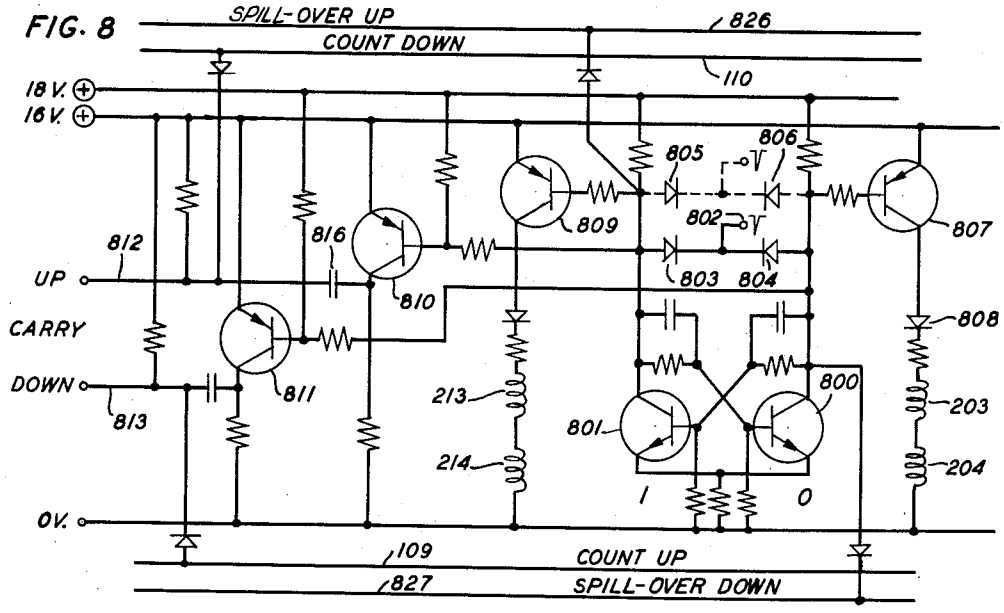
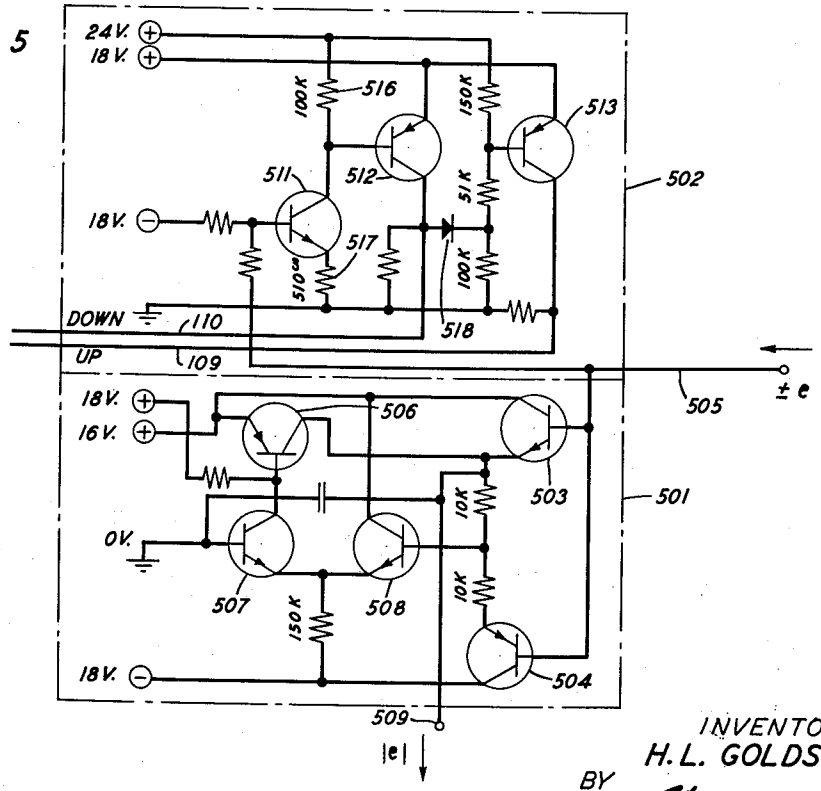


FIG. 5



INVENTOR
H. L. GOLDSTEIN
BY
George C. Ford
ATTORNEY

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Patented Jan. 23, 1962

3,018,431
ALTERNATING CURRENT VOLTAGE REGULATOR

Hans L. Goldstein, Hanover Township, Morris County, N.J., assignor to Bell Telephone Laboratories, Incorporated, New York, N.Y., a corporation of New York

Filed Jan. 4, 1960, Ser. No. 329
9 Claims. (Cl. 323—45)

This invention relates to regulator systems and particularly to voltage regulators for alternating current power supply.

One type of system for providing voltage regulation for alternating current power supply employs boosting or bucking transformers, or both, having their secondaries connected in series between the main source and the load. Switching circuits are provided for connecting the primary windings of these transformers to the source as the auxiliary voltages provided by their secondaries are required to hold the output voltage to its normal value. In such circumstances it has been the practice to employ boosting or bucking transformers which contribute to the load voltage on a unitary or step-by-step basis. It is also more usual to employ electromagnetic switches or relays for controlling the switching of the transformers.

It is an object of the present invention to increase the range and speed of regulation of alternating current power supply systems.

It is a further object of the invention to provide a voltage regulator giving reliable operation at high powers with high efficiency and low wave form distortion.

In accordance with this invention a regulator for an alternating voltage supply system is provided with auxiliary transformers which contribute to the output voltage, components that are related on the basis of a numerical system. Since the binary system is readily adaptable to the use of electronic switching, the transformers can be designed to provide steps such as 1, 2, 4, 8, et cetera percentages of the output voltage. By arranging the control circuit to select various combinations of these auxiliary transformers, a wide range of regulation may be provided with a very small number of transformers. In particular, the output voltage of the regulator is provided with a sensing unit or comparator which periodically produces an error voltage that is a measure of the deviation of the output voltage from the nominal or standard value. This error voltage is transformed from an analog representation to a digital representation in which it comprises a train of pulses, the number of which is proportional to the value of the error voltage. This train of pulses is impressed upon an electronic binary counter, the various stages of which are associated with the appropriate one of the auxiliary transformers. As a result of the activation of the various stages of the counter by the train of pulses there will be switched into circuit those auxiliary transformers appropriate for making the proper correction in the output voltage. All of the control circuits and the transformer switching circuits are of the electronic type particularly employing magnetic or solid state components. Thus the use of moving parts or vacuum tubes is avoided and rapid regulation with reliability of operation is achieved.

This invention may be more readily understood by reference to the following detailed description in connection with the drawing, in which:

FIG. 1 is a block schematic of a specific embodiment of an alternating current voltage regulator in accordance with the present invention;

FIG. 2 is a schematic circuit diagram of one of the auxiliary transformers and its magnetic amplifier switching control;

FIG. 3 is a block schematic diagram of a timer circuit which may be employed in the system of FIG. 1;

FIG. 4 is a schematic circuit diagram of the sensing circuit employed in FIG. 1;

FIG. 5 is a schematic circuit diagram of the inverter of the regulator system;

FIG. 6 is a schematic circuit diagram of the encoder employed in the regulator;

FIG. 7 is a block schematic diagram of the counter used in the regulator; and

FIG. 8 is a schematic circuit diagram of a typical counter stage.

FIG. 1 shows in block schematic form the preferred embodiment of the present invention in a regulator for an alternating current voltage supply. The other circuits show in more detail various component elements of the system of FIG. 1 and the same reference numerals are used for corresponding circuit components, throughout the drawing.

The regulator of FIG. 1 provides a constant voltage supply to the load **112** from an alternating current source of 60 cycles, for example, **103**. Connected in series between the source **103** and load **112** are the secondary windings of auxiliary transformers **101**, **102**, **104**, and **108**. These transformers are of the step-down type and provide across their secondary windings voltages related in value by the denominational orders of a binary system. For example, transformer **101** may provide a voltage of one percent of the nominal value of the output voltage, in which case that of transformer **102** is two percent, transformer **104** four percent, and transformer **108** eight percent. The primary winding of each of the auxiliary transformers is provided with two switches. Thus, the primary of transformer **101** has a switch **105** which, when closed, short-circuits the primary winding and a switch **106** which, when closed, connects the primary winding to the source **103** on the regulated side of the regulator circuit. (The relative polarities of the transformer windings in this and other figures of the drawing are indicated by dots in accordance with the usual convention.)

The timer **300** controls the cyclic operation of the regulator. As will be explained in more detail in the discussion of FIG. 3, this timer derives from the 60 cycle power supply controlly or command signals for initiating the various steps in the cyclic operation of the regulator. The first is a sensing command signal S which is a negative voltage step lasting for one cycle of the 60 cycle current and recurring every 8 cycles of the 60 cycle supply. The second is the encoding signal E which is a negative voltage step generated in the cycle following that in which the sensing pulse is produced.

The sensing circuit **400** produces an error voltage which is proportional to the deviation of the output voltage of the regulator from its normal or standard value. This error voltage is produced during each sensing command signal from the timer **300**. The error voltage e is positive when the output voltage is too high (above its normal value) and negative when the output voltage is too low. These positive or negative voltages are supplied from the sensing unit **400** to the inverter **500**.

Two functions are performed by the inverter **500**. First, it produces a voltage equal to the absolute value $|e|$ of the error voltage e from the sensing unit **400**. The second function of the inverter is to supply control voltages to the up bus **109** and the down bus **110** which control voltages to the up bus **109** and the down bus **110** which control the direction in which the counter **700** will count. Thus, as will be explained in more detail in connection with the description of FIG. 5, when the error voltage is zero or negative the up bus **109** is clamped to positive **18** volts and the down bus is at zero voltage. As will be later explained in detail, this causes the

counter to count up. When the error voltage is positive the up bus will be at zero volts and the down bus at plus 18 volts and the counter will count down.

The encoder **600** is essentially an analog-to-digital converter. It is controlled by the absolute value of the error voltage $|e|$ and operates to produce a train of 100 kilocycles per second pulses, the number of pulses of the train being proportional to the value of the error voltage. This train of pulses is supplied to the binary counter **700**.

The counter **700** is basically a conventional transistor binary counter employing a series of stages of transistor flip-flop circuits with controls for providing reversible counting (up or down). Each of the counter stages is interconnected to a corresponding switching circuit for the transformers **101**, **102**, **104**, and **108**.

The simplest arrangement for the transformer circuits would be that in which their secondaries are connected so that all of their voltages will be additive. With such a connection the only correction in the output voltage which could be made would be in the positive direction and the regulator could only compensate for negative deviations in the source voltage. With this type of circuit the connections of the switches to each of the counter stages would be the same and would be such that when the counter stage is in the "0" position the short-circuiting switch **105** would be closed and the connecting switch **106** open, while when the counter is in the "1" position the short-circuit switch **105** would be open and the connecting switch **106** closed.

However it is possible, by connecting one or more of the transformers **101**, **102**, **104**, **108** in a bucking direction, to cover a range of voltages including negative values. In the circuit shown in FIG. 1 the transformer **104** is connected so that the voltage of its secondary is opposite to and bucks the voltage supplied by the other transformers. Accordingly it is necessary that the switches for controlling transformer **104** be connected to counter stage IV in the opposite manner to which the other switches are connected to their respective counter stages. Thus the shorting switch **115** is connected so that it is closed when the counter stage IV is in the "1" position and the connecting switch **116** is connected so that it will be closed when the counter stage IV is in the "0" position.

FIG. 2 shows schematically the circuit for one of the transformers **101** and its switching circuits **105** and **106**. These circuits are of the so-called "doubler" magnetic amplifier type as described in Magnetic Amplifiers, by H. F. Storm, John Wiley and Sons, 1955, page 245, or Patent 2,126,790 to Logan, August 16, 1938. The magnetic amplifier **105** for example comprises the magnetic windings **201** and **202** connected in series with the respective diodes **223** and **224** which are oppositely poled to provide conducting paths for both the positive and negative cycles of the alternating current. The windings **201** and **202** are each provided with control windings **203** and **204** respectively.

In addition there are provided bias windings (not shown) to which is supplied current of such magnitude and direction as to keep the switch in the open condition when no current is flowing in the control windings. Direct current is supplied from amplifiers associated with and controlled by the counter circuit to the control windings **203** and **204** to operate each magnetic amplifier in only one of two conditions. The switch **105** is either fully on when it acts as a short circuit across the primary of the transformer **101** or fully off when it forms a substantial open circuit across primary windings. The switch is on when the current is supplied to the windings **203** and **204** from the respective counter stage.

Switch **106** is of similar construction and is controlled by the saturating windings **213** and **214**.

FIG. 3 shows the timing circuit **300** which provides the timing pulses for controlling the cycling of the regulator. This comprises a conventional pulse generator **303** which produces a pulse at the beginning of each cycle of the 60 cycle voltage supplied to its input. The resulting output pulses are supplied to a conventional three stage binary counter comprising three stages of transistor flip-flops, **301**, **302** and **304**. As is typical of binary counters, a carry pulse is supplied from one stage to the next through a differentiating circuit when any stage switches from its "1" position to its "0" position. The zero side of each of the counter stages is connected to an AND circuit **305**. As a result there will appear in the output of the AND circuit **305** a negative signal each time that all counter stages are in their zero positions (corresponding to the binary numeral 0 0 0). This command signal S in the output of the AND circuit **305** will last for one cycle of the 60 cycle voltage and will appear once every eight cycles of that supply. The AND circuit **306** is connected to the "1" side of the binary stage **301** and to the "0" sides of the stages **302** and **304**. Consequently a negative signal will appear at the output of tthe AND circuit **306**, on each cycle of the 60 cycle input current following that at which a signal appears in the output of the AND circuit **305** (binary number 001). This signal also lasts for one cycle and is the encoding command signal E.

FIG. 4 shows in detail the sensing circuit **400** of FIG. 1 which operates to produce an error voltage proportional to the variation in the output voltage of the regulator from its standard value. The general principle of operation of this circuit will be described first. At the beginning of a sensing cycle a switch comprising the transistors **401** and **402** is closed and a current proportional to the output voltage of the regulator obtained from the rectifier **403** starts to charge the capacitor **404**. At the same time there is supplied to the capacitor **404** a discharging current obtained from the constant current source **405**. The value of this constant current is the standard for the regulator so that when the output voltage is of the required magnitude the ultimate voltage on the capacitor is zero. Under other conditions the ultimate voltage of the capacitor **404** will have a value e of magnitude and polarity dependent upon the variation of the output voltage of the regulator from its required or standard value. At the end of the sensing cycle charging switch (**401—402**) is opened and a second switch comprising the transistors **406** and **407** is closed to discharge the capacitor **404** and prepare the circuit for the next sensing cycle.

The operation of the circuit of FIG. 4 by means of which these functions are performed will now be described in detail. The output voltage of the regulator is supplied through the input transformer **408** to the full wave rectifier **403**. When the negative sensing signal S is applied to the input terminal **409** the transistor **410** is shifted from OFF to ON. The resulting positive voltage step is supplied through the blocking condenser **411** to the right hand terminal of the primary winding of transformer **412**. The resulting voltages developed across the secondary windings **413** and **414** are in such a direction as to cause the transistors **401** and **402** to turn ON. This effectively closes the switch for supplying charging and discharging current to the capacitor **404**, transistor **401** providing a path in one direction and transistor **402** in the opposite direction. As previously discussed, the capacitor **404** will charge from the rectified current supplied by the rectifier **403**. At the same time discharging current of constant amplitude from the constant current source **405** is also connected to the capacitor **404** through the same paths. At the end of a fixed period determined by the length of the sensing command S, the voltage across the capacitor **404** will accordingly be proportional to the variation between the voltage supplied to the primary of transformer **408** and a standard voltage determined by the value of the current from the constant current source **405**, that is, the error in the output voltage of the regulator.

At the termination of the sensing command signal S the transistor **410** will turn OFF due to the positive 18 volts from battery **415**. The resulting negative voltage step is applied to the right hand terminal of the primary of transformer **412**, inducing in the secondary windings **416** and **417** voltages in such a direction as to turn transistors **406** and **407** ON, providing a path for the discharge of a charge of either polarity on the capacitor **404**, thus preparing the circuit for the next succeeding sensing cycle.

Each of the transistors **401**, **402**, **406**, and **407** is provided with a diode connected in series in its collector lead. Each such diode blocks voltages which otherwise might bias the collector junctions in the forward direction causing the respective transistor to conduct even when its emitter junction is reverse biased as is required for the open switch condition. A sufficiently high bias voltage at the bases of the transistors cannot be used because this would exceed the emitter-base reverse voltage rating of the transistors.

FIG. 5 shows in schematic circuit form the details of a circuit that may be used to perform the operations of the inverter **500**. This circuit comprises two sections operating essentially independently of each other and comprising the inverter proper enclosed in the dash-dot lines **501** and the polarity indicator enclosed in the dash-dot lines **502**.

As discussed in connection with the block schematic of FIG. 1, the function of the inverter proper is to produce a voltage $|e|$ equal to the absolute value of the error voltage e obtained from the sensing unit **400**, that is of positive polarity independent of the polarity of the error voltage. Each of the transistors **503** and **504** has its base connected to the lead **505** through which the error voltage is supplied from the sensing unit. When error voltage e is negative, transistor **503** is OFF and the transistors **506**, **507**, **508**, and **504** act like a conventional series regulator. In this regulator circuit transistor **506** is the series transistor and supplies to the output lead **509** a positive voltage the value of which is determined by the magnitude of the negative input voltage e. In performing this function transistors **507** and **508** operate as a differential amplifier controlling the transistor **506**. The input voltage e from the lead **505** is applied through the transistor **504**, operating as an emitter follower, to this differential amplifier and serves as a negative reference voltage for regulating the value of the output voltage on the lead **509**.

When the error voltage e is positive, transistor **504** is OFF and transistor **508** is saturated, resulting in the cut-off of transistors **506** and **507**. For this positive value of e transistor **503** is ON, operating as a conventional emitter follower with a voltage gain of unity and supplying the error voltage to the output lead **509**.

The polarity indicator **502** comprises the transistors **511**, **512**, and **513** and their associated circuits. As previously indicated, the function of the polarity indicator is to provide the proper voltages on the up and down busses **109** and **110**, respectively, to control the operation of the counter **700** in accordance with the polarity of the error voltage e. Actually the busses **109** and **110** are alternately switched between the voltages of plus 18 volts and 0. An examination of the circuit of the polarity indicator with the interconnection of the transistors and bias voltages as shown will readily indicate the following conditions with respect to the polarity of the error voltage e on the input lead **505**.

With the error voltage e either zero or negative, transistors **511** and **512** will be OFF due to the bias voltages on their respective bases. On the other hand transistor **513** will be ON. As a result the up bus **109** will be connected directly to plus 18 volts through the low collector to emitter resistance of transistor **513** in its ON condition, clamping the up bus **109** to positive 18 volts. At the same time the down bus **110** will be at 0 volt.

When a positive error voltage appears on the lead **505** the transistor **511** goes ON, drawing current from the base of the transistor **511**, so that the transistor **512** will go ON. The resistor **517** limits the current through the transistor **511** to a safe value. The current through the resistor **516** which serves to bias the transistor **512** OFF when the transistor **511** is OFF can be neglected when both transistors are ON. As a result diode **518** is biased in the forward direction and the base of transistor **513** rises above the positive 18 volts of its emitter causing the transistor **513** to go to the OFF condition. The up bus **109** will therefore drop to 0 volt while the down bus **110** will rise to a positive 18 volts supplied through the collector emitter path of transistor **512**.

FIG. 6 is a schematic circuit diagram of a circuit that may be used for the encoder **600**. This unit is essentially an analog-to-digital converter and other circuits well known in the art could alternately be used. In essence it comprises a pulse generator including two transistors **601** and **602** connected as a conventional free-running multivibrator. This generator is normally biased OFF, but in response to an encoding command signal E from the timing generator applied to the terminal **603** and the joint presence on the input terminal **604** of an error voltage $|e|$, of at least the minimum value for which the regulator is adjusted to compensate, the pulse generator is turned ON. When the pulse generator operates it delivers an array of pulses of a frequency of 100 kilocycles per second through the emitter-follower transistor **605** to an output terminal **606**. This array of pulses is supplied to the counter as described in connection with FIG. 1. At the same time that the pulse generator starts, the capacitor **607** begins to charge with a constant current furnished by the transistor **608** and its associated feedback circuit. When the voltage on the capacitor **607** reaches the magnitude of the error voltage $|e|$ (supplied through the emitter-follower transistor **609**) the comparison circuit including the transistor **610** will operate to stop the oscillator, thus terminating the train of pulses. In this way the number of pulses generated during any encoding period will be proportional to the error voltage for which correction is required.

We will now consider the operation of the circuit in more detail. Under normal conditions, that is, when the error voltage $|e|$ is 0 or lower than the minimum voltage to be compensated, transistor **610** will be ON due to the positive bias supplied to its base from the 16 volt source **611** through the potentiometer **612**. The use of this potentiometer makes it possible to set the value of the error voltage at which the first pulse appears, thus establishing the sensitivity of the regulator. With transistor **610** ON, current is drawn through its collector-emitter path and resistor **613**, bringing the base of the transistor **614** down to such a voltage that the transistor conducts and clamps the base of transistor **602** at positive 16 volts preventing the multivibrator from oscillating.

When the error voltage $|e|$ applied to the transistor **610** through the emitter-follower transistor **609** reaches such a value that transistor **610** is OFF, current ceases to flow through the resistor **613** and the base of transistor **614** reaches a value close to positive 18 volts. Transistor **614** is accordingly OFF, removing the positive voltage from the base of the transistor **602** and putting the multivibrator in a condition in which it can be started by the application of a positive voltage to the base of transistor **601**.

Assuming that the above conditions exist, the multivibrator **601**, **602** will be started by an encoding command signal E (a negative voltage step) applied from the terminal **603** to the base of transistor **615**. This causes the transistor **615** to conduct, applying a positive bias to the base of transistor **601** through the lead **616**. The multivibrator **601**, **602** accordingly starts oscillating, applying a train of pulses through the emitter-follower transistor **605** and the differentiating circuit **617** to the output terminal **606**.

At the same time the positive voltage developed on the lead **616** as a result of the ON condition of the transistor **615** causes the transistor **608** to be ON so that the capacitor **607** begins to charge. Due to the feedback connections for the transistor **608** the capacitor **607** charges with a constant current. As will be recalled, during this period transistor **610** is OFF as a result of the positive error voltage $|e|$ supplied to its emitter. When the voltage on capacitor **607** reaches the value of the error voltage $|e|$ transistor **610** is switched to the ON condition causing a drop in the voltage at the base of the transistor **614** which becomes ON, clamping the base of the transistor **602** to a positive voltage and stopping the oscillation of the multivibrator **601**, **602**. This results in the termination of the pulse train.

It will be observed that the operation of the multivibrator (**601**—**602**) is responsive to two separate controls. It will oscillate (be free-running) only when a positive voltage is applied to the base of the transistor **601** and no positive voltage is applied to the base of the transistor **602**. The application of the positive voltage to the transistor **601** is controlled by the encoding command pulse for the purpose of starting the oscillator. On the other hand the condition of the base of transistor **602** is controlled by the error voltage so that the multivibrator cannot be started until the error voltage exceeds the minimum value for regulation and will be stopped when the length of the train of pulses corresponds to the error voltage.

FIG. 7 is a block schematic diagram of the counter **700**. Basically it comprises four transistor flip-flop circuits **701**, **702**, **704**, and **708** corresponding to the binary stages 1, 2, 4, and 8 respectively. These flip-flop stages are interconnected through differentiating and inhibiting circuits to permit counting in either direction (up or down). Only the interconnections between stages **701** and **702** will be described in detail since the others are identical in operation. The counter is operated by the train of 100 kilocycle pulses supplied to the input terminal **706** from the encoder. Assuming that the counter starts counting up from the "0" position for all stages, that is, with all flip-flops in the OFF condition, the first pulse then moves the stage **701** into the "1" position. The second pulse moves it back to the "0" position, and for counting up a carry pulse is transmitted through the differentiating capacitor **710** and the inhibiting circuit **711** to the second stage **702**. Under this condition the count down bus **110** will be at 0 potential so that the carry pulse is permitted to reach the up carry lead **712**. In counting down the pulses are transferred from one stage to the next when the flip-flop moves from the "0" to the "1" condition, the down carry signal will be transmitted from stage **701** to stage **702** through the differentiating capacitor **717** and inhibit circuit **718**. In this case the up bus **109** will be at 0 voltage, permitting the pulse to reach the down carry lead **713** while the down count bus **110** will be at positive 18 volts inhibiting any pulse from reaching the up carry lead **712**.

When the regulation required to hold the output voltage at its standard value is greater than the range of the regulator as determined by the auxiliary transformer, a spill-over circuit will hold the regulation at the maximum value. If this spill-over control were not provided a condition requiring a regulation slightly beyond the limit of the circuit would produce an entirely erroneous control. Thus, for a nominal operating binary counter a condition of 16 pulses representing an error of 16 percent when the limit of the regulator is 15 percent, would cause the counter to recycle to a value of 1 percent. This would produce an entirely erroneous regulation. With a spill-over circuit the counter is set ultimately into its maximum position for either an up or a down count. For the 16 percent error the counter will be set ultimately in the 15 percent position giving the maximum correction.

The spill-over circuit comprises a delay circuit **721** connected to the up and down carry busses **722** and **723** respectively of the final stage **708** of the counter. This delay circuit may conveniently comprise a transistor monostable flip-flop. The purpose of the delay is to assure that the count is complete before the carry signal is passed on to the spill-over busses. The outputs of the delay circuit **721** are fed through two inhibitor circuits **724** and **725**; the output of the inhibitor circuit **724** is connected to the spill-over up bus **726** and that of the inhibitor **725** to the spill-over down bus **727**. When counting up the positive 18 volts on the count up bus **109** actuate inhibitor **725** to prevent any signal from reaching the spill-over down bus **727**. The spill-over up bus **726** is connected to the "1" sides of each of the counter flip-flops to set each of the flip-flops into their "1" positions. For counting down similar connections cause each of the flip-flops to be set into its "0" position.

FIG. 8 shows the circuit of a typical counter stage, for example stage **701**. This comprises a conventional flip-flop including the transistors **800** and **801**; the incoming train of pulses to be counted is supplied from the input terminal **802** to the bases of the flip-flop transistors through the diodes **803** and **804** respectively. (For subsequent stages there will be two inputs, an up carry and a down carry so that additional diodes **805** and **806** will be required as shown in the dotted line circuit.)

It is assumed for the purpose of this explanation that the "0" condition of the counter stage is that in which the transistor **800** is ON and that the "1" condition is that in which the transistor **801** is ON. Transistor **807** has its base connected to the collector of transistor **800** and has the control windings **203** and **204** of the switch **105** connected to its collector. Thus, when the flip-flop is in the "0" condition, current will be supplied to the windings **203** and **204** to hold the switch **105** closed, short-circuiting the secondary of the transformer **101**. Diode **808** is connected in series with the windings **203** and **204** to prevent positive pulses in the magnetic amplifiers from interfering with the counter operation. A transistor **809** is similarly connected between the collector of transistor **801** and the windings **213** and **214** to control the operation of switch **106**.

Carry signals are transmitted to the transistor amplifiers **810** and **811**. Thus when the transistor **801** shifts from the ON to the OFF condition the potential of its collector carries the base of the transistor **810** to a positive voltage so that transistor **810** goes OFF, producing a negative pulse through the differentiating capacitor **816** on the up carry lead **812**. For counting up the carry down lead **813** will be clamped to positive 18 volts by the voltage from the inverter **500** on the count up lead **109**.

For counting down a negative pulse will be applied to the carry down lead **813** through the transistor **811** in a similar fashion. Under these conditions the carry up lead **812** will be clamped to positive 18 volts by the voltage on the count down bus **110**.

The spill-over up bus **826** and the spill-over down bus **827** are connected to the transistors **801** and **800** respectively to set the flip-flop in the required "1" or "0" condition, as was described in connection with FIG. 7.

What is claimed is:

1. In a regulator for interconnecting a source of alternating voltage and a load circuit, a plurality of transformers the voltage ratios of which are different from each other and are related according to a predetermined plan, said transformers having their secondary windings connected in series between said source and said load circuit, individual switching means normally short-circuiting the primary windings of each of said transformers, a reference source proportional to the voltage required across said load, means for comparing the output voltage across said load with said reference source to produce an error signal, and means responsive to said error signal in accordance with said plan to selectively open-circuit

said primary windings of said transformers and connect them to receive current from said source of alternating voltage.

2. A voltage regulator for association with a source of voltage and a load circuit comprising a plurality of auxiliary sources of voltages of amplitudes differing from each other and corresponding respectively to the denominational orders of a numerical system, means for producing an error signal corresponding to the variation of voltage across said load circuit from a predetermined value, and means responsive to said error signal for actively associating with said source and said load circuit those of said auxiliary sources corresponding to said error signal in said numerical system, in which said auxiliary sources of voltages comprise transformers having their secondary windings connected in series with each other between said source and said load circuit and having their primary windings normally short-circuited and in which the means responsive to said error signal includes switching means associated with each of said transformers for opening the short-circuit connections of the selected primary windings and for connecting said selected primary windings to receive current from said source.

3. A voltage regulator comprising an alternating current source of supply, a load circuit, a plurality of transformers adapted to be energized from said source of supply to produce across their secondary windings voltages lower than that required across said load circuit and related to each other in accordance with the denominational orders of a binary numerical system, a circuit interconnecting said source of supply and said load and including said secondary windings for supplementing the voltage from said source in maintaining the voltage supplied to said load at a predetermined value, means for producing a quantized error signal proportional to the departure of the voltage across said load from said predetermined value, and means responsive to said error signal for rendering operative those of said secondary windings required to restore the voltage across said load to substantially said predetermined value.

4. A voltage regulator comprising an alternating current source of supply, a load circuit, a plurality of transformers adapted to be energized from said source of supply to produce across their secondary windings voltages lower than a predetermined value required across said load circuit and related to each other in accordance with the denominational orders of a binary numerical system, means for periodically producing a train of pulses of number proportional to the departure of the voltage across said load from said predetermined value, a multistage binary counter, connections for supplying said train of pulses to said counter, and switching means controlled by each stage of said counter for operatively associating the respective ones of said secondary windings with said load circuit to restore the voltage across said load circuit to substantially said predetermined value.

5. A voltage regulator for associating with a source of voltage and a load circuit comprising a plurality of transformers adapted to be energized from said source of supply and producing voltages differing from each other and related by the respective denominational orders of a binary numerical system, switching means for each of said transformers for associating the primary winding with said source of supply so that the voltage across the secondary winding supplements the voltage from said source in maintaining the voltage supplied to said load circuit at a predetermined value, means for periodically producing a train of pulses of number proportional to the departure of the voltage across said load from said predetermined value, means for producing a control signal determined by the direction of departure of the voltage across said load from said predetermined value, a reversible multistage binary counter means for controlling the direction of operation of said counter in response to said signal, connections for supplying said train of pulses to said counter for operating the same, and means interconnecting each stage of said counter with the switching means associated with the respective transformers for controlling the operation thereof.

6. A voltage regulator in accordance with claim 5 including means responsive to a train of pulses of number beyond the capacity of said counter for maintaining the counter in its maximum or minimum condition depending upon the direction of counting.

7. A voltage regulator comprising an alternating current source of supply, a load circuit, a plurality of transformers each having a primary winding and a secondary winding, said transformers being so proportioned that the voltages produced across their secondary windings are related to each other in proportion to the powers of 2, said secondary windings being connected in series with each other to supplement the voltage supplied from said source to said load, switching means associated with each primary winding for alternatively short-circuiting the winding or connecting it to receive current from said source, means for periodically producing an error voltage proportional to the departure of the voltage across said load from a predetermined value, means responsive to said error voltage for producing a train of pulses of number proportional to said error voltage, a multistage binary counter, means responsive to each stage of said counter for controlling the switching means associated with that one of said secondary windings producing a voltage proportional to the respective denominational order of the counter stage, and means for supplying said train of pulses to said counter for the operation thereof.

8. A voltage regulator comprising an alternating current source of supply, a load circuit, a plurality of transformers each having a primary winding and a secondary winding, said transformers being so proportioned that the voltages produced across their secondary windings are related to each other in proportion to the powers of 2, said secondary windings being connected in series with each other to supplement the voltage supplied from said source to said load, switching means associated with each primary winding for alternatively short-circuiting at the winding or connecting it to receive current from said source, means for producing an error voltage of absolute magnitude proportional to departure of the voltage across said load from a predetermined value and of sign dependent upon the direction of such departure, means for periodically producing a train of pulses proportional to the absolute value of said error voltage, a reversible multistage binary counter, means for controlling the direction of counting of said counter in accordance with the sign of said error voltage, means for applying said train of pulses to said counter for the operation thereof, and means responsive to the condition of the respective stages of said counter at the end of said count for controlling the switching means associated with that one of said secondary windings producing a voltage of value corresponding to the respective denominational order of the counter stage.

9. A regulator according to claim 8 including means responsive to a train of pulses of number greater than the capacity of said counter for maintaining said counter in the maximum or minimum position depending upon the direction of counting.

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