United States Patent

Goldstone

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[54] ANALOG FERRITE PHASE SHIFTER CONTROL CIRCUIT

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[52] **U.S. Cl.** .....**343/100 SA**, 343/854

[51] **Int. Cl.** **H01q 3/26**

[58] **Field of Search** .....343/100 SA, 854

[56] **References Cited**

UNITED STATES PATENTS

3,484,785	12/1969	Sheldon et al.	343/100 SA
3,582,953	6/1971	Martner	343/854

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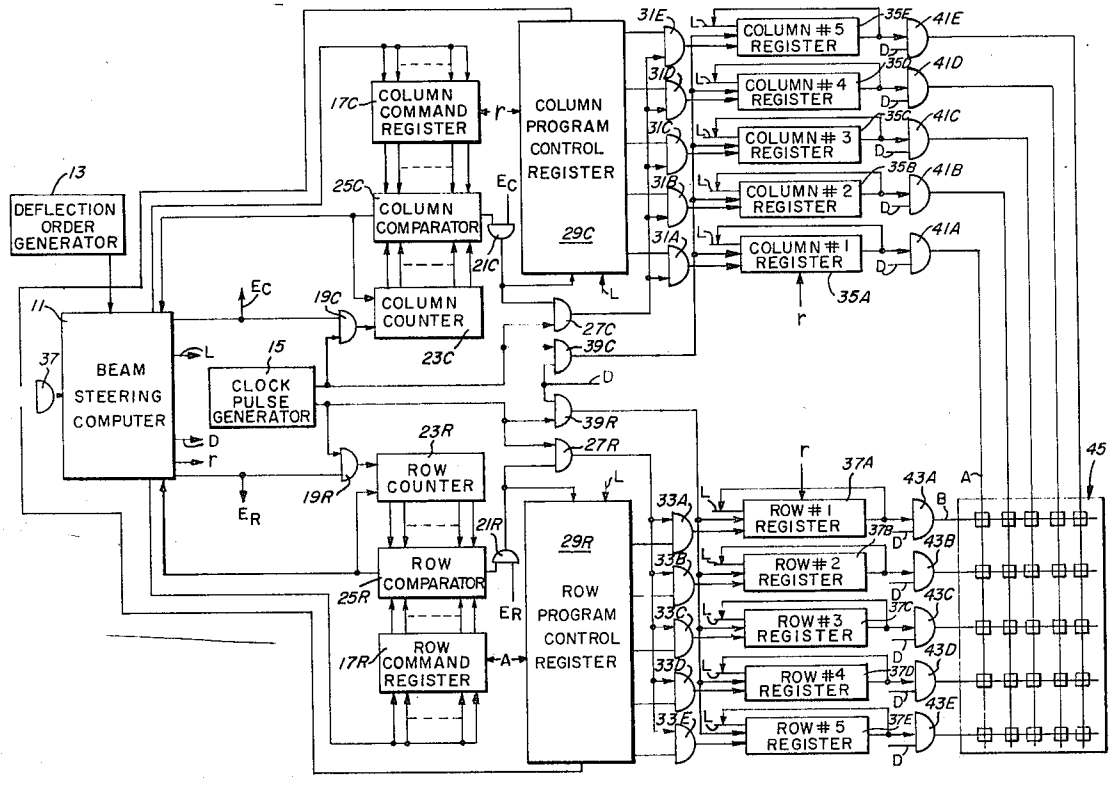
[57] **ABSTRACT**

A control circuit for analog ferrite phase shifters in an antenna array wherein such phase shifters are arranged in rows and columns. The circuit includes a recirculating shift register for each row, each such register repetitively producing a "start" current flow signal for the phase shifters in each row and a recirculating shift register for each column, each such register repetitively producing a "stop" current flow signal for the phase shifters in each column. The various recirculating shift registers are programmed so that the time between the "start" and the "stop" current flow signal to each one of the phase shifters results in the proper average current to accomplish collimation and deflection of the beam from the antenna array.

1 Claim, 2 Drawing Figures



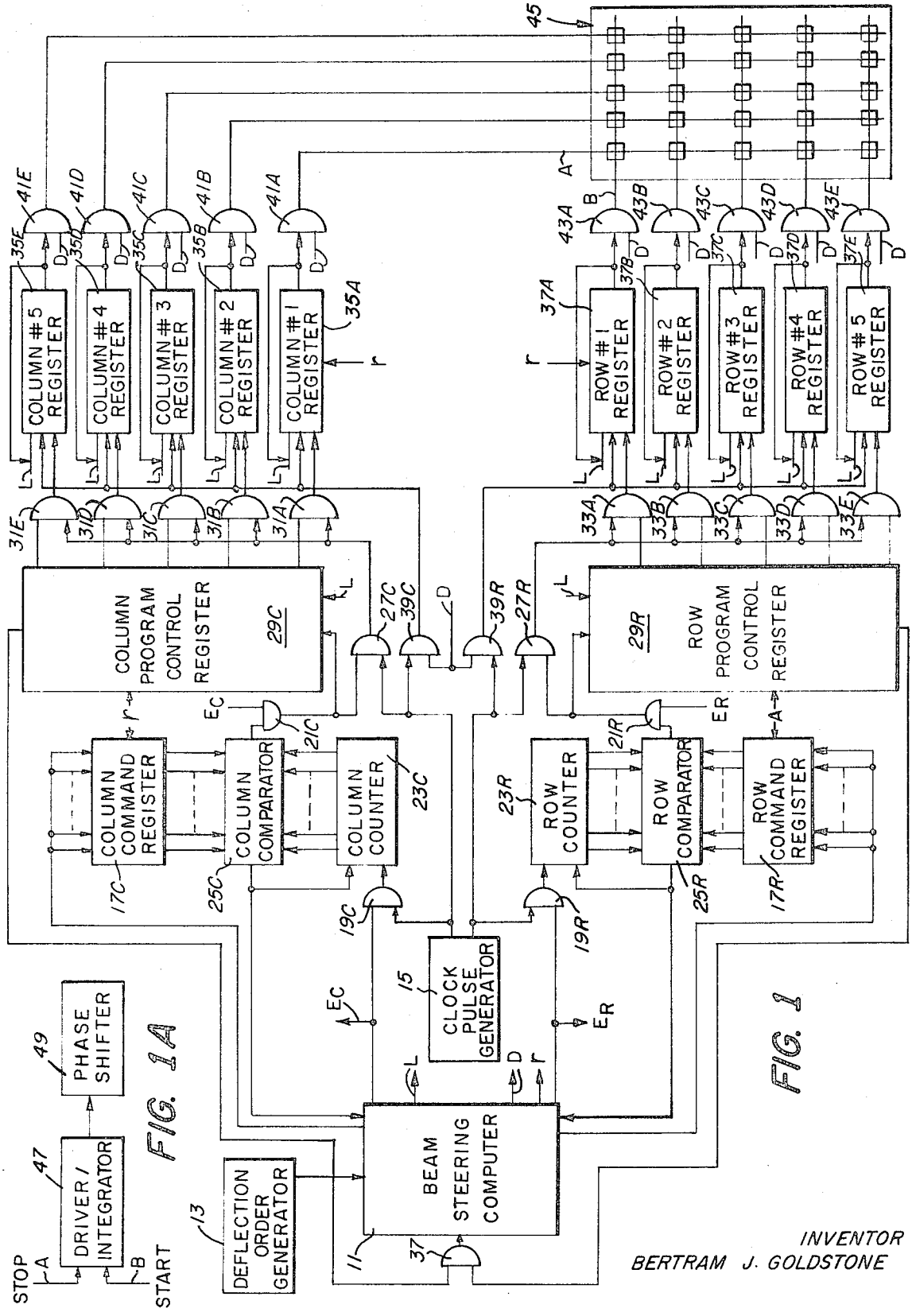


FIG. 1A

FIG. 1

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ANALOG FERRITE PHASE SHIFTER CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

This invention pertains generally to phased array antennas for radar systems and particularly to arrays of such type wherein ferrite phase shifters are used to collimate and direct electromagnetic energy in a directional beam.

It is known in the art that a matrix of analog ferrite phase shifters may be used to adjust the electrical length of the path of electromagnetic energy between a source, as a horn, and an array of radiating elements in order to deflect and propagate a beam of collimated electromagnetic energy. The phase shift imparted to the electromagnetic energy by each phase shifter is dependent on many factors, e.g. the desired deflection angle, the position of the phase shifter in the array and known variations in the response of the phase shifter and associated elements with changes in the operating environment. It is apparent, therefore, that the control circuitry for each phase shifter in an array should be as flexible as possible to obtain proper operation under changing conditions. It is also obvious that such control circuitry should be as simple and as dependable as possible to reduce the overall cost of manufacturing and operating any array.

It is known in the art that analog control signals for ferrite phase shifters in an array may be derived from digital control signals from a computer. Thus, it is known to dispose such phase shifters in a rectilinear matrix and, in response to so-called "row" and "column" command signals from a computer, control the average current (and the phase shift imparted to electromagnetic energy by each phase shifter) through the coil of each ferrite phase shifter. One exemplary way in which such control may be exercised is shown in U. S. Pat. No. 3,484,785 entitled "Beam-Steering Apparatus," Sheldon et al, which patent is assigned to the same assignee as the present application. According to the concepts of the referenced patent, binary counters are actuated in accordance with a computer program to start and stop current flowing through the coil of each ferrite phase shifter. In order to reduce the number of binary counters required in operation, the starting of current flow to the phase shifters in each row is controlled by a corresponding "row" binary counter and the stopping of current flow to the phase shifters in each column is controlled by a corresponding "column" counter. While such control circuitry is satisfactory, it has been found that the required binary counters are relatively complex. Further, in order that the starting and stopping of current flow to each phase shifter be properly accomplished, it is necessary to change the initial count of each row and column counter in accordance with command signals from a computer. The requisite circuitry to make such changes is also relatively complex.

SUMMARY OF THE INVENTION

Therefore, it is a primary object of this invention to provide improved row and column control signal circuitry for providing "start" and "stop" current flow signals to analog ferrite phase shifters in an antenna array.

Another object of this invention is to reduce the size and the complexity of the collimation and deflection circuitry required to form and direct a beam of electromagnetic energy from an antenna array.

These and other objects of this invention are attained by using a separate shift register for each row of an antenna array to produce a "start" signal for current to flow to each one of the analog phase shifters in each such row and a separate shift register for each column to produce a "stop" signal for the current flowing to each one of the phase shifters. Each one of the shift registers is programmed and connected to produce a control signal repetitively, the instant at which each such signal is produced being determined by the initial position of a single "one" in each shift register, the number of stages in each and the rate at which shift pulses are applied.

BRIEF DESCRIPTION OF THE DRAWING

For a more complete understanding of this invention, reference is now made to the following description of a preferred embodiment and to the accompanying drawings, in which:

FIG. 1 is a block diagram, somewhat simplified for clarity, illustrating the manner in which shift registers may be programmed and connected to provide properly timed control signals to each analog ferrite phase shifter associated with an antenna array; and,

FIG. 1A is a block diagram illustrating the connection of an exemplary one of the phase shifters to the shift registers.

It should be noted before proceeding to the description of the drawings that the particular manner in which radio frequency energy is generated and applied to an antenna array has not been illustrated, such detail being deemed to be of common knowledge to one skilled in the art. For the same reason, the details of the antenna array, except for a showing of the arrangement of analog ferrite phase shifters, has not been illustrated. Reference is made to U. S. Pat. No. 3,305,867 to Miccioli & Archer entitled "Antenna Array System" and to U. S. Pat. No. 3,484,785 to E. J. Sheldon et al entitled "Beam-Steering Apparatus" (both of which patents are assigned to the same assignee as this application) for such details of typical arrays.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 1, it may be seen that the circuit according to the invention is operated under the control of a beam steering computer **11**, a deflection order generator **13** to produce program control signals for such computer and a clock pulse generator **15**. These elements, while required for a proper understanding of this invention, are conventional and will not be described in any detail. Suffice it to say here that when a particular deflection order from the deflection order generator **13** (which element may, for example, be the tracking portion of the radar which is adapted to produce digital words indicating target azimuth and elevation angles), is passed to the beam steering computer **11**, that element, in combination with gated clock pulses from the clock pulse generator **15** to program and operate the disclosed circuit in a manner to be shown.

PROGRAMMING ROW & COLUMN REGISTERS

A reset pulse, r, from the beam steering computer **11** resets all registers to zero. A load pulse, L, is then fed to the first stage of all registers except a column command register **17C** and a row command register **17R**. When these preliminary operations are completed the column command register **17C** and the row command register **17R** are empty, i.e. contain all "zeroes," while each other register has a "one" in its first stage. The column command register **17C** and the row command register **17R** are then loaded from the beam steering computer **11** with the command signal for column No. **1** and row No. **1** of the array. Enable signals E_C, E_R are then impressed on AND gates **19C**, **21C**, **19R** and **21R**, thereby permitting clock pulses to pass from the clock pulse generator **15** to a column counter **23C** and a row counter **32R** (and also, in a manner to be described, to the shift terminals of the column No. **1** register and row No. **1** register). Each clock pulse, then, causes each one of such counters to count up one until the count of each is the same as its corresponding command register. When coincidence occurs, an output signal is produced by a column comparator **25C** and a row comparator **25R**. The output signal from each of such comparators is fed, via AND gates **21C**, **21R**, to AND gates **27C**, **27R** and to the shift terminals of column program control register **29C** and row program control register **29R**. AND gates **27C**, **27R**, which are normally enabled, are each inhibited by the output signal passing through AND gates **21C**, **21R**. The output signal from the column comparator **25C** is also passed back to the beam steering computer **11** to cause that element to inhibit AND

gates 19C, 21C. At the same time, column counter 23C is reset to zero. Similarly, the output signal of the row comparator 25R inhibits AND gates 19R, 21R and resets row counter 23R. It will be noted that, during the first period in which AND gates 27C, 27R pass clock pulses from the clock pulse generator 15, only a single one, AND gate 31A, of a group of AND gates 31A, 31B, 31C, 31D, 31E and a single one, AND gate 33A, of a group of AND gates 33A, 33B, 33C, 33D, 33E is enabled. The first groups of clock pulses are, therefore, impressed on the shift terminals of column No. 1 register 35A and of row No. 1 register 37A. The "one" in the first stage of each register is, as noted hereinbefore, shifted part way through the register, the amount of the shift being dependent on the number of clock pulses passed by AND gate 27C, 27R. The just described operations are repeated, the only difference being that AND gates 31B, 31C, 31D and 31E and AND gates 33B, 33C, 33D and 33E are enabled successively, to program each of the registers. Completion of programming is indicated to the beam steering computer 11 when "register filled " signals from both the row program control register 29R and the column program control register 29C are passed through an AND gate 37.

OPERATION OF ROW AND COLUMN REGISTERS

After the column and row registers 35A, 35B, 35C, 35D, 35E, 37A, 37B, 37D, 37E are programmed, the beam steering computer produces an enable deflection signal, D, which enables AND gates 39C, 39R, AND gates 41A, 41B, 41C, 41D, 41E and AND gates 43A, 43B, 43C, 43D, 43E. It may be seen, therefore, that clock pulses are passed through AND gates 39C, 39R to be impressed, simultaneously, on the shift terminals of all such column and row registers. The "one" in each such register is shifted to the last stage of each register, then returned to the first stage, as shown, to be shifted again and again as long as the AND gates 39C, 39R are enabled. Each time the "one" in any register is shifted into the last stage thereof a pulse signal also passes the associated AND gate 41A, 41B, 41C, 41D or 41E and AND gate 43A, 43B, 43C, 43D or 43E to the antenna array 45.

Referring now to FIG. 1A along with FIG. 1, it may be seen that, for example, line A from column No. 1 register 35A is connected through AND gate 41A, to an input terminal (not numbered) of each one of the drive/integrators 47 in a column and line B from row No. 1 register 37A is connected through AND gate 43A, to a second input terminal (not numbered) of each one of the driver/integrators 47 in a row. Each driver/integrator may be conventional, including a bistable multivibrator feeding an RC integrator through a diode. Such an arrangement is well known and will not be further described. Suffice it to say that the average current out of such a circuit is proportional to the duty cycle of the signal out of the bistable multivibrator; such cycle, in turn, is dependent upon the spacing between "start" and "stop" pulses on lines A and B and the time between successive "start" (or "stop") pulses. In other words, the duty cycle of the signal out of the bistable multivibrator is dependent upon the initial position of the "one" in each register, the number of stages in each register and the clock pulse rate. To complete the circuit, the integrator is connected to the current coil (not shown) of an analog ferrite phase shifter 49. That element is, therefore, actuated to shift the phase of electromagnetic energy passing therethrough by an amount related to the value of the average current.

Having described one embodiment of the invention, it will now be apparent to one of skill in the art that changes may be made without departing from the inventive concepts. For example, it is apparent that the programming of the various registers need not be controlled by separate row and column circuitry. Further, it is apparent that the row and column registers may be duplicated to permit programming of one set to be going on while the other is operating to collimate and deflect a beam. Still further, it is apparent that, because of the inductance of the coil in each analog ferrite phase shifter, each such shifter will integrate the control signal applied thereto. Therefore, the separate integrating circuit need not be used. It is felt, therefore, that this invention should not be restricted to its disclosed embodiment, but rather should be limited only by the spirit and scope of the appended claims.

What is claimed is:

1. In a control circuit for repetitively actuating and deactuating, in response to the repetitive occurrence of binary signals, each one of a plurality of electric current switching means, each one thereof being in circuit with a different one of a like plurality of analog ferrite phase shifters, such switching means and phase shifters being arranged in rows and columns corresponding to the radiating elements of an antenna array, the improvement comprising:

a. a first plurality of recirculating shift registers, the number thereof being equal to the number of rows of electric current switching means;

b. a second plurality of recirculating shift registers, the number thereof being equal to the number of columns of electric current switching means;

c. means for connecting the output stage of a different one of the recirculating shift registers in the first plurality thereof to the actuating terminals of the electric current switching means in each different row thereof and for connecting the output stage of a different one of the recirculating shift registers in the second plurality thereof to the deactuating terminals of the electric current switching means in each column thereof;

d. programming means for initially shifting a binary "one" from the input stage of each recirculating shift register to an intermediate stage thereof, the particular intermediate stage in each such register to which the binary "one" is shifted being varied to change the time of actuation and deactuation of each one of the electric switch means; and,

e. clocking means to shift the binary "one" in each recirculating shift register from its initial intermediate stage to the last stage and to recirculate repetitively such binary "one".

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