(12) UK Patent Application (19) GB (11) 2 362 263 (13) A

(43) Date of A Publication 14.11.2001

(21) Application No 0011556.8

(22) Date of Filing 12.05.2000

(71) Applicant(s)
Juses Chao
2Fl,No,3 Alley 39,Lane 64, Sec 1, Peihsin Road, Hsintien City, Taipei Hsien, Taiwan

(72) Inventor(s)
Juses Chao

(74) Agent and/or Address for Service
Langner Parry
High Holborn House, 52-54 High Holborn, LONDON, WC1V 6RR, United Kingdom

(51) INT CL[7]
H01L 21/20 21/203 21/205 33/00

(52) UK CL (Edition S)
H1K KLDBX K1BC K1EA K1EB K2R3A K2S1C K2S1D K2S1E K2S10 K2S16 K2S18 K2S19 K2S20 K2S21 K2S23 K2S27 K2S3A K2S3B K2S3D K2S3E K2S5 K3P2C K3P2D K3P2Y K3P5 K3P8 K9C2 K9C3 K9D2 K9E K9M1 K9N2 K9N3 K9P3 K9S

(56) Documents Cited
EP 0996173 A2 **WO 99/59195 A1** **WO 92/16966 A1** **DE 019855476 A1** **US 6146916 A** **US 5863811 A** **US 4561916 A**

(58) Field of Search
UK CL (Edition S) **H1K KLDBA KLDBB KLDBM KLDBP KLDBT KLDBX**
INT CL[7] **H01L**
ONLINE: WPI, EPODOC, JAPIO

(54) Abstract Title

Amorphous and polycrystalline growth of gallium nitride-based semiconductors

(57) A method of growing an amorphous or polycrystalline semiconductor involves vapour growth of a first amorphous or polycrystalline $In_xAl_yGa_{(1-x-y)}N$ layer (100) (where $0\leq(x,y)\leq1$, and $x+y\leq1$) of thickness up to 10 μm at a temperature between 180 and 1100°C, and vapour growth of a second amorphous or polycrystalline $In_xAl_yGa_{(1-x-y)}N$ layer (102) of thickness up to 10 μm at a temperature between 800 and 1200°C over the first amorphous or polycrystalline $In_xAl_yGa_{(1-x-y)}N$ layer (100). A third amorphous or polycrystalline $In_xAl_yGa_{(1-x-y)}N$ layer (200) may be grown over layer (102) at a temperature lower than the growth temperature of layer (102), and fourth amorphous or polycrystalline $In_xAl_yGa_{(1-x-y)}N$ layer (202) may be grown at a temperature higher than the growth temperature of layer (200). The substrate (10) may be sapphire, GaAs, GaN, Si or SiC, and the $In_xAl_yGa_{(1-x-y)}N$ layers may be p-type or n-type doped.

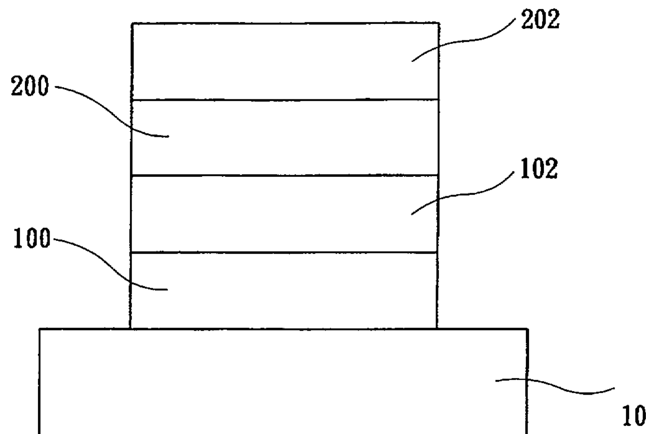

FIG. 2

GB 2 362 263 A

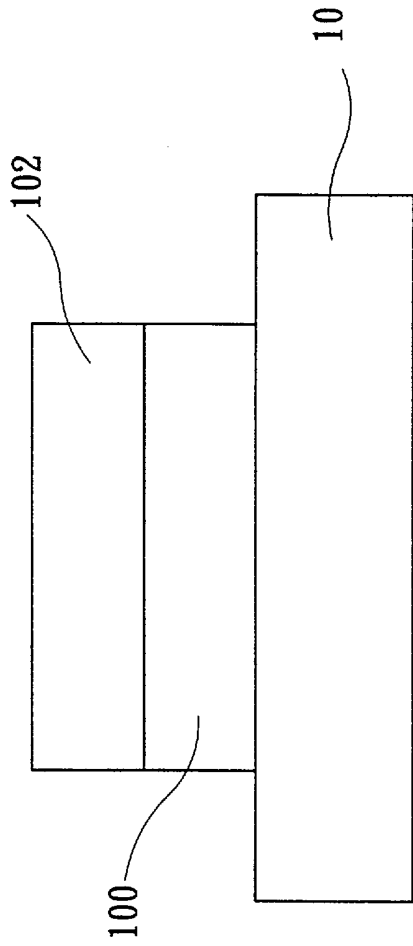

FIG. 1

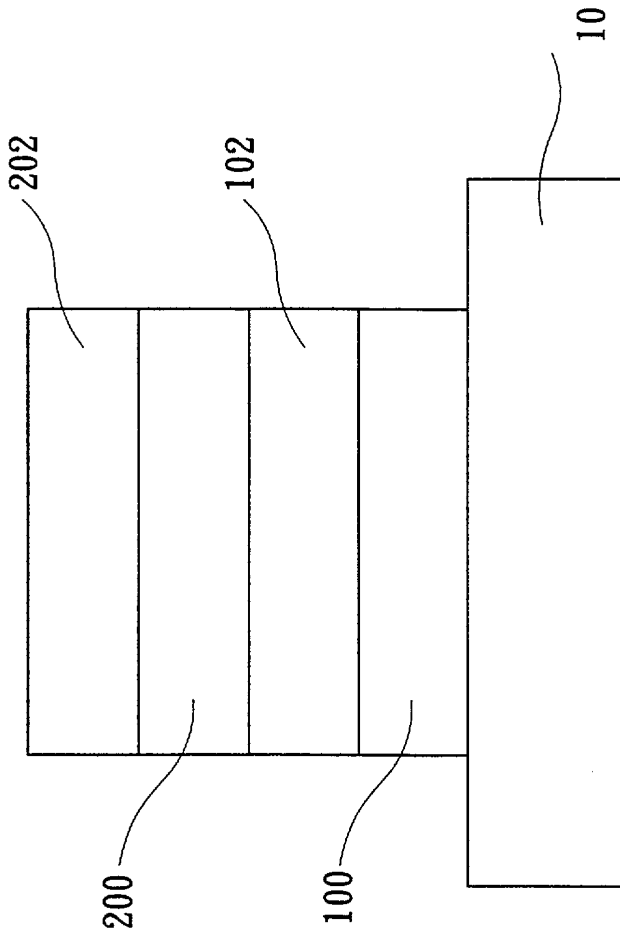

FIG. 2

2362263

AMORPHOUS AND POLYCRYSTALLINE GROWING METHOD FOR GALLIUM NITRIDE BASED COMPOUND SEMICONDUCTOR

Field of the invention

The present invention relates to an amorphous and/or polycrystalline
5 growing method, especially to an amorphous or polycrystalline growing method for gallium nitride based compound semiconductor

Background of the invention

The compound semiconductor devices had been found useful application for display and communication products etc. More particularly, the GaN based
10 compound semiconductors have received much attention because of the blue light emitting ability and its high efficient photon emitting function. The GaN based compound semiconductor is direct band-gap materials with high efficient energy-transferring rate and has wide band-gap distribution.

US Pat, NO. 5,563,422 has proposed a manufacturing method of GaN
15 based compound semiconductors, wherein crystalline GaN based compound semiconductors are specifically used to manufacture light emitting diodes. However, the crystalline GaN based compound semiconductors have the problems of high cost and low yield.

Therefore, it is the object of the present invention to provide a
20 manufacturing method of GaN based compound semiconductors with lower cost and higher yield.

To achieve the above object, the manufacturing method of GaN based compound semiconductors according to the present invention comprises the following steps:

(a) vapor-growing a first amorphous and/or polycrystalline compound semiconductor layer over a substrate by the formation $In_xAl_yGa_{(1-x-y)}N$ ($0 \leq (x,y) \leq 1.0000$, and $(x+y) \leq 1.0000$), at a thickness of 0.0001-10.00um, and at a first growing temperature between 180-1100℃;

5 (b) vapor-growing a first additional amorphous and/or polycrystalline compound semiconductor layer over said first compound semiconductor layer by the same formation, but with or without same parameter, at a thickness of 0.0001-10.00um, and at a second growing temperature between 800-1200℃;

Moreover, the manufacturing method of GaN based compound
10 semiconductors according to the present invention can further comprises the following steps:

(c) vapor-growing a second amorphous and/or polycrystalline compound semiconductor layer over said first additional compound semiconductor layer by the same formation, but at a third growing temperature lower than said
15 second growing temperature;

(d) vapor-growing a second additional amorphous and/or polycrystalline compound semiconductor layer over said second compound semiconductor layer by the same formation, but at a fourth growing temperature higher than said third growing temperature.

20 The various objects and advantages of the present invention will be more readily understood from the following detailed description when read in conjunction with the appended drawing, in which:

Brief description of drawing:

Fig. 1 is a sectional view of the compound semiconductor device

manufactured according to the first preferred embodiment of the present invention;

Fig. 2 is a sectional view of the compound semiconductor device manufactured according to the second preferred embodiment of the present invention.

Detail description of preferred embodiment

The present invention is intended to provide an amorphous and polycrystalline growing method for gallium nitride based compound semiconductor. The compound semiconductor device manufactured according to the first preferred embodiment of the present invention is shown in Fig. 1.

Firstly, the method vapor-grows a first amorphous and/or polycrystalline compound semiconductor layer 100 over a substrate 10, by the formation $In_xAl_yGa_{(1-x-y)}N$ ($0.0000 \leq (x,y) \leq 1.0000$, and $(x+y) \leq 1.0000$), at a thickness of 0.0001-10.00um, and at a first growing temperature between 180-1100℃. The substrate 10 can be one of the sapphire, GaN, Si, SiC or GaAs.

Afterward, the methods vapor-grows a first additional amorphous and/or polycrystalline compound semiconductor layer 102 over the first compound semiconductor layer 100 by the same formation, but with or without same parameter, at a thickness of 0.0001-10.00um, and at a second growing temperature between 800-1200℃.

The first compound semiconductor layer 100 and the first additional compound semiconductor layer 102 can be doped with p- and/or n-type impurities with concentration 10^{14-22}EA/cm^3 to provide rectifier, LED or light detector devices. Moreover, the first compound semiconductor layer 100 and

the first additional compound semiconductor layer 102 can be doped with i-type impurities with concentration 10^{14-22}EA/cm^3 to provide resistivity-function element in high or low.

The p-type impurity is selected form the group consisting of Zinc, 5 Magnesium, Beryllium, Strontium, Barium and Cadmium. The n-type impurity is selected form the group consisting of Silicon, Germanium, Tin, Sulfur, Tellurium and Selenium. Moreover, heating, annealing, electron-beam shooting for temperature between 601℃ to 1200℃, and operation time between 1 to 50 minutes can be performed after above process.

10 The reaction gas contains ammonia or hydrazine, or ammonia-hydrazine combined trimethylaluminum and the reaction gas can further contain the single or combined gas from the trimethyl gallium and/or triethyl gallium. Moreover, the reaction gas further contains at least one gas of diethyl-zinc, trimethyl-zinc, trimethyl-indium, and cyclopentadienyl –magnesium.

15 Fig. 2 is a sectional view of the compound semiconductor device manufactured according to the second preferred embodiment of the present invention.

Firstly, the method vapor-grows a first amorphous and/or polycrystalline compound semiconductor layer 100 over a substrate 10 by the formation 20 $In_xAl_yGa_{(1-x-y)}N$ ($0.0000 \leq (x,y) \leq 1.0000$, and $(x+y) \leq 1.0000$), at a thickness of 0.0001-10.00um, and at a first growing temperature between 180-1100℃. The substrate 10 sapphire, GaN, Si, SiC or GaAs.

Afterward, the methods vapor-grows a first additional amorphous and/or polycrystalline compound semiconductor layer 102 over the first compound

semiconductor layer 100 by the same formation, but with or without same parameter, at a thickness of 0.0001-10.00um, and at a second growing temperature between 800-1200℃.

Afterward, the method vapor-grows a second amorphous and/or polycrystalline compound semiconductor layer 200 over the first additional compound semiconductor layer 102 by the same formation, but at a third growing temperature lower than said second growing temperature.

Afterward, the method vapor-grows a second additional amorphous and/or polycrystalline compound semiconductor layer 202 over the second compound semiconductor layer 200 by the same formation, but at a fourth growing temperature higher than said third growing temperature.

The first compound semiconductor layer 100 and the first additional compound semiconductor layer 102; the second compound semiconductor layer 200 and the second additional compound semiconductor layer 202 can be doped with i-, p- and/or n-type impurities with concentration 10^{14-22}EA/cm^3 to provide pin, P/N structure device or other devices.

The p-type impurity is selected form the group consisting of Zinc, Magnesium, Beryllium, Strontium, Barium and Cadmium. The n-type impurity is selected form the group consisting of Silicon, Germanium, Tin, Sulfur, Tellurium and Selenium. Moreover, heating, annealing, electron-beam shooting for temperature between 601℃ to 1200℃, and operation time between 1 to 50 minutes can be performed after above process.

The reaction gas contains ammonia or hydrazine, or ammonia-hydrazine combined trimethylaluminum and the reaction gas can further contain the

single or combined gas from the trimethyl gallium and/or triethyl gallium. Moreover, the reaction gas further contains at least one gas of diethyl-zinc, trimethyl-zinc, trimethyl-indium, and cyclopentadienyl –magnesium.

The compound semiconductor layer can be applied together or
5 individually in homostructure, heterostructure, or double heterostructure, e.g., the quantum well/multi- quantum well or super-lattice, of different band-gap designs for different compound semiconductors.

Moreover, the semiconductor developing steps of vapor growing, spotting, epoxy attaching, deposition, electric platting and MBE can be incorporated into
10 above processes.

The following table explains the possible compositions of two-layer system shown in Fig. 1.

No	1st layer	2nd layer	junction type	possible devices
1	N	N	homo/hetero	diode
2	N	N	hetero	diode
3	N	I	hetero	diode
4	P	N	hetero	diode
5	P	P	homo/hetero	diode
6	P	I	hetero	diode
7	I	N	hetero	diode
8	I	P	hetero	diode
9	I	I	homo/hetero	resistor

* homo: homojunction; hetero: heterojunction

Moreover, the above table can be generalized to more complex compound
15 semiconductor layer system. For examples, the double heterojunction can be formed by system with more layers.

Although the present invention has been described with reference to the preferred embodiment thereof, it will be understood that the invention is not

limited to the details thereof. Various substitutions and modifications have
suggested in the foregoing description, and other will occur to those of ordinary
skill in the art. Therefore, all such substitutions and modifications are intended
to be embraced within the scope of the invention as defined in the appended
5 claims.

I claim

1. An amorphous and/or polycrystalline growing method for based compound semiconductor, comprising the following steps:

(a) vapor-growing a first amorphous and/or polycrystalline compound
5 semiconductor layer over a substrate by the formation $In_xAl_yGa_{(1-x-y)}N$ ($0.0000 \leq (x,y) \leq 1.0000$, and $(x+y) \leq 1.0000$), at a thickness of 0.0001-10.00um, and at a first growing temperature between 180-1100℃;

(b) vapor-growing a first additional amorphous and/or polycrystalline compound semiconductor layer over said first compound semiconductor layer
10 by the same formation, but with or without same parameter, at a thickness of 0.0001-10.00um, and at a second growing temperature between 800-1200℃;

2. The amorphous and/or polycrystalline growing method as in claim 1, further comprising the following steps:

(c) vapor-growing a second amorphous and/or polycrystalline compound
15 semiconductor layer over said first additional compound semiconductor layer by the same formation, but at a third growing temperature lower than said second growing temperature;

(d) vapor-growing a second additional amorphous and/or polycrystalline compound semiconductor layer over said second compound semiconductor
20 layer by the same formation, but at a fourth growing temperature higher than said third growing temperature.

3. The amorphous and/or polycrystalline growing method as in claim 1 or 2, further comprising a step of adding an i- and/or p- and/or n-type impurity into said compound semiconductor layer at a concentration between 10^{14-22}

EA/cm^3.

4. The amorphous and/or polycrystalline growing method as in claim 3, wherein the p-type impurity is selected form the group consisting of Zinc, Magnesium, Beryllium, Strontium, Barium and Cadmium.

5 5. The amorphous and/or polycrystalline growing method as in claim 3, wherein the n-type impurity is selected form the group consisting of Silicon, Germanium, Tin, Sulfur, Tellurium and Selenium.

6. The amorphous and/or polycrystalline growing method as in claim 3, further comprising step of heating, annealing, electron-beam shooting for

10 temperature between 601℃ to 1200℃, and operation time between 1 to 50 minutes.

7. The amorphous and/or polycrystalline growing method as in claim 1 or 2, wherein an ammonia or hydrazine, or ammonia-hydrazine combined trimethylaluminum reaction gas s used to develop said compound

15 semiconductor layer and the reaction gas contains the single or combined gas from the trimethyl gallium and/or triethyl gallium.

8. The amorphous and/or polycrystalline growing method as in claim 7, said reaction gas further contains at least one gas of diethyl-zinc, trimethyl-zinc, trimethyl-indium, and cyclopentadienyl –magnesium.

20 9. The amorphous and/or polycrystalline growing method as in claim 1 wherein the substrate can be sapphire, GaN, Si, SiC or GaAs.

10. The amorphous and/or polycrystalline growing method as in claim 1 or 2 wherein said compound semiconductor layer can be applied together or individually in homostructure, heterostructure, or double heterostructure, e.g.,

the quantum well/multi- quantum well or super-lattice, of different band-gap designs for different compound semiconductors.

11. The amorphous and/or polycrystalline growing method as in claim 1 or 2, further comprising semiconductor developing steps of vapor growing,

5 spotting, epoxy attaching, deposition, electric platting and MBE.

11

Application No: GB 0011556.8 **Examiner:** T P Marlow
Claims searched: 1 to 11 **Date of search:** 2 May 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H1K: (KLDBA) (KLDBB) (KLDBM) (KLDBP) (KLDBT) (KLDBX)

Int Cl (Ed.7): H01L

Other: ONLINE: WPI, EPODOC, JAPIO, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0996173 A2	XEROX CORPORATION - see especially buffer layers (24) and (26) in Fig. 2 and page 4 lines 31 to 38	1 to 11
X	WO 99/59195 A1	NATIONAL UNIVERSITY OF SINGAPORE - see especially amorphous or polycrystalline buffer layers in figures; final five lines on page 5 mention growth temperatures of layers	1 to 11
X	WO 92/16966 A1	BOSTON UNIVERSITY - see abstract mentioning two-step growth process of GaN layers, one at low temperature and one at high temperature	1 to 11
X, &	DE 19855476 A1	MURATA - see e.g. InGaN buffer (33) and InGaN layer (34) in Fig. 5	1 to 11
X, &	US 6146916	MURATA - see buffer layer between substrate and light-emitting layers in figures; col. 2 lines 56 to 65 mention the layer as amorphous and growth temperature	1 to 11

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
		E	Patent document published on or after, but with priority date earlier than, the filing date of this application.
&	Member of the same patent family		

12

INVESTOR IN PEOPLE

Application No: GB 0011556.8
Claims searched: 1 to 11

Examiner: T P Marlow
Date of search: 2 May 2001

Category	Identity of document and relevant passage		Relevant to claims
X	US 5863811	SONY - see buffer layers in figures, and col. 4 lines 1 to 32, especially lines 27 to 31 which mentions an amorphous or polycrystalline buffer	1 to 11
X	US 4561916	AGENCY OF INDUSTRIAL SCIENCE AND TECHNOLOGY - see polycrystalline film (2) in Fig. 1 and col. 2 lines 33 to 41 and col. 3 lines 6 to 18	1 to 11

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
		E	Patent document published on or after, but with priority date earlier than, the filing date of this application.
&	Member of the same patent family		