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(54) **Title**: INTERCONNECT DEVICE, ELECTRONIC DEVICE, AND METHOD OF USING A SELF-HEATABLE CONDUCTIVE PATH OF THE INTERCONNECT DEVICE

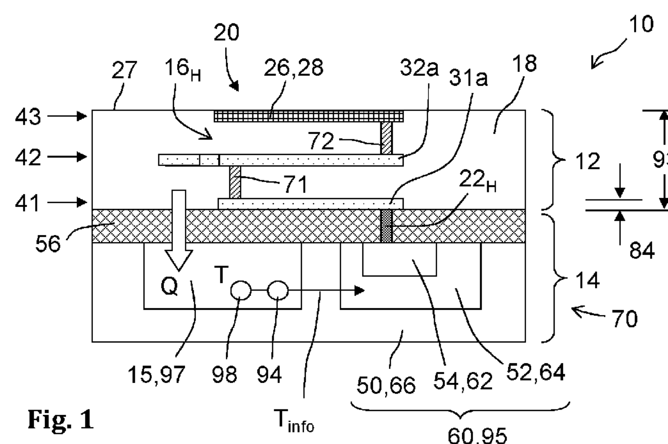


Fig. 1

(57) **Abstract**: An interconnect device (12) having terminal pads (26), a positioning area (13) for arranging a semiconductor element (15) at the positioning area (13), and a plurality of conductive paths (16), wherein at least a subset thereof is prepared for electrically connecting an arranged semiconductor element (15) to at least a subset of the terminal pads (26), wherein a self-heatable one (16_H) of the plurality of conductive paths (16) has a total resistance (R) of more than 90 Ohms. An electronic device (10) comprises said interconnect device (12) and a semiconductor element (15) arranged at the positioning area (13) and electrically connected by conductive paths (16) to at least a subset of the terminal pads (26). A self-heatable conductive path (16_H) of the interconnect device (12) described above may be used to increase temperature (T) of a semiconductor element (15) by more than 10° K by arranging and electrically connecting the interconnect device (12) to the semiconductor element (15) and by applying voltage (U) to the self-heatable conductive path (16) arranged in the interconnect device (12).

Interconnect Device, Electronic Device, and Method of Using a Self-heatable Conductive Path of the Interconnect Device

The claimed invention relates to an interconnect device having a plurality of conductive paths for electrically connecting an arranged semiconductor device to at least a subset of the terminal pads. The invention also relates to an electronic device comprising the inventive interconnect device and a semiconductor device. Further, the invention relates to a method of using a self-heatable conductive path of an interconnect device to increase temperature of a semiconductor device (use claim) and a heating method (operating process).

Yu in IBM TDB, December 1, 1982, www.IP.com, document **IPCOM 50868D**, "Self Heating Test Chip for Reliability Life Test" deals with accelerated reliability life tests for semiconductor products chips where chips are stressed at elevated temperatures. In the self-heating test chip design, groups of unused resistors are brought out in parallel to chip pads. These resistor chains serve as heating elements to heat the chips to a desired junction temperature during reliability life tests. The junction temperature can be monitored by an in situ measurement of a forward voltage drop of an on-chip temperature diode. This temperature-sensitive voltage drop can be fed back to a control circuit that can regulate a power level delivered to the resistor chains, thereby maintaining a precise junction temperature during life tests.

US 6,046,433 A (William Gross et al., Linear Technology) provides an integrated circuit die containing a metal heater resistor disposed around a periphery of a circuit whose temperature coefficient is to be measured, such as a voltage reference circuit that is included as part of a larger integrated circuit containing other circuitry. One end of the metal heater resistor is connected to a first bond pad, and the other end of the heater resistor connected to a second bond pad.

US 4,356,379 A (Jerald Graeme, Burr-Brown) refers to an apparatus for compensating thermal drift of temperature sensitive circuitry in a integrated circuit by heating the temperature sensitive circuitry by applying power to a heating element in the integrated circuit, testing the temperature sensitive circuitry, and trimming a thin film resistor in accordance with testing results. The heating element is an integrated resistor adjacent to or surrounding the temperature sensitive circuitry.

Reilly and Prosser in IBM TDB, November 1, 1971, www.IP.com, document **IPCOM 75763D** "Self Contained Chip Heater" discloses a reliability concern in the fabrication of FET transistors originating from the presence of excessive charge in the

gate oxide. To screen out potentially bad products, voltage and temperature stress is conventionally applied to the gate oxide to detect mobile ions causing gate oxide charge. High temperatures can be obtained on a semiconductor chip without the use of external heating sources, by placing a diffused resistor in close proximity to and surrounding the integrated circuit device to be temperature-stressed. The chip can then be heated locally by passing a current through the diffused resistor. The diffused resistor-heater can be calibrated with the aid of a thermocouple, whereby the relationship between temperature and power dissipated in the resistor can be obtained and used in the stressing of further standard product. Alternatively, either the diffused resistor PN junction itself, or a separate PN junction formed in a capacitor adjacent the device to be stressed and having an identical diffused resistor around it, can be employed to calibrate the heating effect produced by the diffused resistor heater. The forward current-voltage characteristic of a PN junction is a function of a temperature of the chip in which the junction is formed. Thus, the means for heating the chip and the means for calibrating the chip heater conveniently are formed integrally with the chip itself, using standard integrated circuit processing techniques.

An object of the invention is to provide an interconnect device and an electronic device, facilitating manipulation of temperature in a semiconductor device. The result should be cost-efficient in production and easy in control of temperature. Integrated circuits should be performed in 'chips'.

Disclosed and claimed is an interconnect device (claim 1) having terminal pads, a positioning area for arranging a semiconductor element at the positioning area, and a plurality of conductive paths, wherein at least a subset thereof is prepared for electrically connecting an arranged semiconductor element to at least a subset of the terminal pads, wherein a self-heatable one of the plurality of conductive paths has a total resistance of more than 90 Ohms (referred to as "Ω" - one or more - in the following).

The provision of a self-heatable conductive path of the interconnect device having a resistance within the specified range facilitates to use this self-heatable conductive path as an internal heating element of the interconnect device. Hence, a necessity for additional chip area to heat the semiconductor device can be avoided. Therefrom the benefit results that area (horizontal portion) can be increased that may be used for other purposes of the interconnect device and/or of the semiconductor device.

The semiconductor element may comprise a single semiconductor component like a power MOSFET or an electronic circuit comprising a small number of semiconductor components (such as a voltage regulation circuit) or an integrated circuit having high number of logic gates. The semiconductor device may be a single die, for example a flip

chip. The interconnect device may form a piece different to the piece of the die of the semiconductor element. Alternatively, the interconnect device may be formed by wafer processing in one piece with the die of the semiconductor element.

The claimed value that is given as a minimum value 90 Ω for the self-heatable conductive path represents that heat is provided in a place of a chip that is further down the surface. Tests and experiments have resulted that with metal layers that are stacked, several layers of heat production can be provided and a reasonable value that was achieved for one shape in one metallic layer is about 100 Ω ± 10%.

Using at least one metallic layer and its path to produce heat (and temperature) as claimed will thus result in a minimum value of resistance of at least 90Ω. In practice according to the results and tests, no more than two or three layers in downward direction should be used, which may result in an upper limit of the resistance of no more than 270Ω or preferably 450Ω.

Four to five layers at maximum, preferably only two metallic layers are used for providing heat into the depth of the chip (device).

The self-heatable one of the conductive paths may at least partially overlap the positioning area (claim 2). 'Overlapping' is interpreted as a projection of the conductive path images a ground plan of the conductive path at least partially onto the positioning area, when the projection is perpendicular to the positioning area. By arranging the self-heatable one of the conductive paths above the semiconductor element not only chip area can be saved, but also package area lateral to the positioning area can be saved.

At least one of the terminal pads may at least partially overlap the self-heatable one of the conductive paths (claim 3). 'Overlapping' is interpreted as a projection of the terminal pad images a ground plan of the terminal pad at least partially onto the conductive path, when the projection is perpendicular to a top surface of the terminal pad. By arranging the self-heatable one of the conductive paths below a terminal pad the self-heatable one of the conductive paths may be located where it cannot interfere with other portions of the interconnection device. Preferably, the self-heatable one of the conductive paths may be positioned below a terminal pad located at a periphery of the interconnection device.

The self-heatable one of the conductive paths may be arranged exclusively outside any semiconductor substrate arranged within the positioning area for arranging a semiconductor element therein (claim 4). By arranging the self-heatable one of the conductive paths exclusively outside any semiconductor substrate valuable positioning area can be reserved for interconnecting one or more semiconductor elements to terminal pads.

In particular cases, the self-heatable conductive path may have a total resistance of more than 180Ω and/or less than 450Ω (claim 5).

A specific electrical resistance (resistivity) of the first conductive heating layer of the interconnect device may for a different conductive material be at least n times as high as a specific electrical resistance of the terminal pad, wherein n is 2, in particular 4 or 8, especially preferred 16 (claim 6). Thereby, manufacturing of space-efficient heating elements having a sufficient high resistance value is facilitated, but using a different material than in the top pad.

The self-heatable conductive path may comprise at least one terminal pad which is at least partially located outside the positioning area and is accessible at a surface of the interconnect device (claim 7). Thereby, a heating current can be led from a separate heating current source to the interconnect device. Even, if the semiconductor device comprised a driver circuit for controlling the heating current, the heating current of only one heating current feed line needs to be led through the semiconductor device, wherein the corresponding return line for the heating current may be led directly to the terminal pad without any detour through the semiconductor device.

A second via may electrically connect a self-heatable portion of the self-heatable conductive path to a terminal pad (claim 8). Thereby, the self-heatable portion can be connected cost-efficiently by a standard process to a terminal pad.

The self-heatable conductive path may comprise at least one contact for connecting the self-heatable conductive path to the semiconductor device (claim 9). Thereby, an electrical connection for heating current control by the semiconductor device can be facilitated.

The interconnect device may comprise a first interconnection layer and a second interconnection layer, wherein said self-heatable conductive path comprises a first self-heatable portion in the first interconnection layer and a second self-heatable portion in the second interconnection layer, and at least one first via electrically connecting the first self-heatable portion of the self-heatable conductive path to the second self-heatable portion of the self-heatable conductive path (claim 10). By this measure, a standard structure of pairs each having an interconnection layer and a via (providing connection between interconnection layers) can be employed. The design of a heating element extending over more than one interconnection layer allows non-destructive generation of high thermal output within the interconnect device. Further, the design of a heating element extending over more than one interconnection layer allows for adjusting a vertical temperature profile in the interconnect device.

A self-heatable portion of the self-heatable conductive path may have at least partially one of a meander structure and a spiral structure (claim 11). This measure helps to provide a heating element having a space-saving build and a sufficient high value of resistance.

A filling material arranged between the conductive paths of the interconnect device may be predominantly made of at least one of following materials: oxide, silicate, glass, fused silica, other ceramic material, resin, elastomer, semiconductor material, other insulating material (claim 12). Thereby, the interconnect device can be provided as a self-supporting structure with insulation between the conductive paths (that shall not be in electrically connected).

In order to achieve the object mentioned above, the electronic device may comprise one of the interconnect devices described above and a semiconductor element arranged at the positioning area and electrically connected by conductive paths to at least a subset of the terminal pads (claim 13). Thereby, a device can be provided capable to process information and/or electrical energy, while simultaneously being capable to perform a self-heating function.

A semiconductor device may comprise the semiconductor element, wherein the interconnect device is partially arranged on top of a surface area of the semiconductor device, wherein said surface area is different to the positioning area (claim 14). Thereby, a reliable build of the semiconductor device can be provided, which can be manufactured cost-efficiently.

At least one terminal pad at least partially located outside the positioning area may be accessible at a surface of the interconnect device which is facing away from the semiconductor element (claim 15). Thereby, a cost-efficient wafer production and bonding of the electronic device is facilitated.

The self-heatable conductive path may have an extension for distributing heat (claim 16). This may help to equalize a horizontal temperature profile in the interconnect device and/or in the semiconductor device. An additional or alternative benefit of a heat distribution function can be to transmit heat to a location in the interconnect device or in the semiconductor device where heat is required, but cannot be generated.

A semiconductor device may comprise the semiconductor element, wherein the semiconductor device comprises a heat controller prepared to control generation of heat in said self-heatable conductive path by using temperature information for controlling a heating current through said self-heatable conductive path (claim 17). The use of temperature information may help to decouple the adjustment of a temperature level (or

temperature profile) in the semiconductor device from environmental influences like ambient temperature.

The semiconductor device may comprise a temperature sensor for providing said temperature information to the heat controller (claim 18). The temperature information needed for the heat controller may be most significant if the temperature sensor is located in the semiconductor device.

The temperature sensor may comprise at least one of a diode and a bipolar transistor (claim 19). Thereby, the temperature sensor can be realized cost-efficiently using a standard manufacturing process.

A semiconductor device may comprise the semiconductor element, wherein the semiconductor device comprises a substrate, wherein a deep well is provided in the substrate, wherein a shallow well is deposited in the deep well, wherein the shallow well is oppositely doped compared with the deep well, and wherein the self-heatable conductive path is electrically connected to the shallow well (claim 20). Thereby, a cost-efficient manufacturing of a driver circuit for the heating current is facilitated. Here, the deep well is called deep well, because it is at least 1.1 times as deep, preferably at least 1.5 times or at least 2.0 times as deep, as the shallow well.

The electronic device may comprise a drive circuit for supplying the self-heatable conductive path with heating current, wherein the drive circuit is prepared to act as a constant current source or as a PTC thermistor sensing a temperature at an application location of heat generated by the self-heatable conductive path (claim 21). Thereby, an influence of operating conditions on a temperature at the application location of heat can be reduced.

In order to achieve the object mentioned above, a self-heatable conductive path of one of the interconnect devices described above may be used for increasing temperature of a semiconductor device by more than 10° K by arranging and electrically connecting the interconnect device to the semiconductor element and by applying a voltage to the self-heatable conductive path arranged in the interconnect device (claim 22).

Thereby, the heating function facilitates performing thermal tests of a semiconductor element. In addition or alternatively, the heating function can be employed for an at least partial compensation of environmental influences on temperature of the semiconductor element. Preferably, the conductive path can be used for increasing temperature of a semiconductor element by more than 30°K or by more than 50°K.

Preferred **embodiments** of the invention are now described with reference to the drawings. They are not limiting the claimed invention. They are covered by the claims and provide enabling disclosure.

Figure 1 schematically shows a vertical cross section of a first embodiment of an electronic device having a vertical three-dimensional heating structure.

Figure 2 schematically shows a horizontal cross section in the second interconnection layer 42 of the first embodiment.

Figure 3 shows an equivalent electrical circuit of the first and second embodiments.

Figure 4 schematically shows a vertical cross section of a second embodiment of an electronic device having a vertical three-dimensional heating structure.

Figure 5 schematically shows a horizontal cross section in the second interconnection layer 42 of the second embodiment.

The electronic device 10 of which a vertical cross section A-A is shown in **Figure 1** comprises an interconnect device 12 and a semiconductor device 14. The interconnect device 12 has a positioning area 13 for arranging a semiconductor element 15 at the positioning area 13.

The interconnect device 12 comprises conductive paths 16 and filling material 18 holding the conductive paths 16. The semiconductor device 14 comprises a semiconductor element 15. The semiconductor element 15 may comprise, for example, a single semiconductor component like a power MOSFET or an electronic circuit comprising a small number of semiconductor components like a voltage regulation circuit or an integrated circuit having high number of logic gates.

The semiconductor device 14 may be a single die, for example a flip chip. The interconnect device 12 may form a piece different to the piece of the die of the semiconductor element 15. Alternatively, the interconnect device 12 may be formed by wafer processing in one piece with the die of the semiconductor element 15. The interconnect device may be partially arranged on top of a surface area 17 of the semiconductor device 14, wherein the surface area 17 is different to the positioning area 13.

The conductive paths 16 are predominantly enclosed by the filling material 18 and provide a multilayer connection network 20 between contacts 22 on the semiconductor device 14 and terminal pads 26 (which may be bonding pads) on a side of the interconnect device 12 (surface 27) facing away from the semiconductor element 15.

The elements 22_H, 26, 31a, 32a, 71, 72 of a self-heatable one 16_H of all conductive paths 16 that are not shown apart from path 16_H are made of conductive material(s), for example of metal, metal alloy, or conductive semiconductor material, e.g. PolySi. The vias 71, 72 may be made of tungsten. The terminal pads 26 are typically made of metal or metal alloy. The filling material arranged between the conductive paths of the interconnect device may be predominantly made of at least one of following materials: oxide, silicate, glass, fused silica, other ceramic material, resin, elastomer, (insulating) semiconductor material, other insulating material.

In general, a majority of the conductive paths 16 (not shown in the drawings apart from path 16_H)are designed for providing electrical energy and signals to the semiconductor element 15 and to collect signals from a semiconductor element 15 (embedded in a semiconductor substrate 50). In addition, the interconnect device 12 has at least one self-heatable conductive path 16_H designed for converting electrical energy by ohmic loss into heat Q. Therefore, the self-heatable conductive path 16_H comprises a first meander 31a arranged in a first interconnection layer 41, a second meander 32a arranged in a second interconnection layer 42, and a top plate 28 (terminal pad) arranged in a top layer 43. The meanders 31a, 32a are made of conductive materials, for example of metal, metal alloy, or semiconductor material.

The semiconductor device 14 comprises a semiconductor substrate 50, a deep well 52 embedded in the semiconductor substrate 50, an oppositely doped shallow well 54 embedded in the deep well 52, and an insulating layer 56 on top of the shallow well 54 and the semiconductor substrate 50. The shallow well 54 may be a shallow p well implant, the deep well 52 may be an n well implant, and the substrate 50 may be a p substrate. The shallow well 54 may form an emitter 62 of a bipolar transistor 60. The deep well 52 may form a base 64 of the bipolar transistor 60, and the substrate 50 may form the collector 66 of the bipolar transistor 60. Analogously, the concept can be applied to an npn structure, as well.

Typically, the insulating layer 56 (belonging to the semiconductor device 14) is made of an oxide. An electric contact 22_H (belonging to the self-heatable conductive path 16_H) penetrates the insulating layer 56 for electrically connecting the first meander 31a to the shallow well 54. A first via 71 electrically connects the second meander 32a to the first meander 31a. A second via 72 electrically connects the top plate 28 to the second meander 32a.

The value R of the electrical resistance 80 of the self-heatable conductive path 16_H in **Figure 3** can be adjusted by selecting suitable widths 82, thicknesses 84, lengths 86, and specific electrical resistances ρ (resistivity) of conductive segments 88a and 88a' contributing to the total self-heatable conductive path 16_H.

In the first interconnection layer 41 and in the second interconnection layer 42, self-heatable portions of the self-heatable conductive path 16_H have the structure of a meander, to fit long conductive lines into the positioning area 13 as shown in **Figure 2**. Preferably, a subset or all of the interconnection layers 41, 42 has a uniform specific electrical resistance ρ (resistivity), for facilitating manufacturing the interconnect device 12.

Heat-conductive structures 91 can be specifically designed as a thermal distribution line or network 91 to direct or distribute heat Q. The heat-conductive structures 91 may be designed to distribute the heat Q laterally within same interconnection layers and/or vertically into the semiconductor element 15.

In each interconnection layer 41, one or more extensions of the self-heatable conductive path 16_H may extend beyond a periphery of the respective self-heatable conductive path 16_H (or even beyond a periphery of the interconnect device 12) for conducting heat Q (horizontally and/or vertically) from the self-heatable conductive path 16_H to any area of the electronic device 10, where additional heat Q is required. The use of such a thermal network 91, together with independent control of heating current I_H in each self-heatable conductive path 16_H allows for complex horizontal temperature profiles to be created across the semiconductor element 15. Each heat source 16_H can also be configured independently to create customized heat profiles across the semiconductor element 15. This can be performed by varying the resistance R_{31}, R_{32} of each path in each layer 41, 42, for example, by forming specific shapes of resistors 31, 32 in a stack of resistors 31, 32. Also, time-varying (or even position-varying) thermal profiles may be generated. Such features offer improved control options and improved stressing options.

Summarizing the interconnect device 12 used for connecting a semiconductor element 15 to a package, or to a building assembly, is designed such that the interconnect device 12 has at least one internal heating element 31, 32 forming an effective on-chip heating structure. Advantageously, such an internal heating element 31, 32 does not require additional chip area for heating the semiconductor element 15. With the proposed structure, the heating elements 31, 32 are thermally connected to the semiconductor element 15, but electrically isolated from the semiconductor element 15.

Each part 22_H, 31a, 32a, 71, 72, 88a, 88a', ... of the serial electrical circuit 80 as seen in Figure 3 acts as a converter of electric energy to heat Q. Typically, wherein the two

meanders 31, 32 having the highest resistance values of all parts 22_H, 31a, 32a, 71, 72, 88a, 88a', ... of the serial circuit 80 contribute strongest to the heat production. Hence, the contribution of heat production of each part 22_H, 31a, 32a, 71, 72, 88a, 88a', ... of the self-heatable conductive path 16_H can be adjusted by selecting suitable widths 82, thicknesses 84, lengths 86, and specific electrical resistance ρ (resistivity) of conductive segments 88a belonging to the self-heatable conductive path 16_H. By adjusting a distribution of a resistance R of the total self-heatable conductive path 16_H, the heat production can be distributed equally or unequally to the different interconnection layers 41, 42. This allows adjusting and controlling a vertical temperature profile. Preferably, a subset or all of the interconnection layers 41, 42 has a uniform specific electrical resistance ρ (resistivity).

For achieving the needed value of the resistance R, the self-heatable conductive path 16_H may be arranged into meander 31a, 32a, adapting at least one of length 82, width 84, and thickness 86 of the conductive segments 88a. For the same purpose, a self-heatable conductive path 16_H comprising one or more spirals 31b, 32b or other long structures may be used, as well, see **Figure 4**. Conductive segments 88b, 88b' and 88b" as well as others concatenated segments build the spiral shape 32b in layer 42. Similar in layer 41 with spiral shape 31b.

For example, a meander or spiral having a resistance of 150 Ohms may be 0.6 μm wide and 900 μm long. Another example of a meander (or of a spiral) having a resistance of 180Ωmay be 1 μm wide and 1800 μm long (comprising for example 1800 squares each providing 0.1 Ohm). For example, a meander 31a, 32a may comprise any number between 4, 8, 16, 32, or more than 32 direction-changes 89a. Correspondingly, a spiral 31b, 32b may comprise any number between 2, 4, 8, 16, or more than 16 windings 89b.

A further increase of the value of the resistance R on a same positioning area 13 can be achieved by stacking vertically self-heatable portions 31, 32 (general view of 31a,32a or 31b,32b) of the self-heatable conductive path 16_H, thus forming a vertically-stacked heating element 16_H. This may be considered as a three-dimensional heat source 16_H.

Thereby, a need of lateral heating elements can be avoided, and building space and/or chip area can be saved.

The minimum amount of components of the vertically-stacked heating element 16 may be one (resistive) conductive segment 88a or 88b in layer 41 and one via 72. One or more additional pairs of resistive layers and vias may be stacked for increasing the height 93 and the resistance R of the vertically-stacked self-heating conductive path 16_H. For example, in the embodiment of Figure 1 two layers 41, 42 are designed as meanders 31a, 32a, electrically interconnected in height by the first via 71.

A controlling element 60 for controlling the heating current I_H through the heating elements 31, 32 of at least one self-heatable conductive path 16_H may be located directly below the three-dimensional heat source 16_H. According to an advantageous embodiment, the controlling element 60 may be a bipolar device, e.g. a bipolar transistor. Preferably, the bipolar device 60 is a vertical bipolar device.

According to an advantageous embodiment, the self-heatable conductive path 16_H may be connected to an implanted shallow well 54 in the substrate 50. The shallow well 54 may be deposited in an oppositely doped deep well 52. The self-heatable conductive path 16_H is electrically connected to the implanted shallow well 54 in the substrate 50 by a contact 22_H.

A base to emitter voltage U_{BE} can be changed by controlling a voltage between the base 64 and the emitter 62. Thereby, the heating current I_H can be controlled directly, and the generated heat Q can be controlled indirectly by changing the base to emitter voltage U_{BE}. Analogously, the concept can be applied to an npn structure, as well.

As an advantageous option, the self-heatable conductive path 16_H is driven by a constant current source. Using a constant current source (instead of a constant voltage source) for supplying electrical energy P to the self-heatable conductive path 16_H can help to reduce undesired variations of heat generation (i.e. rate of conversion of electrical power P to heat Q). A bipolar transistor may be considered as a current source, wherein the emitter to collector current is controlled by the voltage between the base 64 and the emitter 62. Hence, a simple constant current source may be provided by keeping the voltage between the base 64 and the emitter 62 constant.

Alternatively, a PTC thermistor (i.e. resistor having a significant positive temperature coefficient) or an drive circuit 70 behaving like a PTC thermistor can be employed for driving the self-heatable conductive path 16_H. To provide (as a result) a resistance having positive temperature coefficient, the heating current I_H may be feed-back-controlled. For achieving this, analogue or digital temperature information T_{info} from an application location 97 of the heat Q may be employed to control the controlling element 60 affecting the heating current I_H. The analogue or digital temperature information T_{info} may be used to affect a voltage between the base 64 and the emitter 62, thereby controlling the heating current I_H flowing through the self-heatable conductive path 16_H. The temperature information T_{info} may be inferred from knowledge of how a test current across a PN junction 98 (e.g. of a bipolar device like a diode or a transistor) changes over temperature T. Preferably, the constant current source or the drive circuit 70, respectively, is integrated into the semiconductor device 14.

Figure 3 shows an equivalent electrical circuit of the first and second embodiments. The equivalent circuit is a serial circuit of following resistors: resistance R_{72} of the second via 72 (which is typically in the range between 1Ω to 5Ω), resistance R_{32} of the second meander 32a (which is typically between 5Ω and 10Ω, or between 10Ω and 20Ω in average per each rectangle shown in Figures 2 or 5), resistance R_{71} of the first via 71 (which is typically in the range between 1Ω to 5Ω), resistance R_{31} of the first meander 31a (which is typically between 5 Ω and 10 Ω, or between 10 Ω and 20Ω in average per each rectangle 16' or 16'' shown in Figures 2 or 5), resistance R_{22} of the contact 22_H (which is typically in the range between 2Ω to 20Ω), and resistance between emitter 62 and collector 66 of the transistor 60 (i.e. between the shallow well 54 and the silicon substrate 50).

The interconnect device of Figure 1 has about 9 segments in each interconnection layer 41, 42. The second layer 42 is shown in Figure 2. Applying $U^2 = P*R$, from this results a typical heating voltage U of about 1 V to achieve heating power P = dQ/dt of 10mW, and of about 3.16 V to achieve heating power of 100mW for a self-heatable conductive path 16_H having a total resistance of 100 Ohm.

The second embodiment of the electronic device 10 shown in Figure 4 is different to the first embodiment of the electronic device 10 in that the self-heatable conductive path 16_H comprises a first spiral 31b arranged in the first interconnection layer 41 and a second spiral 32b arranged in the second interconnection layer 42 as seen in **Figure 5**.

To contact the central end 33 of the second spiral 32b, the first via 71 is arranged at a center 33 of the first spiral 31b as seen in Figures 4 and 5. The equivalent electrical circuit of Figure 3 also applies to the second embodiment. The spirals 31b, 32b are made of conductive materials, for example of metal, metal alloy, or semiconductor material. The top plate 28 is typically made of metal or metal alloy.

The example interconnect device of Figures 4 and 5 has about 18 segments in each interconnection layer. Applying $U^2 = P*R$, from this results a typical heating voltage U of 4.24 V to achieve heating power P = dQ/dt of 10 mW, and of 13.4 V to achieve heating power of 100 mW for a self-heatable conductive path 16_H having a corresponding total resistance. This could be 1.8 kOhm.

The described on-chip interconnect device 12 having an internal heating structure 31, 32, can be used for conducting measurements under high temperature conditions. The measurements may be part of standard process control monitoring tests performed on every wafer or may be part of other reliability measurements.

The electronic device 10 having a self-heating electrically-conductive structure 16_H (and as an option also a thermally-conductive structure 91) for specifically heating a semiconductor element 15 provides inter alia following application benefits:

Routine controls of a manufacturing process performed while (on-chip) heating the electronic device 10 (having an internal heating structure 31, 32, 91) can be much faster and more accurate than using a hot chuck or an oven (as traditionally used for high-temperature measurements). Such high-temperature measurements, if offered to a customer via a manufacturing process specification or a manufacturing process reliability document, may enhance effectiveness of technology offered to the customer.

Customized (on-chip) burn-in can be performed by specifically heating a semiconductor device 14 by the internal heating structure 31, 32, 91 of the interconnect device 12. After burn-in, a functional test may be employed to remove weak semiconductor devices (chips), leaving more reliable semiconductor devices 14. The interconnect device 12 having the internal heating structure 31, 32, 91 enables testing at high temperature T and stressing the semiconductor element 15 to characterize degradation. There is also potential to run the semiconductor device 14 at higher temperatures T, thereby shortening the burn-in time. Hence, a cheaper and faster development and/or production process is facilitated. Burn-in tests may lead to a reduced failure rate in the field. For example, automotive suppliers perform burn-in tests routinely to accelerate failure mechanisms. If the interconnect device 12 having internal heating structures 31, 32, 91 is used for burn-in, traditional burn-in ovens are no longer required for testing, which facilitates cost-effective solutions. If used for high-temperature measurements of integrated circuits or more simple devices, the invention makes hot-chuck measurement systems dispensable. By offering qualified electronic devices 10 for this purpose, a customer can reduce expenses for performing necessary burn-in tests.

Summarized, the heat source shaped in many different ways and arranged in the electronic device 10 based on resistor elements 31, 32 placed in an intercommunication device 12 attached to a semiconductor element 15 is producible by standard manufacturing processes. Thereby, contrary to known heating structures, a need of additional chip area for a lateral heating structure can be avoided. In addition, a controlling element 60 for controlling a heating current I_H through the resistors 31, 32 and an internal temperature sensor 98 for controlling the controlling element 60 may be integrated into the semiconductor device 14.

* * * * *

Claims.

1. **Interconnect device** having terminal pads (26) and further having
   - a positioning area (13) for arranging a semiconductor element (15) therein;
   - a plurality of conductive paths (16), wherein at least a subset thereof is prepared for electrically connecting the arranged semiconductor element (15) to at least a subset of the terminal pads (26);
   - wherein a self-heatable one (16_H) of the plurality of conductive paths (16) has a total resistance (R) of more than 90 Ohm.

2. The interconnect device of claim 1, wherein the self-heatable one (16_H) of the conductive paths (16) at least partially overlaps the positioning area (13).

3. The interconnect device of claim 1, wherein at least one of the terminal pads (26) overlaps at least partially the self-heatable one (16_H) of the conductive paths (16).

4. The interconnect device of claim 1, wherein the self-heatable one (16_H) of the conductive paths (16) is arranged exclusively outside any semiconductor substrate (50) arranged within the positioning area (13) for arranging a semiconductor element (15) therein.

5. The interconnect device of claim 1, wherein the self-heatable conductive path (16_H) has a total resistance (R) of more than 180 Ohms and/or less than 450 Ohms, preferably in no more than two interconnect layers (41, 42).

6. The interconnect device of claim 1, wherein a specific electrical resistance (ρ) of the first layer (41) of the interconnect device (12) is at least n times as high as a specific electrical resistance of the terminal pad (26), wherein n is 2, in particular 4, 8 or 16.

7. The interconnect device of claim 1, wherein said self-heatable conductive path (16_H) comprises at least one terminal pad (26) which is at least partially located outside the positioning area (13) and is accessible at a surface (27) of the interconnect device (12).

8. The interconnect device of claim 7, wherein a second via (72) electrically connects a self-heatable portion (32a,32b) of the self-heatable conductive path (16_H) to a terminal pad (26).

9. The interconnect device of claim 1, wherein the self-heatable conductive path (16_H) comprises at least one contact (22_H) for connecting the self-heatable conductive path (16_H) to a semiconductor device (14) comprising the semiconductor element (15).

10. The interconnect device of claim 1, comprising a first interconnection layer (41) and a second interconnection layer (42), wherein said self-heatable conductive path (16_H) comprises a first self-heatable portion (31a,31b) in the first interconnection layer (41) and a second self-heatable portion (32a,32b) in the second interconnection layer (42), and at least one first via (71) electrically connecting the first self-heatable portion of the self-heatable conductive path (16_H) to the second self-heatable portion of the self-heatable conductive path.

11. The interconnect device of claim 1, wherein a self-heatable portion (31,32) of the self-heatable conductive path (16_H) comprises a meander structure (31a,31b) or a spiral structure (32a,32b).

12. The interconnect device of claim 1, wherein a filling material (18) arranged between the conductive paths (16) of the interconnect device (12) comprises at least one of following insulating materials: oxide, silicate, glass, fused silica, other ceramic material, resin, elastomer, insulating semiconductor material.

13. **An electronic device** comprising the interconnect device according to one of claims 1 to 12, and
- a semiconductor element (15) arranged at the positioning area (13) and electrically connected by at least a subset of said conductive paths (16) to at least a subset of the terminal pads (26).

14. The electronic device of claim 13, wherein a semiconductor device (14) comprises the semiconductor element (15) and wherein the interconnect device (12) is partially arranged on top of a surface area (17) of the semiconductor device (14), wherein said surface area (17) is different to the positioning area (13).

15. The electronic device of claim 13, wherein said at least one terminal pad (26) at least partially located outside the positioning area (13) is accessible at a surface (27) of the interconnect device (12) which is facing away from the semiconductor element (15).

16. The electronic device of claim 13, wherein the self-heatable conductive path (16_H) has an extension (91) for distributing heat (Q).

17. The electronic device of claim 13, wherein a semiconductor device (14) comprises the semiconductor element (15) and wherein the semiconductor device (14) comprises a heat controller (94) configured to control generation of heat (Q) in said self-heatable conductive path (16_H) and having an input to use temperature information (T_{info}) for controlling a heating current (I_H) through said self-heatable conductive path (16_H).

18. The electronic device of claim 17, wherein the semiconductor device (14) comprises a temperature sensor (98) for providing said temperature information (T_{info}) to the heat controller (94).

19. The electronic device of claim 18, wherein the temperature sensor (98) comprises at least one of a diode and a bipolar transistor.

20. The electronic device of claim 13, wherein
    - a semiconductor device (14) comprises the semiconductor element (15);
    - the semiconductor device (14) comprises a substrate (50);
    - a deep well (52) being provided in the substrate (50);
    - a shallow well (54) being deposited in the deep well (52);
    - the shallow well (54) being oppositely doped compared to the deep well (52);
    - the self-heatable conductive path (16_H) being electrically connected to the shallow well (54).

21. The electronic device of claim 13, comprising a drive circuit (70) for supplying the self-heatable conductive path (16_H) with heating current (I_H), wherein the drive circuit (70) configured as a constant current source or as a PTC thermistor, sensing a temperature (T) at an application location (97) of heat (Q) generated by the self-heatable conductive path (16_H).

22. **Method of using a self-heatable conductive path** (16_H) of the interconnect device of claim 1, to increase a temperature (T) of a semiconductor element (15) by more than 10°K by arranging and electrically connecting the interconnect device (12) to the semiconductor element (15) and by applying a voltage (U) to the self-heatable conductive path (16_H) arranged in the interconnect device (12).

23. **Method** of electrically controlled increasing a temperature (T) of a semiconductor element (15) by more than 10°K by arranging and electrically connecting an interconnect device (12) to the semiconductor element (15) and by applying a voltage (U) to a self-heatable conductive path (16_H) arranged in the interconnect device (12).

* * * * *

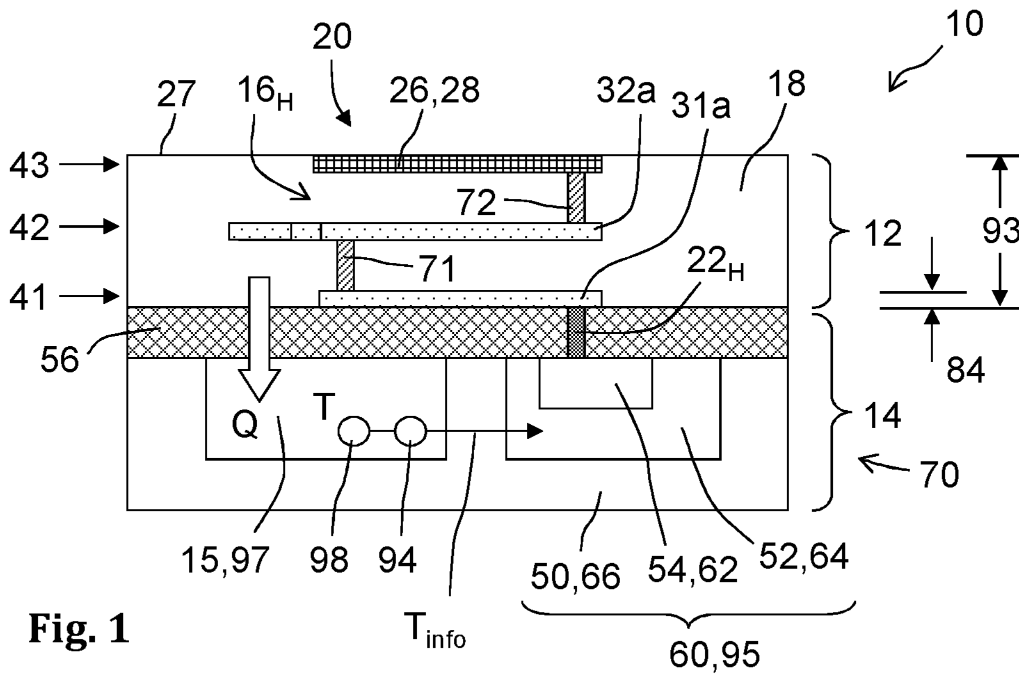
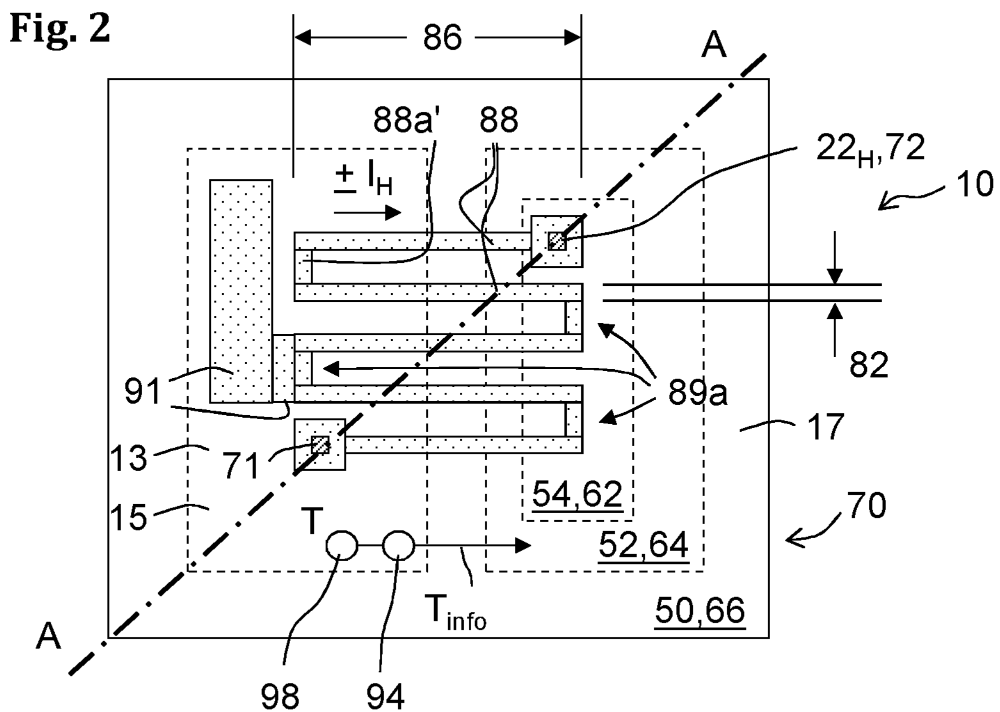


Fig. 1

Fig. 2



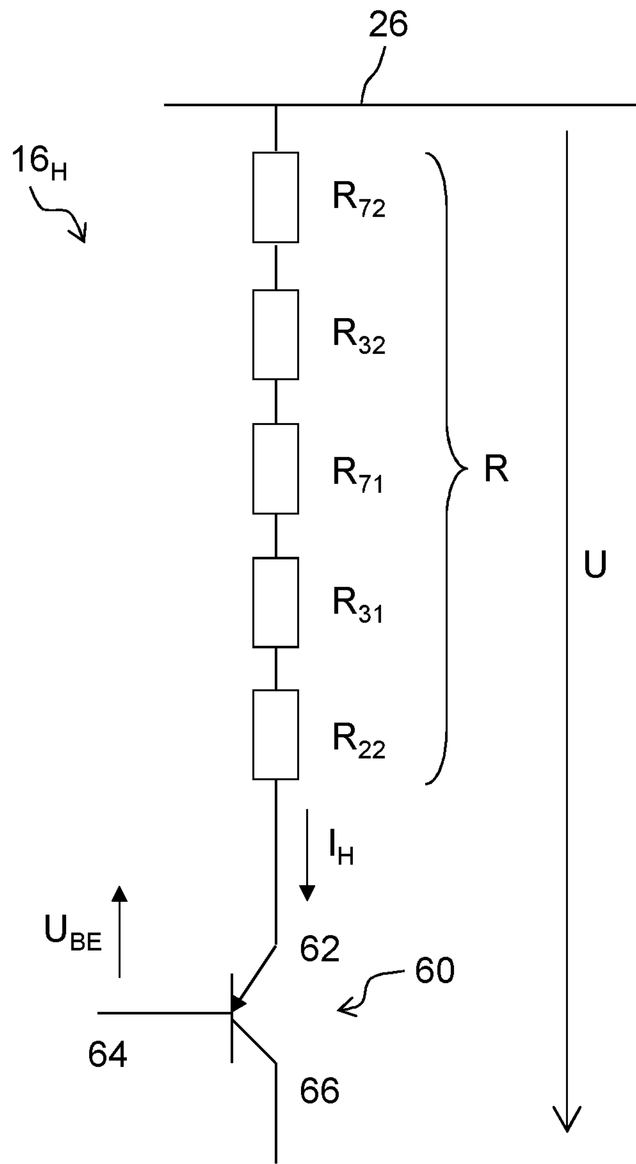


Fig. 3

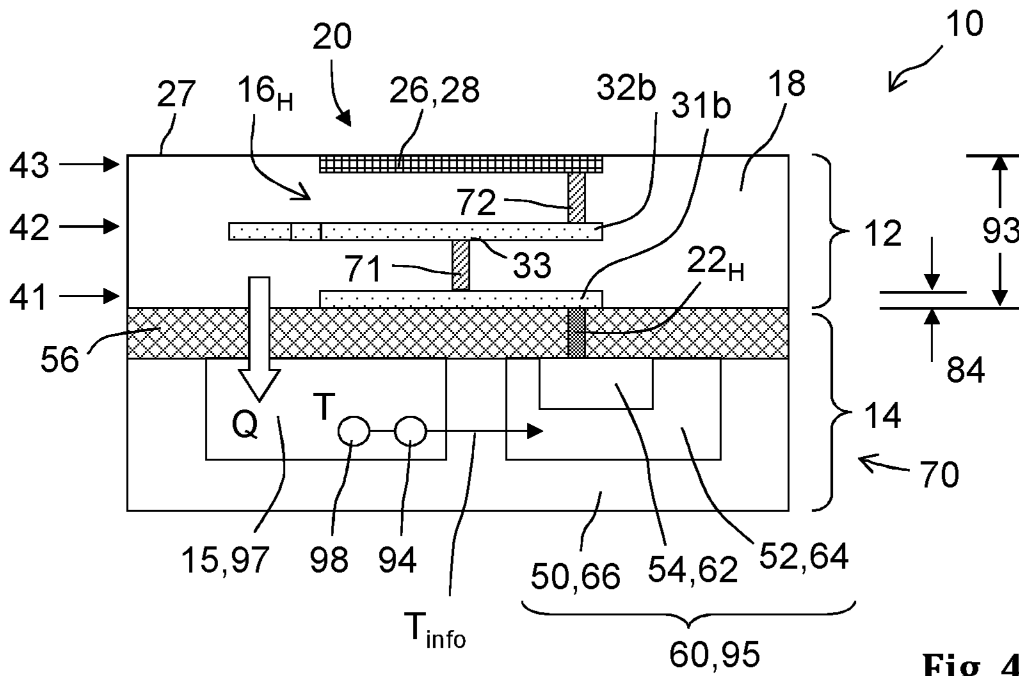


Fig. 4

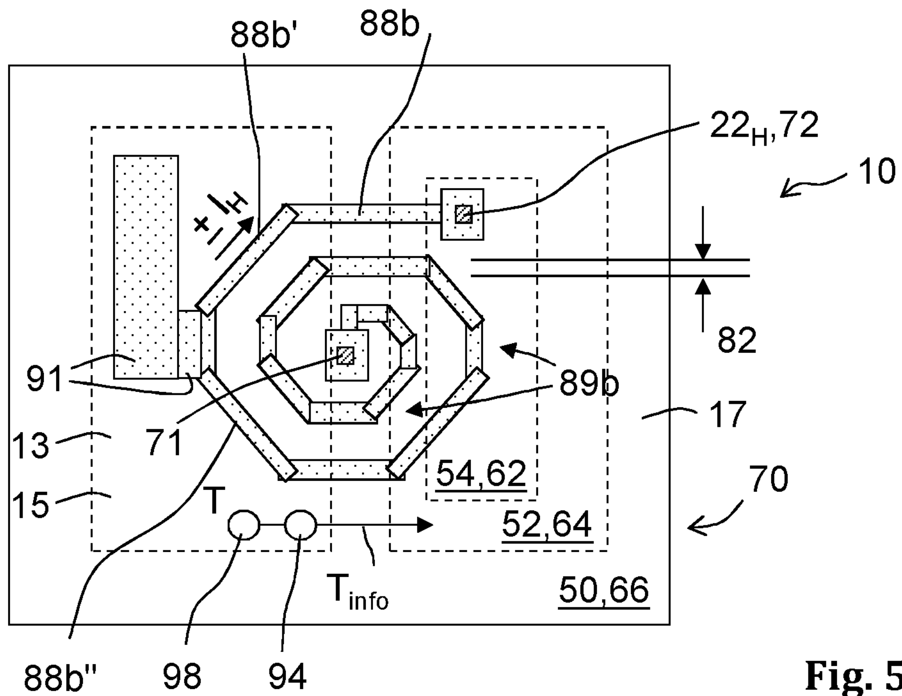


Fig. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/069628

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/34 H01L23/522
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

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Y	figures paragraph [0031] - paragraph [0064] paragraph [0088] -----	2,3,5,6, 8-10,16, 18-21
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Y	paragraph [0011] - paragraph [0021] -----	5,6,8, 14,16, 19-23

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search	Date of mailing of the international search report
25 July 2012	02/08/2012

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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