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(54) **SEMICONDUCTOR DEVICE HAVING SILICON CARBIDE AND CONDUCTIVE PATHWAY INTERFACE**

(75) Inventors: **Judy H. Huang**, Los Gatos, CA (US); **Christopher Dennis Bencher**, Sunnyvale, CA (US); **Sudha Rathi**, San Jose, CA (US); **Christopher S. Ngai**, Burlingame, CA (US); **Bok Hoen Kim**, San Jose, CA (US)

Correspondence Address:
MOSER, PATTERSON & SHERIDAN, LLP
APPLIED MATERIALS INC
595 SHREWSBURY AVE
SUITE 100
SHREWSBURY, NJ 07702 (US)

(73) Assignee: **Applied Materials, Inc.**

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(60) Division of application No. 10/655,438, filed on Sep. 4, 2003, now Pat. No. 6,946,401, which is a continuation of application No. 10/013,182, filed on Dec. 7, 2001, now Pat. No. 6,700,202, which is a division of application No. 09/365,129, filed on Jul. 30, 1999, now Pat. No. 6,355,571, which is a continuation-in-part of application No. 09/193,920, filed on Nov. 17, 1998, now abandoned.

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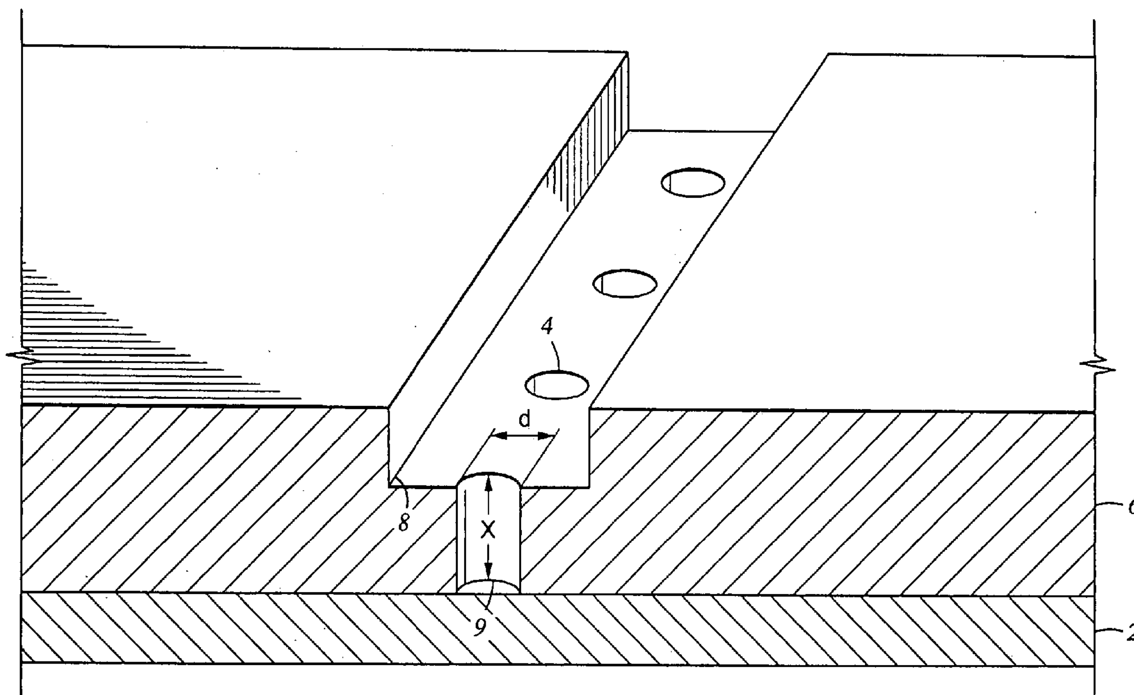
(57) **ABSTRACT**

The present invention provides an in situ plasma reducing process to reduce oxides or other contaminants, using a compound of nitrogen and hydrogen, typically ammonia, at relatively low temperatures prior to depositing a subsequent layer thereon. The adhesion characteristics of the layers are improved and oxygen presence is reduced compared to the typical physical sputter cleaning process of an oxide layer. This process may be particularly useful for the complex requirements of a dual damascene structure, especially with copper applications.



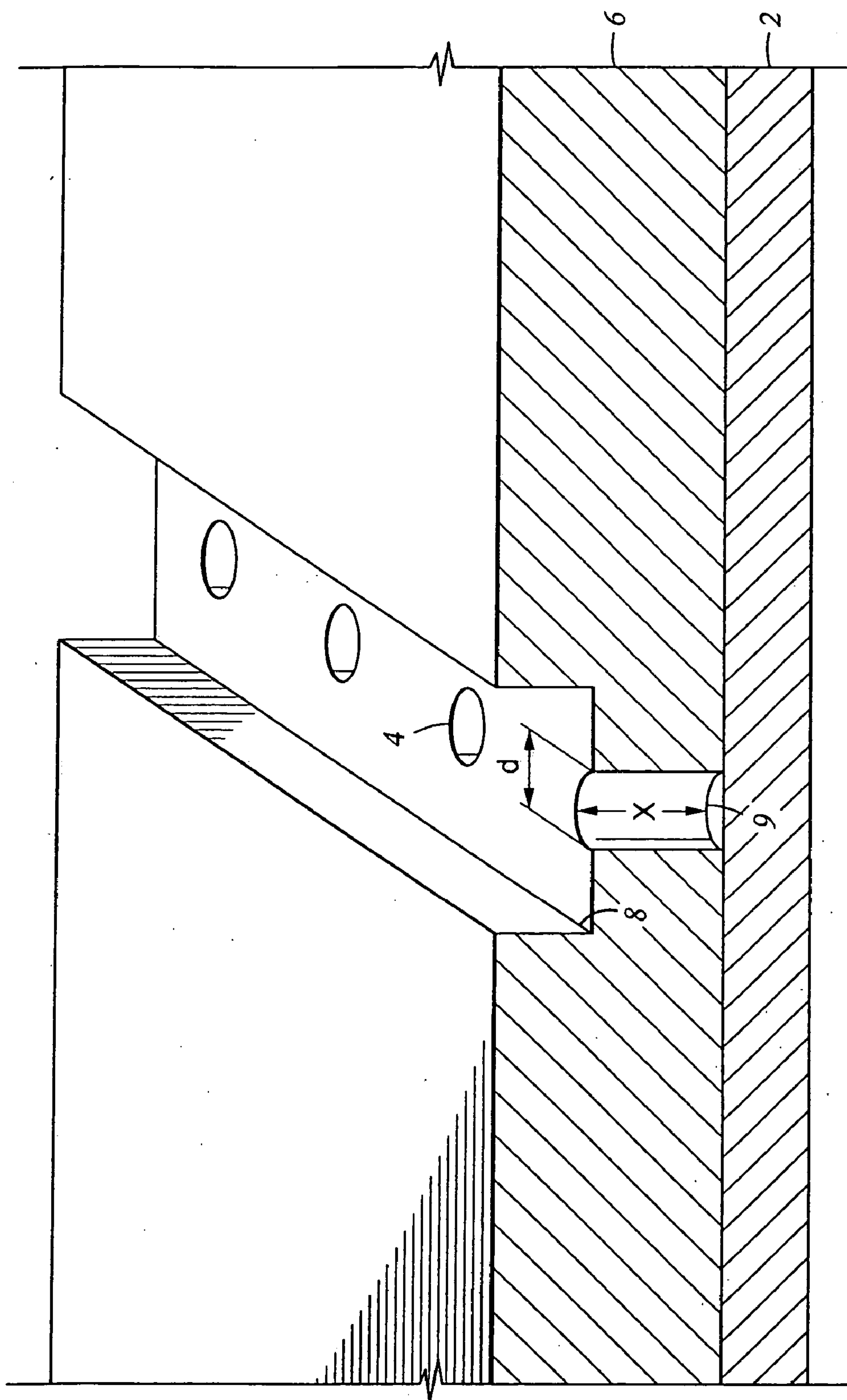


Fig. 1

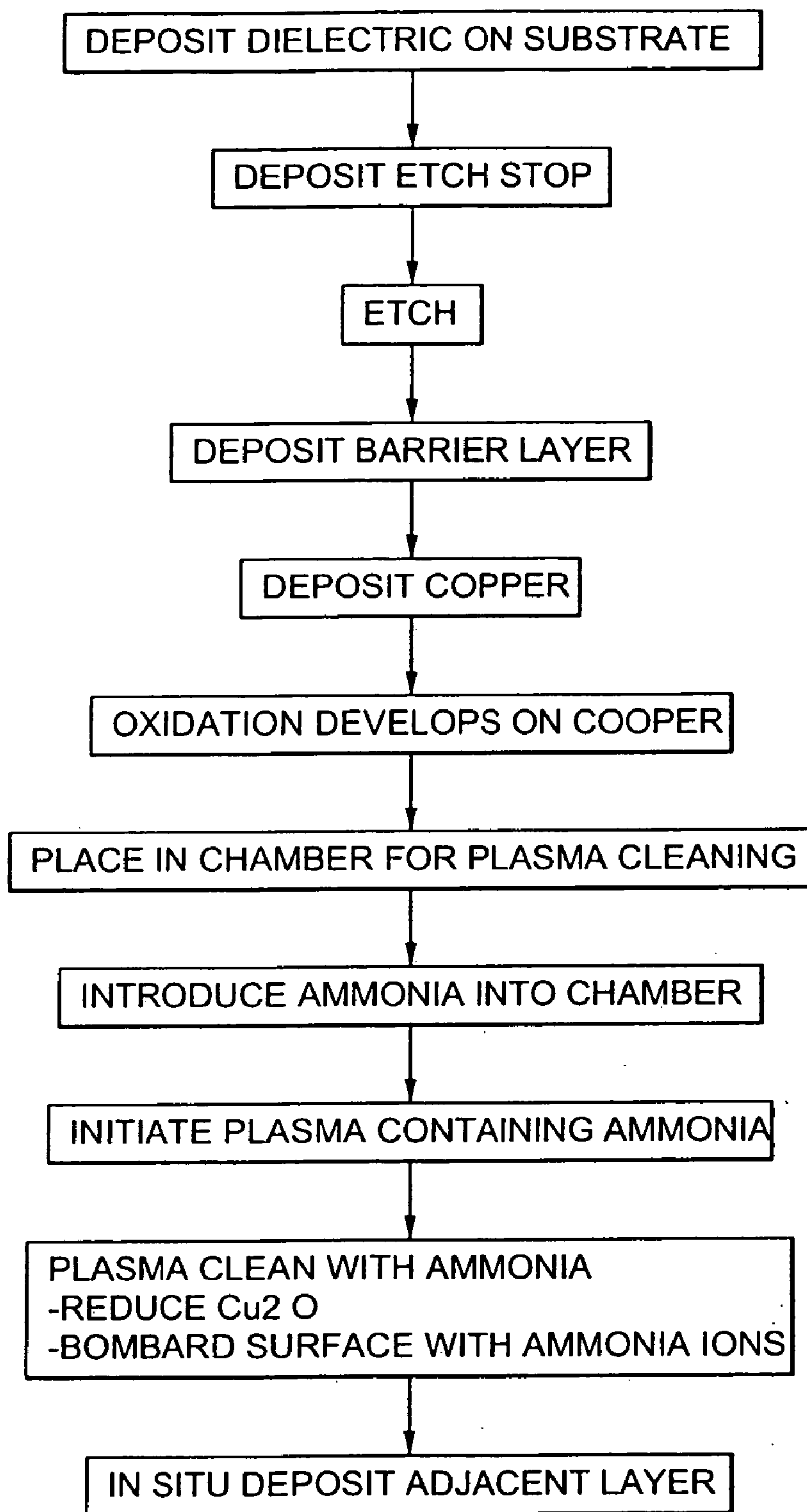


Fig. 2

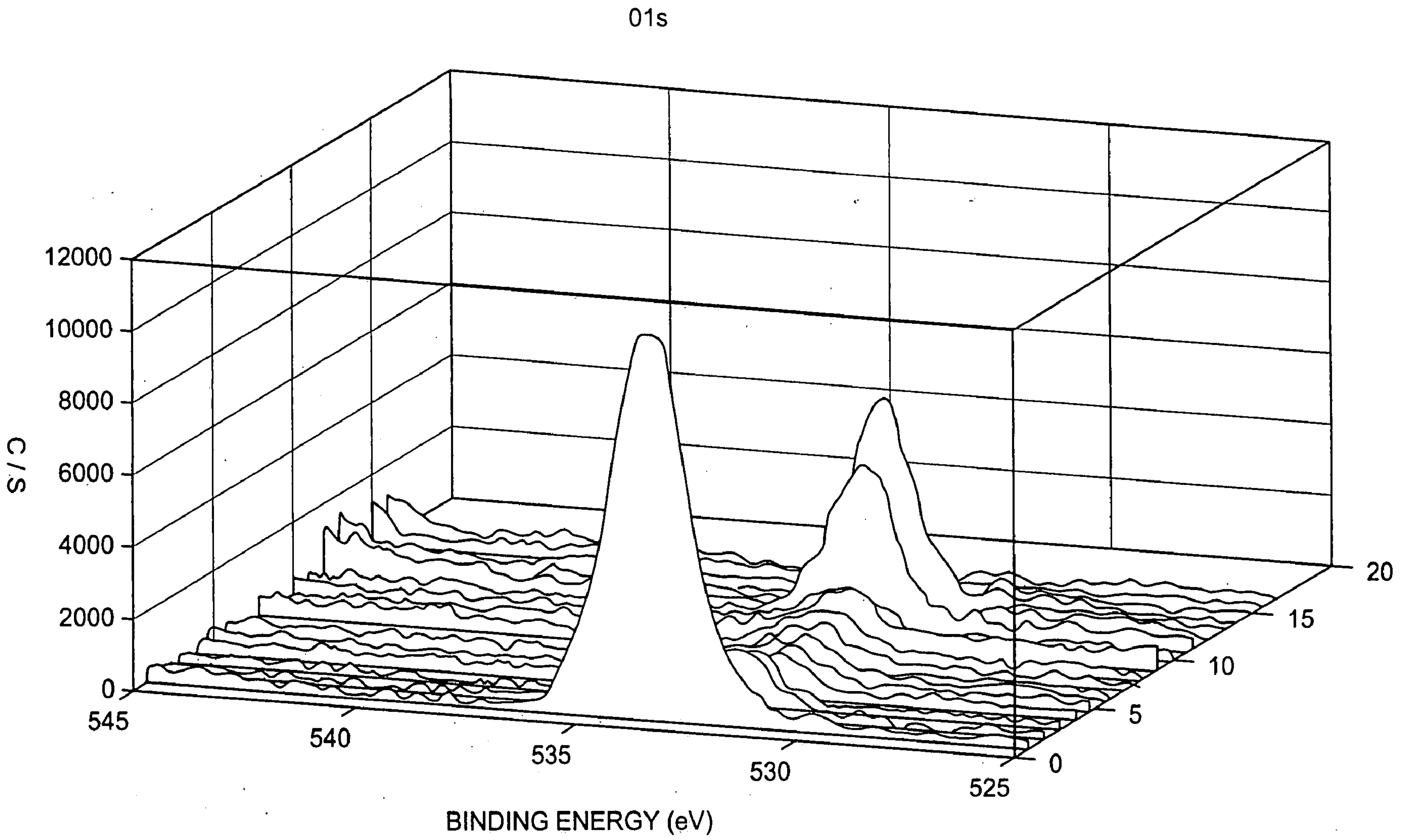


Fig. 3

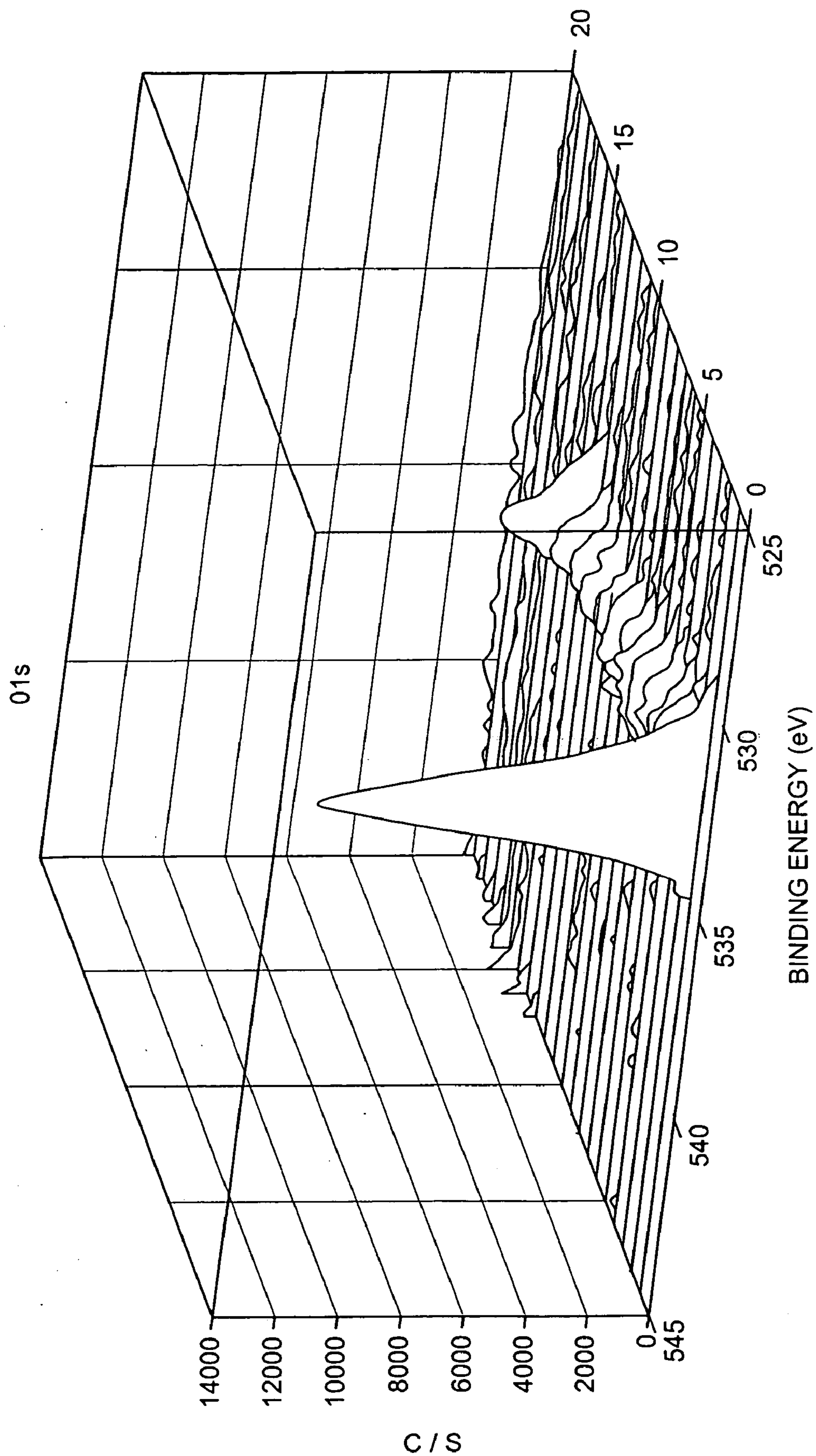


Fig. 4

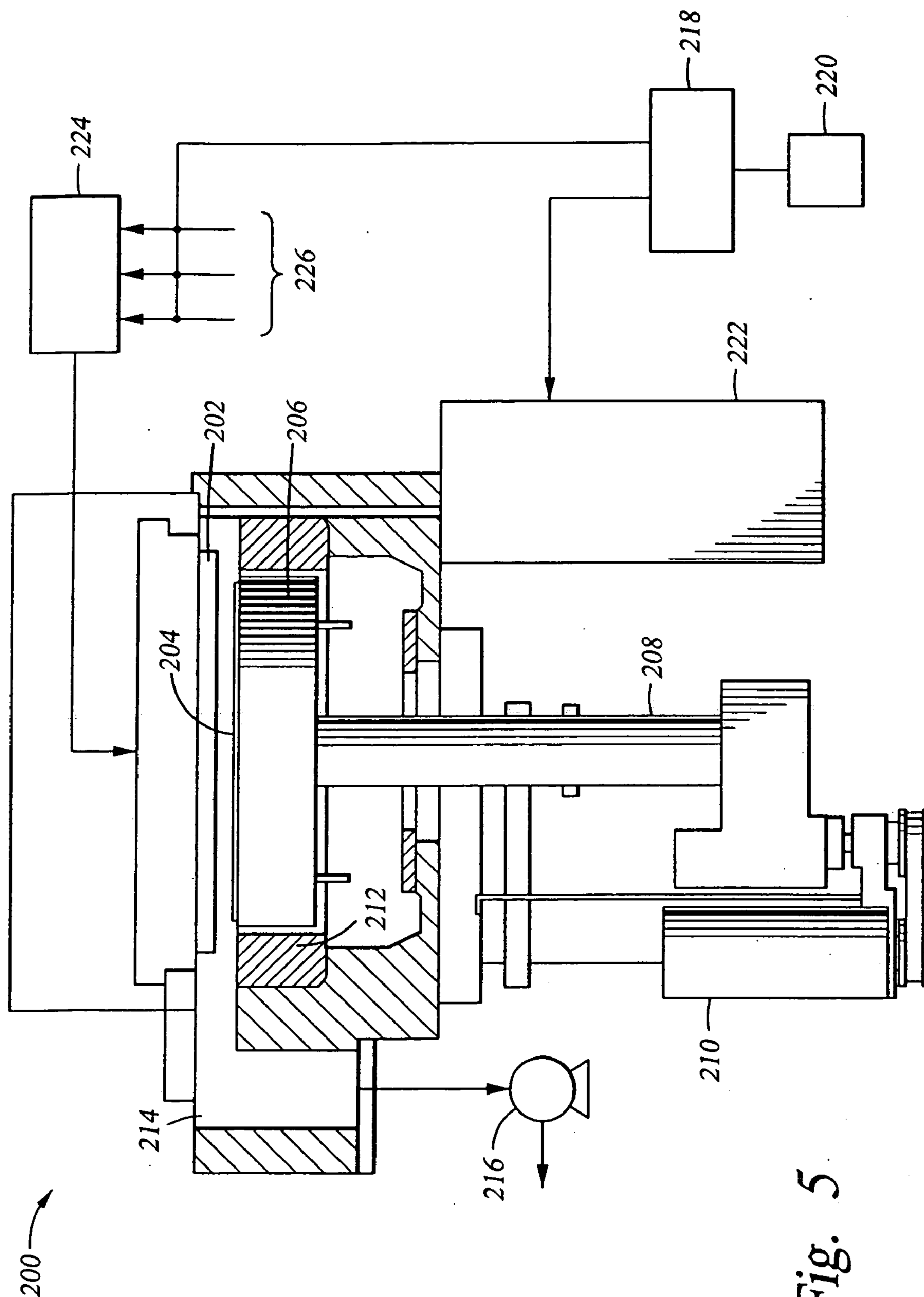


Fig. 5

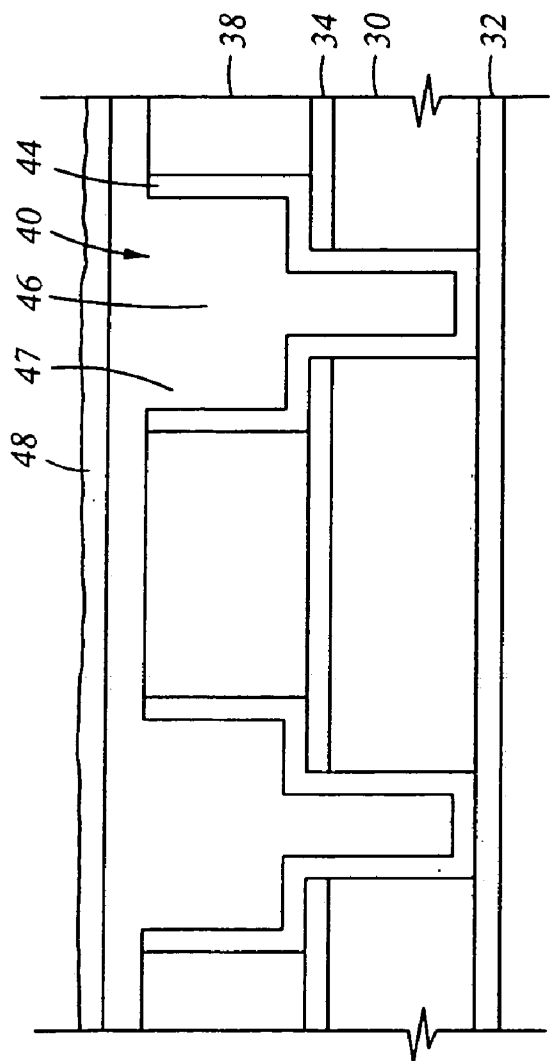


Fig. 6

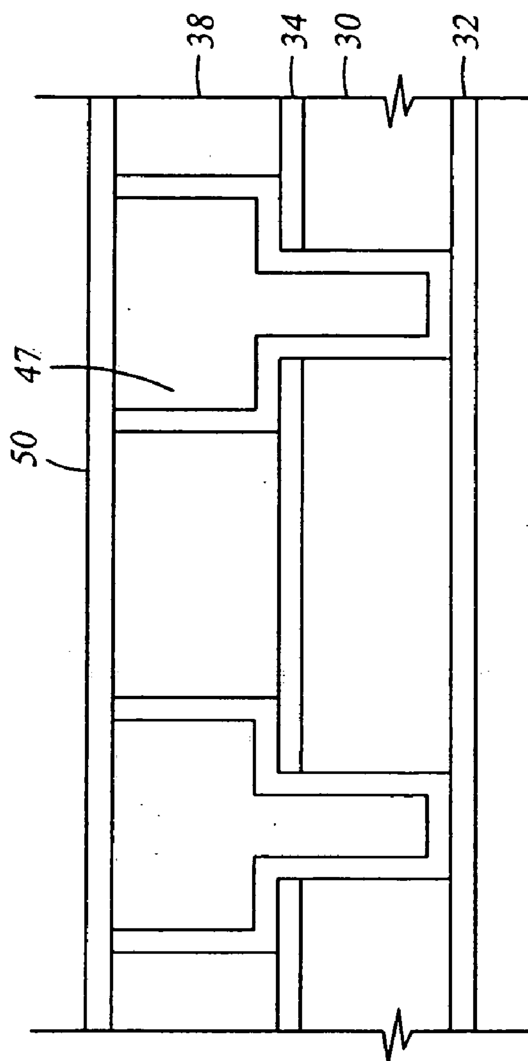


Fig. 7

SEMICONDUCTOR DEVICE HAVING SILICON CARBIDE AND CONDUCTIVE PATHWAY INTERFACE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional application of co-pending U.S. patent application Ser. No. 10/655,438, filed Sep. 4, 2003, which is a continuation of U.S. patent application Ser. No. 10/013,182, filed Dec. 7, 2001, which is a divisional of U.S. patent application Ser. No. 09/365,129, filed Jul. 30, 1999, which is a continuation-in-part of U.S. patent application Ser. No. 09/193,920, filed Nov. 17, 1998, all of which are hereby incorporated by reference in their entireties.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates generally to the fabrication of integrated circuits on substrates. More particularly, the invention relates to a method of reducing oxides on a substrate prior to depositing a layer thereover in the fabrication process.

[0004] 2. Background of the Invention

[0005] Reliably producing sub-half micron and smaller features is one of the key technologies for the next generation of very large scale integration (VLSI) and ultra large scale integration (ULSI) integrated circuits. However, as the fringes of circuit technology are pressed, the shrinking dimensions of interconnects in VLSI and ULSI technology has placed additional demands on the processing capabilities. The multilevel interconnects that lie at the heart of this technology require careful processing of high aspect ratio features, such as vias and other interconnects. Reliable formation of these interconnects is very important to the VLSI and ULSI success and to the continued effort to increase circuit density and quality of individual substrates and die.

[0006] Conventional chemical vapor deposition (CVD) and physical vapor deposition (PVD), and now electroplating, techniques are used to deposit electrically conductive material into the contacts, vias, lines, or other features formed on the substrate. Considerable effort has focused on reliably depositing material in these high aspect ratio, smaller interconnects.

[0007] One issue that still needs improvement as feature sizes shrink is the reduction of oxides in these very small features. **FIG. 1** shows a substrate **2** with a via **4** formed within an electrically insulative or dielectric layer **6**. With current technology, the aspect ratio has increased to approximately 5:1 for the height to width ratio, shown in **FIG. 1** as x with respect to d. As a result, it is becoming more difficult to properly prepare the surfaces within the small features for subsequent processing, especially in the lower interconnect portions, such as in the interconnect areas **8**, **9**.

[0008] In part, this attention to improved cleaning is due to a desired change in the conductor metal. For example, copper is now being considered as an interconnect material in place of aluminum, because copper has a lower resistivity (1.7 $\mu\Omega$-cm compared to 3.1 $\mu\Omega$-cm for aluminum) and higher current carrying capacity. However, copper is highly susceptible to oxidation. With copper depositions, oxidation is considered a detriment and interferes with adhesion on the adjacent layer, affects conductivity of the copper feature, and reduces the reliability of the overall circuit. Furthermore, present processes utilize oxygen for a variety of reasons in some instances and in other instances, oxygen is a byproduct of the reactions. Thus, even carefully controlled environments may contain oxygen that may oxidize copper or other conductive materials, such as aluminum, to the detriment of the circuit.

[0009] Copper has other difficulties. Because copper is difficult to etch in a precise pattern, traditional deposition/etch processes for forming interconnects has become unworkable, and accordingly, a "dual damascene" structure is being used for copper interconnects. In a typical dual damascene structure, the dielectric layer is etched to define both the contacts/vias and the interconnect lines. Metal is then inlaid into the defined pattern and any excess metal is typically removed from the top of the structure in a planarization process, such as CMP. This complex approach increases the importance of obtaining properly cleaned surfaces within the interconnects.

[0010] Prior to the present invention, an inert gas plasma, such as an Argon (Ar) plasma, physically cleaned the surfaces of interconnects and metal layers, such as aluminum and copper, as ions were attracted to the substrate surface to physically bombard the surface and remove the surface of the uppermost layer. However, the Ar ions in the plasma depend on directionality to clean and with the decreasing sizes of the interconnects, the increasing aspect ratios, and the resulting shading that can occur, this process is ineffective in removing oxides in the small features.

[0011] Therefore, there is a need for an improved cleaning process to reduce oxides formed on the surface of substrates and materials deposited thereon.

SUMMARY OF THE INVENTION

[0012] The present invention provides a process for removing oxides and other contaminants comprising initiating a plasma containing a reducing agent in a chamber and exposing at least a portion of a substrate surface having a reducible contaminant to the reducing agent. In a preferred embodiment, the reducing agent comprises a compound containing nitrogen and hydrogen, preferably ammonia. One example may include introducing a reducing agent comprising nitrogen and hydrogen into a chamber, initiating a plasma in the chamber, and exposing an oxide to the reducing agent. The plasma process parameters to reduce an oxide, such as copper oxide, using ammonia include a pressure range of about 1 to about 9 mTorr, an RF power of about 100 to about 1000 watts for a 200 mm wafer to the chamber with a power density of about 1.43 to 14.3 watts/cm^2, a substrate temperature of about 100° to about 450° C., a showerhead to substrate spacing of about 200 to about 600 mils, and a reducing agent flow rate of about 100 to about 1000 sccm.

[0013] An exemplary process sequence of the invention, such as for forming a dual damascene structure, includes depositing a dielectric on a substrate, depositing an etch stop, etching the etch stop, depositing a barrier layer, depositing a metal layer, initiating a reducing agent plasma,

reducing oxides which may form on at least some of the metal surface with the reducing agent, such as ammonia, and in situ depositing a layer, such as a nitride layer, over the reduced surface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0015] It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0016] **FIG. 1** shows a schematic of a multilevel substrate with interconnects;

[0017] **FIG. 2** is a flow chart of one example of a deposition/etching process using the plasma reducing process;

[0018] **FIG. 3** is a graph of dielectric compatibility showing oxygen levels obtained from a copper wafer after a CMP process;

[0019] **FIG. 4** is a graph in comparison to **FIG. 3** showing an improvement by the plasma reducing process of the present invention, having decreased oxygen levels;

[0020] **FIG. 5** shows a cross-sectional view of one commercially available CVD plasma reactor in which the plasma reducing process of the present invention may be performed;

[0021] **FIG. 6** is a dual damascene structure showing an oxide layer on a conductor; and

[0022] **FIG. 7** is a dual damascene structure with a layer deposited on the cleaned conductor.

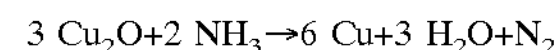
DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

[0023] The present invention provides a process for removing oxides and other contaminants comprising initiating a plasma containing a reducing agent and exposing at least a portion of a substrate surface having a reducible contaminant to the plasma and the reducing agent. The reducing process is believed to increase the adhesion of the adjoining layer and to decrease the electrical resistance of the combined layers by decreasing the oxygen content in the oxidized layer. At least in part, these adverse oxide effects are believed to be due to the metal oxides, such as copper oxide (Cu_2O), reducing the mobility of the metal, e.g., copper (Cu). In the preferred embodiment, the process is performed in situ to minimize re-contamination before the deposition of a subsequent layer. In situ processing may be particularly important with copper, because of its rapid susceptibility to oxidation.

[0024] In an integrated circuit (IC) fabrication, a metal layer is deposited at some point in the deposition process and typically comprises aluminum or copper. Because copper is being considered for the conducting material, much of the discussion herein is addressed to copper. However, the present invention may be used for any oxidized metal layers, such as Ti, TiN, Ta, TaN, Al, and others. It may also be used for other layers, including silicon oxides. The present invention combines the chemical reactive cleaning of a reducing agent, such as a compound containing nitrogen and hydrogen, including ammonia, with the physical bombardment of the ions from a plasma, and so may be used on a variety of materials to effectuate the reduction of contaminants, such as oxides. While oxides are clearly discussed in the specification, other contaminants would fall within the scope of the present invention. It is believed that the nitrogen combined with hydrogen allows a reduced energy level to break the hydrogen bonds and otherwise disassociate the molecules and more effectively utilize the reducing agent to clean the contaminants.

[0025] Before depositing a layer over the metal, such as a nitride, the metal is cleaned according to the teaching of the present invention. By "cleaning", the term is meant to include a reduction of an oxide or other contaminants. Cleaning may be necessary due to exposure to an oxygen source (such as air, diatomic oxygen, or oxygen contained in a molecular compound). This cleaning may take place in the same CVD or plasma enhanced chemical vapor deposition ("PECVD") chamber in which the subsequent layer is deposited, as an in situ process. The term "in situ" is intended to include in a given chamber, such as in a plasma chamber, or in a system, such as an integrated cluster tool arrangement, without exposing the material to intervening contamination environments. An in situ process typically minimizes process time and possible contaminants compared to relocating the substrate to other processing chambers or areas.

[0026] In one embodiment, the reduction process typically includes introducing the reducing agent, such as ammonia, into a vacuum chamber and initiating a plasma where the plasma excites the ammonia into an energized ionic state. The energized ions chemically react with the oxide and the oxides are removed according to the following equation:



$$3\ Cu_2O + 2\ NH_3 \rightarrow 6\ Cu + 3\ H_2O + N_2$$

[0027] The plasma provides the energy necessary to dissociate the ammonia and to provide the desired ion bombardment. The ionized particles impact the oxidized surfaces in the reduction process to further enhance the cleaning. The combination of chemical reactions and physical bombardment of ions increases the likelihood that all surfaces in small features are cleaned or oxides reduced.

[0028] The process of the invention is believed to afford at least two advantages. First, the cleaned surface is better prepared for increased adhesion to an adjoining layer. Removal of the oxide allows a better bond to the base conducting material. Secondly, oxides are known to increase resistance of a layer or combined layers. Thus, the reduction of the oxide decreases the resistance or impedance of the combined layers.

[0029] The plasma process parameters for at least one embodiment, using ammonia to reduce the copper oxide, include a pressure range of about 1 to about 9 mTorr, an RF power of about 100 to about 1000 watts to a chamber, that may have a reaction zone, to create the plasma having a power density of about 1.43 to about 14.3 watts/cm^2, a substrate surface temperature of about 100° to about 450°

C., a showerhead to substrate spacing of about 200 to about 600 mils, and a reducing agent flowing at a rate of about 100 to about 1000 sccm into the chamber. The gas dispersion element, such as a "showerhead", is commonly known to those with ordinary skill in the art and is used interchangeably herein, and includes other gas dispersion elements. The "reaction zone" is the zone between the showerhead and the substrate surface in the chamber, such as one in a CENTURA DxZ™ CVD reactor, fabricated and sold by Applied Materials, Inc. of Santa Clara, Calif.

[0030] A preferred process range includes a pressure range of about 3 to about 7 mTorr, an RF power of about 100 to about 500 watts for a 200 mm wafer having a power density of about 1.43 to about 7.14 watts/cm^2, a substrate temperature of about 200° to about 400° C., a showerhead to substrate spacing of about 200 to about 500 mils, and a reducing agent flowing at a rate of about 100 to about 500 sccm. A most preferred process range includes a pressure range of about 4 to about 6 mTorr, an RF power of about 200 to about 400 watts having a power density of about 2.86 to about 5.72 watts/cm^2, a substrate temperature of about 300° to about 400° C., a showerhead to substrate spacing of about 300 to about 400 mils, and a reducing agent flowing at a rate of about 200 to about 300 sccm. Additionally, carrier gases may be used in conjunction with the above process parameters to assist in stabilizing the gas flow and the plasma reaction. The flow rate of the carrier gases, such as helium, argon, and nitrogen, could be approximately 0 to 2000 sccm.

[0031] The plasma reducing process reduces, treats, or otherwise modifies the surface in about 5 to about 60 seconds. Preferably, the ammonia plasma is generated in one or more treatment cycles and purged between cycles. However, in most cases, one treatment cycle lasting 10 seconds effectively removes oxygen from an oxidized copper surface. Naturally, the parameters could be adjusted for other materials besides copper and other contaminants besides oxides.

[0032] **FIG. 2** shows a deposition/plasma reducing sequence of one example of the present invention. Other sequences, fabrication techniques, and processes may be used. Typically, a dielectric such as silicon dioxide, silicon nitride, or silicon carbide is deposited on a substrate. The term "substrate" herein includes the IC base or the IC including deposited materials or levels thereon, as the context may indicate. An etch stop is deposited over the dielectric and interconnects are etched therethrough to form a pattern. Horizontal interconnects are typically referred to as lines and vertical interconnects are typically referred to as contacts or vias; contacts extend to a device on the underlying substrate, while vias extend to an underlying metal layer, such as **M1**, **M2**, etc. Once the lines and contacts/vias are patterned, such as shown in **FIG. 1**, a barrier layer, such as a TiN layer, is deposited over the pattern to restrict the diffusion of the conductor into the dielectric layer(s). The conducting material may then be deposited over the barrier layer. An oxidation may form on the conducting material, impeding adhesion and conductance. The substrate may be placed in a processing chamber for plasma cleaning that may be in situ with prior or subsequent processes. Typically, the system would initiate a plasma and introduce a reducing agent into the chamber, whereupon the plasma cleaning would occur. The plasma would assist in energizing the reducing agent molecules to clean and otherwise reduce the oxide.

[0033] After the conductor is cleaned, another layer, such as a nitride, may be in situ deposited over the conductor to reduce further contamination from an adverse environment, such as one with oxygen. Typically, this layer is a dielectric layer, but can include other types of layers, such as a barrier layer, an etch stop, or a passivation layer. Alternatively, the reduced substrate may be transported to a different chamber for subsequent processing. The cleaning is not restricted to the conductor—other layers before and after the conductor layer could be plasma cleaned using the underlying concepts of the present invention.

EXAMPLE 1

Without an Ammonia Plasma Reducing Process

[0034] **FIG. 3** shows the oxygen detected through a 500 Å nitride layer deposited on a copper surface after a CMP process without a plasma reducing process. The x-axis represents the binding energy in electron volts (ev), the y-axis represents counts per signal (c/s), and the z-axis represents a relative depth profile through the nitride film layer. The x-axis, showing the binding energy, is element specific and the substrate layers have been tested at an oxygen binding energy level to detect its presence. The y-axis represents the oxygen level detected at an oxygen-specific binding energy. Because the z-axis is relative, the distance between the two largest peaks along the z-axis is the approximate thickness of the 500 Å nitride layer. Beyond the 500 Å nitride layer, the signal count drops to approximately zero because copper is a conductor. **FIG. 3** shows a first high peak closest to the origin of the z-axis of ~11000 c/s. This first and highest peak represents the surface of the nitride layer and may be ignored for the present purposes. The last large peak at a depth of ~500 Å represents the oxygen level of ~6000 c/s at the nitride/copper interface. This interface has a quantity of copper oxide that has not been reduced in accordance with the teaching of the present invention.

EXAMPLE 2

With an Ammonia Plasma Reducing Process

[0035] **FIG. 4** is a graph corresponding to **FIG. 3**, showing the results from an exemplary copper surface substrate treated by an ammonia plasma reducing process of the present invention. **FIG. 4** can be compared to **FIG. 3** and the axes represent similar scales and values. Similar to the substrate surface of **FIG. 3**, a 500 Å nitride layer was deposited on the copper after applying the plasma reducing process of the present invention. **FIG. 4** shows an overall lower oxygen level beyond the initial surface peak, where the initial surface peak may again be ignored for the present purposes. Noticeably, the oxygen level at the nitride/copper interface, represented by the second peak at a depth of about 500 Å, has been lowered to a level of ~3000 c/s due to the elimination or reduction of the oxide from the copper surface.

[0036] **FIG. 5** is a cross-sectional view of a CVD plasma reactor in which the above plasma reducing process may be performed, such as a CENTURA DxZ™ mentioned above. The present invention could be used in other reactors, such

as a lamp heated reactor. Reactor **10** contains a gas distribution manifold **11**, which may be the above described showerhead, for dispersing process gases through perforated holes (not shown) in the manifold to a substrate or wafer **16** that rests on a substrate support plate or susceptor **12**. Susceptor **12** is resistivity heated and is mounted on a support stem **13**, so that susceptor **12** and the wafer supported on the upper surface of susceptor **12** can be controllably moved by a lift motor **14** between a lower loading/off-loading position and an upper processing position, which is spaced closely adjacent to the manifold **11**. When susceptor **12** and the wafer **16** are in the processing position, they are surrounded by an insulator ring **17**. During processing, gases inlet to manifold **11** are uniformly distributed radially across the substrate surface. The gases exhaust through a port **24** by a vacuum pump system **32**.

[**0037**] The deposition process performed in reactor **10** can be either a thermal process or a plasma enhanced process. In a plasma process, a controlled plasma is formed adjacent to the wafer by RF energy applied to distribution manifold **11** from RF power supply **25** with susceptor **12** grounded. Gas distribution manifold **11** is also an RF electrode, while susceptor **12** is grounded. RF power supply **25** can supply either single or mixed frequency RF power to manifold **11** to enhance the decomposition of any reactive species introduced into chamber **15**. A mixed frequency RF power supply typically supplies power at a high RF frequency (RF**1**) of 13.56 MHz and at a low RF frequency (RF**2**) of 350 kHz. The system controller **34** and memory **38** control the activities of the CVD reactor. An example of such a CVD reactor is described in U.S. Pat. No. 5,000,113, which is incorporated by reference and entitled "Thermal CVD/PECVD Reactor and Use for Thermal Chemical Vapor Deposition of Silicon Dioxide and In-situ Multi-step Planarized Process," issued to Wang et al. and assigned to Applied Materials, Inc., the assignee of the present invention.

[**0038**] With the present invention, the above chamber can be used to plasma reduce an oxide with a reducing agent and particularly a copper oxide with ammonia. The reducing agent can be introduced through manifold **11** and be uniformly distributed radially across the wafer surface for the plasma reducing process in the manner described above, followed by the gases exhausting through the port **24**.

[**0039**] The above discussion applies in general to the improvement provided by the plasma reducing process and can be used in multiple environments, on substrates, and in a variety of processes. This plasma reducing process has particular applicability to the increased density and complexity of a dual damascene structure. The following discussion briefly discusses aspects from a dual damascene structure and how the plasma reducing process may be utilized.

[**0040**] **FIGS. 6 and 7** represent a dual damascene structure which can be cleaned using the techniques of the present invention. In forming one type of dual damascene structure, a first dielectric layer **30** is deposited on a substrate **32**, followed by an etch stop **34** deposition. The etch stop is pattern etched to define contact/via openings **40** and to expose the first dielectric layer in the areas where the contacts/vias are to be formed. A second dielectric layer **38** is deposited over the etch stop and patterned to define interconnect lines, preferably using conventional photolithography processes with a photoresist layer, as would be known to those with ordinary skill in the art. The interconnects and contacts/vias are then etched using reactive ion etching or other anisotropic etching techniques and any photoresist or other material used to pattern the layers is removed using an oxygen strip or other suitable process. A barrier layer **44** is then preferably deposited conformally in the metallization pattern to prevent metal migration into the surrounding silicon and/or dielectric material.

[**0041**] With the present invention, the above plasma reducing process may be useful on the barrier layer or other layers deposited prior or subsequent to the metal layer. The regime and parameters discussed above for the plasma reduction of the conductor could be adjusted for the particular layer in question.

[**0042**] The metal layer **47** is deposited in the vias and lines and is preferably a conductive material such as aluminum, copper, tungsten or combinations thereof with the recent trend being copper. The metal layer is deposited using either CVD, PVD, electroplating, or combinations thereof to form the conductive structure. Once the structure has been filled with copper or other metal, a CMP process may be used to planarize the metal surface. In other embodiments, a sacrificial layer may be deposited on the field areas between the interconnects prior to the metal deposition, and then the sacrificial layer stripped after the metal is deposited, leaving a surface suitable for the next stage of the deposition process. The structure surface may be planarized, using a CMP process at this stage and/or at other stages. The above plasma reducing process may be initiated to remove or reduce a contaminant layer **48**, such as copper oxide, that may have formed on the metal layer **47**, including the interconnects **46**. In the preferred embodiment, the plasma reducing process is applied in situ with the deposit of the adjoining layer **50**, shown in **FIG. 7**. This layer may be another dielectric layer, a barrier layer, a passivation layer, or some other layer beside the metal layer.

[**0043**] Specifically, the process steps could include: depositing a first dielectric layer, such as a fluorinated silicate glass (FSG) layer, on a substrate, depositing a low k dielectric etch stop on the first dielectric layer, patterning the etch stops to define the contacts/vias, stripping the patterning medium such as a photoresist layer, depositing a second dielectric layer, such as an FSG layer, and patterning a resist layer on the second dielectric layer to define one or more interconnects. Once the dual damascene structure has been formed, the process can include: depositing a barrier layer in the structure, depositing a metal layer such as copper, and exposing an oxidized surface of the metal layer to a plasma with the reducing agent to reduce the oxide. Another layer, such as a nitride, may then be deposited over the surface in situ with the reducing process.

[**0044**] While the foregoing is directed to the preferred embodiment of the present invention, other and further embodiments of the invention may be devised without departing from the basis scope thereof, and the scope thereof is determined by the claims that follow. Furthermore, in this specification, including particularly the claims, the use of "comprising" with "a" or "the", and variations thereof means that the item(s) or list(s) referenced includes at least the enumerated item(s) or list(s) and furthermore may include a plurality of the enumerated item(s) or list(s), unless otherwise stated.

1. A semiconductor device comprising:

an interface defined by a first insulating layer comprising silicon carbide and one or more conductive pathways disposed within said layer, the interface having oxidation reduced portions; and

a second insulating layer disposed upon said interface coincident with removal of said oxidation reduced portions.

2. The semiconductor device of claim 1 wherein the second insulating layer comprises at least one layer selected from the group consisting of a patterned etch stop layer, a barrier layer, and a film comprising silicon carbide.

3. The semiconductor device of claim 1 wherein the conductive pathways are formed from at least one of copper, titanium, tantalum, and tungsten.

4. A semiconductor device comprising:

an interface defined by a first insulating layer and one or more conductive pathways disposed within said layer, the interface having oxidation reduced portions; and

a second insulating layer comprising silicon carbide disposed upon said interface coincident with removal of said oxidation reduced portions.

5. A semiconductor device interface comprising:

a layer comprising silicon carbide;

one or more conductive devices disposed within said layer, said layer and conductive devices defining said interface,

wherein said interface is treated with a continuous plasma treatment to remove oxidation and deposit a second layer thereupon.

6. The semiconductor device interface of claim 5 wherein the conductive devices are formed from at least one of copper, titanium, tantalum, and tungsten.

* * * * *