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KROKOSZINSKI et al.

(54) **METHOD FOR PRODUCING MONOCRYSTALLINE N-SILICON SOLAR CELLS, AS WELL AS A SOLAR CELL PRODUCED ACCORDING TO SUCH A METHOD**

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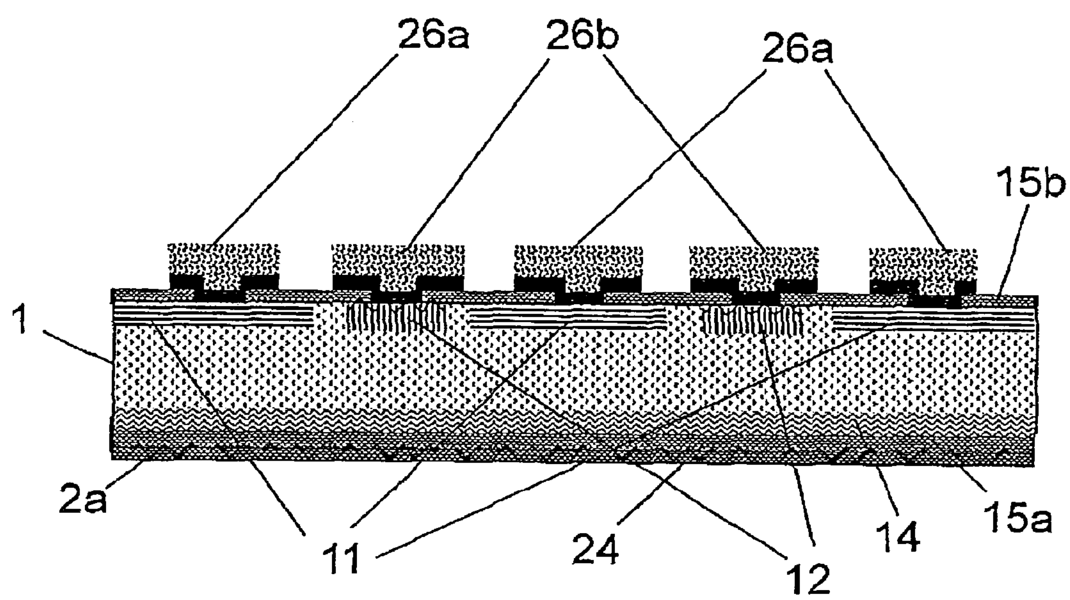
USPC **136/256**

(57) **ABSTRACT**

A method for producing monocrystalline n-silicon solar cells having a rear-side passivated p^+ emitter and rear-side, spatially separate heavily doped n^{++}-base regions near the surface, as well as an interdigitated rear-side contact finger structure, which is in conductive connection with the p^+-emitter regions and the n^{++}-base regions. An aluminum thin layer or an aluminum-containing thin layer is first deposited on the rear side of the n-silicon wafer, and the thin layer is subsequently structured so that openings are obtained in the region of the future base contacts. In a further process step, the aluminum is then diffused into the n-silicon wafer in order to form a structured emitter layer.



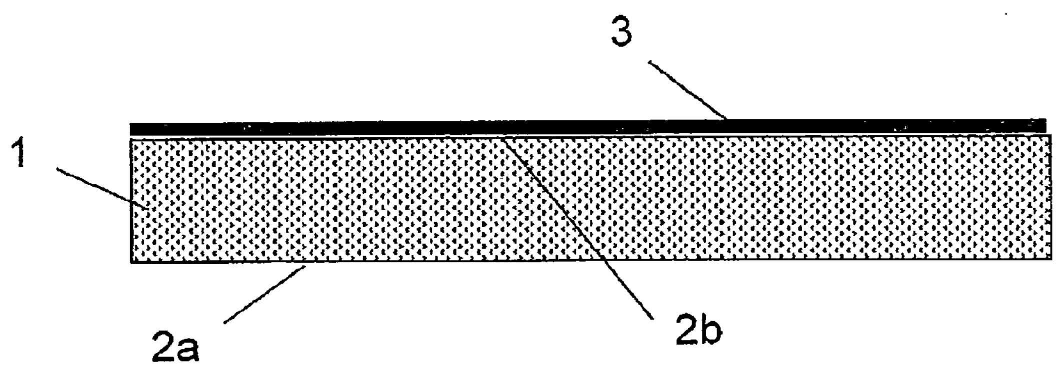


Fig. 1

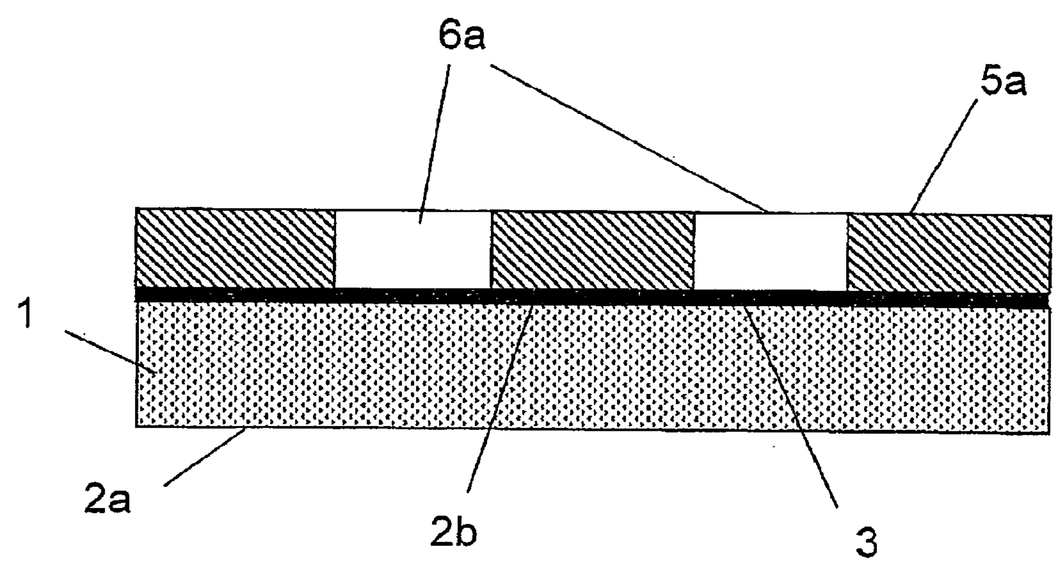


Fig. 2

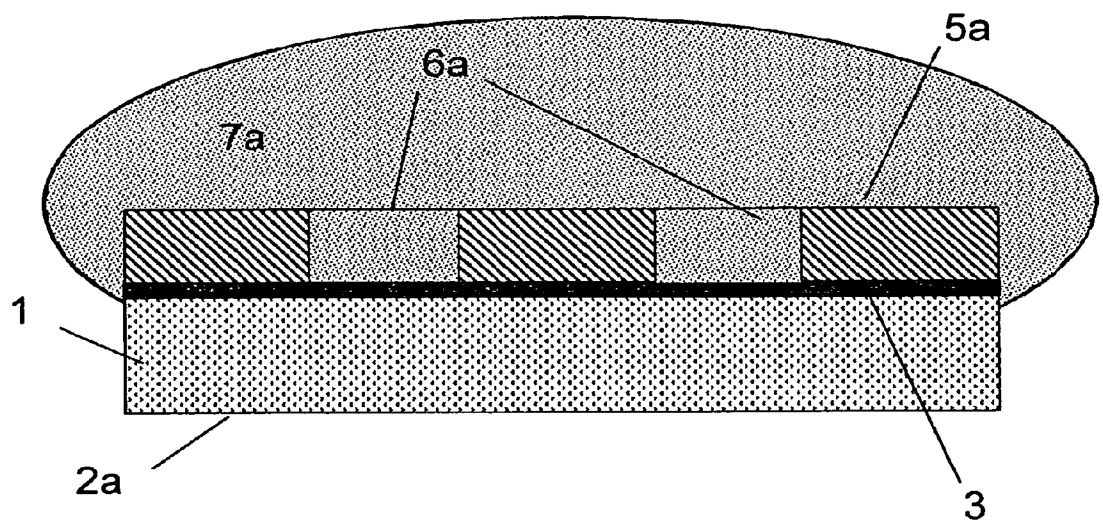


Fig. 3

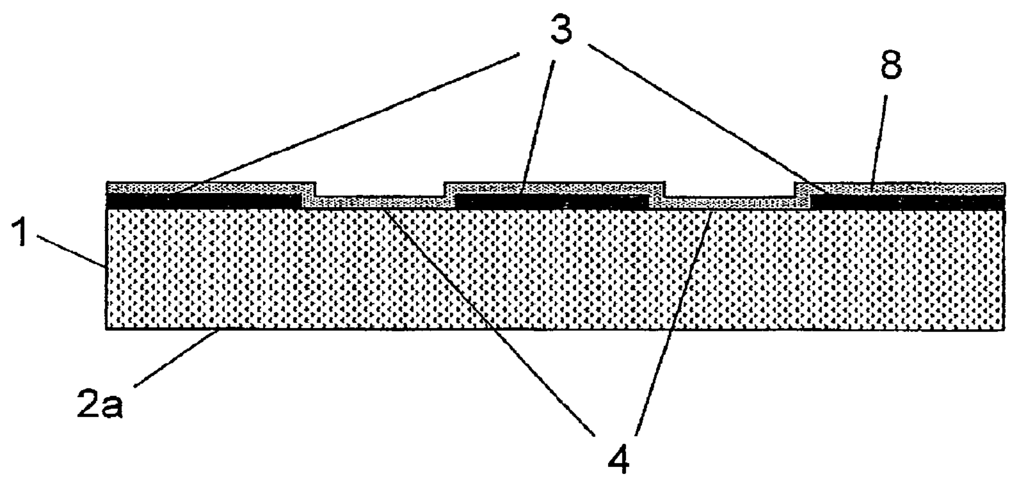


Fig. 4

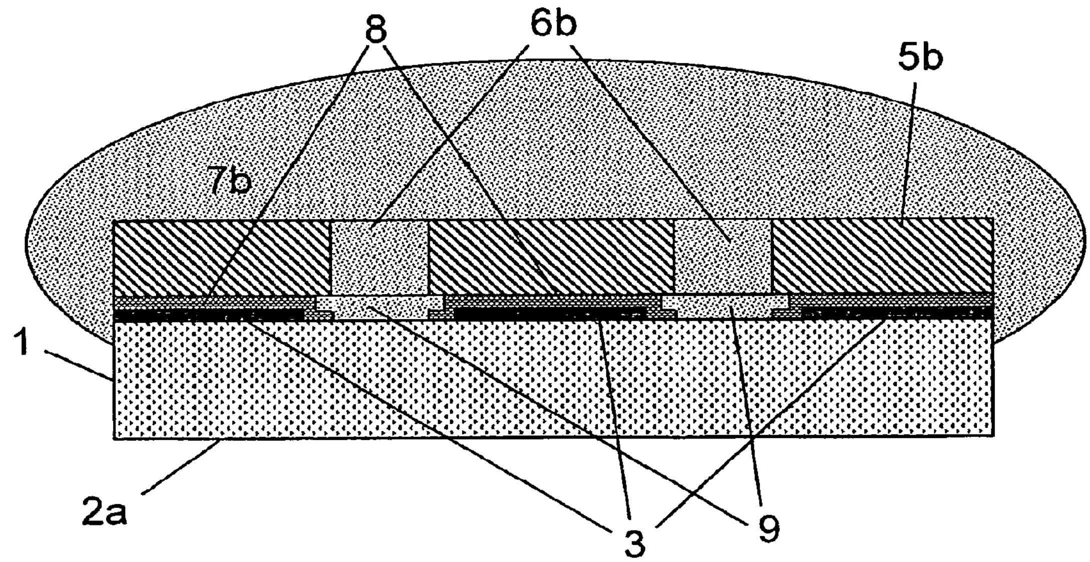


Fig. 5

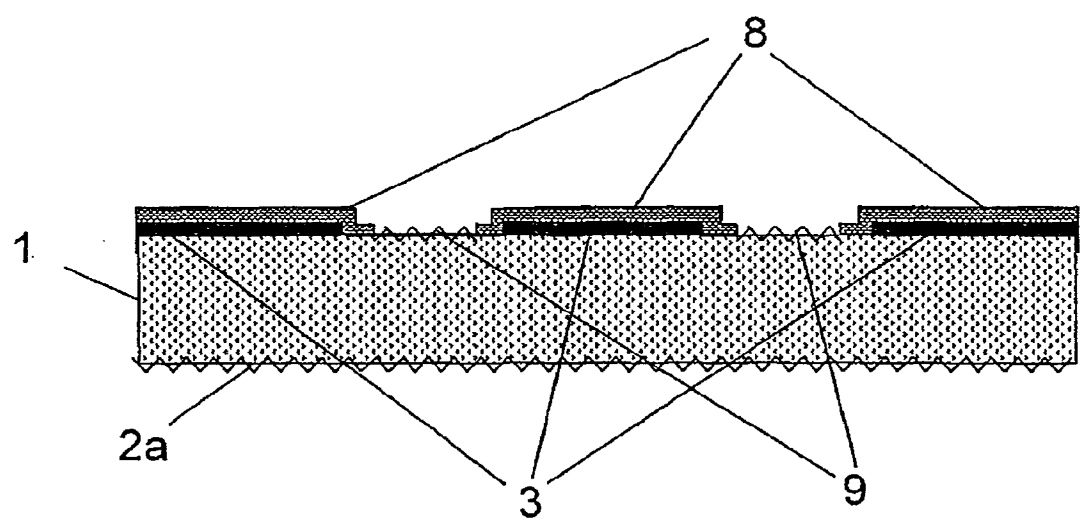


Fig. 6

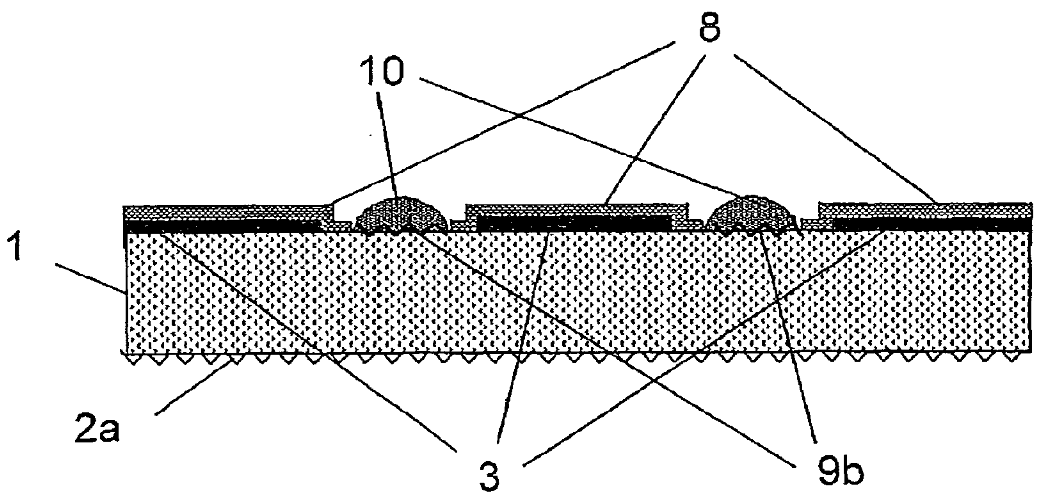


Fig. 7

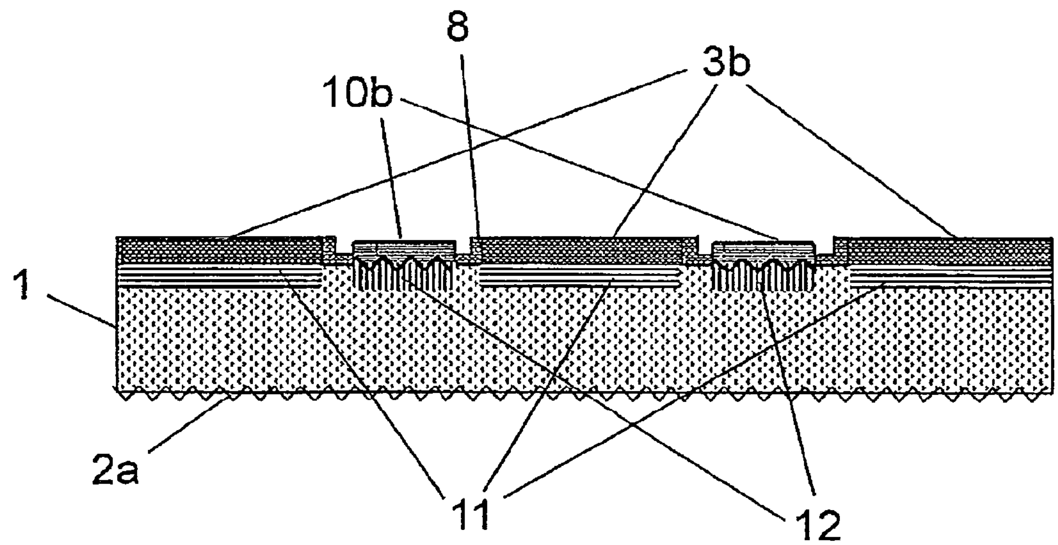


Fig. 8

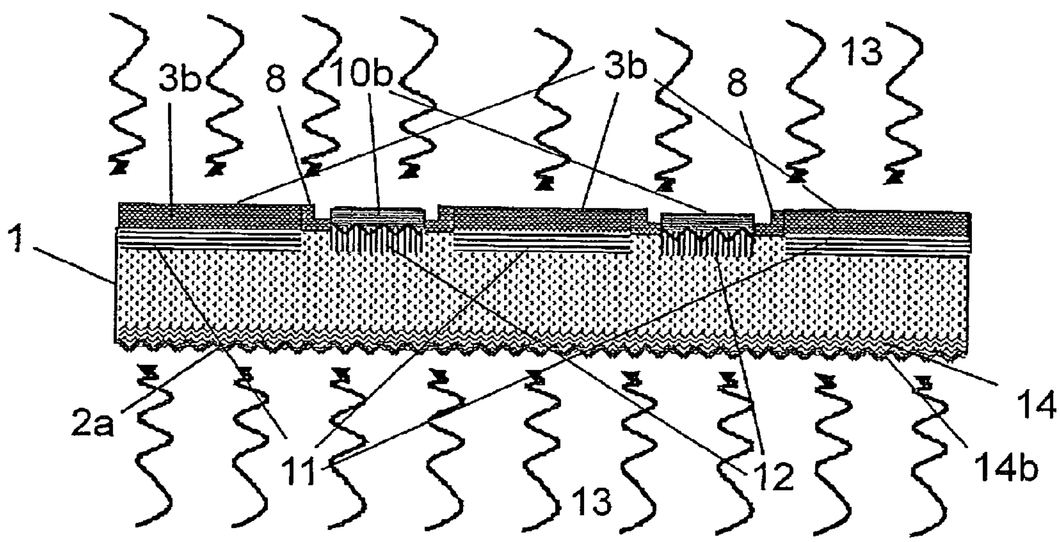


Fig. 9

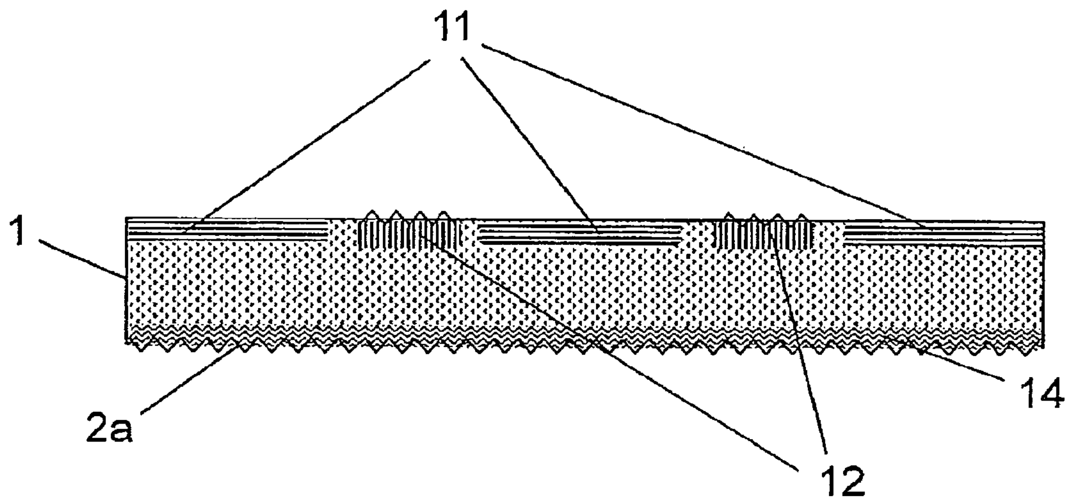


Fig. 10

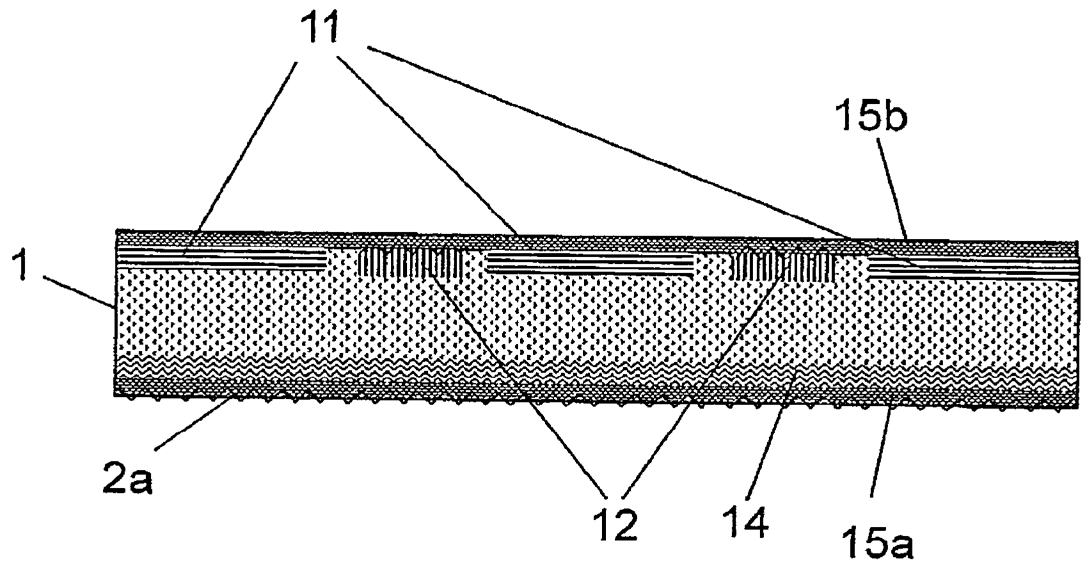


Fig. 11

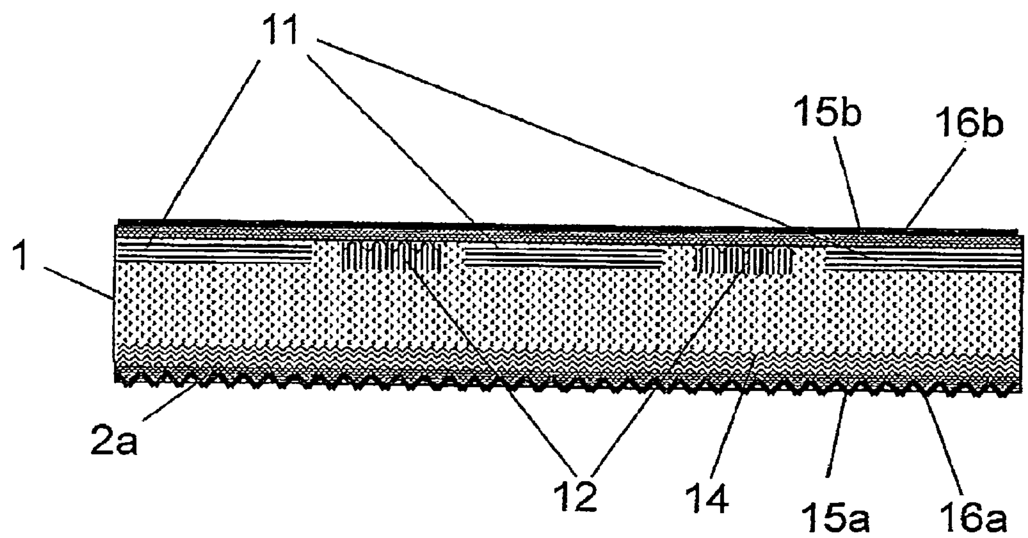


Fig. 12

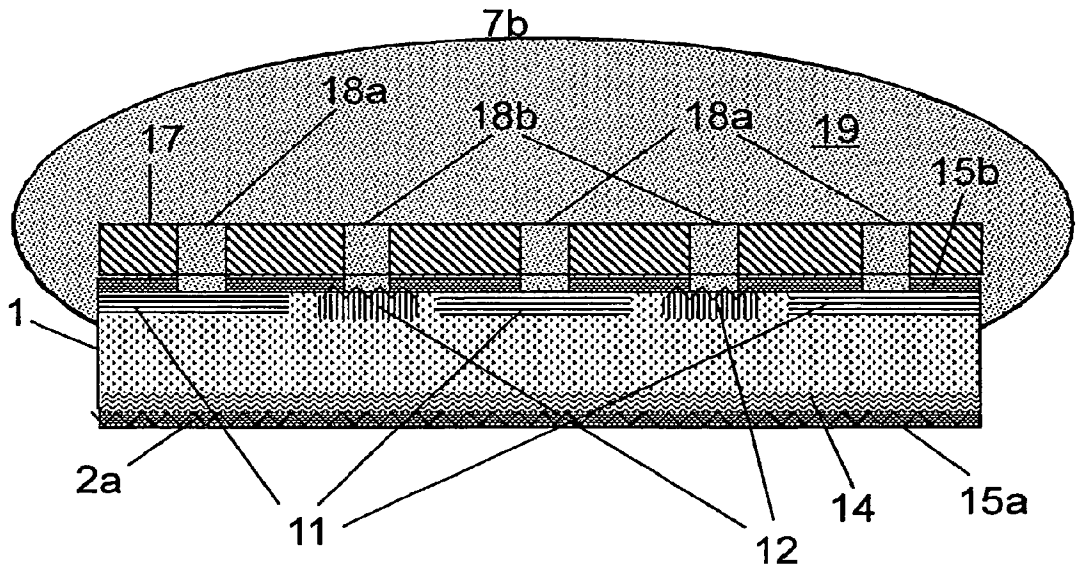


Fig. 13

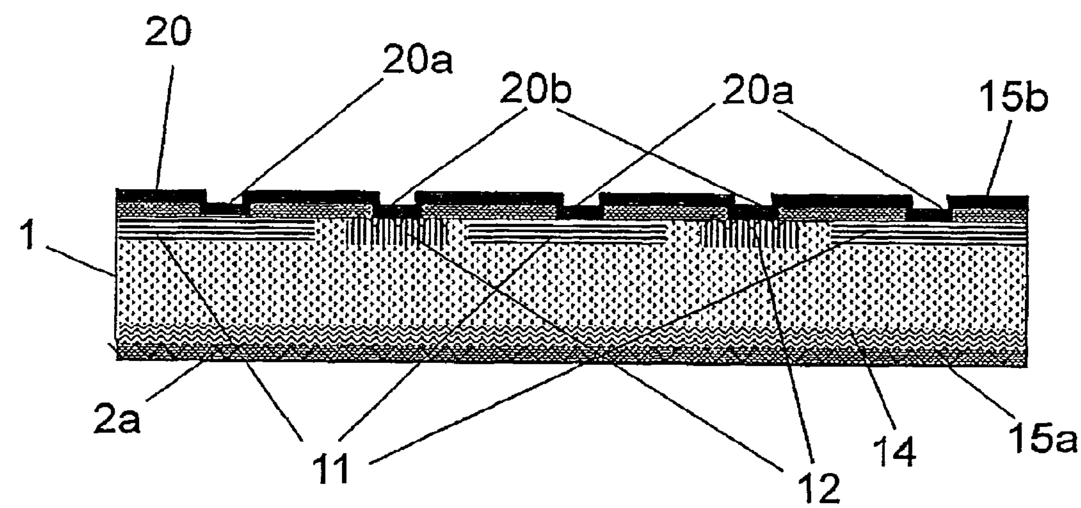


Fig. 14

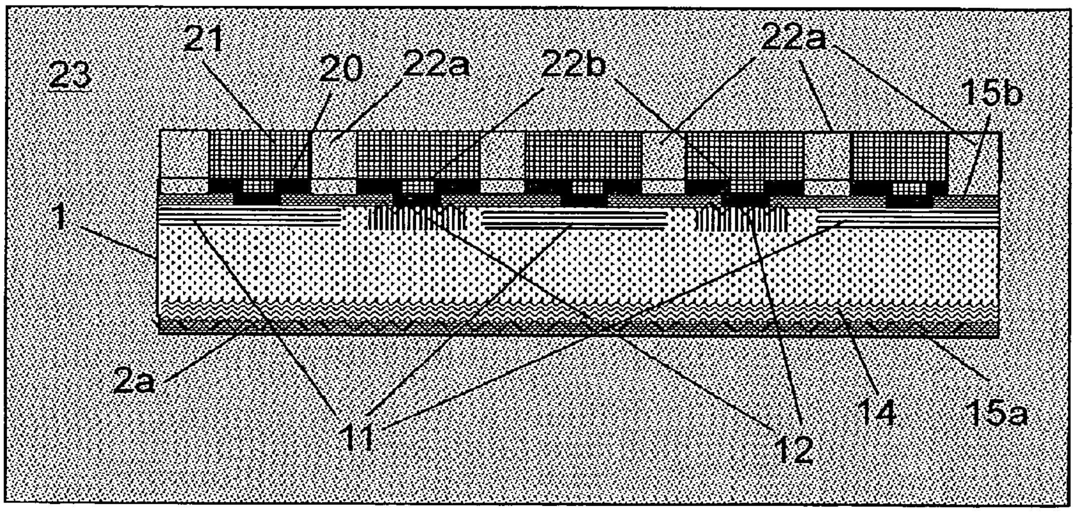


Fig. 15

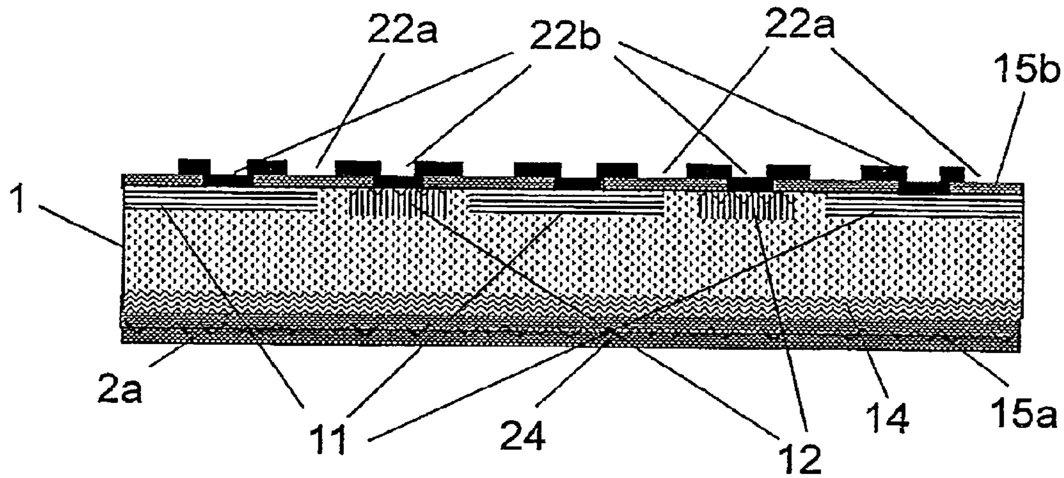


Fig. 16

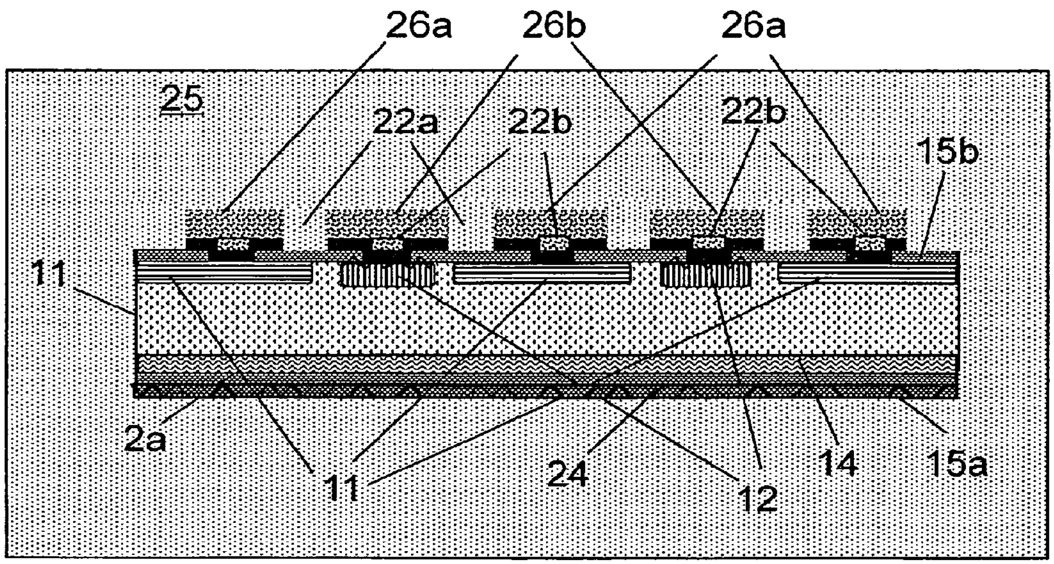


Fig. 17

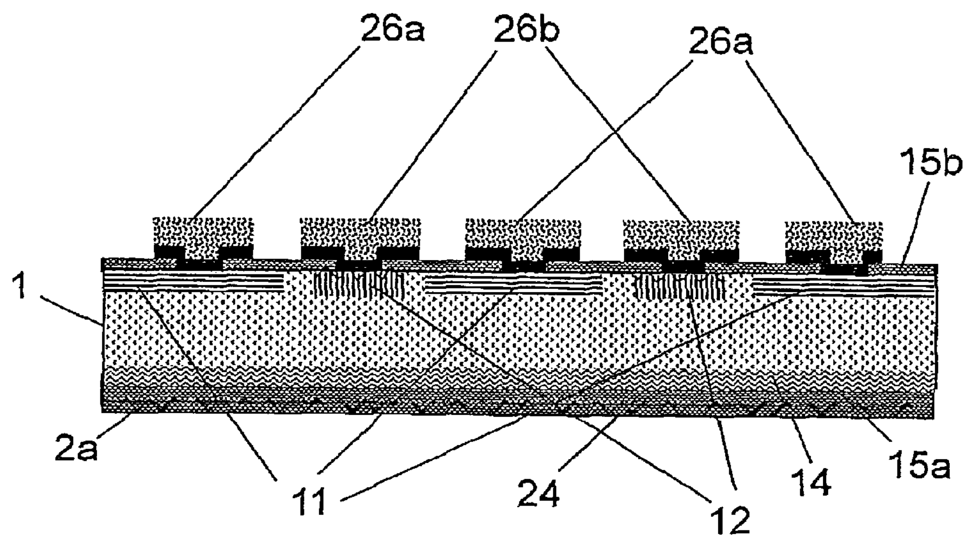


Fig. 18

METHOD FOR PRODUCING MONOCRYSTALLINE N-SILICON SOLAR CELLS, AS WELL AS A SOLAR CELL PRODUCED ACCORDING TO SUCH A METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a divisional application of U.S. patent application Ser. No. 12/735,751, filed on Oct. 25, 2010, which is a national phase application of International Patent Application No. PCT/EP2009/051569, filed Feb. 11, 2009, and claims priority to German Patent Application No. 10 2008 009 268.1, filed Feb. 15, 2008 and to German Patent Application No. 10 2008 013 446.5, filed Mar. 10, 2008, all of which are hereby incorporated herein by reference in their entireties.

FIELD OF THE INVENTION

[0002] The present invention relates to a method for producing monocrystalline n-silicon solar cells having a p^+ emitter on the rear side and spatially separate, heavily doped n^{++} base regions near the surface on the rear side, as well as an interdigitated rear-side contact finger structure, which is in conductive contact with the p^+ emitter regions and the n^{++} base regions, and it also relates to a solar cell produced according to such a method.

BACKGROUND INFORMATION

[0003] Back contact solar cells on monocrystalline n-Si wafers have been developed by different solar cell manufacturers for a number of years, and some of these cells are already available on the market.

[0004] For example, reference is made to the so-called A300 cell by SunPower (cf. W. D. Mulligan, D. H. Rose, M. J. Cudzinovic, D. M. DeCeuster, K. R. McIntosh, D. D. Smith, R. M. Swanson, "Manufacture of solar cells with 21% efficiency," Proceedings of the 19th European Photovoltaic Solar Energy Conference, Paris, France (2004)). The A300 cell is a so-called interdigitated back contact cell (IBC), which means that both the emitter and the BSF (back surface field) or base contact strips are situated on the rear side of the cell and are developed in the form of two meshing fork structures.

[0005] The required electrical separation of adjacently located n-doped and p-doped semiconductor regions on the same surface may be achieved in different ways. For example, there is the possibility of placing the two regions at different levels by removing the silicon oxide precipitated on the rear surface around the regions provided as base contacts using laser ablation (P. Engelhardt, N.-P. Harder, T. Neubert, H. Plagwitz, B. Fischer, R. Meyer and R. Brendel, "Laser Processing of 22% Efficient Back-Contacted Silicon Solar Cells," 21st European Photovoltaic Solar Energy Conference, Dresden, 2006, p. 1).

[0006] Once the surface damage caused by the laser process, and approx. 20 μm of the silicon have been removed by wet-chemical etching, the emitter doping with phosphorus into the deeper-lying regions of the rear side, the front side and the connecting holes between front emitter and rear side emitter is implemented simultaneously, with the aid of a standard $POCl_3$ process.

[0007] The metallic coating of both regions then takes place in a single aluminum vapor deposit step, the contact regions being electrically separated from each other by tearing the thin metal layer at the produced, virtually perpendicular step structure in the semiconductor surface.

[0008] Technologies for the production of passivated emitters and of local spot contacts to the two semiconductor regions of base and emitter are likewise known and acknowledged in the literature (cf. R. A. Sinton, Y. Kwark, R. M. Swanson, "Recombination Mechanisms in Silicon Solar Cells," 14th Project Integration Meeting, Photovoltaic Concentrator Technology Project, June 1986, p. 117-125).

[0009] The local opening of the passivation layer, which simultaneously is the insulation between the semiconductor regions and the superposed metallic current paths, is increasingly implemented with the aid of lasers. On the one hand, so-called laser ablation is employed for removing the insulation layer only locally. On the other hand, the so-called laser-fired contact method (LFC) is employed, in which laser flashes move the vapor-deposited or sputtered aluminum layer through the insulating layer in order to contact the semiconductor regions lying underneath.

[0010] From DE 696 31 815 T2, it is known to use an AlSi eutecticum as conductor base for the p-emitter structure, which is produced on the surface once the aluminum has diffused into the silicon through a previously inwardly diffused n^+ layer of the rear side. The solution there also uses screen printing of aluminum paste through oxide windows above the n-base regions. The disadvantage of this solution is that the aluminum doping and the contacting of the aluminum emitter must be implemented in one step, i.e., across a large surface, so that the surface of the emitter and the surface of the metal contacting are identical. Thus, no passivation of the emitter with local contacts is possible. This results in a large surface recombination rate and thus relatively low efficiency.

[0011] Both the laser ablation and the LFC method for the production of local contacts have the disadvantage that these methods are of sequential nature. In other words, the holes for each wafer must be produced individually, one after the other.

SUMMARY OF THE INVENTION

[0012] In view of the above, it therefore is an object of the exemplary embodiments and/or exemplary methods of the present invention to provide a further developed method for producing monocrystalline n-silicon solar cells having rear-side, passivated p^+ emitters and spatially separate, heavily doped n^{++} base regions near the surface, as well as an interdigitated rear-side contact finger structure, which allows high productivity and avoids the disadvantages of the related art.

[0013] Furthermore, it should be possible to combine technological steps, particularly steps that cost considerable time in the production process, in order to ensure a further improvement in productivity.

[0014] Furthermore, the use of wafer-protecting technologies known from the production of microelectronics chips, such as sputtering, vapor deposition, CVD, masked dry-etching of aluminum and of oxides using different halogen plasmas, as well as ink-jetting are to be made available for the production of solar cells.

[0015] According to the exemplary embodiments and/or exemplary methods of the present invention, for the method this objective is achieved by the features described herein, and with regard to the solar cell, it is achieved by a subject matter according to the feature combination as further described herein, the further embodiments representing at least useful specific developments and further improvements.

[0016] An important aspect as to the exemplary embodiments and/or exemplary methods of the present invention is the production of a rear-side, locally diffused and passivated aluminum emitter and the possibility of carrying out simultaneous two-sided and local n^+ doping of n-silicon in the rear-side and front-side n-base regions near the surface. According to the exemplary embodiments and/or exemplary methods of the present invention, the diffusion steps for the emitters and the BSF or FSF region to be produced may be carried out in a common thermal treatment step for the diffusion of the selected emitter doping material of aluminum and the selected BSF/FSF dopant of phosphorus.

[0017] The wafer may already be textured on one side before the aluminum-containing starting layer for the emitter doping is deposited and structured. However, it is also quite possible to carry out the texturing of the wafer only after the aluminum has been deposited and coated with an etch-resistant oxide on the rear side, so that the emitter, and thus the largest part of the rear side, remains untextured.

[0018] As for the rest, the exemplary embodiments and/or exemplary methods of the present invention also shows the process sequence leading up to the finished rear-contacted solar cell, i.e., including the passivation of the front and back sides as well as the production of the contact structure, including the chemical or galvanic reinforcement.

[0019] Essential for the exemplary embodiments and/or exemplary methods of the present invention is also the lateral separation of the emitter and base doping materials embodied in the finished solar cell, and thus the cell production technology, which is novel for solar cells.

[0020] The basis of the method according to the present invention is the deposition of an aluminum or aluminum-containing thin layer on the rear side of the n-silicon wafer as well as the subsequent structuring of this thin layer, through which openings are obtained in the region of the future base contacts. In a further process step, the aluminum is then diffused into the n-silicon wafer in order to form a structured emitter layer. Thus, the aluminum or aluminum-containing layer is structured before being diffused into the wafer itself.

[0021] The mentioned aluminum thin layer may be deposited on the wafer by a vapor-deposition or sputter process.

[0022] The structuring of the deposited aluminum thin layer is performed in the form of strips, which may be by selective etching. Toward this end, dry-etching methods via a metal shadow mask may be employed, but the use of an organic mask is possible as well. Wet-chemical etching may of course be performed as well or selective etching using local printing of an etching paste.

[0023] In a further method step, the structured emitter layer is covered by a dielectric protective layer across the entire surface. Furthermore, this protective layer is opened up in future base doping regions, which may again be realized by etching or with the aid of an etching mask.

[0024] Then, the silicon wafer is subjected to texturing, which takes place on the front side of the wafer and in the region of the openings in the dielectric protective layer.

[0025] These openings may be formed via a strip-etching mask, the width of the produced openings being smaller than the width of the strip-shaped regions in the aluminum-free wafer.

[0026] Material having high phosphorus content is deposited in the region of the openings in the dielectric protective layer in order to produce the heavily doped n^{++} BSF base regions near the surface.

[0027] This deposition may also be implemented by applying a paste using screen printing or stencil printing, by ink-jetting in local deposits or by similar methods.

[0028] If necessary, the applied paste is subjected to a drying step.

[0029] The BSF doping material is then diffused in a thermal treatment step consisting of one step or multiple steps.

[0030] The diffusing of the aluminum as emitter dopant and the diffusing of the BSF doping material may be performed in a common treatment step in an especially economic process.

[0031] A flat phosphorus diffusion layer (FSF—front surface field) on the front side of the wafer in the region of the openings in the dielectric protective layer may be produced by an additional thermal treatment in a phosphorus-containing atmosphere, in particular a $POCl_3$ atmosphere, which has a layer resistance that is adjustable via the treatment temperature and the treatment time.

[0032] With the aid of an etch bath, residual doping material, produced phosphorus silicate glass, residue from the insulation layer as well as produced AlSi eutecticum layers are removed, so that the emitter regions, the BSF region, and the possibly existing front-side n^+-FSF structure are exposed.

[0033] Subsequently, the wafer is covered by a passivation layer, e.g., a silicon oxide layer. The passivation layer is then locally removed in the emitter regions and the BSF regions on the rear side of the wafer. The entire rear side of the wafer is then covered by a conductive layer, especially an aluminum layer. This conductive layer is used to form the interdigitated contact-finger structure.

[0034] A new type of solar cell is obtained as a result of the briefly outlined method, the n^{++} base regions on the wafer's rear side having a lateral clearance from the p^+-emitter regions, and at least the n^{++}-base regions having a concentration of the emitter doping material that lies below the n-base concentration of the initial wafer.

[0035] The exemplary embodiments and/or exemplary methods of the present invention will be explained in greater detail in the following text with the aid of an exemplary embodiment, using schematic illustrations of the individual process steps.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] FIG. **1** shows in a first method step, an entire rear side **2***b* of n-silicon wafer **1**, which is untextured in the illustrated example, is covered by an aluminum or aluminum-containing layer **3**, which forms the emitter dopant.

[0037] FIG. **2** shows aluminum-containing layer **3** is brought into contact with a shadow mask **5***a*.

[0038] FIG. **3** shows a dry-etching step in plasma **7***a* containing chlorine gas.

[0039] FIG. **4** shows a further process step according to the present invention that pertains to the coating of the strip-shaped, structured, aluminum-containing layer **3** by a dielectric layer **8**.

[0040] FIG. **5** shows, in a further method step, dielectric layer **8** is then removed by a masked etching step in the region of openings **6***b* of an additional mask **5***b*.

[0041] FIG. **6** shows standard-type texturing is then implemented by dipping in a bath of KOH and isopropyl alcohol (IPA).

[0042] FIG. 7 and FIG. 8 show a first thermal treatment step takes place at temperatures ranging from 900° C. to 1100° C. in a nitrogen-oxygen mixture, which causes the desired co-diffusion.

[0043] FIG. 9 shows an optional second thermal treatment step at said usually lower temperatures, only this time using the $POCl_3$ atmosphere.

[0044] FIG. 10 shows, in the following further course of the process, the residues of doping paste **10***b*, produced phosphorus silicate glass PSG **14***b*, dielectric masking layer **8**, and AlSi eutectic layer **3***b* are etched off in suitable etch baths, so that emitter regions **11**, BSF region **12**, and front-side n^+ layer **14** are exposed.

[0045] FIG. 11 shows both sides are coated by a dielectric in a further method step, e.g., by thermal oxidation of both sides of the wafer in a water vapor atmosphere, so that a silicon oxide layer results on front side **15***a* and rear side **15***b*.

[0046] FIG. 12 shows that the annealing process realized in the manner described leads to excellent surface-passivation results.

[0047] FIG. 13 shows passivation layer **15***b* is locally removed on the rear side in all emitter and BSF regions, i.e., simultaneously by masked dry etching in a plasma **7***b* containing fluorine gas, or without masking by laser ablation, for instance.

[0048] FIG. 14 shows, in the following process step, the entire rear side is covered by an aluminum layer **20**, so that all contact surfaces **20***a* and **20***b* exposed in the preceding etching step are metalized, but otherwise are insulated from the semiconductor regions emitter **11** and BSF **12** by layer **15***b*.

[0049] FIG. 15 shows that by applying an acid-resistant layer **21**, which may be by structured inkjet-printing, aluminum layer **20** is then subdivided into emitter contact traces and BSF contact traces, and this application is performed so that narrow interspaces **22***a* between planned contact regions **22***b* are left free, in which the aluminum is removed by an acid **23** that etches aluminum selectively, that is to say, does not attack silicon oxide.

[0050] FIG. 16 shows, in a supplementary process step, an anti-reflection layer **24**, which may be of silicon nitride, is formed on the front side.

[0051] FIG. 17 shows all contacts on the rear side may simultaneously and additionally be provided with a thick metallic conductive layer in a chemical or galvanic bath **25** or with the aid of a possibly light-based deposition process.

[0052] FIG. 18 shows, after rinsing and drying the wafer, the back-contacted solar cell is functional.

DETAILED DESCRIPTION

[0053] In a first method step according to FIG. 1, entire rear side **2***b* of n-silicon wafer **1**, which is untextured in the illustrated example, is covered by an aluminum or aluminum-containing layer **3**, which forms the emitter dopant. The front side of the wafer is denoted by reference numeral **2***a*, and the rear side by reference numeral **2***b*.

[0054] In a further step, aluminum-containing layer **3** is brought into contact with a shadow mask **5***a* and structured by a dry-etching step in plasma **7***a* containing chlorine gas (cf. FIGS. 2 and 3).

[0055] As an alternative, an organic mask layer may be applied as well, e.g., by so-called ink-jetting, and the aluminum in the regions that have remained free then be etched in a wet-chemical manner.

[0056] The two discussed technological variants produce longitudinal openings **4** in the form of strips in the region of breakthroughs **6***a* of mask **5***a*.

[0057] At a later point, the BSF doping material is diffused into strip-shaped openings **4** in aluminum layer **3** at a lateral distance to the aluminum edge.

[0058] A further process step according to the exemplary embodiments and/or exemplary methods of the present invention then pertains to the coating of the strip-shaped, structured, aluminum-containing layer **3** by a dielectric layer **8** (cf. FIG. 4). Dielectric layer **8** may be made from an oxide, e.g., SiO_2, TiO_2, or Al_2O_3.

[0059] It is also possible to form a silicon nitride layer, which likewise is impermeable to phosphorus diffusion. The deposition of layer **8** may be performed by reactive sputtering or by a CVD- or PECVD method.

[0060] In a further method step, dielectric layer **8** is then removed by a masked etching step in the region of openings **6***b* of an additional mask **5***b* according to FIG. 5.

[0061] This may be a dry-etching step in a plasma **7***b* containing fluorine gas, penetrating a metal foil mask, or by a dry-etching step in a plasma atmosphere containing fluorine gas, penetrating an organic mask layer, or a wet-chemical etching process, penetrating an organic mask layer.

[0062] According to the exemplary embodiments and/or exemplary methods of the present invention, the strip-shaped openings **6***b* in mask **5***b* and the resulting strip-shaped regions **9** exposed in dielectric layer **8** are smaller than the strip-shaped openings **6***a* in mask **5***a*, and thus in aluminum-containing layer **3**.

[0063] This prevents the occurrence of a short-circuit between the emitter regions and the BSF regions during the phosphorus doping in the next process step.

[0064] According to the illustration in FIG. 6, standard-type texturing is then implemented by dipping in a bath of KOH and isopropyl alcohol (IPA), for example. Since aluminum-containing layer **3** is protected by dielectric layer **8**, the texturing in the desired manner takes place only on front side **2***a* of the wafer and in the exposed strip-shaped regions **9***b* on the rear side of the wafer.

[0065] Subsequently, openings **9** in cover layer **8** in the openings of emitter layer **4** are covered by a material having a large phosphorus component, which may be a paste, which is able to be deposited on the surface of wafer **1** in local deposits **10** by screen printing, stencil printing or ink-jetting, for example. If necessary, this paste is subjected to a drying step at temperatures of 150° C. to 200° C., for example.

[0066] According to the illustrations in FIGS. **8** and **9**, a one-step, or optionally a two-step, thermal treatment takes place with the possibility of a co-diffusion of the emitter dopant aluminum and the BSF doping material phosphorus from the dried, phosphorus-containing layer **10***b*.

[0067] A first thermal treatment step takes place at temperatures ranging from 900° C. to 1100° C. in a nitrogen-oxygen mixture, which causes the desired co-diffusion (FIG. **8**). A second treatment step optionally takes place at temperatures between 800° C. and 1000° C., i.e., in a phosphorus-containing gas **13**, which may be $POCl_3$.

[0068] The first high-temperature step causes an interdiffusion of silicon and aluminum and leads to a near-surface, mixed crystal layer **3***b* having an eutectic AlSi structure and the p^+-doping layer with Al profile **11**.

[0069] At the same time, the phosphorus from precursor deposit **10***b* diffuses into BSF regions **9***b*, into the silicon surface, and leads to a deep n^{++} doping **12**.

[0070] Due to the high temperatures of >1000° C. required for the aluminum diffusion, the diffusion profile of the phosphorus has a deeper characteristic than in P-diffusion processes around 900° C. that are otherwise the norm.

[0071] The optional second thermal treatment step at said usually lower temperatures, only this time using the $POCl_3$ atmosphere according to FIG. **9**, brings about not only the deep P-diffusion in the BSF regions of rear side **9***b*, but additionally a flat P-diffusion on front side **2***a*, which forms an FSF layer (front surface field) **14** having a layer resistance that is adjustable via the temperature and time, i.e., which may be high layer resistance.

[0072] Of course, the first thermal treatment step may also be performed prior to the step of coating with the phosphorus-containing paste and independently of the subsequent second thermal treatment step. In this case one advantage results from the fact that the process parameters of the second diffusion step at a lower temperature are able to be optimized, regardless of the process parameters of the first diffusion step at a higher temperature.

[0073] In the same way, the additional flat diffusion in the phosphorus-containing gas atmosphere, which may be by using $POCl_3$, may also be omitted if no front surface field layer **14** is desired as front-side passivation. On the other hand, this passivation could also be performed in an additional third diffusion process, in particular if the first phosphorus diffusion step has also been realized using $POCl_3$.

[0074] In the following further course of the process, the residues of doping paste **10***b*, produced phosphorus silicate glass PSG **14***b*, dielectric masking layer **8**, and AlSi eutectic layer **3***b* are etched off in suitable etch baths, so that emitter regions **11**, BSF region **12**, and front-side n^+ layer **14** are exposed, i.e., according to FIG. **10**.

[0075] As illustrated in FIG. **11**, both sides are coated by a dielectric in a further method step, e.g., by thermal oxidation of both sides of the wafer in a water vapor atmosphere, so that a silicon oxide layer results on front side **15***a* and rear side **15***b*.

[0076] Optionally, it is possible to coat both sides with a thin aluminum layer once a thermal oxide has formed on both wafer surfaces. The layer thickness may amount to a range between 10 nm and 100 nm. An aluminum layer **16***a* subsequently results on the front side, and an aluminum layer **16***b* on the rear side. The wafers, coated in this way, are then subjected to a thermal treatment at a range between 350° C. and 450° C. The annealing process realized in this manner leads to excellent surface-passivation results (cf. FIG. **12**).

[0077] When the aluminum layer has been etched off, the wafer is once again in a state as shown in FIG. **11**.

[0078] Furthermore, as shown in FIG. **13**, passivation layer **15***b* is locally removed on the rear side in all emitter and BSF regions, i.e., simultaneously by masked dry etching in a plasma **7***b* containing fluorine gas, or without masking by laser ablation, for instance. In the same way, the generally known LFC method may be used once the base metal coating has been deposited.

[0079] Openings **18***a* above emitter regions **11**, and openings **18***b* above the BSF regions in mask **17** are smaller than openings **6***b* in mask **5***b* of the preceding etching step.

[0080] For one, this facilitates the adjustment of the shadow mask or mask layer **17** on the already existing structure; for another, the contact regions of the metallization to the semiconductor material are to be small, if possible, in order to restrict the surface recombination.

[0081] In the following process step, the entire rear side is covered by an aluminum layer **20**, so that all contact surfaces **20***a* and **20***b* exposed in the preceding etching step are metalized, but otherwise are insulated from the semiconductor regions emitter **11** and BSF **12** by layer **15***b* (cf. FIG. **14**).

[0082] By applying an acid-resistant layer **21**, which may be by structured inkjet-printing, aluminum layer **20** is then subdivided into emitter contact traces and BSF contact traces. This application is performed in such a way that narrow interspaces **22***a* between planned contact regions **22***b* are left free, in which the aluminum is removed by an acid **23** that etches aluminum selectively, that is to say, does not attack silicon oxide (cf. FIG. **15**). During the inkjet printing, either an organic paste is used which dries on the surface, or a hot-melt wax is used, which is injected while warm and then solidifies on the wafer while cooling. Another possibility is the use of suitable ink, which is subjected to a drying process.

[0083] In a supplementary process step, as shown in FIG. **16**, an anti-reflection layer **24**, which may be of silicon nitride, is formed on the front side. With regard to thickness and refractive index, this anti-reflection layer is developed with a view toward optimum efficiency with respect to trapping energy from sunlight. Plasma-aided CVD or reactive sputtering, for instance, may be used to deposit this anti-reflection layer **24**.

[0084] It is preferred if the plasma CVD method is used for this purpose because it takes place at temperatures above 400° C. yet below 500° C. and therefore causes annealing of aluminum contact layer **20** and thus a reduction in the contact resistance, without risking an AlSi liquefaction at the eutectic temperature of 577° C.

[0085] According to FIG. **17**, all contacts on the rear side may simultaneously and additionally be provided with a thick metallic conductive layer in a chemical or galvanic bath **25** or with the aid of a possibly light-based deposition process. This results in the production of emitter circuit trace reinforcements **26***a* or BSF circuit trace reinforcements **26***b*. The individual layers may either consist of a single material of nickel, copper or silver, or of a plurality of individual layers of different metals, such as Ni+Cu+Sn or Ni+Ag or Ni+Au, for example.

[0086] After rinsing and drying the wafer, the back-contacted solar cell is functional, as shown in FIG. **18**. An edge insulation is not required since the lateral clearance and the oxide cover ensure the separation of emitter regions **11** and BSF regions.

What is claimed is:

1. A monocrystalline n-silicon solar cell, comprising:

a deposited thin layer, formed of one of aluminum and an aluminum-containing material, on a rear-side of an n-silicon wafer, wherein the thin layer is structured so that openings in the region of future base doping are obtained; and

a structured emitter layer, which is formed by diffusing aluminum into the n-silicon wafer in a further process;

wherein the monocrystalline n-silicon solar cell includes:

a p^+ emitter on the rear-side of the n-silicon wafer;

heavily doped n^{++}-base regions near the surface on the rear-side of the n-silicon wafer and spatially separate from the p^+ emitter; and an interdigitated rear-side contact finger structure, which is in conductive connection with the p^+-emitter regions and the n^{++}-base regions.

2. The solar cell of claim **1**, wherein the n^{++} base regions on the rear side of the wafer have a lateral clearance from the p^+-emitter, and wherein at least the n^{++}-base regions have a concentration of the emitter doping material that is below the n-base concentration of the n-silicon wafer.

3. The solar cell of claim **1**, wherein:

the n^{++}-base regions are formed of base doping deposited in the openings, and the rear-side p^+ emitter includes p^+ emitter regions in which the openings that include the base doping are formed; and

the diffused aluminum is aluminum of the thin layer.

4. The solar cell of claim **3**, wherein the diffusion of the aluminum as emitter dopant and a diffusion of the doping material for the n^{++}-base regions occurs in a common treatment operation.

5. The solar cell of claim **4**, wherein an insulaing layer is deposited over the the thin layer, and the doping material for the n^{++}-base regions is deposited into the openings subsequent to the deposition of the insulating layer.

6. The solar cell of claim **4**, wherein the thin layer is deposited by one of a vapor deposit process and a sputter process.

7. The solar cell of claim **4**, wherein the structure of the deposited thin layer is in the form of strips by selective etching.

8. The solar cell of claim **7**, wherein the selective etching includes dry-etching with a metal shadow mask.

9. The solar cell of claim **7**, wherein the selective etching includes dry-etching with an organic mask.

10. The solar cell of claim **7**, wherein the selective etching is performed in a wet-chemical manner using an organic ink mask.

11. The solar cell of claim **7**, wherein the selective etching is performed by local printing of an etching paste.

12. The solar cell of claim **4**, wherein residue of the existing thin layer is removed once the aluminum diffusion has been completed.

13. The solar cell of claim **4**, wherein the structured emitter layer is covered by a dielectric protective layer across the full surface, and wherein the dielectric protective layer is opened up in the regions of the future base contacts.

14. The solar cell of claim **13**, wherein the openings are formed in regions of the future base doping, with the aid of an etching mask.

15. The solar cell of claim **14**, wherein the openings are formed via a strip-mask, and wherein the width of the produced openings are smaller than the width of the aluminum-free, strip-shaped regions in the wafer.

16. The solar cell of claim **13**, wherein the silicon wafer is subjected to texturation.

17. The solar cell of claim **1**, wherein:

the diffused aluminum is aluminum of the thin layer;

the structured emitter layer is covered by a dielectric protective layer across the full surface;

the dielectric protective layer is opened up in the regions of the future base contacts; and

the silicon wafer is subjected to texturation that takes place on the front side of the wafer and in the region of the openings in the dielectric protective layer.

18. The solar cell of claim **17**, wherein material having a high phosphorus content is deposited in the region of the openings in the dielectric protective layer to produce the heavily doped n^{++}-base regions as back surface field (BSF) regions located near the surface.

19. The solar cell of claim **18**, wherein the deposition is implemented by applying a paste using one of screen printing, stencil printing, and ink-jetting in local deposits.

20. The solar cell of claim **19**, wherein the deposited paste is subjected to a drying operation.

21. The solar cell of claim **18**, wherein the doping material for the n^{++}-base regions is diffused in a thermal treatment operation.

22. The solar cell of claim **21**, wherein a further thermal treatment in a phosphorus-containing atmosphere, which includes $POCl_3$, occurs to produce a flat phosphorus diffusion layer (FSF—front surface field) on the front side of the wafer featuring a layer resistance that is adjustable by the treatment temperature and the treatment time.

23. The solar cell of claim **1**, wherein:

the diffused aluminum is aluminum of the thin layer; and

the p^+ emitter and the n^{++}-base regions are exposed by removal of the following via an etch bath: a residual doping material, a produced phosphorus silicate glass, residues of an insulation layer, and a produced AlSi eutecticum layer material.

24. The solar cell of claim **23**, wherein the wafer is covered by at least one passivation layer.

25. The solar cell of claim **24**, wherein the rear side of the wafer is locally freed of the passivation layer in the p^+-emitter and n^{++}-base regions to form local contact points.

26. The solar cell of claim **25**, wherein the entire rear side of the wafer is covered by a conductive layer, which includes an aluminum layer.

27. The solar cell of claim **26**, wherein the conductive layer is structured to form the interdigitated contact fingers.

28. The solar cell of claim **23**, wherein the diffusion of the aluminum as emitter dopant and diffusion of the doping material for the n^{++}-base regions occurs in a common treatment operation.

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