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(continued on next page)

(54) Abstract Title: **Filtered bias voltage for a MEMS capacitive transducer circuit**

(57) A MEMS capacitive transducer circuit comprises a MEMS capacitive transducer 3 having first and second electrodes, e.g. a microphone or an accelerometer. The first and second electrodes are biased by respective first and second bias voltages V1, V2. An amplifier 9 is connected to receive a first analogue signal generated by the capacitive transducer on an input terminal, and to generate a second analogue signal on an output terminal 9. A digital feedback circuit is 100 connected between the output terminal of the amplifier and the input terminal of the amplifier. The digital feedback circuit is configured to provide one of said first or second bias voltages. The output of a voltage source 5 which provides the other bias voltage for the capacitive transducer is filtered by a low pass filter 40. The low pass filter may comprise a switched capacitor filter circuit or an R-C filter circuit (fig 5b).

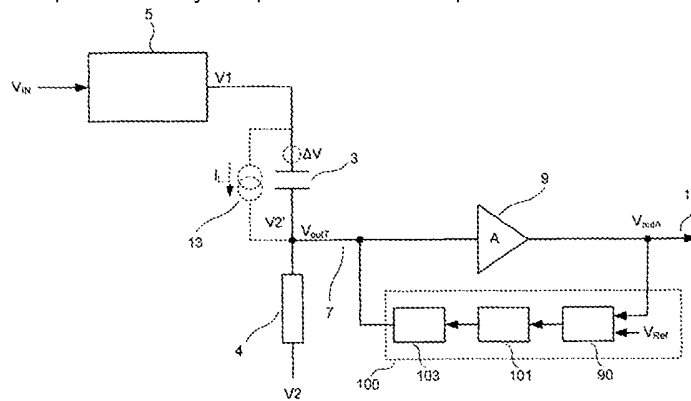


Figure 2

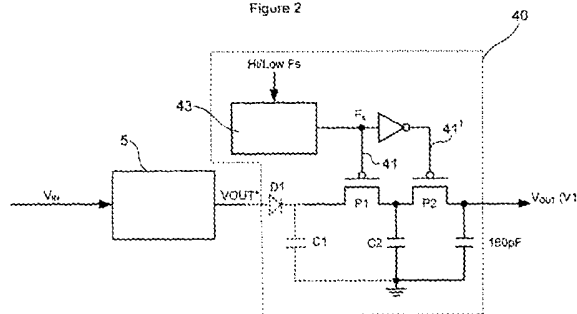


Figure 5a

**GB 2459864 A continuation**

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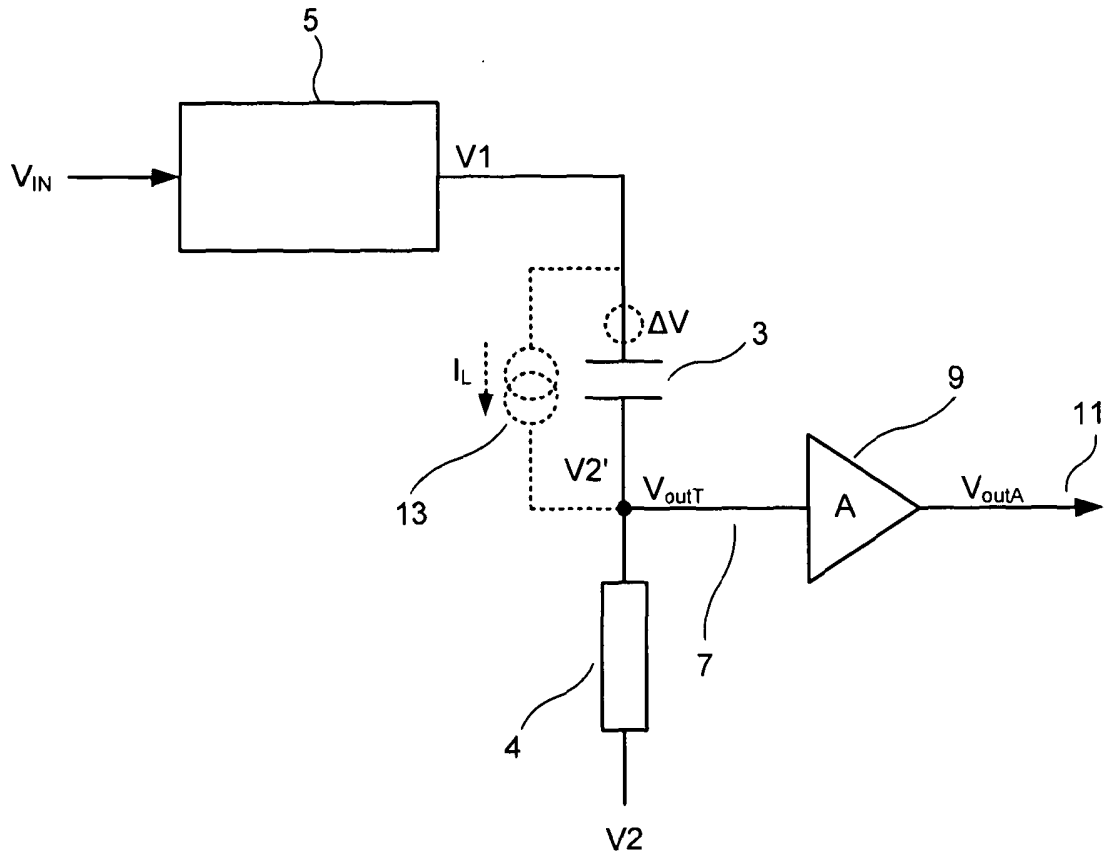


Figure 1

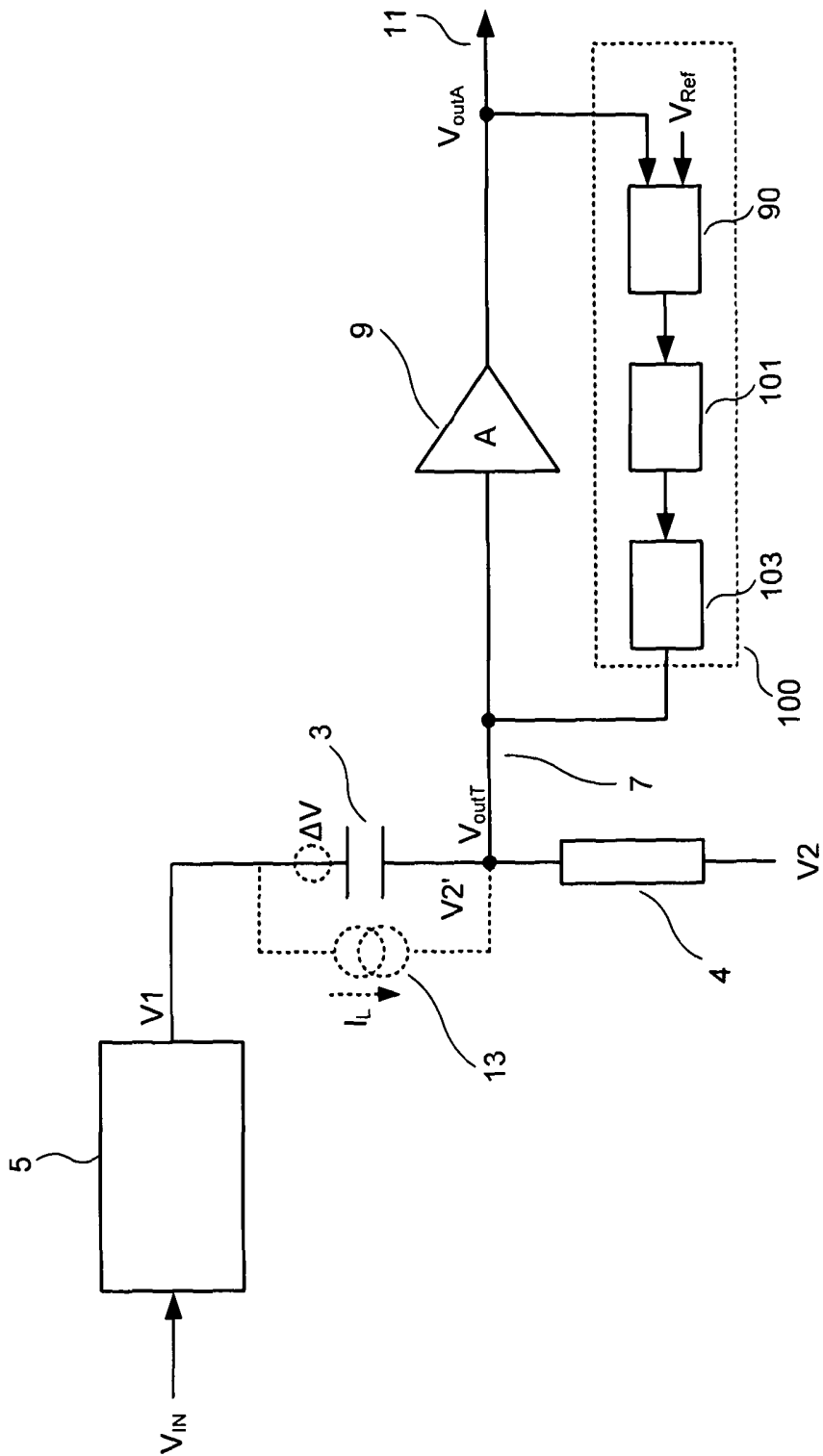


Figure 2

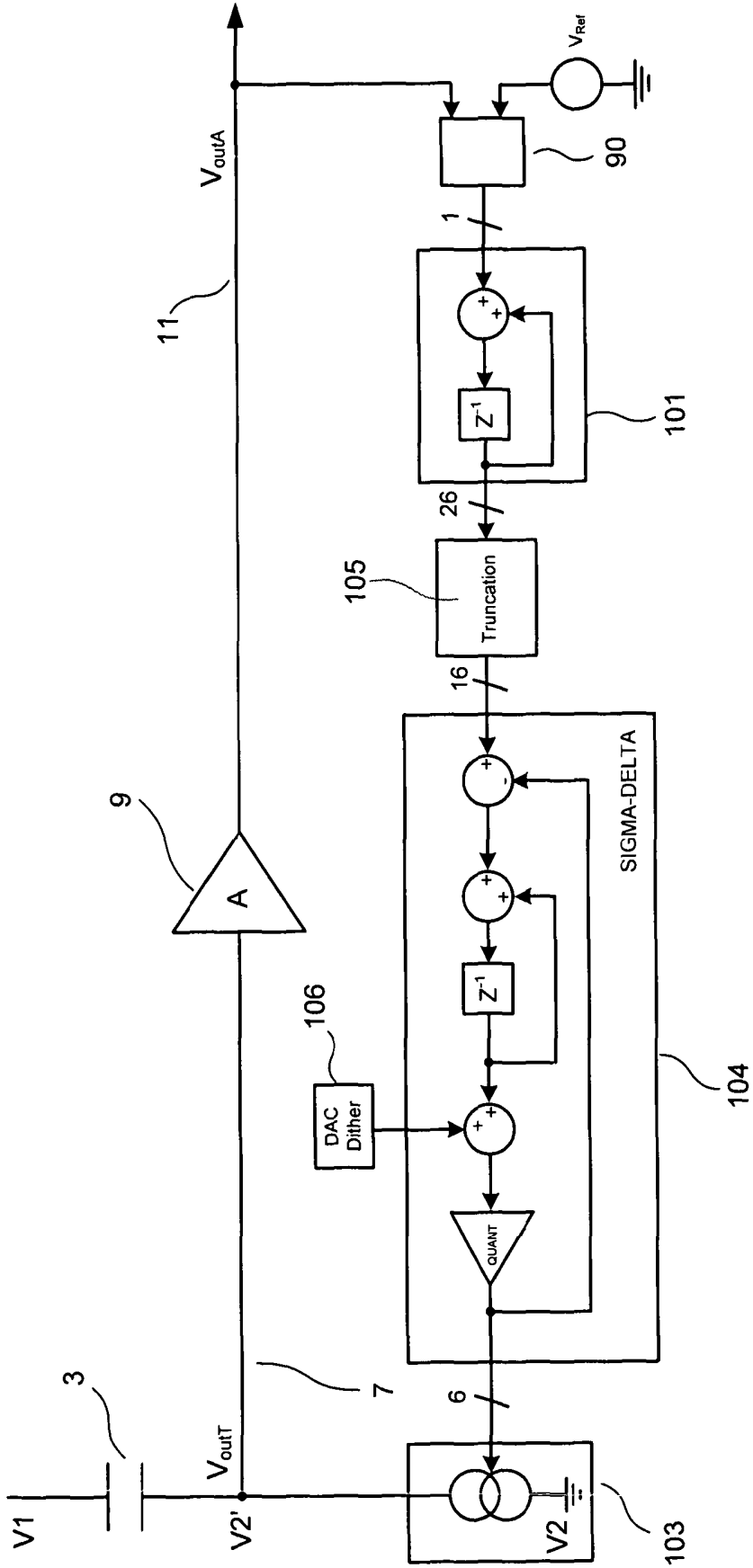


Figure 3

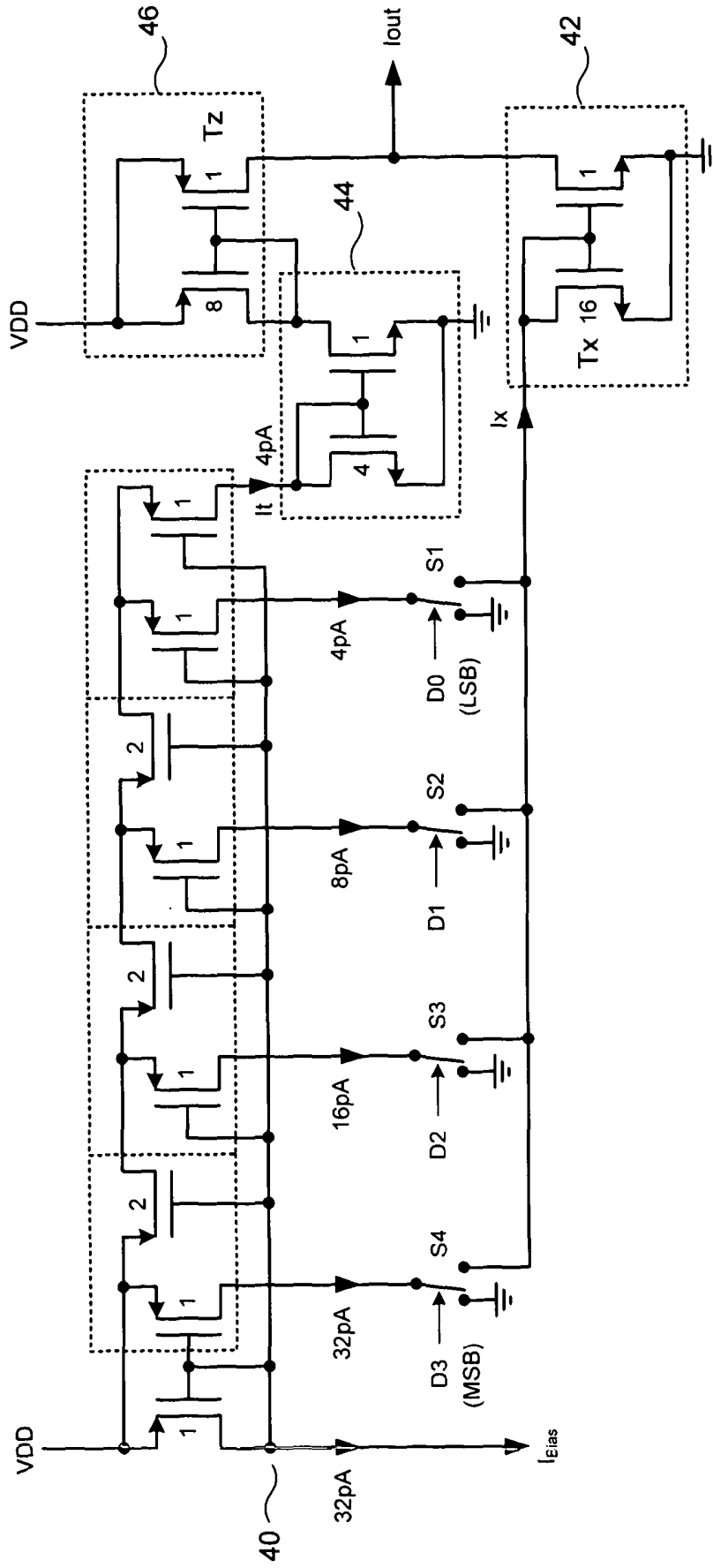


Figure 4

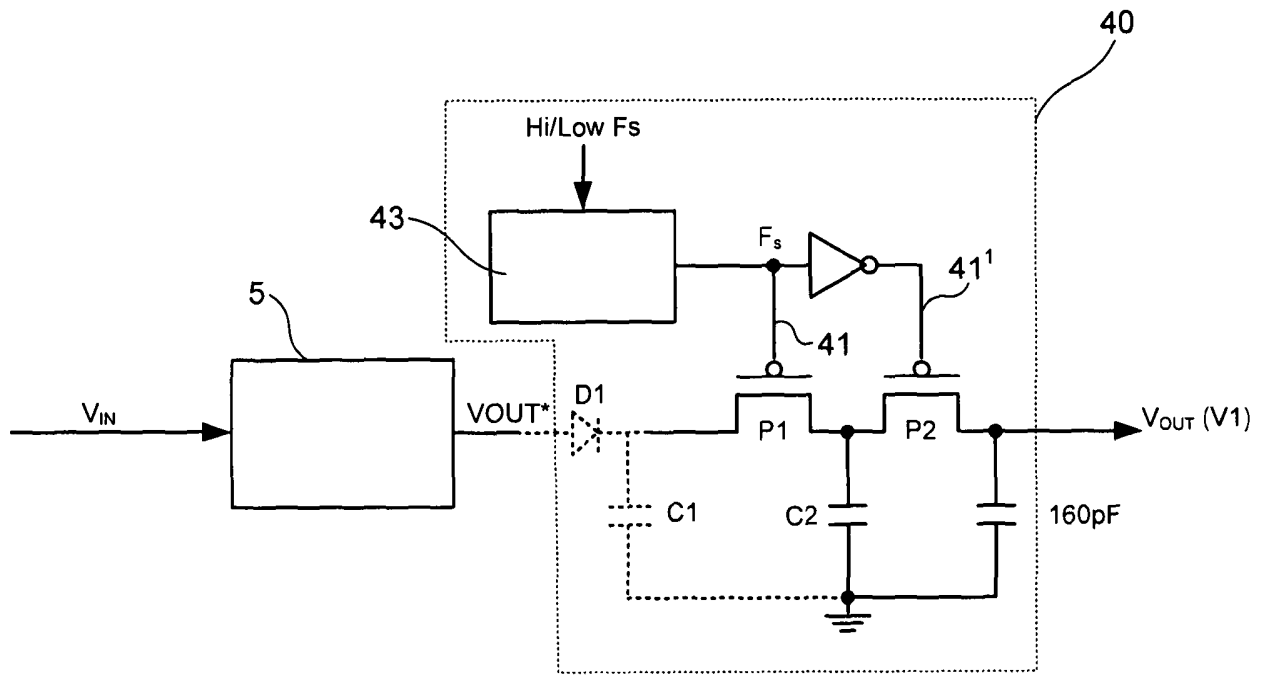


Figure 5a

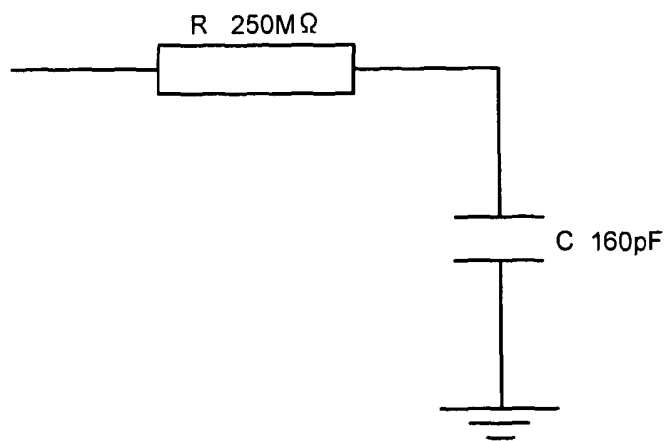


Figure 5b

## CAPACITIVE TRANSDUCER CIRCUIT AND METHOD

### Field of the invention

This invention relates to a capacitive transducer circuit and to a method of biasing a  
5 capacitive transducer, and in particular, but not exclusively, to a MEMS capacitive  
transducer such as a MEMS microphone.

### Background of the invention

10 Figure 1 shows a capacitive transducer 3 comprising a first electrode that is biased to a  
first bias voltage  $V_1$  supplied by a voltage source 5, and a second electrode that is  
connected to a node 7 biased to a second bias voltage  $V_2'$  via a high resistance 4. The  
voltage  $V_{outT}$  on node 7 is input to an amplifier 9, which outputs a corresponding voltage  
 $V_{outA}$  on an output terminal 11.

15

The transducer is designed so that its capacitance changes according to some input  
stimulus. For example, transducer 3 may be a MEMS microphone, where one  
electrode is fixed, and the other one moves in response to the pressure waves of  
incident sound. Since the capacitive transducer is arranged to drive into a high  
20 impedance on node 7, the charge on the capacitor does not change significantly.  
Therefore, the change in the capacitance of the transducer due to the stimulus results  
in a change  $\Delta V$  in the voltage across the transducer capacitance.

This transducer signal component  $\Delta V$  is proportional to the relative change in  
25 capacitance of the transducer 3. It is also proportional to the charge stored on the  
capacitor, and so is proportional to the applied bias  $V_1-V_2'$ . Typically  $\Delta V$  is only a few  
millivolts for normal audio signals from a MEMS microphone, since the electrode  
displacement is only small and there are practical limits to the applied bias voltage  
across the transducer for both the sensor and the voltage supply. Typically, the bias  
30 voltage  $V_2'$  will be near ground, and the bias voltage  $V_1$  about 12V.

The voltage source 5 may be a capacitive charge pump, for example, since the bias  
voltage  $V_1$  may be higher than any external voltage  $V_{IN}$  supplied to the system; it may  
also be other circuitry such as an inductive DC-DC converter, and it may comprise a



linear regulator, perhaps fed using a bandgap reference circuit to act as a reference voltage. Each of these sources will present some thermal noise at their output. However, any noise voltage on the bias voltage V1 output from the voltage source 5 will be indistinguishable from the small transducer signal  $\Delta V$  mentioned above. Thus, it is preferable that the voltage source 5 is designed to inject minimal noise in the signal band.

The DC bias V2' of the other transducer terminal at node 7, coupled to the input of the amplifier 9, is defined by a bias voltage V2 and a series resistance 4. V2' will usually be near to ground in order to maximise the voltage across the transducer element. It is also preferable that the circuitry providing this bias does not inject any appreciable noise into the system.

It will be appreciated from inspection of Figure 1 that the transducer signal  $\Delta V$  will appear on node 7, high-pass filtered by the transducer capacitance and the bias resistance 4. A typical MEMS microphone will have a capacitance of the order of only 1pf. Thus, to provide a  $-3\text{dB}$  corner frequency of 20Hz requires a bias resistance of approximately  $8\text{G}\Omega$ . Such a high value resistance is difficult to implement accurately as an actual resistor, and therefore the resistance 4 may be obtained by using a diode near the origin of its I-V characteristic. However, it is still difficult to define such a high resistance accurately, so the corner frequency, and possibly the start-up time, of such transducer circuitry is difficult to predict or to maintain in volume production. To guarantee a minimum value of  $8\text{G}\Omega$  the typical value may have to be much higher, for example  $25\text{G}\Omega$  to  $80\text{G}\Omega$ , or even higher.

Also, it is preferable that the amplifier 9 used to pick up the signal  $V_{\text{outT}}$  from the capacitive transducer 3 has a higher input resistance than the (minimum) value of resistance 4, as must any additional circuitry attached to node 7.

Furthermore, the amplifier 9 must also have an input capacitance substantially lower than the transducer capacitance in order to avoid attenuating the small change in voltage  $\Delta V$  generated by the movement of the membrane. Any other circuitry attached to node 7 must also present only a small capacitance.

In practical implementations of the circuit shown in Figure 1, there may be leakage currents onto node 7. For example, a leakage current  $I_L$  can flow across the terminals of the biased transducer 3. Such leakage currents  $I_L$  will alter the current through resistance 4, thus creating an error in the output signal  $V_{outT}$  from the capacitive transducer 3, and hence the analogue output signal  $V_{outA}$ . For example, if resistance 4 is  $80G\Omega$ , even  $100fA$  of leakage will give rise to a DC offset of  $8mV$ , which is comparable with a normal peak audio signal. This DC offset voltage may disturb the operating point of the amplifier and thus degrade its linearity, or give an objectionable effect downstream such as reducing the available dynamic range of downstream circuitry, such as gain amplifiers or an ADC.

It will be appreciated by those skilled in the art that  $V_{outT} = V2' \pm \Delta V$  where  $V2'$  represents the DC (bias) voltage and  $V_{outT}$  represents the AC (signal) voltage.

An aim of the present invention is to provide a capacitive transducer circuit, and a method of biasing a capacitive transducer, which provides a predictable DC output voltage (and hence corner frequency) with low added noise.

#### Summary of the invention

20

According to the present invention, there is provided a capacitive transducer circuit comprising: a voltage source; a capacitive transducer receiving a bias voltage from the voltage source; and a low pass filter circuit provided between the voltage source and the capacitive transducer.

25

According to another aspect of the present invention, there is provided a method of biasing a capacitive transducer circuit comprising a voltage source and a capacitive transducer receiving a bias voltage from the voltage source, the method comprising the steps of: providing a low pass filter circuit between the voltage source and the capacitive transducer.

30

### Brief description of the drawings

For a better understanding of the invention, and to show more clearly how it may be carried into effect, reference will now be made, by way of example only, to the accompanying drawings in which:

5

Figure 1 shows a conventional circuit incorporating a capacitive transducer;

Figure 2 shows a circuit comprising a capacitive transducer having a DC servo loop;

10

Figure 3 shows a further example of a circuit comprising a DC servo loop;

Figure 4 shows an example of a current DAC for use with the circuit of Figure 2 or Figure 3;

15

Figure 5a shows a circuit according to the present invention; and

Figure 5b shows an equivalent electrical circuit relating to Figure 5a.

### Detailed description of the preferred embodiment

20

As described above, Figure 1 shows a capacitive transducer 3 comprising a first electrode that is biased to a first bias voltage  $V_1$  supplied by a voltage source 5, and a second electrode that is connected to a node 7, the second electrode being biased to a second bias voltage  $V_2'$  via a high resistance 4. The voltage  $V_{outT}$  on node 7 is input to  
25 an amplifier 9, which outputs a corresponding voltage  $V_{outA}$  on an output terminal 11.

It is possible that significant and unpredictable leakage currents, for example as shown by  $I_L$ , can appear on node 7. These, imposed on the high and variable resistance 4, result in a variable and significant offset and variability in the quiescent bias voltage of  
30 node 7. This variable offset may disturb the operating point of the amplifier and thus degrade its linearity, for instance causing the amplifier output to clip prematurely or to introduce distortion as its output approaches ground. It may also reduce the available dynamic range of downstream circuitry such as gain amplifiers or an ADC. In a

microphone application, it may also introduce pops and clicks, when switching on and off or between channels, or when adjusting gain downstream.

Figure 2 shows a capacitive transducer circuit. This circuit diagram includes components as shown in Figure 1, with like components numbered correspondingly. According to the circuit of Figure 2, the capacitive transducer circuit also comprises a feedback circuit 100 connected between the output terminal 11 of the amplifier 9 and its input terminal 7.

- 10 The feedback circuit 100 is arranged to compare the amplifier output  $V_{outA}$  with a target output bias voltage  $V_{REF}$  and to feed back a corresponding current onto node 7. Provided there is enough gain around the loop comprising feedback circuit 100 and amplifier 9, this will result in the output voltage  $V_{outA}$  settling to a voltage equal to  $V_{REF}$ . Except for minor effects such as the possible small input offset voltage of amplifier 9, 15 this will also define the voltage at node 7, independent of any leakage current 13.

- The choice of DC reference voltage  $V_{REF}$  will depend on system requirements. For example, in a system where the maximum (overload) output that must be handled without clipping is say +/-200mV at the output of amplifier 9, then a reference voltage 20  $V_{REF}$  of 200mV + 10%, for example, as headroom may be a suitable choice. This will allow the amplifier 9 to suitably drive the output signal  $V_{outA}$  above ground without clipping. The amplifier 9 may be a unity-gain follower. The amplifier 9 may alternatively be a gain stage in which case  $V_{REF}$  may be chosen such that it is, for example, 400mV so that the quiescent voltage ( $V_2'$ ) on node 7 is also 400mV, which will allow for the 25 gain stage and any potential overload. Having a suitable amount of headroom avoids the amplifier input swinging below ground, avoiding the need for an amplifier with a common-mode input range spanning below ground, while only reducing the voltage across the transducer capacitance from 12V to  $(12V - V_{REF})$  (i.e 11.6V for  $V_{REF}=400mV$ ). The choice of 400mV for the input bias is also convenient in providing 30 headroom for the output of the current-output DAC 103 of the feedback circuit 100. For other requirements or technological restrictions, a different choice of DC reference voltage  $V_{REF}$  may be preferred.

The design of the feedback circuit 100 poses several problems. In use, high-amplitude signals may appear at the output of amplifier 9. If these high-amplitude signals pass through from node 11 to node 7, the output audio band signal will be attenuated by this negative feedback. Also, any distortion in the signal as it passes through the feedback circuit 100 may cause harmonics to be introduced, or result in asymmetric rectification of the fed-back audio signal resulting in a signal-dependent offset. Also, the output stage of the feedback circuit 100 must not introduce appreciable noise onto node 7, as this would add noise to the output signal. Furthermore, the output stage of the feedback circuit 100 must not degrade the low-frequency resistance of node 7, nor add appreciable capacitance to node 7.

In a steady state, the current output from feedback circuit 100 will settle to a value that cancels out the net effect of leakage current  $I_L$  and the small current necessary to impose the desired voltage (possibly zero) across the high value resistance 4. The leakage current to be cancelled may range from a few femtoamperes to say 100pA. The total audio-band noise budget of say 4uV on a 1pf sensor is equivalent to 4aC, i.e. some 25 electrons. The value of resistance 4 as discussed above will be at least 8G $\Omega$ , probably higher. The lower cut-off frequency required from the microphone output may be as low as 20Hz, which is difficult to achieve with integrated analogue circuitry, especially at these low noise levels.

According to the circuit illustrated in Figure 2, the feedback circuit 100 comprises an analogue-to-digital converter (ADC) 90 for converting the analogue signal  $V_{outA}$  from the output 11 of the amplifier 9 into a digital signal. A digital filter 101, for example an integrator, receives the output of the ADC 90. The output of the digital filter 101 is connected to a current-output digital-to-analogue converter (IDAC) 103, the output current  $I_E$  of which is fed back to the input of the amplifier 9.

A suitable choice for the architecture of ADC 90 is a 1-bit sigma-delta modulator. This is naturally a high sample rate, mitigating anti-aliasing issues, and is a simple structure. The output of a 1-bit sigma-delta modulator will be heavily filtered, so audio-band quantisation noise can be tolerated. However, it is noted that multi-bit delta-sigma modulators, or other architectures or forms of ADC are possible.

The digital filter 101 is configured such that the feedback circuit 100 only affects frequencies below the audio band, for example audio signals below 20Hz. Signals at 20Hz and above are heavily attenuated by this filter. Thus, the stages following the digital filter 101 need handle only the low-frequency low-amplitude offset signals, rather  
5 than having to handle voice-band signals with enough resolution to avoid the above-mentioned harmonic distortion or rectification effects.

For example, the digital filter 101 may be an integrator that adds up the stream of digitised output samples from the ADC 90, thereby acting as a filter. For a 1-bit  $\Sigma\Delta$   
10 ADC, the integrator reduces to a simple up-down counter. The use of a digital filter 101 enables easier realisation of such low frequency time constants, without requiring unfeasibly high resistor or capacitor values as would be required in an analogue solution, especially an integrated circuit implementation.

15 In addition to the requirement to substantially filter out any audio-band signal, the digital filter 101 will generally have a very-low frequency response to maintain loop stability. There are many poles and delays around the loop, including the finite bandwidth of amplifier 9, the delay through the ADC, and the somewhat variable pole introduced by the IDAC 103 feeding into the transducer capacitance 3 and the bias resistance 4. The  
20 digital filter 101 may provide the dominant low frequency pole of the loop, and so may have a sub-Hz pole.

The use of a digital filter 101 rather than an analogue network has the advantage of enabling the poles in the feedback loop to be controlled more accurately and easily, for  
25 example by choice of filter length and scaling. Also, if a more complex frequency compensation loop is required, this may be achieved relatively easily with a digital rather than analogue solution.

However, the realisation of time constants for sub-audio, or even sub-Hz filter poles,  
30 with a digital filter receiving data at perhaps 2.4MHz from the sigma-delta ADC 90, inherently results in a long filter word-length, for example that from a 26-bit counter. In principle, this 26-bit word could be passed directly to a 26-bit IDAC 103, but such a DAC is not practical. It is preferable to reduce the number of bits passed to the DAC 103, for example using measures discussed below.

According to another circuit as shown in Figure 3, the feedback circuit 100 may comprise an ADC 90, digital filter 101 and IDAC 103 as shown in Figure 2. However, according to the example of Figure 3, the feedback circuit 100 further advantageously  
5 comprises a truncation block 105 for truncating the number of bits taken from the digital filter 101. For example, if the digital filter is realised using a 26-bit counter, the truncation block 105 can be configured to omit a predetermined number of upper bits, for example the upper, i.e. most significant, ten bits of the counter, since these are unlikely to be used, except in gross overload conditions, where truncation block 105 is  
10 arranged to output a maximum signal, i.e. to clip rather than roll over. As such, the truncation block 105 is configured to output a 16-bit signal in the example provided. It will be appreciated that the counter may be configured to output any number of bits "n", while the truncation block can be configured to truncate the n-bits to m-bits, where m is less than n.

15

The example of Figure 3 may also comprise a word-length-reduction block 104 for reducing further the number of bits supplied to the IDAC 103. Simple truncation of further upper bits would limit the range, while simple truncation of lower bits would introduce too much quantisation noise. However, a lower-bit bit-reduction circuit that  
20 does not introduce significant quantisation noise in the audio-band, albeit introducing quantisation noise at higher frequencies is acceptable, bearing in mind that the current DAC 103 feeding into the transducer capacitance will act as a low-pass post-filter. For example, the word-length-reduction block 104 may comprise a sigma-delta modulator, as will be known to a person skilled in the art. The use of a word-length-reduction block  
25 104 enables a less complex current DAC 103 to be used, which in turn reduces cost. In the example provided the word-length-reduction block 104 is shown as reducing the 16-bit input signal to a 6-bit output signal. It will be appreciated, however, that the word length reduction block can be configured to receive any number of bits "x", and output any number of bits "y", where y is less than x.

30

The word-length-reduction block 104 may be adapted such that dither 106 is applied to the word-length-reduction operation, thereby removing any unwanted effects caused by harmonics or possible idle tones.

To ensure that the digital filter provides the dominant pole in the loop, the loop bandwidth may need to be placed below the worst-case (minimum) corner frequency of the input node 7. It is possible that drift of the leakage current with temperature or ambient humidity will often occur over a long time scale, so this is usually acceptable.

5 However, balanced with this very low cut-off frequency requirement is a need for the feedback circuit 100 to react as quickly as possible during certain conditions, such as start-up for example. The digital filter 101 may therefore be configured to have a different time constant during said certain conditions. For example, the digital filter 101 may be provided with a variable gain facility that allows the digital filter 101 to react  
10 more quickly during start-up and return to a point of convergence, whereby the error voltage  $V_{ERR}$  input to the feedback circuit 100 as a whole tends to zero much more quickly than if the digital filter 101 was allowed to count up or down with a step-size of one.

15 In addition, the digital filter 101 can be adapted to react to sudden changes. For example, an extreme pressure wave, for example dropping the microphone on the floor or slamming a car door, may result in a persistent change in bias conditions on the input. This may be detected, for example, by detecting when a large number of consecutive 1's or 0's is received from the ADC 90. The time constant, i.e. bandwidth,  
20 of the digital filter 101 may therefore be changed in such a situation, for example by changing the step-size of the count, so that the feedback circuit 100 settles more quickly following the sudden change.

The IDAC 103 can be a conventional current-steering structure, for example based on  
25 a sub-threshold MOS R-2R ladder as shown (as a 4-bit IDAC) in Figure 4. The example shown in Figure 4 comprises an input PMOS, a 4-bit MOS R-2R ladder with multiple outputs, a bank of two-way switches connected to respective outputs, and three ratioed current mirrors. It will be appreciated by those skilled in the art that the numbers associated with the various PMOS & NMOS transistors of Figure 4 reflect  
30 their respective aspect ratios W/L.

In operation a bias current  $I_{Bias}$ , say 32pA is applied to (i.e. sunk from) terminal 40. The MOS R-2R ladder replicates and scales this bias current  $I_{Bias}$  by binary division at each ladder node to deliver a set of binary weighted currents of 32pA, 16pA, 8pA, and 4pA



to the respective switches S4-S1. Depending on the state of a respective input data bit D0-D3, each respective switch S1-S4 either discards its respective current to ground or applies it as a component of the input current of mirror input device 42. Thus, mirror device 42 receives a current  $I_x$  between zero and  $15 \times 4\text{pA} = 60\text{pA}$  in  $4\text{pA}$  steps,

5 according to the state of the switches S1-S4, i.e. according to the input word comprised of the respective input data bits D0-D3. This current  $I_x$  is scaled by the ratio of the NMOS transistors (equal to 16 in this example) in this current mirror 42 to give an output current  $I_{out}$  between a minimum of zero and a maximum of  $3.75\text{pA}$  (i.e.  $60\text{pA}/16$ ) in  $0.25\text{pA}$  steps (i.e.  $4\text{pA}/16$ ). It is noted that  $I_x=60\text{pA}$  is the maximum

10 current into current mirror 42 which is divided by 16, the ratio of the NMOS transistors in current mirror 42. It is also noted that the  $4\text{pA}$  is the amount of current associated with the LSB which when input to current mirror 42 is scaled down by 16. The  $4\text{pA}$  termination current  $I_t$  of the ladder is also scaled by a factor of 32 by the two current mirrors 44 & 46, i.e.  $4:1 \times 8:1$ , to give a constant source current of  $0.125\text{pA}$  (i.e.

15  $4\text{pA}/32$ ).

Thus, the net output current of the IDAC 103 shown in Figure 4 can be varied from  $-0.125\text{pA}$  to  $+3.625\text{pA}$  in  $0.25\text{pA}$  steps.

20 A similar 6-bit design could give a maximum current of about four times this value, i.e. nearly  $15\text{pA}$ . If desired, an extra control bit could be derived and used to pulse the small source current, to avoid any small thermal noise that may be generated due to the IDAC 103, i.e. transistor  $T_z$ , being always on.

25 For large signals, i.e. to compensate for gross leakage up to say  $15\text{pA}$ , all of these 6-bits are exercised. It is noted that the output from sigma-delta modulator 104 is noise-shaped, such that quantisation noise in the audio band is suppressed. For small signals, to compensate for sub-pA leakage, as is more likely in normal operational conditions, only the LSB toggles, which means that the sigma-delta modulator 104

30 becomes essentially a 1-bit sigma-delta modulator. For example, a very small leakage current of  $2.5\text{fA}$  can be compensated for by a  $0.25\text{pA}$  pulse every 100 cycles: at a sample rate of  $2.4\text{MHz}$ , this is related to a base frequency of some  $24\text{kHz}$ , above audible frequency range. The quantisation noise is still noise-shaped, avoiding audio-band noise and artefacts, the timing between these pulses being modulated suitably by

the sigma-delta modulator 104. Furthermore, any audio-band noise will be attenuated by the integrating effect of the transducer capacitance.

Also, the output current  $I_{out}$  of the IDAC 103 may be increased by switching out

5 elements of the mirror input devices to alter the respective ratios. For example, referring to Figure 4, if the 15 of 16 parts of the 16x mirror input transistor Tx are turned off, so this mirror effectively becomes a 1:1 mirror rather than 1:16, then the maximum current (and the LSB) will be increased by 16.

10 Thus far, it has been assumed that the ADC 90 serves only to provide an output signal for the feedback path, while the amplified output signal  $V_{outA}$  is passed to external circuitry. However, there is also the requirement for a “digital microphone” where a digital representation of the transducer signal is required. One convention is to output a single-bit output stream, quantised using a 4<sup>th</sup> order delta-sigma modulator. In such a  
15 case, such a modulator is interposed between  $V_{outA}$  and the external terminal of the microphone assembly. Therefore, according to another example, rather than using a distinct ADC 90, the output of a higher-performance ADC provided for other reasons may be used instead. In other words, ADC 90 of the feedback circuit 100 may be a high performance 4<sup>th</sup> order delta-sigma modulator, the output of which is transmitted to  
20 the external world in addition to being used in the feedback circuit 100.

According to the present invention, Figure 5a shows a circuit for providing a clean bias voltage to the capacitive transducer 3. A DC voltage source 5, for example a capacitive charge pump, generates a voltage  $V_{OUT}^*$ . A DC voltage source 5 realised as  
25 a capacitive charge pump may comprise a series of charge pump stages. Typically, a charge pump will “gain-up” thermal noise on its input by a similar gain factor as the step-up factor of the charge pump (e.g. by a factor of 10 for a charge pump which steps up from 1.2V to 12V). The input voltage  $V_{IN}$  to the voltage source 5 may be pre-regulated by a regulator, which will have its own thermal noise, including wide-band  
30 noise aliased down by the sampling action of the charge pump input stage. The reference voltage for the regulator may be derived itself from a noisy source, for example a bandgap reference. It is noted that bandgap references are inherently noisy, as their output voltage inherently includes a component equivalent to a small  $\Delta V_{be}$  voltage that has been multiplied. Therefore, it is possible to have noise injected from a

number of different stages in a power supply/regulation system that may be amplified from one stage to another.

5 For many circuits, this thermal noise is unimportant, as it appears only on amplifier supply voltages, and is attenuated by the amplifier power supply rejection before appearing on any signal path. In this application, however, any noise on VOUT\* may be indistinguishable from the transducer signal  $\Delta V$ , so must be preferably reduced as much as possible, for example to a sub-microvolt level.

10 Thus, according to the invention, the output of the DC voltage source 5 is passed through a low pass filter circuit 40. If implemented as a simple RC filter, as can be seen from Figure 5b, to achieve the required filter characteristics for an audio signal, the resistance R in Figure 5b must have a value of around 250M $\Omega$  when used with a capacitor C having a capacitance of 160pF to give a 4Hz corner frequency, to provide  
15 some attenuation by 20Hz. However, as will be appreciated by a person skilled in the art, it is difficult to realise a high value accurate resistor such as 250M $\Omega$ , particularly in a CMOS integrated circuit due to physical size constraints and process variations. Therefore, according to this aspect of the invention, a switched capacitor circuit is used to simulate such a high value resistor. For example, switches P1, P2 and capacitor C2  
20 of the low pass filter circuit 40 are used to form the resistance R in the equivalent circuit shown in Figure 5b. The switches P1 and P2 are switched by complementary switching signals 41, 41' having a switching frequency  $F_S$ . This has the advantage of providing an effective resistance of about 250M $\Omega$ , but without the size constraints associated with a conventional resistor element.

25

The provision of such a low pass filter circuit 40 for smoothing the output voltage of the DC voltage source 5 poses conflicting problems. On the one hand a low switching frequency  $F_S$  is required for the switches P1, P2 so that the value of the capacitor C2 can be made low, such that the capacitor C2 requires less physical space. The  
30 effective resistance R is given as:

$$R = 1/F_S C$$

Thus, for a capacitor C2 having a value of 0.1pF, for example, the switching frequency  $F_s$  must be around 40KHz to give an effective resistance of about 250M $\Omega$ .

5 It is noted that the DC output impedance of this circuit is about 250M $\Omega$ . Thus, even a  
1nA load will cause a voltage drop across the filter of some 250mV. Also any  
impedance from the output to ground comparable with 250M $\Omega$  will alter the time  
constant of the filter. Thus this technique is not useful for applications where the charge  
pump has to supply any appreciable output current. However in this application, the  
charge pump output serves more as a reference voltage than a power supply. The load  
10 is less than 100pA, typically only a few femtoamperes, which means that this novel  
circuit is well-suited to this application.

The long time constant associated with filter circuit 40 has the disadvantage of  
providing a very slow start-up phase (or during events such as recovery from overload  
15 as discussed above) due to the RC time constant. To overcome this disadvantage, the  
low pass filter circuit 40 can be switched with a first (high) switching frequency during  
start-up, and a second (Low) switching frequency during normal operation. For  
example, a clock generator 43 can be configured and controlled (Hi/Low  $F_s$ ) to provide  
a first high frequency output clock signal for switching the switches P1, P2 during start-  
20 up, and a second low frequency output clock signal 45 for switching the switches P1,  
P2 during normal operation.

For example, during start up the clock generator 43 can output a clock signal having a  
switching frequency  $F_s$  of 1 MHz, for example. This results in the resistor R of the  
25 equivalent circuit 5b having an effective resistance of 10M $\Omega$  during start-up, giving a  
time constant of 1.6ms, settling to 1% in 16ms. During normal operation the clock  
generator 43 can be configured to provide an output clock signal 45 having a lower  
switching frequency  $F_s$ , for example 40 KHz as mentioned above, thus providing the  
required 250M $\Omega$  resistance value during normal operation.

30

This aspect of the invention has the advantage of providing a low pass filter for  
smoothing the output of the DC voltage source 5 during normal operation, but also  
having the advantage of a faster start-up response.

It is noted that, although the circuit of Figure 5a shows switching devices in the form of PMOS devices, it is noted that other switching devices may also be used (possibly requiring suitable adjustments to the circuit), for example NMOS devices.

- 5 It will be appreciated that the various aspects of the invention described above have the advantage of providing an improved capacitive transducer circuit, for example a MEMS capacitive microphone circuit, and overcome the problems associated with biasing the capacitive transducer.
- 10 Although the circuits of Figures 2, 3 and 5a have been described in terms of the capacitive transducer 3 being a MEMS capacitive microphone, it will be appreciated that the circuit is equally applicable to any form of capacitive transducer. For example a similar accelerometer, or ultrasonic transducer; or a chemical sensor where the capacitance is modulated by a change in dielectric constant of the dielectric between  
15 transducer electrodes.

Furthermore, it will be appreciated that the various values used in the discussion of the embodiments (such as the number of bits, current values, voltage values, etc) are provided as examples only, and that other values may be used without departing from  
20 the scope of the invention, as defined in the appended claims.

In addition, as mentioned above the voltage source 5 can be a switched voltage source, such as a switched capacitor charge pump. However, it is noted that the voltage source can also comprise other forms of voltage sources, such as regulated  
25 voltage sources, linear type voltage sources or bandgap type switching sources, all of which will be well known to a person skilled in the art.

It is noted that the invention may be used in a number of applications. These include, but are not limited to, consumer applications, medical applications, industrial  
30 applications and automotive applications. For example, typical consumer applications include laptops, mobile phones, PDAs and personal computers. Typical medical applications include hearing aids. Typical industrial applications include active noise cancellation. Typical automotive applications include hands-free sets, acoustic crash sensors and active noise cancellation.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word  
5 “comprising” does not exclude the presence of elements or steps other than those listed in a claim, “a” or “an” does not exclude a plurality, and a single feature or other unit may fulfil the functions of several units recited in the claims. Any reference signs in the claims shall not be construed so as to limit their scope.

**CLAIMS**

1. A capacitive transducer circuit comprising:  
5 a voltage source;  
a capacitive transducer receiving a bias voltage from the voltage source;  
and  
a low pass filter circuit provided between the voltage source and the  
capacitive transducer.  
10
2. A capacitive transducer circuit as claimed in claim 1, wherein the low pass filter  
circuit comprises a switched capacitor filter circuit.
3. A capacitive transducer circuit as claimed in claim 1 or 2, wherein the switched  
15 capacitor filter circuit comprises first and second switching devices and a capacitor  
device.
4. A capacitive transducer circuit as claimed in claim 1 or 2, wherein the switched  
capacitor filter circuit comprises:  
20 a capacitor having a first terminal connected to ground;  
a first switching device having a first drain/source terminal connected to receive  
a supply voltage from the voltage source, a gate terminal for receiving a clock signal,  
and a second drain/source terminal connected to a second terminal of the capacitor;  
and  
25 a second switching having a first drain/source terminal connected to the second  
terminal of the capacitor, a gate terminal for receiving the inverted clock signal, and a  
second drain/source terminal for providing the bias voltage for the capacitive  
transducer.
- 30 5. A capacitive transducer circuit as claimed in any one of claims 2 to 4, wherein the  
switched capacitor filter circuit is switched at a first clock frequency during a first mode  
of operation, and a second clock frequency during a second mode of operation.

6. A capacitive transducer circuit as claimed in claim 5, wherein one of said first or second modes comprises a start-up mode.
7. A capacitive transducer circuit as claimed in any one of the preceding claims,  
5 wherein the voltage source comprises a regulating voltage source, a switching type voltage source, a linear type voltage source or a bandgap type switching source.
8. A method of biasing a capacitive transducer circuit comprising a voltage source and a capacitive transducer receiving a bias voltage from the voltage source, the  
10 method comprising the steps of:  
    providing a low pass filter circuit between the voltage source and the capacitive transducer.
9. A method as claimed in claim 8, wherein the step of providing a low pass filter  
15 comprises the step of providing a switched capacitor filter circuit.
10. A method as claimed in claim 9, wherein the switched capacitor filter circuit comprises first and second switching devices and a capacitor device.
- 20 11. A method as claimed in claim 9 or 10, further comprising the steps of:  
    providing a capacitor having a first terminal connected to ground;  
    providing a first switching device having a first drain/source terminal connected to receive a supply voltage from the voltage source, a gate terminal for receiving a clock signal, and a second drain/source terminal connected to a second terminal of the  
25 capacitor; and  
    providing a second switching having a first drain/source terminal connected to the second terminal of the capacitor, a gate terminal for receiving the inverted clock signal, and a second drain/source terminal for providing the bias voltage for the capacitive transducer.
- 30 12. A method as claimed in any one of claims 9 to 11, further comprising the steps of switching the switched capacitor filter circuit at a first clock frequency during a first mode of operation, and a second clock frequency during a second mode of operation.



13. A method as claimed in claim 12, wherein one of said first or second modes comprises a start-up mode.
14. A method as claimed in any one of claims 8 to 13, wherein the voltage source  
5 comprises a regulating voltage source, a switching type voltage source, a linear type voltage source or a bandgap type switching source.
15. An electronic device comprising a capacitive transducer circuit as claimed in any  
10 one of claims 1 to 7.
16. A communications device comprising a capacitive transducer circuit as claimed in  
any one of claims 1 to 7.
17. A portable telephone device comprising a capacitive transducer circuit as claimed  
15 in any one of claims 1 to 7.
18. An audio device comprising a capacitive transducer circuit as claimed in any one  
of claims 1 to 7.
- 20 19. A computer device comprising a a capacitive transducer circuit as claimed in any  
one of claims 1 to 7.
20. A vehicle comprising a capacitive transducer circuit as claimed in any one of  
25 claims 1 to 7.
21. A medical device comprising a capacitive transducer circuit as claimed in any one  
of claims 1 to 7.
22. An industrial device comprising a capacitive transducer circuit as claimed in any  
30 one of claims 1 to 7.
23. A micro-electrical-mechanical-systems (MEMS) device comprising a capacitive  
transducer circuit as claimed in any one of claims 1 to 7.

24. An integrated circuit comprising a capacitive transducer circuit as claimed in any one of claims 1 to 7.

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**Examiner:** Peter Easterfield

**Claims searched:** 1 to 24

**Date of search:** 2 September 2008

**Patents Act 1977: Search Report under Section 17**

**Documents considered to be relevant:**

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1,7,8,14 and 15-24	WO 2007/132422 A1 (NXP) see fig 9 and page 12 line 11 to page 13 line 11
A	-	EP 1906704 A1 (SONLON)
A	-	US 2006/0062406 A1 (KINOSHITA)

**Categories:**

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

**Field of Search:**

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC<sup>X</sup> :

Worldwide search of patent documents classified in the following areas of the IPC

B81B; H04R

The following online and other databases have been used in the preparation of this search report

WPI, EPODOC

**International Classification:**

Subclass	Subgroup	Valid From
H04R	0019/00	01/01/2006
B81B	0003/00	01/01/2006
G01P	0015/125	01/01/2006
H04R	0019/04	01/01/2006