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(71) Applicant
Intel Corporation

(Incorporated in USA-California)

3065 Bowers Avenue, Santa Clara, California 95051, United States of America

(72) Inventors
Winston K M Lee
Duane H Oto
Simon M Tam

(74) Agent and/or Address for Service
Potts Kerr & Co
15 Hamilton Square, Birkenhead, Merseyside, L41 6BR

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H3X
Selected US specifications from IPC sub-class G11C

(54) **Self-limiting erase scheme for EEPROM**

(57) An over-erase condition of a one-transistor EEPROM cell is prevented by monitoring drain voltage. In one embodiment, during an erase cycle, a drain voltage is fed back to a floating gate to counteract a positive erase voltage on the source of the memory cell and therein reduce the electric field across the tunnel oxide leading to the cessation of erase. In another embodiment, the drain voltage is fed back to deactivate the erase voltage when a predetermined drain voltage value V ref is exceeded.

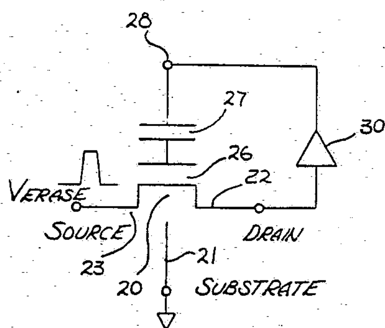

Fig. 2

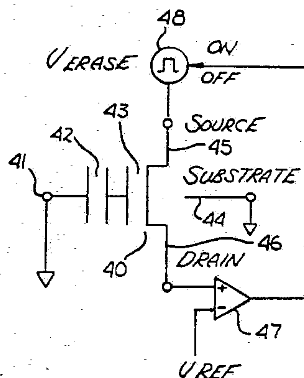

Fig. 3

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The drawing(s) originally filed was (were) informal and the print here reproduced is taken from a later filed formal copy.

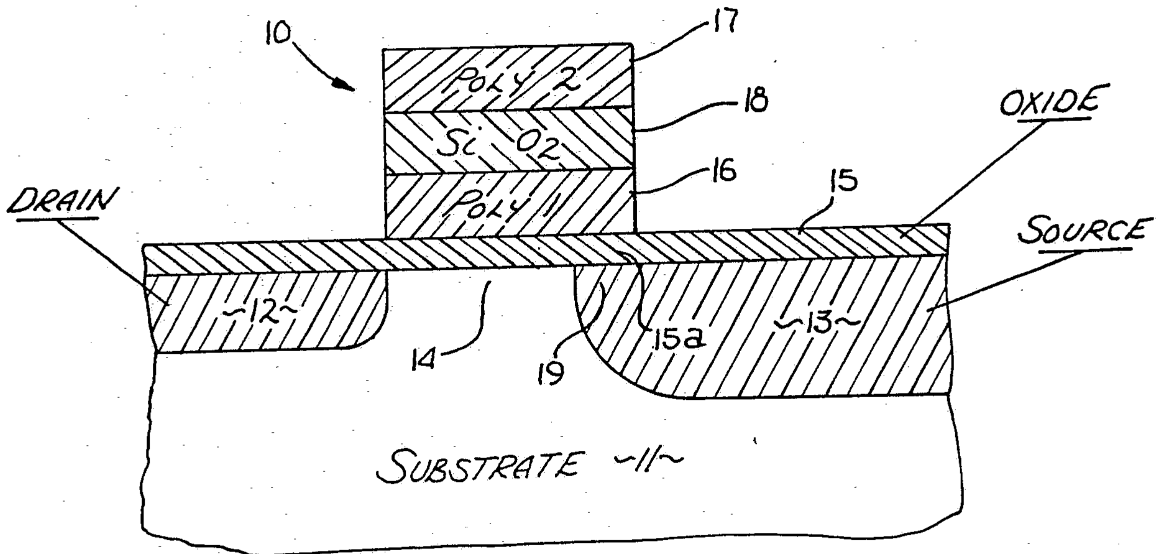

Fig. 1

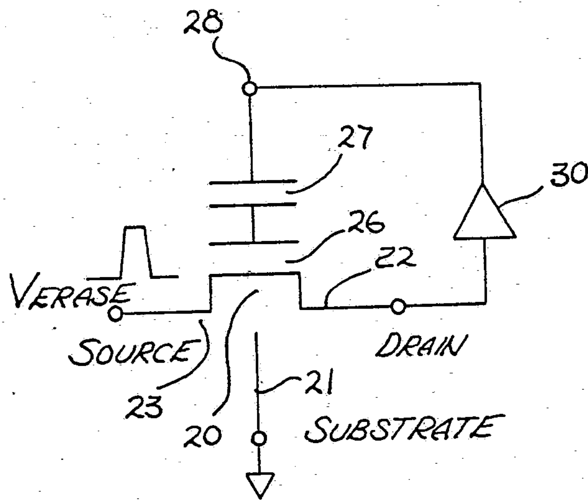

Fig. 2

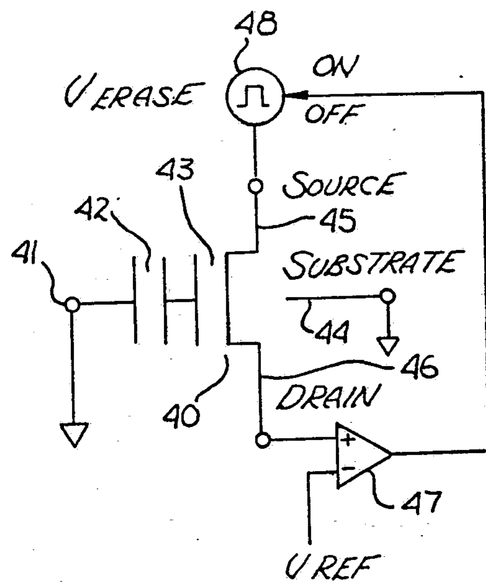

Fig. 3

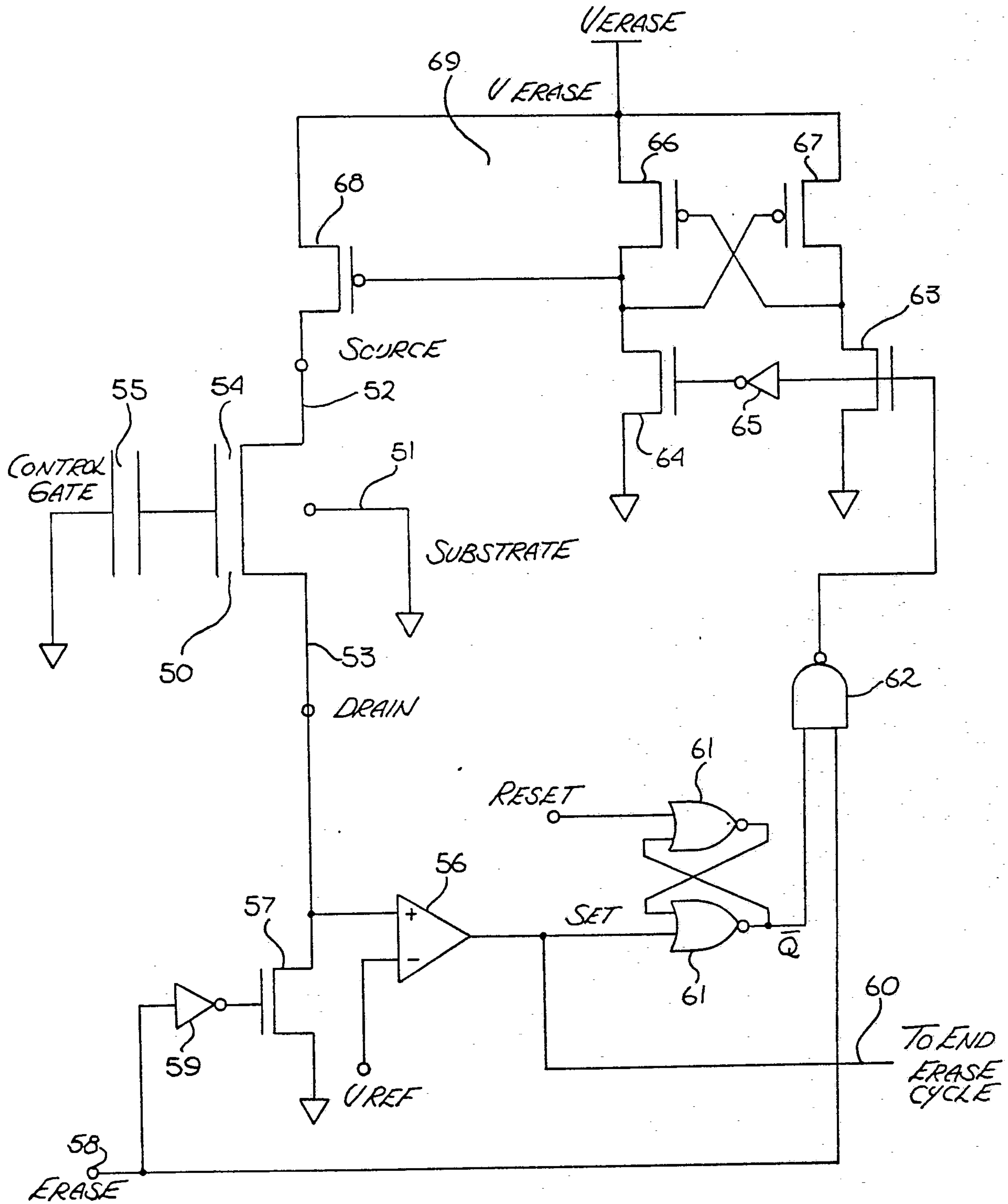

Fig. 4

SELF-LIMITING ERASE SCHEME FOR EEPROM

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BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates to the field of electrically programmable and electrically erasable memory cells and more particularly the erase of memory cells employing floating gates.

2. Prior Art.

The fabrication of electrically programmable read-only memories (EPROMs) utilizing metal-oxide-semiconductor (MOS) technology is well-known in the prior art. These EPROMs employ memory cells utilizing floating gates which are generally formed from polysilicon members completely surrounded by an insulator. Electrical charge is transferred into the floating gate using a variety of techniques such as avalanche injection, channel injection, Fowler-Nordheim tunnelling, channel hot electron injection, etc. A variety of phenomena have been used to remove charge from the floating gate including exposing the memory to ultraviolet radiation. The floating gate is programmed when a charge is stored in the floating gate. The cell is in an unprogrammed, or erased, state when the floating gate is discharged.

Because of complex and time consuming procedures required to erase EPROMs, these devices have been used primarily in applications requiring read-only memories. Electrically programmable and electrically erasable read-only memories (EEPROMs) were developed to provide the capability of electrically erasing programmed memory cells. These EEPROMs have also been referred to as electrically alterable read-mostly memories. Commercially available EEPROMs have generally used a

thin oxide region to transfer the charge into and from a floating gate. In a typical memory, a two-transistor cell is used. For instance, U.S. Patent No. 4,203,158 discloses the fabrication of such an EEPROM cell. Further, U.S. Patent No. 4,266,283 discloses the arrangement of EEPROMs into an array wherein X and Y select lines provide for the selection, programming and reading of various EEPROM cells. These EEPROM cells do not lend themselves to being reduced in substrate area as due the EPROM cells.

Various techniques have been implemented to reduce the size of the memory array by providing higher density cells. One such technique is disclosed in U.S. Patent No. 4,432,075. Further, the use of a single 5 volt potential supply to provide the requisite current and voltage for the proper operation of EEPROMs is crucial to the manufacture of the more recent EEPROM technology. U.S. Patent No. 4,432,075 discloses the sharing of a single source of hot electrons by a number of cells to provide the additional current required for programming the various cells. Further, the use of a single 5 volt external supply to generate on-chip a higher potential which is required for programming is known in the prior art.

A further attempt to provide higher density, low voltage EEPROM cell is disclosed in a U.S. Patent Application, Serial No. 892,446 filed August 4, 1986 and entitled Low Voltage EEPROM Cell and is assigned to the assignee of the present application. In this copending application, a one-transistor EEPROM cell which uses channel injection for charging the floating gate and tunnelling for discharging the gate is disclosed. A single 5 volt potential is used with a higher programming/erasing

potential of approximately 11-15 volts being generated on-chip. However, the EEPROM of the one-transistor design uses the same transistor and the same oxide separating the transistor elements from the floating gate to both program and erase the floating gate. Because of the one-transistor design, over-erased condition of a memory cell is more prevalent than in the two-transistor design. An over-erase condition must be avoided in order to prevent the one-transistor EEPROM memory cell from becoming a depletion-like transistor in the read mode. During the read mode an over-erased memory cell will disable a whole column of a memory array if the memory cells are structured as an array. The over-erase problem is not typically a concern with the two-transistor design or the quasi-one-transistor EEPROM design, which is disclosed in a copending patent application, Serial No. 009,998 filed February 2, 1987 which is also assigned to the assignee of the present invention. However, again, the two-transistor design will require much bigger cell area while the quasi-one-transistor EEPROM described in the Serial No. 009,998 reference requires more processing steps.

The present invention provides for a scheme to self-limit the electrical erase of a single transistor floating gate EEPROM cell, wherein whole arrays are not disabled due to an over-erase condition of a single EEPROM cell.

SUMMARY OF THE INVENTION

The present invention describes an apparatus and a method for self-limiting electrical erase of one-transistor floating gate EEPROM cells. In one scheme, drain voltage is fed back to the control gate of an EEPROM cell. When an erasing potential is placed on the source of the cell, electrons discharge to the source by tunnelling and cause the floating gate to become more positive. This increase in the positive potential is reflected at the drain, which voltage is a cell threshold below the floating gate voltage. Because of the drain-to-gate feedback, the control gate also becomes more positive and couples the floating gate positively as well. The floating gate potential increase will decrease the potential and electric field across the tunnel oxide, wherein accelerating the termination of erase to prevent an over-erase condition.

In an alternative scheme, the control gate is grounded and the drain potential controls the deactivation of the erase voltage. After the erasing sequence commences, electrons are discharged from the floating gate until the drain reaches a predetermined potential. At this point, a signal is sent to de-energize the erase voltage.

In one circuit implementation an amplifier is used to set the gain of the feedback voltage in the first scheme. In the alternative scheme, a comparator is used to compare the drain potential to a presettable voltage reference, such that the output of the comparator changes states to initiate the deactivation of the erase voltage when the drain potential exceeds the voltage reference.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional elevation view of an embodiment of a one-transistor EEPROM cell.

Figure 2 illustrates a scheme of providing self-limiting electrical erase by providing a feedback signal to a control gate of a one-transistor EEPROM cell.

Figure 3 illustrates an alternative scheme wherein a feedback signal is used to control an erase voltage present on a source region of a one-transistor EEPROM cell.

Figure 4 illustrates a circuit implementation for the feedback to source scheme of Figure 3.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

An apparatus and a method for self-limiting the eletrical erase of a one-transistor floating gate EEPROM cell is described. In the following description, numerous specific details are set forth, such as specific circuit configuration, components, etc., in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known processes have not been described in detail in order not to unnecessarily obscure the present invention.

Referring to Figure 1, a one-transistor EEPROM cell 10 is shown. The formation of EEPROM 10 is described in a copending application, Serial No. 892,446, filed August 4, 1986, and assigned to the assignee of the present application. The one-transistor EEPROM cell 10 is comprised of a substrate 11, drain 12, source 13, and a channel region 14 separating drain 12 and source 13. An oxide layer 15 is formed above the channel region 14, wherein floating gate 16 and control gate 17 are formed above region 14. Floating gate 16 is comprised of a first polysilicon layer. A second polysilicon layer which comprises the control gate 17 is separated by a silicon oxide (SiO_2) layer 18 which operates as a dielectric medium separating the two polysilicon layers 16 and 17. As described in the copending application, EEPROM cell 10 uses channel injection to inject electrons from channel region 14 into floating gate 16. The one-transistor EEPROM cell 10 also utilizes Fowler-Nordheim tunnelling for discharging the floating gate 16 to erase the

memory cell by causing electrons to tunnel across thin gate dielectric layer 15. As explained in the copending application, the erase sequence is achieved because source 13 extends under a portion of floating gate 16, such that electrons from floating gate 16 are able to tunnel across oxide layer 15 into region 19 underlying floating gate 16.

During an erasing sequence, a high voltage (10 volts to 15 volts) is applied to source 13 of EEPROM cell 10. Due to capacitive coupling, a potential will be established across gate tunnel dielectric 15a between the floating gate 16 and source overlap region 19. Under a normal erasing operation, control gate 17 is at 0 volts and drain 12 is left floating. A potential of approximately 12 volts is placed on source 13. As the EEPROM cell 10 is being erased, electrons are removed from floating gate 16 and gate 16 potential increases positively. Because drain 12 is open, the potential of drain 12 will increase also and eventually will result in a voltage difference between floating gate 16 and drain 12, such that potential at drain 12 is lower than the potential at gate 16 by the threshold voltage of the MOS transistor.

If the erasing sequence continues, electrons will continue to tunnel from floating gate 16 into overlap region 19, resulting in a net positive potential of the floating gate. An over-erase condition occurs when as a result of erase, the floating gate potential is sufficiently high, such that during a read condition the unselected cell conducts current. Typical voltages for an unselected cell are 0 volts on the control gate, 0 volts at the source and approximately 1.5 volts at the drain. Whereas, during a read condition, unprogrammed (erased) EEPROM

cells should only conduct when that cell is selected by having a voltage, typically 5 volts, applied to control gate 17, an over-erased cell 10 will conduct even when it is not selected (0 volts on control gate 17), thereby providing an erroneous reading. If cell 10 is part of a memory array, cell 10 can provide an erroneous reading on its corresponding matrix output line.

This over-erase problem can be eliminated with a two-transistor design or the quasi-one-transistor EEPROM design as described in the earlier mentioned references. However, as previously stated, the two-transistor design will require much bigger cell area while the quasi-one-transistor EEPROM requires more processing steps.

Referring to Figure 2, it illustrates a scheme of the present invention for providing a self-limiting erase implementation. An EEPROM cell 20, equivalent to EEPROM cell 10 of Figure 1, is shown having substrate 21, drain 22, source 23, floating gate 26 and control gate 27. During an erase condition, substrate 21 is grounded and an erasing potential (V_{ERASE}) is impressed on source 23. An amplifier 30 is coupled between drain 22 and gate terminal 28 of control gate 27. Amplifier 23 basically provides feedback between drain 22 and control gate 27.

In this configuration, control gate 27 is no longer set to 0 volts, but is connected to drain 22 through the feedback amplifier 30, such that during an erasing condition the potential on drain 22 is fed back to control gate 27. As V_{ERASE} is imposed on source 23, electrons tunnel from floating gate 26 into source 23. As electrons leave floating gate 26, the

potential on the drain will increase proportionately. However, now that the drain is coupled to gate 27, the increase in the potential of drain 22 is also felt at terminal 28. Therefore, as the drain potential increases, potential at terminal 28 increases accordingly. Due to the control gate 27 to floating gate 26 capacitive coupling, the potential at control gate 27 is coupled to floating gate 26. As drain potential increases positively, the feedback provided at terminal 28 causes the potential at floating gate 26 to increase accordingly in a positive direction. Therefore, as more electrons leave gate 26, the feedback voltage increases and provides a more positive voltage on control gate 27 to counter V_{ERASE}.

Because of the strong relationship between the Fowler-Nordheim tunnelling current and voltage, the tunnel erase current will decrease due to the positive voltage coupled back to floating gate 26 and eventually stopping the tunnelling process. By carefully adjusting the gain of amplifier 30, a proper feedback voltage will be impressed on terminal 28 as drain 22 increases in potential during erase. The positive voltage on control gate 27 will be coupled through to floating gate 26, thereby increasing the positive voltage potential at floating gate 26. As the floating gate 26 voltage increases, the tunnelling process will decrease and eventually stop prior to putting the cell into an over-erase condition. By properly adjusting the gain of amplifier 30, the tunnelling sequence can be made to terminate prior to cell 20 entering an over-erase condition. Once the erase threshold has been reached, a continued application of V_{ERASE} will have no effect on the erasing of cell 20. Although drain 20 can be coupled directly

to gate 28 without the use of amplifier 30, a more precise adjustment of the feedback voltage can be achieved by using an amplifier having a presettable gain. A buffer and amplifier combination will also function equivalently. The ability to adjust the amount of feedback will result in the ability to control the final floating gate potential.

Referring to Figure 3, it illustrates an alternative feedback scheme for an EEPROM cell 40, which is equivalent to the EEPROM cell 10 of Figure 1. In this scheme, terminal 41 of control gate 42 is coupled to ground, thereby placing a ground potential on control gate 42. Substrate 44 is also grounded. An erase voltage supply 48 is coupled to source 45. Drain 46 is coupled to one input terminal of comparator 47 and the other input terminal of comparator 47 is coupled to a reference voltage, V_{REF}. The output of the comparator is coupled back to control V_{ERASE} supply 48. Comparator 47 provides a feedback signal to turn off V_{ERASE} supply 48.

In this embodiment, erase potential V_{ERASE} is applied to source 45 by turning on supply 48. As cell 40 undergoes an erasing sequence by electron tunnelling from floating gate 43 to source 45, the potential on drain 46 increases proportionately. The output of comparator 47 is configured to provide a control signal which permits supply 48 to activate V_{ERASE} to be impressed on source 45. However, as drain potential increases during the erasing sequence, drain potential will eventually surpass that of the reference voltage V_{REF}, causing the output of comparator 47 to change states and shutting off V_{ERASE} supply 48. By presetting the value of V_{REF}, comparator 47 can be made to shut off V_{ERASE} supply 48 when drain 46 potential reaches a

predetermined point where erasing is completed. Therefore, comparator 47 controls to deactivate V_{ERASE} supply 48, so that floating gate 43 will not continue to release electrons resulting in an over-erase condition of cell 40.

Referring to Figure 4, it shows a more detailed circuit implementation of the feedback to source scheme illustrated in Figure 3. An EEPROM cell 50 having a substrate 51, source 52, drain 53, floating gate 54, control gate 55, is shown. Cell 50 is equivalent to the EEPROM cell 10 of Figure 1 and is configured to have a ground coupled to control gate 55, as was the case in Figure 3. Drain 53 of EEPROM 50 is coupled to the positive input terminal of comparator 56 as well as to one terminal of transistor 57. The other side of transistor 57 is coupled to ground. The negative terminal of comparator 56 is coupled to reference voltage, V_{REF}. Terminal 58 is coupled to the gate of transistor 57 through inverter 59. Terminal 58 receives an erase signal from control source (not shown) for activating an erase sequence of cell 50.

The output of comparator 56 is coupled to line 60 for providing a signal to deactivate the erase signal on terminal 58. The output of comparator 56 is also coupled to provide a set signal to RS flip-flop pair 61. A reset signal is also coupled to the RS flip-flop 61. The output of the RS flip-flop pair 61 is coupled as one input to NAND gate 62 and a second input of NAND gate 62 is coupled to terminal 58. The output of NAND gate 62 is coupled to the gate of transistor 63 and to the gate of transistor 64 through inverter 65. The drain of transistor 63 is coupled to the gate of transistor 66 and the drain of transistor 64 is coupled to the gate of transistor 67

such that transistors 63 and 66 conduct together when transistors 64 and 67 are off, and vice-versa. The drains of transistor 66 and 67 are coupled to a supply V_{ERASE}, as well as to one input of transistor 68. The other terminal of transistor 68 is coupled to source 52. Drain of transistor 64 is coupled to gate of transistor 68 such that circuit 69, comprised of components 63-68, provides the control for placing V_{ERASE} on source 52.

The erase command signal at terminal 58 going high will initiate an erase cycle by turning off transistor 57 and causing drain 53 to go into a float condition. At this point V_{REF} has a higher magnitude potential than that of drain 53 causing the output of comparator 56 to be low. The output from SR flip-flop 61 is high, due to a reset signal resetting flip-flops 61 prior to presenting the erase signal on terminal 58. The reset signal originates from a control source (not shown). The output of NAND gate 62 goes low and, due to inverter 65, activates transistors 64 and 67. Activating transistor 64 turns on transistor 68. Transistor 68 functions as a switch and when turned on places V_{ERASE} on source 52.

As the cell 50 continues to erase, the floating gate 54 potential increases positively and the drain node potential of drain 53 increases as a result of cell sub-threshold conduction charging this node. When the drain node voltage of drain 53 exceeds the reference voltage V_{REF} the output of comparator 56 goes high to set the ouput of latch 61 low and results in a high output from NAND gate 62. Transistors 64 and 67 are turned off as transistors 63 and 66 are turned on. Due to a high state of

the gate of transistor 68, transistor 68 is turned off removing V_{ERASE} from source 52.

Using this feedback scheme the electron discharge level of floating gate 54 can be adjusted to a predetermined desired level by adjusting the reference voltage V_{REF}. The output of comparator 56 is fedback on line 60 to turn off the erase signal on terminal 58 and activating transistor 57 to place a ground on drain 53. The erase cycle is completed.

Although a particular circuit implementation is shown, it is appreciated that various other circuits can be used without departing from the spirit and scope of the invention.

Thus, a self-limiting erase scheme for EEPROMs has been discribed.

CLAIMS

1. An apparatus for self-limiting an electrical erase of a floating gate electrically programmable and electrically erasable read-only memory (EEPROM) cell having a source, drain, floating gate and control gate, comprising:

voltage supply means coupled to said source to provide an erase voltage for discharging of electrons from said floating gate;

feedback means coupled to said drain for providing a feedback signal to limit said discharging;

whereby said erasing cycle is terminated prior to over-erasing said EEPROM cell.

2. The apparatus as defined in Claim 1, wherein said feedback means is coupled to said drain and said control gate for providing a feedback voltage proportional to a potential of said drain, such that as said electrons discharge from said floating gate, said feedback voltage increases proportionately to provide a counteracting potential on said control gate to inhibit said discharging.

3. The apparatus as defined in Claim 2, wherein said feedback means is comprised of an amplifier having a predetermined gain.

4. The apparatus as defined in Claim 3, wherein said voltage supply means provides a positive erase voltage.

5. The apparatus as defined in Claim 4, wherein said feedback means further includes a buffer coupled to said amplifier.

6. The apparatus as defined in Claim 1 is further comprised of switching means coupled to said feedback means and said voltage supply means for deactivating said voltage supply means, said switching means being controlled by a control signal from said feedback means.

7. The apparatus as defined in Claim 6, wherein said feedback means monitors a potential of said drain, such that as said electrons discharge from said floating gate, said drain potential increases proportionately; said feedback means generating said control signal to turn off said voltage supply means.

8. The apparatus as defined in Claim 7, wherein said feedback means further includes a comparator for comparing said drain potential to a reference source, such that said comparator generates said control signal to turn off said voltage supply source when said drain potential exceeds said reference source.

9. The apparatus as defined in Claim 8, wherein said voltage supply means provides a positive erase voltage.

10. A method for self-limiting an electrical erase of an electrically programmable and electrically erasable read-only memory (EEPROM) cell having a source, drain, floating gate and control gate, comprising the steps of:

providing an erasing potential on said source to cause electrons to tunnel from said floating gate to said source;

coupling a potential of said drain as feedback to said control gate, such that as said floating gate is discharged of said electrons, said drain potential increases proportionately to said discharge and said feedback also causes a proportionate increase in potential at said control gate to counteract said erasing potential;

whereby said electron discharge is inhibited to prevent over-erasing of said EEPROM cell.

11. A method for self-limiting an electrical erase of an electrically programmable and electrically erasable read-only memory (EEPROM) cell having a source, drain, floating gate and control gate, comprising the steps of:

providing an erasing potential on said source to cause electrons to tunnel from said floating gate to said source;

monitoring a potential of said drain, wherein as said electrons discharge from said floating gate, said drain potential increases proportionately;

comparing said drain potential to a predetermined reference value;

deactivating said erasing potential when said drain potential exceeds said predetermined reference value;

whereby said electron discharge is terminated to prevent over-erasing of said EEPROM cell.

12. The method as defined in Claim 11 further comprising the step of grounding said control gate prior to providing said erasing potential.

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