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(54) Title of the Invention: **Housing for accommodating a photonic integrated circuit chip**
Abstract Title: **Photonic integrated circuit chip housing having chambers**

(57) A housing 2 having a first 6 and second 8 chamber wherein one chamber accommodates a photonic integrated circuit (PIC) chip 4, the other chamber accommodates the PIC chip's electronics 10. The housing has an external first wall having first 12 and second 16 wall portions which partially define the first chamber. The first wall portion comprises an optical fibre connection interface 14 in which to connect external optical fibres with the PIC chip. The second wall portion comprises a window 18. The housing comprises an internal second wall 20 to separate and thermally insulate the chambers. The first wall may comprise a third and fourth wall portion; one wall comprises a user input interface, the other a user display. The second wall may comprise means for electrical connections to pass across the chambers. The first chamber may comprise first and second optical fibres. The housing may comprise a battery (300, Fig. 4) and one or more light sources; each light source having different central wavelengths. Light may be incident upon the PIC chip, the reflections exit via the window having a magnifying lens. An integrated optic waveguide, a PIC chip and a photonics teaching module are also claimed.

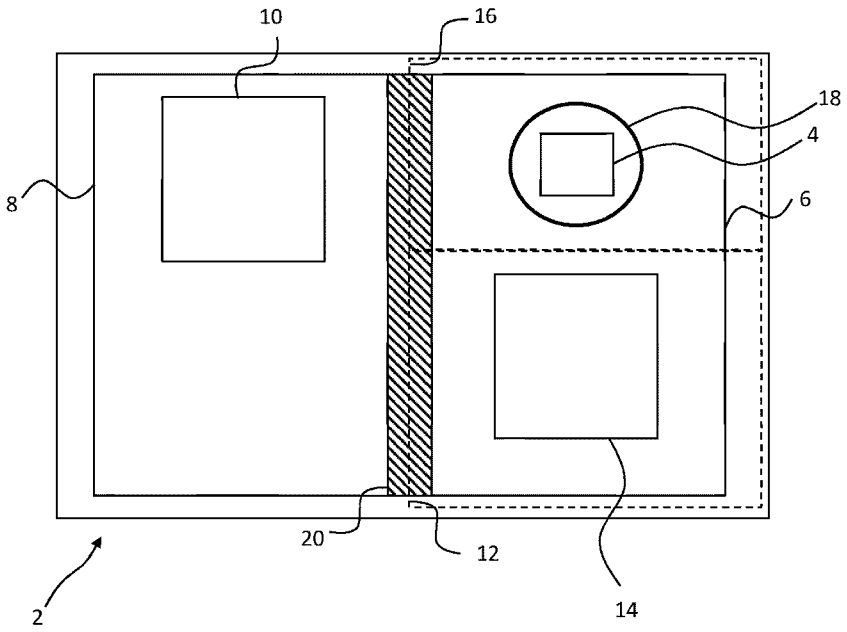

Fig. 1

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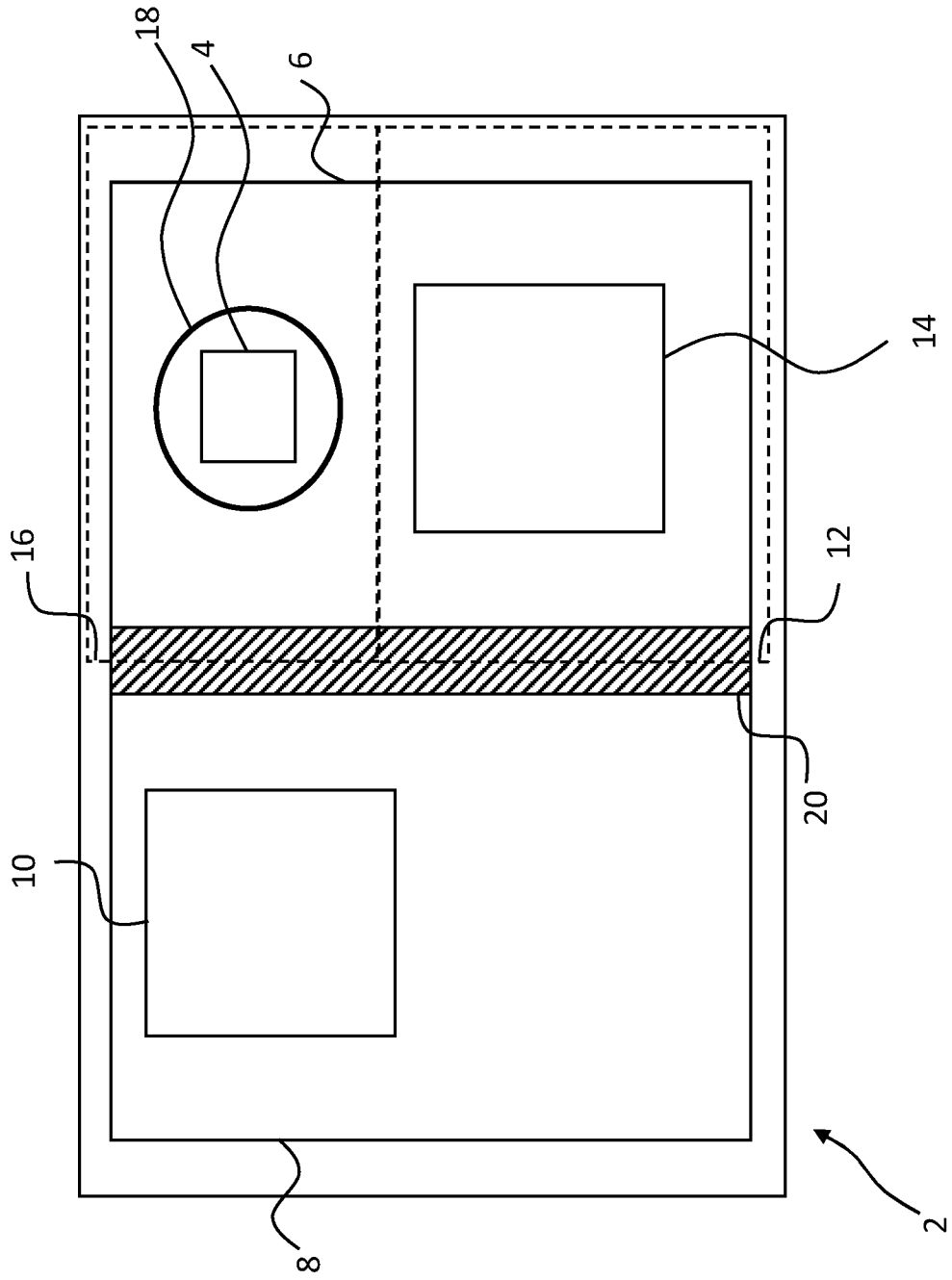

Fig. 1

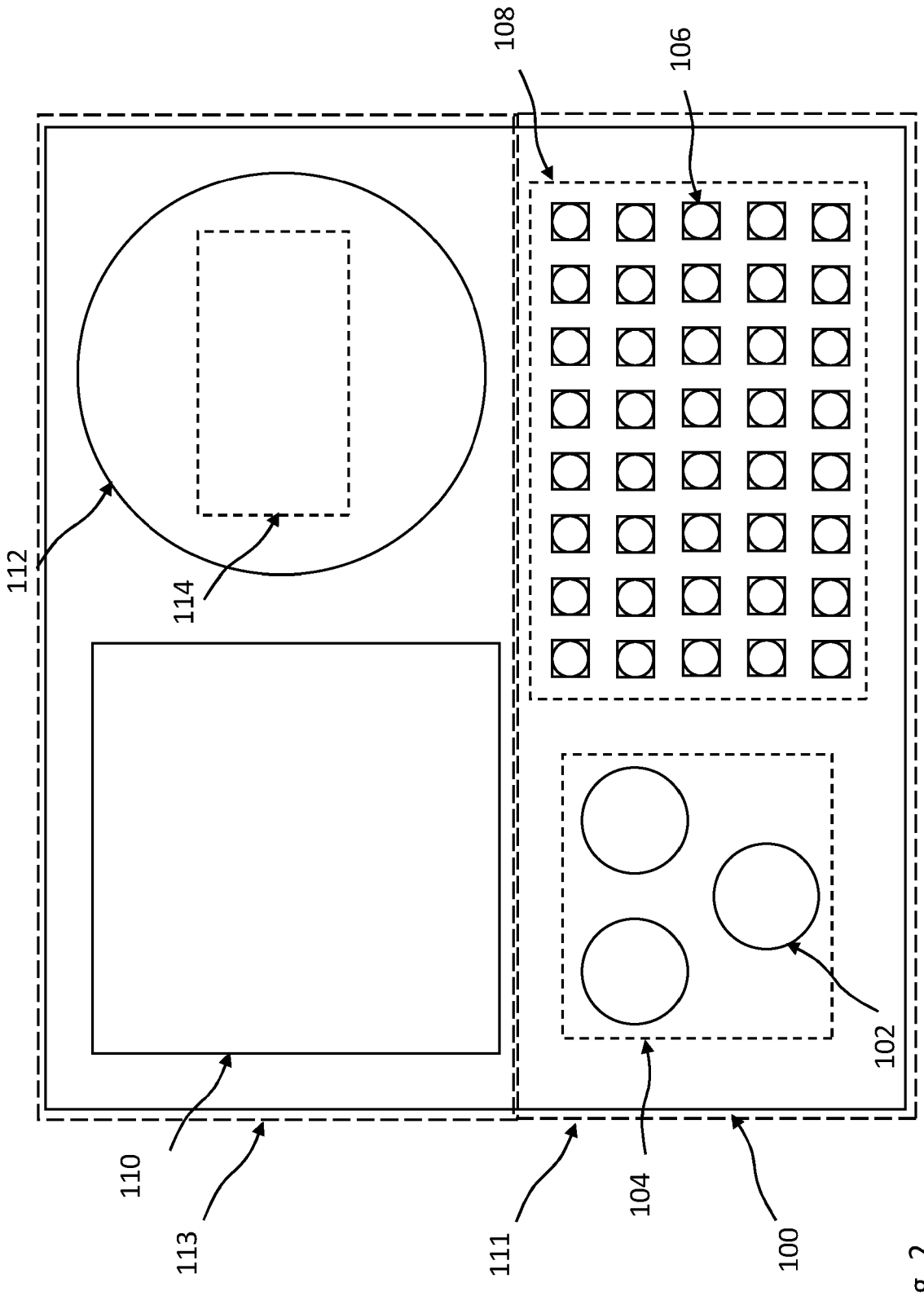

Fig. 2

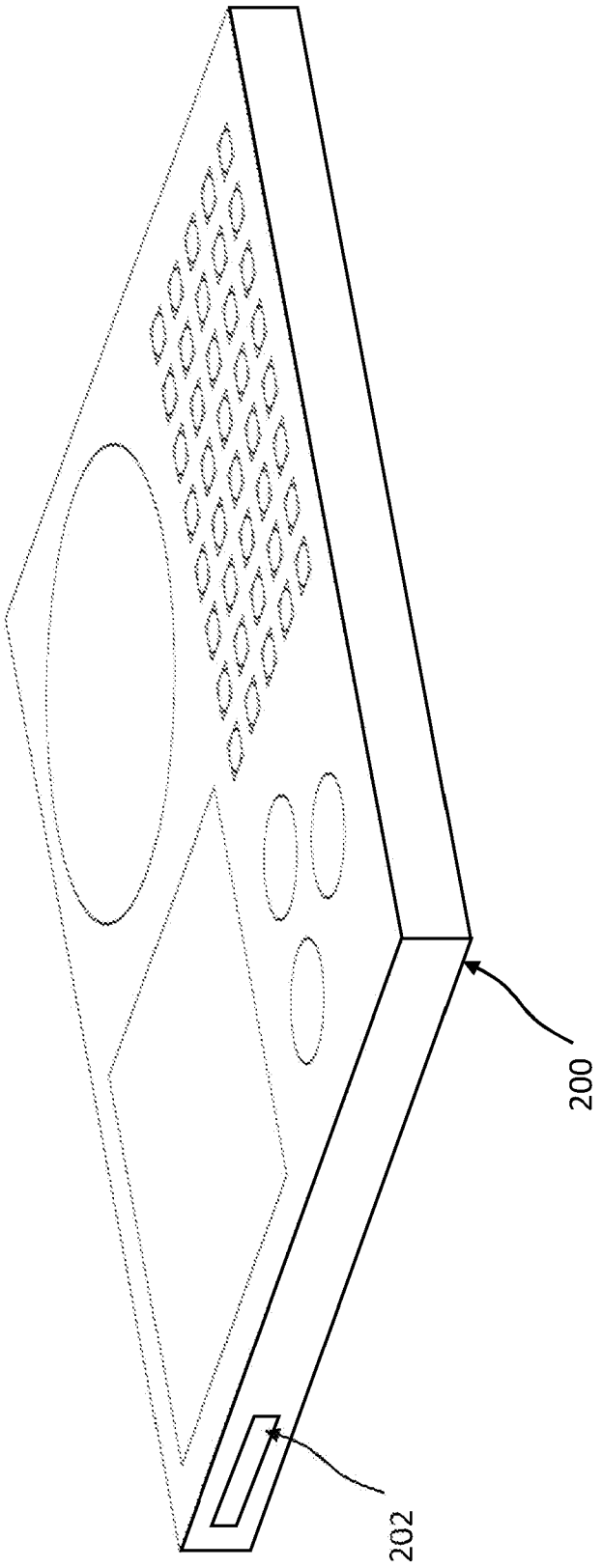

Fig. 3

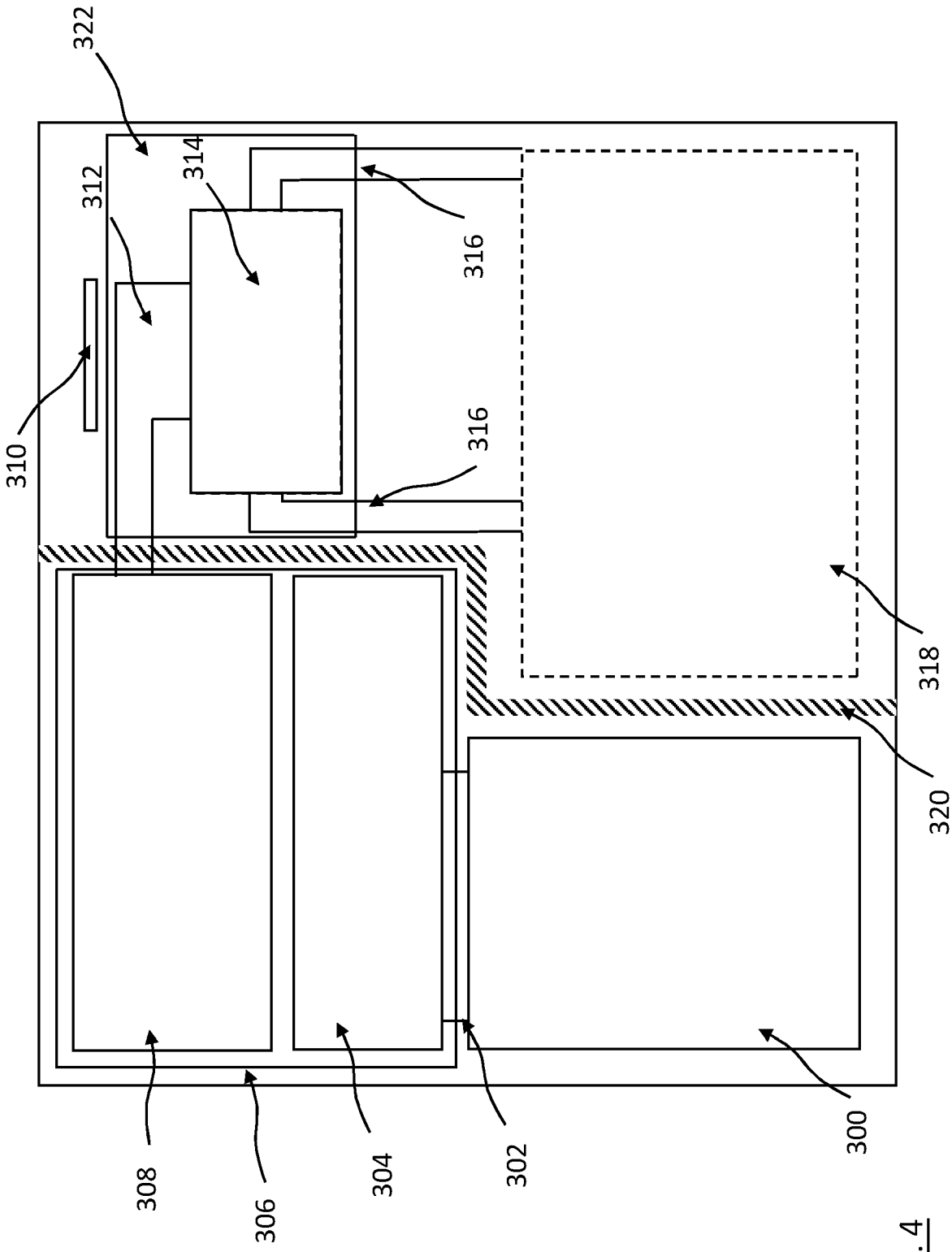

Fig. 4

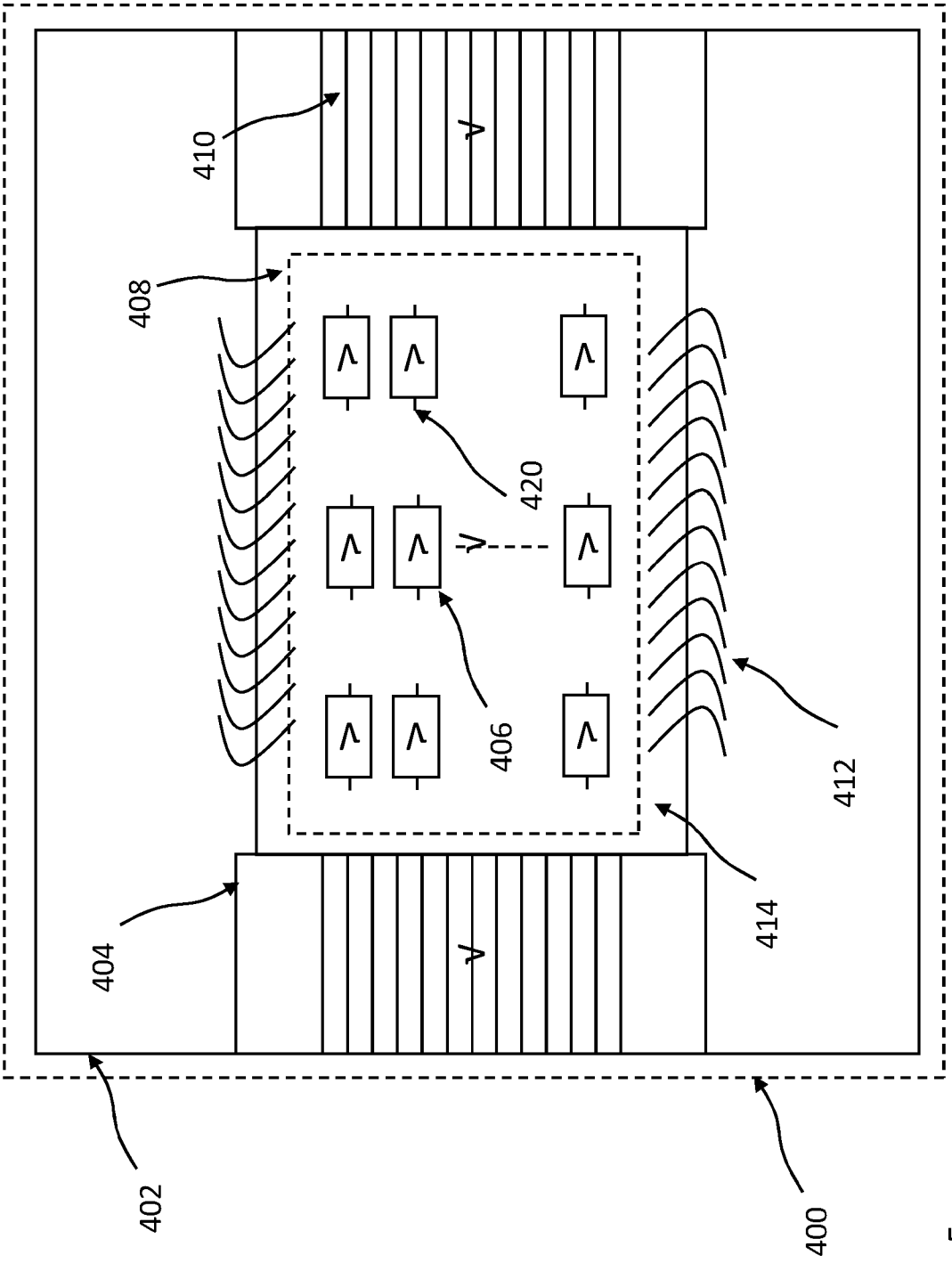

Fig. 5

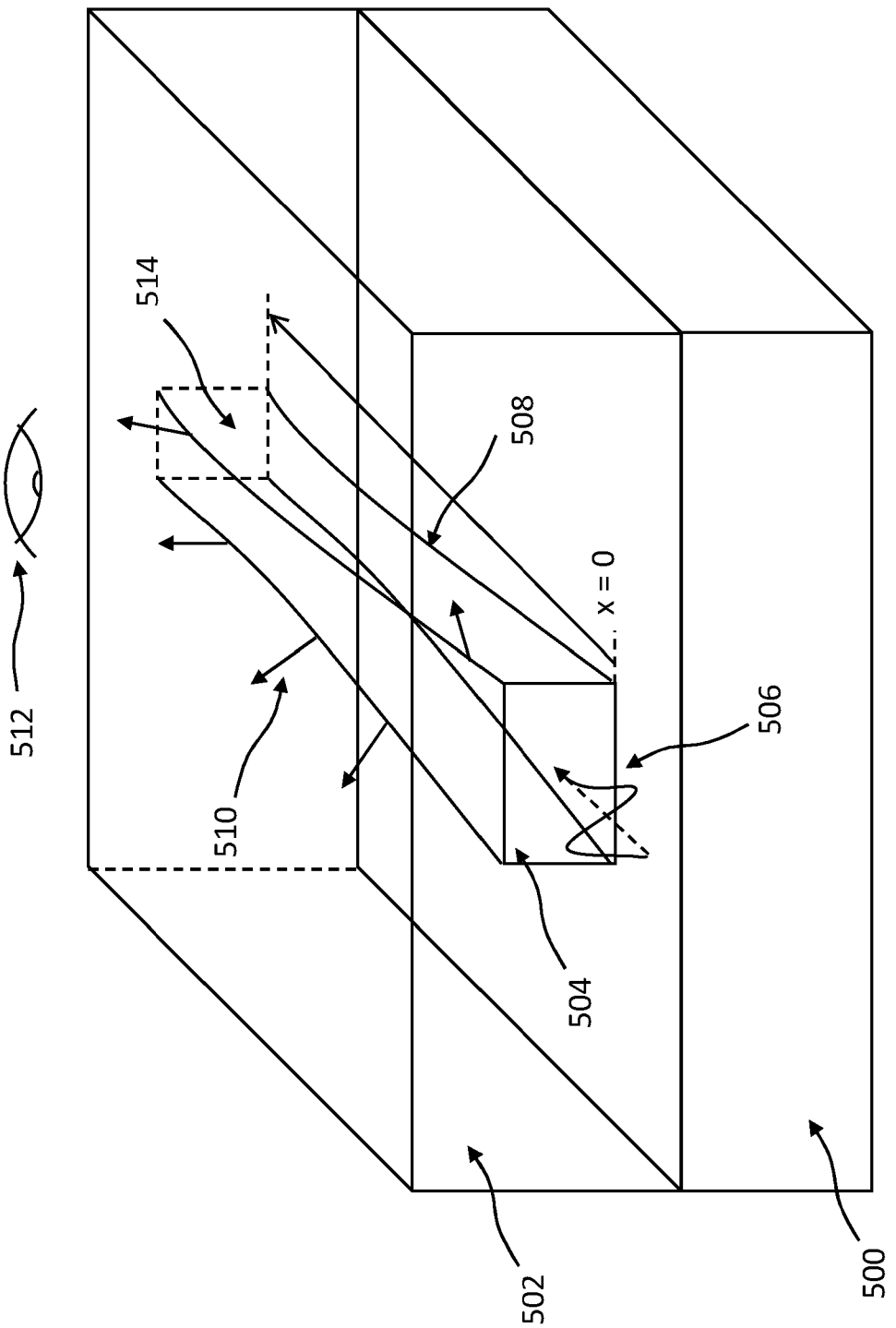

Fig. 6

Housing for accommodating a photonic integrated circuit chip

Field of invention

The present disclosure relates to an integrated photonics education module.

Background

In integrated photonics, waveguides of high-index material are embedded in a low index material layer to guide light around a chip. By optically patterning these waveguides onto a chip, complex structures can be built which perform specialised functions on the guided light field. These structures - known as integrated photonic components - can be concatenated together to form photonic integrated circuits (PICs) which typically perform some computation or measurement of the environment. The key benefit afforded by PICs is the ability to pattern many components into a single, phase stable chip that can then be deployed much more easily than an equivalent fibre or bulk-glass setup.

Current educational devices in photonics are limited to simple bulk-glass components such as prisms, mirrors, lenses, etc. These devices are great for teaching the student about core principles of photonics such as diffraction, reflection, and magnification, however, they are much less suited to demonstrating other more complex concepts, such as waveguiding, interference and nonlinear optics, which often require the assembly of multiple components to demonstrate.

Summary of invention

This invention leverages the key benefits of PICs to bring a suite of components to the user in a module that is designed to teach core photonic principles in a clear, fun and interactive way.

Using an integrated photonic component module to provide access to a host of basic components in a package that affords quick-and-easy, plug-and-play experimentation removes the need for difficult and lengthy alignment procedures often required with bulk or fibre-based components, allowing the user to explore these more advanced concepts over the course of a single lesson.

In this education module we provide a photonics microchip with direct access to simple photonic componentry (e.g., waveguides, bends, beamsplitters, phase shifters, reflectors, filters) via a grid of fibre ports that the student can connect to form a particular circuit with fibre patch cords. The chip will be positioned in the module so that the user has a clear, magnified view of the device with waveguides engineered to provide the optimal level of scattering so that the viewer may see in real time how visible laser light passes through their light circuit. By giving the user a live visual of the light traces through their circuit, we will be able to more easily teach them about key concepts such as interference.

The educational module will have on on-board processor outputting to a screen which will be used to walk the student through basic, example experiments. The user will be able to manipulate the properties of some components by setting the voltage of metal wires that overlay them. In doing so, they will see first-hand how phase-differences can affect the path light takes through the chip. A back light will illuminate the chip, showing labels for each component that map to the fibre port they interact with.

Integrated photonics is a growing, global market and is currently facing a shortage of integrated photonic engineers. By getting interactive, integrated photonics devices into high schools and undergraduate university labs we will help promote integrated photonics as a potential career path for the next generation.

According to the invention, an apparatus suitable for providing the user with a direct and magnified view of the photonic chip comprising: a photonic integrated circuit, means for photonic chip housing, means for optical magnification of the chip, and means for constant-brightness waveguide routing.

The photonic integrated circuit comprising: (i) means to optically couple light in and out of the chip, (ii) means for performing manipulation of the light field via popular componentry, (iii) means to thermally tune these components separately and (iv) means to label components for enhanced education and ease of use. The photonic chip housing comprising: (i) means for environmental isolation of the device, (ii) means for direct line of sight to the chip surface through the housing and (iii) means for backlighting the chip for a clear view. The optical magnification of the chip for vertical, live viewing comprising: (i) means for optical magnification and (ii) means for direct line of sight.

The photonic integrated circuit is preferably achieved by using one singular chip with one guiding layer, but could be achieved with several guiding layers or several chips of different or

the same material composition. Means of coupling is preferably achieved via edge couplers butt-coupled to a fibre array, but could be achieved via photonic wire bonds, gratings, or photonic interposers. Fibre is preferably polarisation maintaining fibre to ensure optimal coupling in and out of the chip but can be any other type of fibre such as single mode, hollow core, or multimode fibre.

Means for performing manipulation of the light field via popular componentry include but are not limited to the patterning of buried waveguides, air-clad waveguides, rib or multilayer waveguides, metallic overlays for localised heating, or localised doping for electro-optic effects. Components include but are not limited to waveguides, bends, phase shifters, beamsplitters, filters, reflectors, polarisation control, tuneable delays and interferometers. Components need not be limited to passive componentry and may include integrated modulators, detectors, lasers, or wavelength converters that require additional electronic signals or which rely on nonlinear optics for more advanced education.

Means to thermally tune these components separately involve setting the voltage or current through a section of metallic overlay that changes the optical characteristics of a given component. Tuning may also be achieved by changing the temperature of local regions of the chip via other methods of localised heating or via global heating of the chip.

Means to label components for enhanced education are preferably using metal or waveguide layers to pattern labels into the chip but could be post processed onto the chip or overlaid via an additional layer on the chip.

Means for environmental isolation of the chip is preferably achieved via a hermetically sealed housing but could be achieved via resin overlay of the entire chip. Means for direct line of sight to the chip's surface through the housing is preferably achieved via a glass window in the chip housing. Direct line of sight could also be achieved via live camera feed to a screen atop the module. Means for optical magnification of this chip is preferably achieved via a series of magnification lenses positioned above the chip. Magnification could also be achieved via live camera feed or with a series of parabolic mirrors.

According to the invention, an apparatus suitable for providing the user with a light trace of substantially constant, or constant, brightness along each routing waveguide for clear and consistent highlighting of each component in use. Constant brightness provided by means to vary the rate of photon scattering along the length of the routing waveguide such that the total number of photons scattered per length remains constant, or substantially constant or constant

within an upper and lower level of brightness. This is preferably achieved by varying the width of the waveguide along its propagation axis in a nonlinear manner such that the total number of photons scattered per length remains constant (see detailed drawings for more detail). This can also be achieved by artificially increasing the sidewall roughness of the waveguide.

According to a first aspect of the present invention there is presented a housing (2) for accommodating a photonic integrated circuit, PIC, chip (4); the housing comprising: a first chamber (6) configured to accommodate the PIC chip; a second chamber (8) for accommodating electronics (10) for operating the PIC chip; a first wall comprising: a first wall portion (12), at least partially defining the first chamber, and comprising an optical fibre connection interface (14) for removably connecting one or more external optical fibres to the housing; the optical fibre connection interface for optically linking the PIC chip to the one or more external optical fibres; a second wall portion (16), at least partially defining the first chamber, and comprising a window (18) for observing the chip from the outside of the housing; wherein the first wall forms an external wall of the housing; a second wall (20) separating, and thermally insulating, the first chamber from the second chamber; the second wall being internal to the housing.

The first aspect may be adapted according to any feature or configuration described herein, including but not limited to any one or more of the following options.

The housing may comprise a third wall wherein at least a portion of the third wall defines the first chamber; wherein the second wall connects the first wall to the third wall. The third wall may be a rear wall for contacting a supporting surface in use.

The housing may comprise a substantially rectangular box-like shape. The box may be substantially planar, in that the box is relatively shallow (or others 'short' in height compared to its other perpendicular dimensions, wherein the height is the dimension extending from the third wall to the first wall.

The first wall may be substantially planar. The different wall portions of the first wall may be regions of the wall that are adjacent and connect to one another. The entire wall may be unitary in nature in that the different wall portions may be formed as one piece, optionally with other parts of the housing such as, but not limited to the second (or another) wall. The housing, or any part of it, may be formed of a heat insulating material such as a plastic. Other materials may also be used. The housing may be modular in that different parts of the housing. The materials forming the outer walls of the housing, and optionally other walls of the housing may be opaque or substantially opaque to visible light. The window in the

second wall portion may be an aperture within opaque material of the said second wall portion. The window

The second wall may be an elongate strip. The second wall may run from one end of the housing to another end of the housing, for example from an end adjacent to or comprising the first wall portion (of the first wall) to an opposite end adjacent to or comprising the second wall portion.

The housing may comprise a plurality of edge-walls connecting the first wall with the third wall wherein each edge wall comprises a surface bordering and facing the external environment. The edge walls may be mechanically connected together (through any means, including being unitary with each other). Different edge walls may be connected via corners. The edge walls may have planes that extend substantially perpendicular to the planes of the first and third walls. The edge walls may define a periphery of the housing that runs around, and connects to, the edge of the first wall. A first edge-wall and second edge wall may be opposite each other, with each taking a different end of the housing. The second wall may internally connect the first edge wall with the second edge wall. Third and fourth edge walls may also connect the first and second edge walls wherein the second wall is spaced from the third edge wall and the second edge wall. The second wall may run substantially parallel to the third edge wall and the fourth edge wall.

Any of the first chamber and/or second chamber may extend between the first wall and the third wall. The first chamber may extend between the second wall and the third edge-wall. The second chamber may extend between the second wall and the fourth edge-wall. Any of the first and second chamber may extend between the first and second edge walls. The edge walls and the first and third walls may form the outer walls of the housing.

The second wall may take a nonlinear (i.e., non-straight) path between the first and second edge walls. The second wall may extend proximal to, but not contact edge walls. In such examples, gaps may be used to run features such as electrical connections and/or may be filled with a resin or adhesive.

The electronics for operating the PIC chip may comprise processors or controllers that are powered by an electrical power source (such as a battery) and may output one or more electrical control signals for operating features of the PIC chip or other feature of the housing such as a light source. The housing may comprise internal quadrant regions wherein two quadrant regions are of the first chamber whilst the other two quadrant regions are of the second chamber. The quadrant regions may not be identically shaped. The quadrant region accommodating an electrical power source may be: a) adjacent the quadrant region of the

second chamber accommodating the electronics for operating the PIC chip; b) adjacent the quadrant, underneath the optical fibre connection interface, in the first chamber; c) diagonally opposite the quadrant of the first chamber accommodating the PIC chip. The quadrant underneath the optical fibre connection interface may comprise optical fibres that run from that quadrant to the adjacent quadrant accommodating the PIC chip.

The housing may be configured such that the first wall comprises:

a third wall portion, at least partially defining the second chamber, and comprising a user input interface.

The user input device may comprise one or more buttons or control manipulandum.

The housing may be configured such that the first wall comprises: a fourth wall portion, at least partially defining the second chamber, and comprising a user display.

The user display may comprise a touch-input display.

The housing may be configured such that the second wall comprises one or more features for allowing electrical connections to pass between the first and second chambers.

These features may be through holes. The through holes may accommodate the electrical connections and may be sealed (for example with an adhesive) to prevent fluid passing through the through hole between the first and second chambers.

The housing may optionally comprise: a first optical fibre in the first chamber; and, a second optical fibre in the first chamber; wherein: the optical fibre connection interface comprises a plurality of optical fibre connection ports, each port configured to mechanically connect, and optically link, to a different external optical fibre; the first optical fibre connects to a first of the optical fibre connection ports; the second optical fibre connects to a second of the optical fibre connection ports; the first optical fibre configured in the housing to input light into a different facet of the PIC chip than the second optical fibre.

The housing may comprise a plurality of further optical fibres. Any of the optical fibres may be single mode or multimode optical fibres. The optical fibres may run from the optical fibre connection interface, substantially parallel to the plane of the first wall, to the PIC chip.

The housing may further comprise one or more light sources for outputting light to be incident upon the PIC chip.

The one or more light sources may be mounted upon an inwardly facing surface of the first wall, preferably the first wall portion of the first wall. The light sources may be mounted within the first chamber.

The housing may be configured such that the one or more light sources are configured to direct light onto the PIC chip such that the said light reflects off the pick chip and directly exits the housing through the window.

The term 'directly' here is intended to mean that the light is incident upon the window without reflecting off another object after reflecting off the PIC chip. The one or more light sources may comprise a plurality of light sources. At least two of the plurality of light sources may direct light onto different portions of the PIC chip.

The housing may be configured such that the one or more light sources comprises a first light source having a first central wavelength and a second light source having a second central wavelength.

Any of the light sources may be controllable by the user input interface of the housing and/or a touch enabled user display of the housing. The light source may be configured to input light at an obtuse or acute angle with respect to the surface normal of the chip. Different light sources may be operative to input light at different angles to the chip than other light sources.

The materials forming the outer walls of the housing, and optionally other walls of the housing may be opaque or substantially opaque to visible light. The window in the second wall portion may be an aperture within opaque material of the said second wall portion. The window may comprise one or more layers of transparent material extending across the entirety of the aperture. The material of the window may be shaped to form one or more lenses (such as a convex lens) that provides magnifying power for a viewer to observe the chip from outside the housing. The housing may comprise a plurality of lenses in a stacked arrangement, to enable the viewer to view the chip under magnification. The stack may extend, in a stacking direction, in a direction parallel to the direction starting from the chip to the window. The lenses may be made of glass or plastic. The lens or lenses may either form the window and/or be disposed above or below the window (i.e., respectively, form part of the housing's first wall, be external to the housing or be internal to the housing).

The housing may further comprise a lens disposed about the window.

The housing may be configured such that the lens is a magnifying lens.

The housing may further comprise a battery for supplying electrical power to the electronics.

The housing may further comprise the PIC chip.

The battery may be disposed towards an opposite end of the housing to the PIC chip. The battery may be disposed in a region of the housing diagonally opposite the regions of the housing accommodating the PIC chip.

The battery may supply power to other elements of the housing or components within the housing including, but not limited to: the user display; a light inside the first chamber for illuminating the PIC chip.

According to a second aspect of the present invention there is presented an integrated optic waveguide comprising: a length along which light propagates; wherein; a first position along the length spaced apart from a second position along the length; wherein light propagates from the first position to the second position; the integrated optic waveguide cross section changes in at least one of the following characteristics: i) waveguide width; ii) waveguide depth; iii) waveguide core refractive index; iv) waveguide core wall surface roughness;; v) cross section proximity features; between the first position and second position such that light propagating between the first and second position scatters substantially the same intensity of light along the length between the first position and second position.

Cross section proximity features may be features introduced to induce scattering. Typically, such features are disposed around the outside of the core waveguide or may be internal as well. They are typically design elements that are perturbations of the usual waveguide profile in cross section that do not substantially extend along the length of the waveguide, for example they may be sub-wavelength in dimension or possibly only extend a number of wavelengths along the length of the waveguide.

The second aspect may be adapted according to any feature or configuration described herein, including but not limited to any one or more of the following options.

The integrated optic waveguide may be configured such that the waveguide changes at least one of the characteristics i)-v) in a nonlinear manner between the first positions and the second position.

The integrated optic waveguide may be configured such that waveguide width is varied nonlinearly between the first position and second position.

The integrated optic waveguide may be configured such that the propagation loss, α (x), of the waveguide varies along the length, x, of the waveguide from the first position to the second position according the following equation:

$$\alpha(x) = \frac{1}{x}\ln\left(\frac{1}{1-\alpha_c x}\right).$$

wherein the starting propagation loss at the first position is α_c.

There is also presented a photonic light wave circuit waveguide design comprising: a first integrated optic waveguide comprising an integrated optic waveguide described above; a second integrated optic waveguide comprising an integrated optic waveguide as described above; a waveguide component connected and optically linked to the first integrated optic waveguide and the second integrated optic waveguide.

The photonic light wave circuit waveguide design may be configured such that the waveguide component comprises a first end connected to the first integrated optic waveguide; and a second end connected to the second integrated optic waveguide; such that light travels along the length of the first integrated optic waveguide, through the waveguide component and subsequently along the length of the second integrated optic waveguide.

There is also presented a device comprising a plurality of photonic light wave circuit designs described above; wherein the first and second integrated optic waveguides of each photonic light wave circuit waveguide design terminate at a separate optical input/output interface of the device.

The device may comprise: a first array of optical fibres for optically coupling to the first integrated optic waveguides of the photonic light wave circuit designs; a second array of optical fibres for optically coupling to the second integrated optic waveguides of the photonic light wave circuit designs.

According to a third aspect of the present invention there is presented a photonics integrated circuit, PIC, device comprising a plurality of integrated optic waveguide-based components distributed as an array over a region of the device wherein each of the said integrated-optic waveguide-based components is respectively connected to: an input integrated optic waveguide running from the component to a device facet; an output integrated optic waveguide running from the component to a device facet; wherein the input integrated optic waveguide is different to the output integrated optic waveguide.

The third aspect may be adapted according to any feature or configuration described herein, including but not limited to any one or more of the following options.

The photonics integrated circuit, PIC, device may be configured such that the array is a periodic distribution of components.

The photonics integrated circuit, PIC, device may be configured such that the distribution is about a plane parallel to the planer extent of the device

The photonics integrated circuit, PIC, device may be configured such that the distribution is substantially grid-like.

The array may comprise a regular distribution, a periodic distribution of components. The PIC device may be substantially planar. The input waveguide may run to a first facet whilst the output waveguide may run to a second facet that is different to the first facet. The first and seconds facets may be at opposite ends of the device.

Any of the input waveguide or output waveguides may be those as described in the second aspect.

The integrated optic waveguide-based components may be any of, but not limited to: optical couplers or combiners, waveguide multiplexers or demultiplexers, interferometers, waveguide bends, waveguide gratings.

There is also presented a photonics teaching module comprising: the housing as described above; and any of: the device as described above; or, the photonics integrated circuit, PIC, device as described above.

Brief description of the drawings

Preferred embodiments of the invention are now described, by way of example only, with reference to the accompanying drawings wherein:

Figure 1 shows a schematic example of a housing for accommodating a PIC chip;
Figure 2 shows an example of a top-down outside view of a housing;
Figure 3 shows an example of a 3D perspective outside view of the housing of the example of figure 2;
Figure 4 shows the inside of the housing of the example of figures 2 and 3;
Figure 5 shows an example of a PIC chip coupled to internal optical fibres of the housing;
Figure 6 shows an example of a waveguide for outputting substantially constant scattered light from along its length.

Detailed description

Figure 1 shows an example of a housing 2 according to one aspect. The housing 2 is for accommodating a photonic integrated circuit, PIC, chip (4). The housing comprises a first chamber 6 configured to accommodate the PIC chip 4. The housing also comprises a second chamber 8 for accommodating electronics 10 for operating the PIC chip. The housing comprises a first wall that forms an external wall of the housing. The first wall comprises a first wall portion 12 that at least partially defines the first chamber. The first wall portion comprises an optical fibre connection interface 14 for removably connecting one or more external optical fibres to the housing. The optical fibre connection interface is for optically linking the PIC chip to the one or more external optical fibres. The first wall comprises a second wall portion 16 that at least partially defines the first chamber. The first wall portion comprises a window 18 for observing the chip from the outside of the housing. The housing also comprises a second wall 20 separating (and thermally insulating) the first chamber from the second chamber. The second wall is internal to the housing. Having an insulating wall preventing heat from electronics affecting optical components in the first chamber is desirable as heat can affect the functioning of the optical components.

Figure 2 shows an example of a module 100 wherein the module can be adapted to: add in further component; remove components; reconfigure components. The module 100 comprises a plurality of sections about which different components are located. The sections may be defined in relation to module edges. Preferably the educational module 100 has a face for facing a user when in use. The face comprises the viewing window 112, through which the user may observe the chip within the chip housing 114. The module may have a shape in the plane of the surface that is rectangular, as exemplified in Figure 2, however other shapes may be used such as pentagon, hexagon etc. The module may have a first end section 111 and a second end section 113 that are adjacent to each other in a plane parallel to the plane of the said user-facing face. The first end section of the module may comprise user-controllable mechanisms for controlling one or more features of the module. Mechanisms may include any of, but not limited to: fibre ferrules 106, push-button dials 102 or otherwise other user-control interfaces that allow a user to input information to the module.

In Figure 2, the first end section 111 is shown near the bottom of the figure and comprises the ferrule grid region 108 and the group of dials 104. It should be noted that the ferrule grid 108 may be any designated area on the top surface of the module where optical fibre ferrules are located, not necessarily always in a grid. The ferrule grid (or otherwise ferrule area or region) of the user-facing surface may comprises a plurality of optical fibre connecting ports, preferably female-like connectors to receive an optical fibre connecting pigtail, such as, but not limited to a male-like FC-PC fibre end, or other male-like fibre connector end. Preferably

the abovesaid first end section of the module is split into two or more sub-end sections wherein each sub-end section is adjacent to the other sub-end section about a plane parallel to the plane of the user-facing face. Each sub-end section may comprise a different type of one or more components. For example, in Figure 2 a first sub-end section is in the bottom left corner and contains the control dials 102, whilst the second sub-end section is in the bottom right corner and contains the ferrule grid 108. The first sub-end section is shown to have three dials placed in a triangular configuration, however, a singular, or multiple, dials may be used, placed in any configuration within the first sub-send section. Buttons may also be used instead of dials.

In Figure 2 the second end section 113 is shown near the top of the figure and comprises the viewing window 112 and the display 110. Similarly, to the first end section 111, the second end section 113 may have sub-end sections wherein: a first sub-end section at the top right of the module 100 in the figure, contains the viewing window; and the second sub-end section, containing user-viewing mechanisms, is in the top left of the module 100 in the figure. The second sub-end section preferably contains a digital display window for interfacing with the user. The digital display is ideally rectangular is shape but could be another shape such as circular. The display could also be touch screen for additional user-control of the module's mechanisms and may be multiple screens instead of one singular screen.

Having the user inputs in one section and the user viewing features in another section allows for optimised location of features such that a user can orientate the module such that the users' hands are close to the first end section, but, when operating the module, these hands are not obscuring the window 112 or display. Furthermore, having the ferrules in this first end section allows the user to group the input fibre tails (to the ferrules) and run them, as a group, away from the module. For example, the user may simply have the input fibres running directly away from the module 100 extending away from the first and second end section in a direction substantially parallel to the plane of the module's user-facing surface. Thus the fibres do not run over and obscure the viewing features 110, 112 . If the module were to have fibre ferrules disposed around the chip viewing area 112, (possibly to coincide close to where the optical input/outputs of the chip are located), then it would be harder for the user to group these fibres without obscuring the view of the display 110 or the window 112. Additionally, if the user-interface dials were disposed around the chip or amongst the fibre grid, operation of these dials would likely disturb the fibres, introducing additional polarisation or phase drift which may affect a given experiment.

The first sub-end section of the second end section 113 at the top right is an opening that allows for magnified viewing into the chip housing 114. A magnified view of the chip allows the user to resolve individual components on the chip so that they can assess where light is passing through the chip to learn about photonics. Preferably, the opening is circular to accommodate a series of lenses, or a singular lens, stacked in a direction parallel to the chip surface to allow for magnification of the chip when viewed from above. The opening may also be other shapes such a rectangular, hexagonal, etc that allow for visual access to the chip housing below.

Preferably, lenses are stacked between the top of the chip housing and the opening. It should be noted that lenses could also be held above the top surface of the module or within the chip housing. By stacking lenses vertically above the chip housing, the user is provided with a magnified view of the entire chip, with minimal edge distortion, using a compact magnification system. If the module were to employ a set of mirrors and lenses to provide a view of the chip from another face of the module, or not directly above the chip house, the user would not be able to monitor both the chip and the user-interface from the same vantage point. By placing the magnification lenses directly above the chip, we also minimise the overall size of the magnification system to ensure the device remains as light and compact as possible for optimal classroom use. A camera may be used instead of a lens system, with the output feed passed either to an additional screen in section 112 or to the user-interface in the adjacent display 110, however, this will not provide chip viewing with the naked eye, detracting from the educational experience provided to the user by the module.

Figure 3 shows a module 200 similar to that of Figure 2. The module 200 has all its sections in a planar configuration for optimal bench-top use in a classroom setting. The height of the module, as depicted in Figure 3, is preferably the smaller of the modules three dimensions, with the width and length of the module allowing for easy transportation by a singular student. It should be noted that the top-facing plane (hence the whole module 200) may be rotated along any edge of the device with additional supports to tilt the device towards the user for seated use. The module, although containing a battery, user-controls and a display window, may require a power charging port and would ideally have an additional USB port, or similar, for optional remote control via a secondary computer. These ports should ideally be placed on one side of the module, closest to the onboard processor, in a group as depicted in 202 to allow for use next to a desktop computer, however, they could be placed on any surface of the module either as a group or spread across the device.

Figure 4 shows the interior of the module 100, 200 of Figures 2 and 3 respectively. The module interior consists of a plurality of sections which are separated out according to their functions, and which align with the four main sub-end section atop the module, described above. Figure 4 depicts these sections, showing main electrical and optical connections between the chip housing 314 and the rest of the module. The first end section of the module, underneath (in module depth dimension) the user control mechanisms and optionally the fibre grid, may comprise of a battery 300, which enables portable use in the classroom and fibre routing sections 316, from the chip housing to the fibre ferrules grid 318 for user-interfacing. Fibre routing sections 316 are preferably walled to form a channel in which resin or glue can be poured to set the fibres in place. This will help promote phase-stability and minimise polarisation drift as the device is moved around the classroom. This could also be achieved by using mechanical fastening such as clips or ties along the length of the fibre routing.

Preferably, the battery is located beneath the user-control interface to allow for ample space below the fibre grid for fibre connectors to bend upwards, perpendicular to the module user-facing plane. Without such space, the fibre bend radius to accommodate for this bend would be too tight, leading to high optical loss in the fibre or a taller module. Optionally the fibre inputs in the fibre grid may substantially align with an end of the chip. In other words, in Figure 4, optical fibre inputs/outputs on the left-hand side of the photonics chip may link to fibre ferrules on the left-hand side of fibre grid area; and correspondingly, optical fibre inputs/outputs on the right-hand side of the photonics chip may link to fibre ferrules on the right-hand side of fibre grid area. This may allow for less fibre to be used internally and less crossing of fibres internally.

The second end section may have sub-end sections wherein a first sub-end section at the top right in Figure 4 is located underneath (in module depth dimension) the chip viewing sub-section 112, and the second sub-end at the top left of Figure 4 is located below the user display sub-section 110. This first sub-end section may comprise of the chip housing which is preferably a butterfly-type package with a clear top which may be soldered into place on a larger supporting printed circuit board 322. The chip housing preferably has optical fibre inputs and outputs on adjacent sides of the housing, with electrical pins perpendicular to these optical ports. Optical and electrical ports may not necessarily address adjacent sides of the chip housing but are preferably in plane with the supporting printed circuit. If this were not the case, ports would obstruct the users view of the chip.

Preferably, the chip housing is hermetically sealed via the use of a clear glass or plastic window material to seal the top side of the housing, whilst allowing a clear line of sight to the

chip, however, the chip housing may be left unsealed with no protective top window. It should be noted that this window may be replaced by a lens which doubles as part of the magnification system. The chip may also be glued directly to the supporting printed circuit board, forgoing the need for a chip housing, or may be mounted atop a metal plate to facilitate heat transfer away from the chip, to maintain the chips temperate with respect to the surrounding environment.

Isolation of the fibre routing and fibre grid from key heat sources within the module is important for providing optical phase stability through the fibre and chip. To isolate the main heat-producing electronics from the optical elements, an insulating wall 320 divides the sub-end sections of both end section. Insulation preferably runs through the entire module to minimise heat transfer. Active heat dissipation may also be used, especially around the battery, to dissipate heat to the environment. This may include a fan, directed at the battery 300, processor 304, or chip-control electronics 308. If the heat producing elements of the device were not kept adjacent, and isolated from the optical elements, the module would be negatively affected while the device is in operation. This would lead to unstable experimentation that may confuse the student, detracting from their learning experience. It should be noted that a stable temperature through the fibres 316 may also be achieved actively by bringing them into thermal contact with a Peltier cooler, or equivalent such technology, controlled by the processor or chip-control electronics and powered by the battery.

A backlight 310 is included to provide the user with an illuminated view of the chip within its housing. The term' backlight' is used here for reference purposes only as it is understood that the light is reflected off the front of the chip. The backlight is preferably situated adjacent to the chip housing, fastened to the underside of the top user-viewing face to allow for light to reflect off the chips surface at an angle towards the user. By placing the backlight such that rays reflect off the chip at an angle, refraction of layers withing the chip may be utilised to further highlight labels that have been patterned directly onto the chip, either in the metal or guiding layer. For example, using striped font that acts as a diffraction grating at the backlight wavelength of light will highlight labels when the backlight is held at the correct angle to the face of the chip. The backlight may also be positioned within the chip housing at the correct angle to achieve the same effect. Multiple backlights may be used, positioned at different angles or along different edges of the chip housing to further highlight the device or to add multiple highlight colours, helping single out different labels for different modes of operation. In addition, a singular chromatic light source may be used, with varied diffraction grating fonts used to highlight different label in different colours.

The second sub-end section may comprise of supporting electronics, required to operate the module, and is preferably located directly under the display section, on the adjacent side of the thermal barrier to the chip housing, connected to the display and user-interface dials via cables. Operational electronics include, but are not limited to, an onboard processing unit 304, with accompanying firmware, and a chip-control module 308 to control electrical signals to the chip. Additional electronics may include a control unit for any active heat control employed within the module such as a fan or Peltier cooler. All electronics are ideally soldered to a larger motherboard 306, with connections to the chip housing through thermally isolated cables 312 to minimise heat flow from one side of the insulation to the other. The motherboard is ideally connected to the battery adjacent to it via cables 302 to minimise heat flow from the battery to the control electronics.

Figure 4 shows the chip-control electronics adjacent to the onboard processing unit within the second sub-end section, however, the electronics within this sub-end section may not be separated out into two self-contained sections of the motherboard and may be mixed into one larger electronic system. Electronics may also be spread across more than one layers of motherboard that are stacked in a plane perpendicular to the motherboard surface within the sub-end section. Additionally, electronics may be soldered onto several smaller printed circuit boards, as opposed to one motherboard, which are connected via wires. The battery-containing sub-end section of the first section and the second sub-end section of the second section may be combined to form one larger section in which the position of all major electronic components may be soldered into a different configuration. Note that in this case, the major heat producing element, the battery, will not be as far removed from the chip as possible, leading to a greater chance of phase instability within the chip.

In Figure 5, the preferred layout of components on the chip, and their electronic and optical connections within the chip housing are shown. Optical ports enter from adjacent side of the chip housing 400, preferably using a V-grooved fibre array 404 that aligns each individual fibre 410 to a coupling structure along the side of the chip. Optical ports may also enter from non-adjacent sides, or a singular side. It should be noted that other methods of optical coupling may also be used such as, but not limited to, photonic wirebonds or tapered fibres. An additional spot size converter chip may be used between the V-grooved array and the chip to optimise coupling. The V-grooved array may also have an offset angle to the side face of the chip or may couple light in from the top surface of the chip via a grating. The figure shows a V-grooved array with regular individual fibre spacing but may also have irregular spacing or singular fibres glued in place individually without a support of a V-grooved array.

The optical chip 414 is preferably a singular chip that contains a collection of components 408 including, but not limited to, variable beamsplitters, phase shifters, tuneable filters, tuneable delays, etc. Each individual component 406 is shown to be positioned in a grid to allow for quick and easy locating of specific components by the user, however, components may be positioned in any configuration within the chip, or on multiple chips that have their own optical and electronic connections. Although this layout method is not the most space efficient, without it the user will find it difficult to identify specific components, especially if they have not used a photonic integrated circuit previously and therefore do not know what each component looks like prior to use.

Electronic connections between the metal wires within the chip and the supporting printed circuit board 402 within the chip housing are ideally achieved via wirebonds 412, but could also be achieved via other means, including but not limited to, solid probes or a flip-chip bonded electronic die. Figure 5 shows wirebonds in two sections of the chip located in rows along opposite sides of the chip to the optical ports. It should be noted that wirebonds may not necessarily be in sections of the chip and may be spread out across the chip. Having the fibre connections couple light from the chip sides, and wirebonds in sections along the chip sides, ensures the user has an unobstructed view of the components spread across the chip surface. If the wirebonds were to connect to the electrical ports of this chip from within the component grid 408, these would likely cover sections of components.

Each component has input and output waveguides that carry light from the fibres to each component 420. Figure 5 shows each component with only one input, directing towards one fibre array, and one output directing towards the adjacent fibre array. It should be noted that each component may have several input and output waveguides connecting to one or more edges of the chip. These waveguides may also enter or leave the component from any direction and may not route to separate fibres. Routing waveguides may also have additional components in them to form a series of components or may split to route one fibre input or output to more than one component port, or to several components. Having adjacent optical ports with inputs entering one side of the chip and outputs exiting the adjacent side of the chip helps reduce the number of bends required in waveguide routing and makes for a more logical, clear configuration to help increase the users understanding of the device.

The routing waveguides are designed to scatter light (depicted in Figure 6, 510) such that the brightness, as seen by the viewer 512, is constant along its length. Below, we present a detailed description of how to achieve constant brightness along a routing waveguide:

Prior to fabrication of the chip 414, the propagation loss of the waveguide as a function of waveguide width, $\alpha(d)$, is modelled. Here, d is defined as the distance from the central line of the waveguide to its sidewall i.e., half the waveguide width.

To solve for $\alpha(d)$ analytically, we use a model presented in Payne, F.P., Lacey, J.P.R. "A theoretical analysis of scattering loss from planar optical waveguides." Opt. Quant. Electron 26, 977–986 (1994), which is incorporated herein by reference; which finds an analytical solution for the propagation loss of a planar waveguide under the reasonable assumption that scattering only occurs from waveguide sidewall roughness that is well described by a spectral density function, $\tilde{R}(\Omega)$, that takes the form of equation 1:

$$\tilde{R}(\Omega) = \int_{-\infty}^{\infty} \sigma^2 e^{\left(-\frac{|u|}{L_c} + i\Omega u\right)} \mathrm{d}u.$$

[Equ. 1]

In Equ. 1, σ is the root mean squared deviation of the waveguide sidewall from flatness and L_c is the characteristic correlation length of the sidewall roughness. These two parameters are typically supplied by the chip fabrication house upon request. u is the distance between any two given points along the waveguide sidewall, and its reciprocal is Ω.

By using Equ.1, the model finds an analytical solution for $\alpha(d)$. We first define the following dimensionless parameters to simplify the maths in equation 2:

$$U \equiv d\sqrt{n_1^2 k_0^2 - \beta^2}, \quad V \equiv k_0 d\sqrt{n_1^2 - n_2^2}, \quad W \equiv d\sqrt{\beta^2 - n_2^2 k_0^2}, \quad s \equiv \frac{WL_c}{d}, \quad \& \ \gamma \equiv \frac{\sqrt{2}n_2 V}{W\sqrt{n_1^2 - n_2^2}}.$$

[Equ. 2]

Here, n_1 is the material index of the waveguide 504, n_2 is the material index of the cladding 502, β is the single-mode propagation constant of the waveguide, and k_0 is the free-space wavenumber. Note β is dependent on waveguide geometry and cross-section and can be calculated using any standard mode solving software (e.g., Lumerical).

$\alpha(d)$ can then be expressed as equation 3:

$$\alpha(d) = \frac{s\sigma^2}{\sqrt{2}k_0 d^4 n_1} \frac{U^2V^2}{(1+W)} \left(\frac{\sqrt{(1+s^2)^2 + 2s^2\gamma^2} + 1 - s^2}{(1+s^2)^2 + 2s^2\gamma^2} \right)^{1/2}.$$

[Equ. 3]

Using this model, we calculate the propagation loss for any given waveguide width in which only the fundamental mode is supported.

Figure 6 depicts an example of a routing waveguide that routes light from a fibre coupling structure 506 at the edge of the chip to a given component optical port 514.

Using the above equation, the propagation loss at the start of the routing waveguide i.e., at $x = 0$, is calculated. We call this starting propagation loss α_c.

To achieve constant brightness along the waveguide, the propagation loss is varied along the length of the waveguide such that it obeys the following equation 4 where x is propagation length along the waveguide:

$$\alpha(x) = \frac{1}{x} \ln\left(\frac{1}{1 - \alpha_c x}\right).$$

[Equ. 4]

This is preferably achieved by varying the width of the waveguide along its length as shown by 508. The required waveguide width as a function of x, can be found using Equ. 3. Specifically, the composition of the inverse of Equ. 3 applied to Equ. 4 gives the correct waveguide width as a function of propagation length. Note this can be solved numerically using these two equations.

Note also that due to the varied nonlinear nature of both $\alpha(x)$ and $\alpha(d)$, a simple linear taper in waveguide width, as typically used in integrated photonics for a variety of functions including fibre-to-chip coupling and mode mixing, cannot result in a routing waveguide of constant brightness. To highlight this, a nonlinear variation of waveguide width 508 is depicted in Figure 6.

It should be noted that the required waveguide width as a function of propagation length may be slightly different for each platform, chip fabrication method, or wavelength of operation due to the dependency of the parameters defined in Equ. 2 on the operational wavelength, material composition, sidewall roughness statistics and cross-sectional geometry.

Figure 6 shows this methodology applied to a straight section of waveguide, however, this may also be applied to bent sections of waveguide in which the propagation loss dominates the bend loss, as is true for wide bends or Euler bends. The methodology described above is applied to a section of routing waveguide that routes light from a fibre coupling component to a component port. The scheme may also be applied in reverse, routing light from a component port to a fibre coupling component. In this case, α_c is the propagation loss constant defined by the waveguide width leaving the component and x is the propagation length from the component port to the fibre coupling component.

The required affect can also be achieved by keeping the waveguide width the same along its length but adding artificial waveguide roughness to modify the propagation loss constant. This is akin to artificially increasing σ in Equ. 3. The characteristics of added noise may follow another probability distribution other than that presented in Equ. 1 across its length including, but not limited to, Gaussian noise, Rayleigh noise or white noise. Constant brightness may also be achieved via a combination of these two techniques.

The chip is shown to have a buried waveguide that sits in a low index material 502 supported by a substrate 500. The waveguide may also be exposed without cladding or suspended without full substrate support. The waveguide width at the fibre coupling component is ideally single mode at the operational wavelength but can also be multimode. As the waveguide width is decreased to induce constant brightness, the minimum width that can be achieved will be lower bounded by the single mode cut-off width of the waveguide at the operational wavelength. This places a limit on the total length of the routing waveguide which may have a constant brightness. Note this scheme may only be applied to strip waveguides due to Equ. 3 not being applicable to other types of waveguides e.g., rib-waveguides, however, the same affect could be achieved with a rib-waveguide by first measuring the form of $\alpha(d)$ with a series of test structures that enable estimation of propagation loss with waveguide width.

Claims

1. A housing (2) for accommodating a photonic integrated circuit, PIC, chip (4); the housing comprising:

a first chamber (6) configured to accommodate the PIC chip;

a second chamber (8) for accommodating electronics (10) for operating the PIC chip;

a first wall comprising:

a first wall portion (12), at least partially defining the first chamber, and comprising an optical fibre connection interface (14) for removably connecting one or more external optical fibres to the housing; the optical fibre connection interface for optically linking the PIC chip to the one or more external optical fibres;

a second wall portion (16), at least partially defining the first chamber, and comprising a window (18) for observing the chip from the outside of the housing;

wherein the first wall forms an external wall of the housing;

a second wall (20) separating, and thermally insulating, the first chamber from the second chamber; the second wall being internal to the housing.

2. A housing as claimed in claim 1 wherein the first wall comprises:

a third wall portion, at least partially defining the second chamber, and comprising a user input interface.

3. A housing as claimed in claims 1 or 2 wherein the first wall comprises:

A fourth wall portion, at least partially defining the second chamber, and comprising a user display.

4. A housing as claimed in any preceding claim wherein the second wall comprises one or more features for allowing electrical connections to pass between the first and second chambers.

5. A housing as claimed in any preceding claim comprising:

a first optical fibre in the first chamber; and,

a second optical fibre in the first chamber;

wherein:

the optical fibre connection interface comprises a plurality of optical fibre connection ports, each port configured to mechanically connect, and optically link, to a different external optical fibre;

the first optical fibre connects to a first of the optical fibre connection ports;

the second optical fibre connects to a second of the optical fibre connection ports;

the first optical fibre configured in the housing to input light into a different facet of the PIC chip than the second optical fibre.

6. A housing as claimed in any preceding claim further comprising one or more light sources for outputting light to be incident upon the PIC chip.

7. A housing as claimed in claim 6 wherein the one or more light sources are configured to direct light onto the PIC chip such that the said light reflects off the pick chip and directly exits the housing through the window.

8. A housing as claimed in claims 6 or 7 wherein the one or more light sources comprises a first light source having a first central wavelength and a second light source having a second central wavelength.

9. A housing as claimed in any preceding claim further comprising a lens disposed about the window.

10. A housing as claimed in claim 9 wherein the lens is a magnifying lens.

11. A housing as claimed in any preceding claim further comprising a battery for supplying electrical power to the electronics.

12. A housing as claimed in any preceding claim further comprising the PIC chip.

13. An integrated optic waveguide comprising:

a length along which light propagates;

wherein;

a first position along the length spaced apart from a second position along the length; wherein light propagates from the first position to the second position;

the integrated optic waveguide cross section changes in at least one of the following characteristics:

i) waveguide width;
ii) waveguide depth;
iii) waveguide core refractive index;
iv) waveguide core wall surface roughness;
v) cross section proximity features

between the first position and second position such that light propagating between the first and second position scatters substantially the same intensity of light along the length between the first position and second position.

14. An integrated optic waveguide as claimed in claim 13 wherein the waveguide changes at least one of the characteristics i)-iv) in a nonlinear manner between the first positions and the second position.

15. An integrated optic waveguide as claimed in claims 13 or 14 wherein waveguide width is varied nonlinearly between the first position and second position.

16. An integrated optic waveguide as claimed in any of claims 13-15 wherein the propagation loss, α (x), of the waveguide varies along the length, x, of the waveguide from the first position to the second position according the following equation:

$$\alpha(x) = \frac{1}{x}\ln\left(\frac{1}{1-\alpha_c x}\right).$$

wherein the starting propagation loss at the first position is α_c.

17. A photonic light wave circuit waveguide design comprising:

a first integrated optic waveguide comprising an integrated optic waveguide as claimed in any of claims 13-16;

a second integrated optic waveguide comprising an integrated optic waveguide as claimed in any of claims 13-16;

a waveguide component connected and optically linked to the first integrated optic waveguide and the second integrated optic waveguide.

18. A photonic light wave circuit waveguide design of claim 17 wherein the waveguide component comprises a first end connected to the first integrated optic waveguide; and a second end connected to the second integrated optic waveguide; such that light travels along the length of the first integrated optic waveguide, through the waveguide component and subsequently along the length of the second integrated optic waveguide.

19. A device comprising a plurality of photonic light wave circuit designs as claimed in claims 17 or 18; wherein the first and second integrated optic waveguides of each photonic light wave circuit waveguide design terminate at a separate optical input/output interface of the device.

20. A device as claimed in claim 19 wherein the device comprises:

a first array of optical fibres for optically coupling to the first integrated optic waveguides of the photonic light wave circuit designs;

a second array of optical fibres for optically coupling to the second integrated optic waveguides of the photonic light wave circuit designs.

21. A photonics integrated circuit, PIC, device comprising a plurality of integrated optic waveguide-based components distributed as an array over a region of the device wherein each of the said integrated-optic waveguide-based components is respectively connected to:

an input integrated optic waveguide running from the component to a device facet;

an output integrated optic waveguide running from the component to a device facet; wherein the input integrated optic waveguide is different to the output integrated optic waveguide.

22. A photonics integrated circuit, PIC, device as claimed in claim 21 wherein the array is a periodic distribution of components.

23. A photonics integrated circuit, PIC, device as claimed in claim 22 wherein the distribution is about a plane parallel to the planer extent of the device

24. A photonics integrated circuit, PIC, device as claimed in claim 22 wherein the distribution is substantially grid-like.

25. A photonics teaching module comprising:

the housing of any of claims 1-11;

and any of:

a) the device of claims 19 or 20; or
b) the photonics integrated circuit, PIC, device of claims 21-24.

Intellectual Property Office

Application No:	GB2219747.9	**Examiner:**	Mr Simon Keohane
Claims searched:	1-12 (first invention only)	**Date of search:**	22 June 2023

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1-12	GB 2601172 A (TOSHIBA) figures 1-2b & 9 and page 8 lines 17-25, page 9 line 26 - page 10 line 33, page 11 line 29 - page 12 line 2 & page 15 line 28 - page 16 line 2
X	1-12	WO 2016/124762 A1 (MEDLUMICS) figure 1 and page 6 lines 27-32, page 7 line 1 - page 8 line 11 & page 8 line 31 - page 9 line 12
A	-	US 2019/0391348 A1 (INFINERA) figures 4-5B and paragraph [0041], [0042] [0053] & [0054]
A	-	EP 4099070 A1 (INTEL) figures 1 & 9 and paragraphs [0027], [0028] & paragraph [0045]

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC[X] :

Worldwide search of patent documents classified in the following areas of the IPC

G02B; H01L

The following online and other databases have been used in the preparation of this search report

WPI, EPODOC, Patent Fulltext

International Classification:

Subclass	Subgroup	Valid From
G02B	0006/42	01/01/2006
G02B	0006/12	01/01/2006

Intellectual Property Office

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Claims searched:	13-20 (second invention), 21-24 (third invention) & 25 (all inventions)	**Date of search:**	12 February 2024

Patents Act 1977
Further Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	13-20 & 25	US 2017/0090103 A1 (QUALCOMM) figure 1B and paragraphs [0029] & [0038]-[0040]
X	13-20 & 25	WO 2010/010878 A1 (NEC CORP) figure 6 and paragraphs [0038] & [0039]
X	13-20 & 25	US 2020/0116939 A1 (HUAWEI TECH) figures 1 & 2 and paragraphs [0025] & [0026]
X	21-25	US 2004/0067006 A1 (INFINERA CORP) figures 7A, 9 & 11 and paragraphs [0085], [0086], [0166], [0174] & [0180]
X	21-25	US 2020/0064404 A1 (FUJITSU) figure 5 and paragraphs [0011], [0028]-[0035], [0044] & [0045]
A	-	KR20160093345 A (JEONG CHANG HEON) figures 5 & 6 and paragraphs [0061]-[0064]

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&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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G02B; G09B

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Intellectual Property Office

International Classification:

Subclass	Subgroup	Valid From
G02B	0006/42	01/01/2006
G02B	0006/12	01/01/2006