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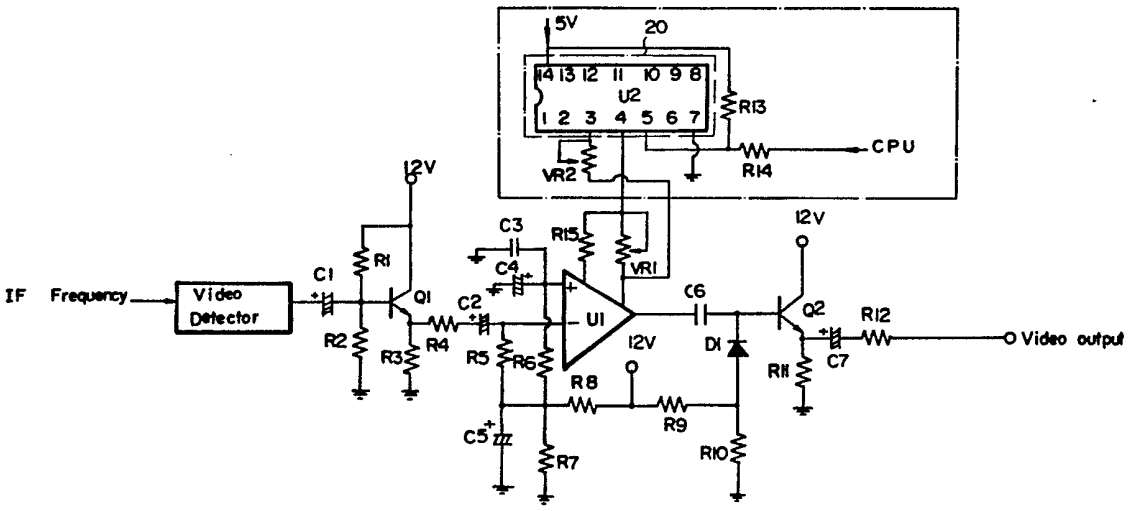
(54) **A video deviation control circuit for a satellite broadcasting receiver**

(57) A video signal level is controlled by switching resistor VR2 in or out of parallel connexion with resistor VR1 in dependence on received frequency.

Fig. 1



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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

Fig. 1

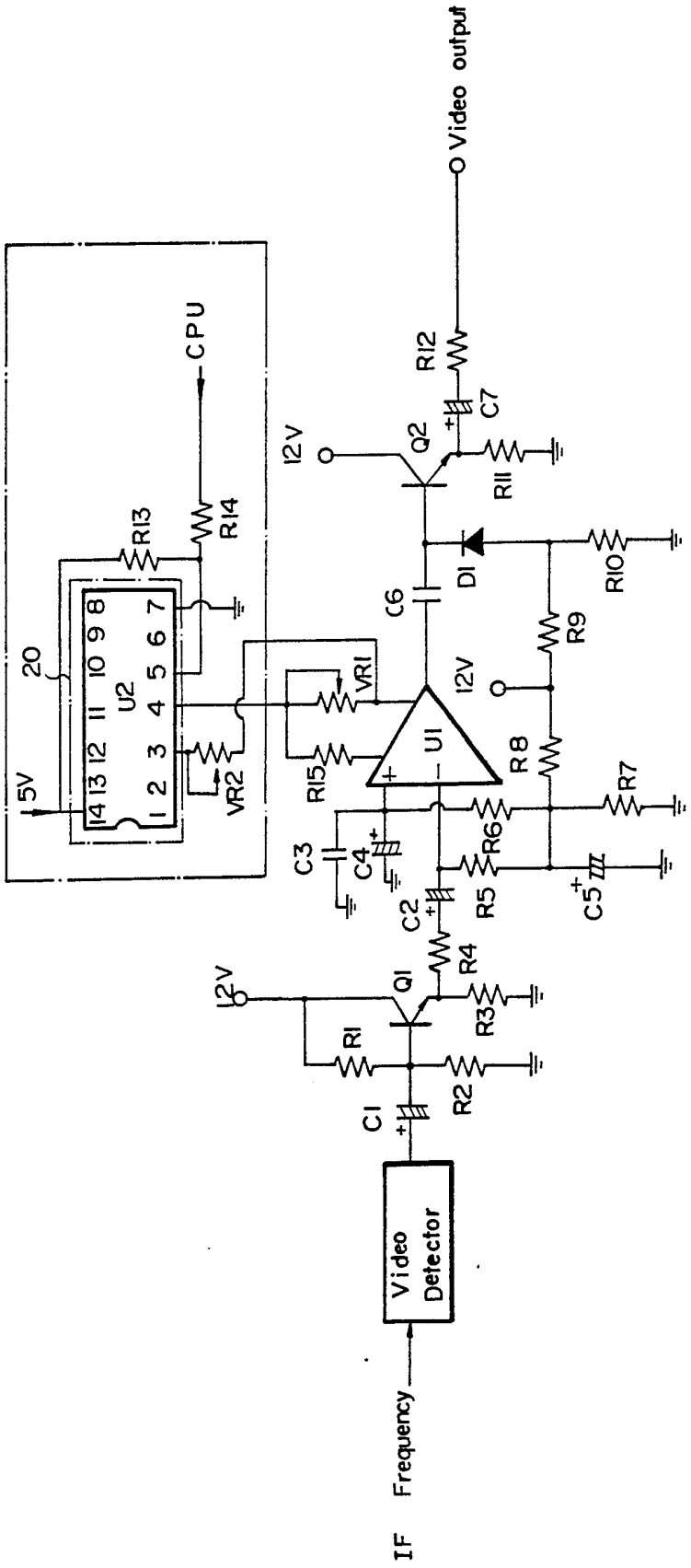
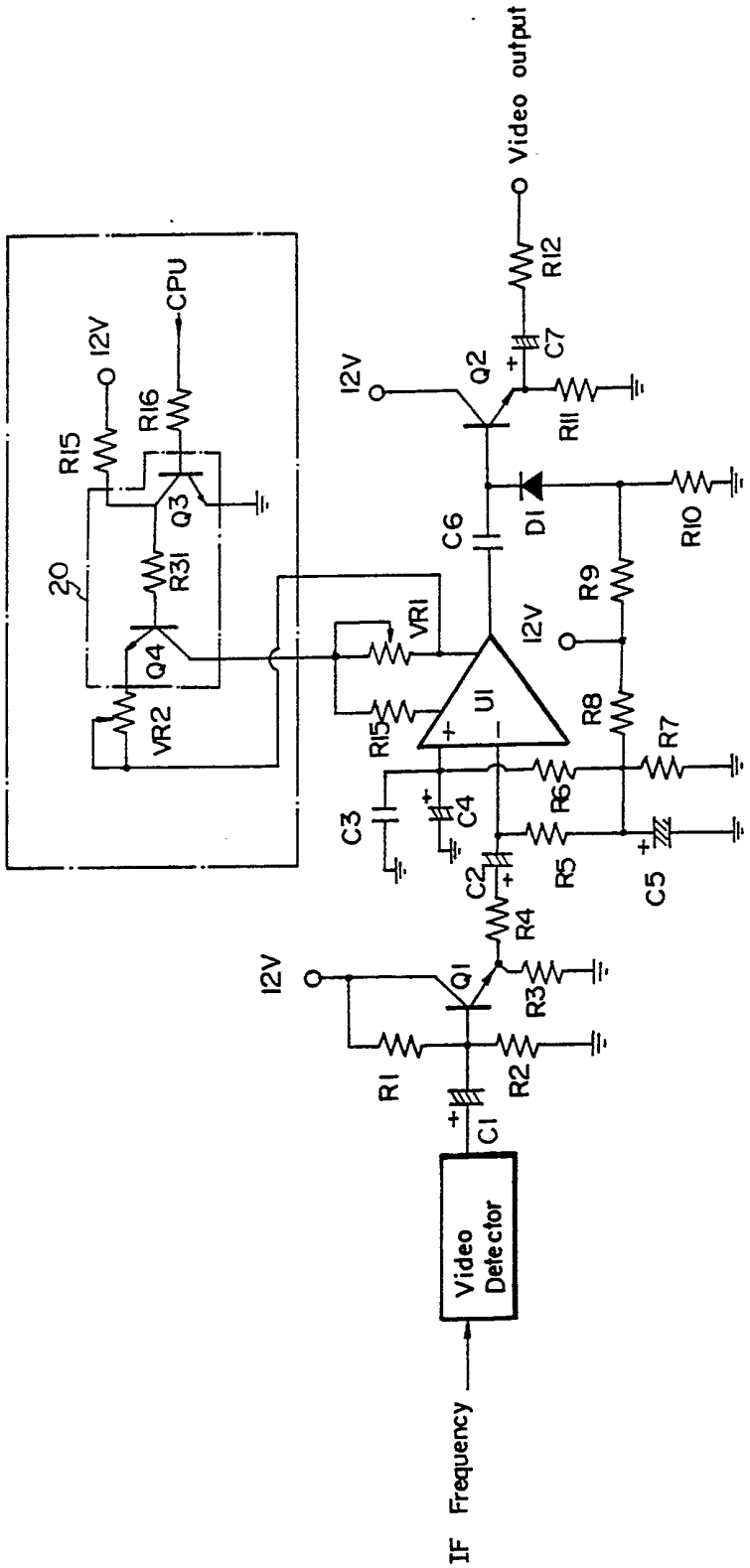

IF Frequency
Video Detector
C1
R1
R2
Q1
12V
R3
R4
C2
R5
R6
C3
C4
C5
R7
R8
U1
VR1
R15
VR2
R9
12V
C6
D1
R10
R11
Q2
12V
R12
C7
Video output
CPU
R13
R14
U2
20
5V
1 2 3 4 5 6 7 8 9 10 11 12 13 14

Fig. 2


IF Frequency
Video Detector
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R5
R6
C5
R7
R8
U1
R9
VR1
R15
VR2
Q4
R31
Q3
R16
CPU
R15
20
C6
D1
R10
Q2
R11
C7
R12
Video output

A VIDEO DEVIATION CONTROL CIRCUIT FOR A SATELLITE BROADCASTING RECEIVER

This invention relates to a video deviation control circuit for eliminating picture brightness variaton caused by various video deviations in receiving various satellite broadcasting programs.

A conventional satellite broadcasting receiver has been set to a normal video outputting level (load resistor 75 ohms) of about 25MHz without respect to the video deviations. Since the picture brightness however is varied according to the video deviations, such a conventional receiver had the problems that the picture brightness required adjustment at all times in receiving each broadcasting program and a picture flicker phenomenon or a picture contrast resisting phenomenon can be caused through such construction.

It is an object of the invention to provide a video deviation control circuit in which a fixed picture brightness can be obtained at all times without respect to various video deviations.

A video deviation control circuit of the present invention comprises a transmission line for transmitting high or low level signal; switching means for selecting video deviation mode according to the level transmitted from the transmission line; a first variable resistor connected to an output terminal of the switching means; and a second variable resistor connected to an output terminal of the switching means.

The features of the present invention will be more readily understood from the following detailed description of specific embodiments thereof when in conjunction with the accompanying drawings as follows:

Fig. 1 is a construction diagram of an embodiment of the invention; and

Fig. 2 is a construction diagram of another embodiment of the invention.

Fig. 1 is a diagram of one embodiment of the invention, and Fig. 2 is a diagram of another embodiment of the invention.

In Fig. 1 and Fig. 2, the reference Q1 to Q4 show transistors, U1 a video amplifier, U2 an analog switching IC (Integrated Circuit), R1 to R16 and R31 resistors, C1 to C7 condensers, VR1 and VR2 variable resistors, D1 a diode, and 20 switching means, respectively.

In Fig. 1, a video deviation control circuit of this invention is composed of the analog switching IC(U2), the variable resistor (VR2), and the resistors (R13,R14).

In case that an output level from CPU (Central Processing Unit) (not shown) is high (+5V), the analog switching IC(U2) turns "ON" state and establish a video outputting level corresponding to the video deviation of 16MHz by the variable resistor (VR2) connected parallel with the variable resistor (VR1) for gain adjustment.

In case that an output level from CPU is low (OV), the analog switching IC turns to "OFF" state and establishes a video outputting level adjusted by the variable resistor (VR1) corresponding to the video deviation of 25MHz.

That is, when the input video deviations are 16MHz or 25MHz, each video outputting level corresponding to the video deviation of 16MHz or 25MHz can be obtained by ON/OFF operations of the analog switching IC(U2), and then the video outputting levels are constant without respect to whether the

outputting levels are constant without respect to whether the video deviation is 16MHz or 25MHz.

A video deviation control circuit of Fig. 2 comprises the circuit using the transistors(Q3,Q4) instead of the analog switching IC(U2) of Fig. 1.

In case that an output level from CPU (not shown) is low(OV), the transistor(Q3) for switching turns "OFF" state and the transistor(Q4) for switching turns "ON", and then a video outputting level corresponding to the video deviation of 16MHz is established by the variable resistor(VR2) connected parallel with the variable resistor(VR1).

In case that an output level from CPU is high(+5V), the transistor(Q3) turns "ON" and the transistor(Q4) turns "OFF", and then a video outputting level corresponding to the video deviation of 25MHz is established by the variable resistor(VR1).

The video outputting levels established by the variable resistors(VR1,VR2) are constant at all times and are inputted to the video amplifier(U1).

As described above, this invention keeps preferred picture conditions in the satellite broadcasting receiver at any time without respect to various video deviations.

CLAIMS:

1. A video deviation control circuit for outputting a fixed video outputting level without respect to various video deviations inputted in a satellite broadcasting receiver, comprising:

a transmission line for transmitting high or low level signal;

switching means for selecting video deviation mode according to the level transmitted from the transmission line;

a first variable resistor connected to an output terminal of the switching means; and

a second variable resistor connected to an output terminal of the switching means.

2. A video deviation control circuit according to claim 1, wherein the switching means comprise a first transistor and a second transistor connected to the first transistor.

3. A video deviation control circuit according to claim 1, wherein the switching means comprise an analog switching IC chip.

4. A video deviation control circuit substantially as hereinbefore described with reference to Figure 1 or Figure 2 of the accompanying drawings.

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