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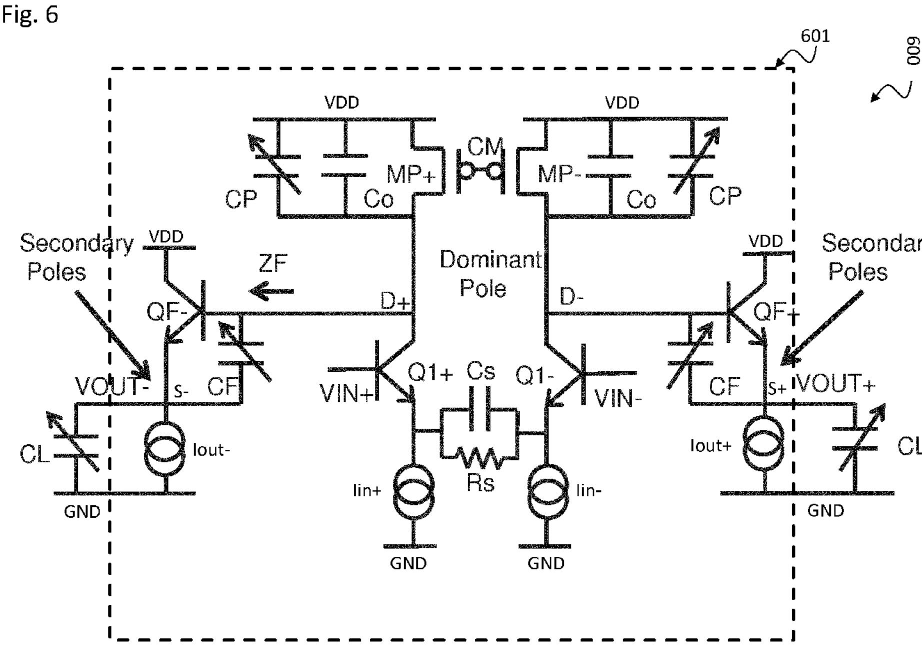
(54) Title: TUNABLE FILTER

Fig. 6



(57) Abstract: The disclosure relates to a tunable filter, comprising: a filter input; a filter output; at least one feedback loop coupled between the filter output and the filter input, wherein the at least one feedback loop comprises at least one tunable feedback capacitance (C1, C2) which is configured to tune a cut-off frequency (fo) of the tunable filter; and an active element (601), in particular an operational amplifier (OPAMP), coupled between the filter input and the filter output and configured to drive the at least one tunable feedback capacitance (C1, C2), said active element having a transfer function with a primary pole (ω_{p1}) and at least one secondary pole (ω_{p2}), wherein the active element comprises a first stabilization element, in particular a first pole capacitance (CP, CF) coupled to a first internal node of the active element, wherein the first stabilization

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element (CP, CF) is configured to establish a linear relationship between a location of the primary pole (ω_{p1}) and a location of the at least one secondary pole (ω_{p2}) of the active element.

TUNABLE FILTER

TECHNICAL FIELD

The present disclosure relates to a tunable filter, in particular designed as a closed loop analogue circuit where the output load can change over a wide range. The disclosure further relates to adaptive stability compensation for wide tuning range filters.

BACKGROUND

Filter with programmable cut-off frequency fo (between fo_min and fo_max) are implemented with variable capacitances C1, C2 or resistances R1, R2, R3 as shown in Fig. 1 illustrating a multi-feedback (MFB) low pass filter 100 with a closed loop DC coupled operational amplifier (OPAMP) 101.

The MFB filter 100 includes an operational amplifier 101 having a first (non-inverse, +) input 111, a second (inverse, -) input 112, a first (non-inverse, +) output 121, a second (inverse, -) output 122. A first feedback path including capacitance C1 is coupled between output 122 and input 111. A second feedback path including capacitance C1 is coupled between output 121 and input 112. A third feedback path including resistors R2 and R3 is coupled in parallel to the first feedback path between output 122 and input 111. A fourth feedback path including resistors R2 and R3 is coupled in parallel to the second feedback path between output 121 and input 112. The first (non-inverse, +) input voltage VIN+ is coupled via resistor R1 and the resistor R3 of the third feedback path to the first input 111. The second (inverse, -) input voltage VIN- is coupled via resistor R1 and the resistor R3 of the fourth feedback path to the second input 112. An input loop including the resistors R3 of the third and fourth feedback paths and a further capacitance C2/2 is coupled between the inputs 111, 112.

Generally, it is preferred to program capacitances since in this way Q-factor and noise performances are kept constant versus operating frequency. The operational amplifier (OPAMP) 101 used in the filter 100 has to drive those capacitances C1, C2. In case the fo tuning range is very large, the ratio between maximum and minimum capacitances (Cmax/Cmin) is high, therefore the OPAMP 101 has to cope with very different loading conditions.

Fig. 2 illustrates a possible realization of the RC Filter 100 depicted in Fig.1 together with its OPAMP 101. The OPAMP 101 may include a non-inverse input path between a drive voltage VDD and ground GND including a first (non-inverse) current source MP+, a first (non-inverse) transistor Q1+ and a second current source (non-inverse) Iin+. A control terminal of Q1+ is coupled to the first input 111 of the OPAMP 101. The OPAMP 101 includes an inverse output path between a drive voltage VDD and ground GND including a second (inverse) transistor QF- and a third current source (inverse) Iout-. A control terminal of QF- is coupled to a first (non-inverse) node D+ of the OPAMP which is located between MP+ and Q1+. A first terminal of QF- is coupled to the second output 122 (VOUT-) of the OPAMP 101. A second terminal of QF- is coupled to the drive voltage VDD. The above described components are additionally used in inverse form as described in the following.

The OPAMP 101 further includes an inverse input path between a drive voltage VDD and ground GND including a first (inverse) current source MP-, a first (inverse) transistor Q1- and a second (inverse) current source Iin-. A control terminal of Q1- is coupled to the second input 112 of the OPAMP 101. The OPAMP 101 includes a non-inverse output path between a drive voltage VDD and ground GND including a second (non-inverse) transistor QF+ and a third (non-inverse) current source Iout+. A control terminal of QF+ is coupled to a first (inverse) node D- of the OPAMP 101 which is located between MP- and Q1-. A first terminal of QF+ is coupled to the first output 121 (VOUT+) of the OPAMP 101. A second terminal of QF+ is coupled to the drive voltage VDD.

A capacitance Cs and a resistor Rs are coupled in parallel between the first terminal of Q1+ and the first terminal of Q1-.

Note that the OPAMP 101 can alternatively be realized as a differential OPAMP as depicted in Fig. 2 or alternatively as a non-differential OPAMP. The non-differential OPAMP 101 has only one first current source MP, one first transistor Q1, one second current source Iin, one third current source Iout, one input and one output without the differentiation of non-inverse and inverse components.

For the specific case of a Multiple Feedback Amplifier (MFB), equations that set the operating frequency, gain H(s) and quality factor of the Filter Q (i.e. its shape) are reported in the following.

$$H(s) = \frac{-R_2 / R_1}{1 + s/(Q\omega_o) + (s/\omega_o)^2} \qquad \omega_o = \frac{1}{\sqrt{C_1 C_2 R_2 R_3}}$$

$$Q = \sqrt{\frac{C_2}{C_1}} \frac{\sqrt{R_2 R_3}}{R_2 + R_3\left(1 + \frac{R_2}{R_1}\right)}$$

In the case that the filter 100 needs to operate at different frequencies, C2 and C1 capacitance are varied in such a way that 1) for a maximum cutoff frequency fo_max, C2 and C1 are set at minimum value; and that 2) for a Minimum cutoff frequency fo_min, C2 and C1 are set at maximum value.

Fig. 3 illustrates the OPAMP 101 of Fig.2 with its equivalent RC load. In the OPAMP 101 capacitances between first internal nodes D+, D- and drive voltage VDD are referred to as Co. C2 and C1 are seen by OPAMP 101 as an equivalent capacitance CL at the node VOUT (i.e. VOUT-, VOUT+) as illustrated in Fig. 3 and for sake of simplicity CL_max and CL_min are defined as the equivalent maximum and minimum equivalent capacitances at node VOUT (i.e. VOUT-, VOUT+) in the two extreme cases fo_min (ωmin) and fo_max (ωmax).

The filter 100 is a system in closed loop around its OPAMP 101: in order to have the filter insensitive to OPAMP 101 parameters, open loop gain has to be high at cutoff frequency fo. This requires a minimum gain-bandwidth-product (GBW). So minimum required GBW_MIN is set by maximum frequency fo_max.

As far as OPAMP 101 open loop gain is considered, assuming that the primary pole (dominant pole, or 1st pole) is located at the nodes D+, D- (output of 1st stage), the equivalent capacitance CL set the position of secondary poles S+, S- of the OPAMP 101, hence its stability. The fact that C1 and C2 (hence CL) can have very different values during filter operation makes the problem of OPAMP stability a big challenge and imposes a trade-off on the maximum Gain*Bandwidth (GBW) product of the OPAMP 101 and the Filter tuning range.

To summarise, in a closed Loop Filter there is an intrinsic trade-off between fo_max and tuning range as illustrated in Figures 4a and 4b. This is due to the fact that: 1) the minimum required GBW = Goamp* ωp1 product is imposed by fo_max (operating frequency) as shown in Figure 4a. In fact the OPAMP used into the filter needs to have large open loop gain (Gopamp) at fo_max. 2) The maximum allowed GBW = Goamp* ωp1 product is limited by fo_min as shown in Figure 4b. In fact, the 2nd pole (wp2) is set by Cmax (when Filter works at fo_min) and the stability condition dictates that ωp2/ ωc=3 to have 70 degree phase margin, where ωc is the frequency where Goamp=0. This means that the location of the primary pole is set by the case when the Filter operates at fo_min, thus GBW product will be limited also when Filter is operated at fo_max.

This characteristics is illustrated in Figures 4a and 4b.

SUMMARY

It is the object of the invention to provide an improved tuneable filter design providing large gain at cutoff frequency and wide and stable tuning range.

This object is achieved by the features of the independent claims. Further implementation forms are apparent from the dependent claims, the description and the figures.

A basic idea of the invention is to break the limitation on MAX GBW product set by Cmax by moving the primary pole together with the secondary poles during frequency tuning. In this way the following holds at CMIN (fo_max): Since ωp2 is at its highest frequency, location of pole ωp1 can be moved at higher frequencies (see Figure 5c). In this condition the maximum possible GBW is achieved (is what is needed to operate at fo_max). At CMAX (fo_min) the following holds: Since ωp2 is at its lowest frequency, location of pole ωp1 can be moved at lower frequencies to improve stability (see Figure b). In this condition GBW is reduced (for operation at fo_min, GBW can be reduced with respect to operation at fo_max).

In order to describe the invention in detail, the following terms, abbreviations and notations will be used:

OPAMP:	Operational Amplifier;
fo_min:	minimum cutoff frequency;
fo_max:	maximum cutoff frequency;
MFB:	Multiple Feedback;
Q:	quality factor;

GBW: gain bandwidth product;

ωp1: primary pole or dominant pole;

ωp2: secondary pole(s).

According to a first aspect, the invention relates to a tunable filter, comprising: a filter input; a filter output; at least one feedback loop coupled between the filter output and the filter input, wherein the at least one feedback loop comprises at least one tunable feedback capacitance which is configured to tune a cut-off frequency of the tunable filter; and an active element, in particular an operational amplifier, coupled between the filter input and the filter output and configured to drive the at least one tunable feedback capacitance, said active element having a transfer function with a primary pole ω_{p1} and at least one secondary pole ω_{p2}, wherein the active element comprises a first stabilization element, in particular a first pole capacitance coupled to a first internal node of the active element, wherein the first stabilization element is configured to establish a linear relationship between a location of the primary pole ω_{p1} and a location of the at least one secondary pole ω_{p2} of the active element.

By establishing a linear relationship between a location of the primary pole ω_{p1} and a location of the at least one secondary pole ω_{p2}, the tunable filter provides the advantage of large gain at cutoff frequency and wide and stable tuning range, since the primary pole is not limited by the maximum load capacitance. A large GBW can be achieved when load capacitance is low which allows implementing filter with closed loop approach at high cutoff frequency, e.g. 700 MHz and higher.

In a first possible implementation form of the tunable filter according to the first aspect, the location of the at least one secondary pole ω_{p2} changes with a tuning of the cut-off frequency (fo) of the tunable filter; and the first stabilization element is configured to change the location of the primary pole ω_{p1} in accordance to the change of the at least one secondary pole ω_{p2}.

This provides the advantage that due to the linear relationship of the location of the primary pole and the secondary poles ω_{p2}, the tunable filter provides the advantage of large gain at cutoff frequency and wide and stable tuning range, since the primary (i.e. primary) pole is not limited by the maximum load capacitance.

In a second possible implementation form of the tunable filter according to the first aspect as such or according to the first implementation form of the first aspect, the first stabilization element is configured to move the location of the primary pole ω_{p1} to higher frequencies when the location of the at least one secondary pole ω_{p2} is tuned to higher frequencies.

This provides the advantage that due to the linear relationship of the location of the primary pole and the secondary poles ω_{p2}, the filter gain is stable across the whole filter tuning range.

In a third possible implementation form of the tunable filter according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, the first stabilization element is configured to move the location of the primary pole ω_{p1} to lower frequencies when the location of the at least one secondary pole ω_{p2} is tuned to lower frequencies.

This provides the advantage of large GBW when load capacitance is low.

In a fourth possible implementation form of the tunable filter according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, the first stabilization element is a function of the at least one feedback capacitance.

When the first stabilization element is a function of the at least one feedback capacitance, the filter shows improved stability.

In a fifth possible implementation form of the tunable filter according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, the primary pole is associated to an internal node total capacitance of the first internal node, the internal node total capacitance being proportional to the at least one feedback capacitance.

Such a proportionality results in improved stability at high tuning ranges.

In a sixth possible implementation form of the tunable filter according to the third implementation form of the first aspect, an internal node total capacitance of the first internal node is proportional to the first stabilization element, the first stabilization element being tunable and configured to be tuned of an amount proportional to the change of the at least one feedback capacitance.

When the first stabilization element is tunable and tuned of an amount proportional to the change of the feedback capacitance, optimal performance tuning ranges of the filter can be easily adjusted.

In a seventh possible implementation form of the tunable filter according to the sixth implementation form of the first aspect, a proportionality constant of the tuning is a function of the first stabilization element.

This provides the advantage of better stability, as the stability condition depends on a quotient of the location of the second poles and the location of the first pole. A proportionality relaxes the stability condition.

In an eighth possible implementation form of the tunable filter according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, the active element comprises: a first transistor coupled between a first input terminal and the first internal node of the active element; and a second transistor coupled between a first output terminal and the first internal node of the active element.

In a ninth possible implementation form of the tunable filter according to the eighth implementation form of the first aspect, the first transistor comprises a first terminal, a second terminal and a control terminal, wherein the control terminal of the first transistor is coupled to the first input terminal of the active element, wherein the second transistor comprises a first terminal, a second terminal and a control terminal, wherein the first terminal of the second transistor is coupled to the first output terminal of the active element; and wherein the first internal node is configured to couple the second terminal of the first transistor to the control terminal of the second transistor.

This provides the advantage that the filter design can be flexibly implemented, e.g. by two bipolar transistors or by two FET transistors.

In a tenth possible implementation form of the tunable filter according to the ninth implementation form of the first aspect, the first stabilization element is coupled between the first internal node and a reference voltage.

This provides the advantage that the first stabilization element can be easily implemented by introducing a capacitive coupling between the first internal node and the reference voltage.

In an eleventh possible implementation form of the tunable filter according to the ninth implementation form of the first aspect, the first stabilization element is variable proportional to a change of a load capacitance of a load applied to the tunable filter.

This provides the advantage that due to the proportionality the stability condition holds for large gains and broad tuning ranges.

In a twelfth possible implementation form of the tunable filter according to any of the eighth to the eleventh implementation forms of the first aspect, the active element comprises: a first current source coupled between the first internal node and a reference voltage; a second current source coupled between the first terminal of the first transistor and a ground terminal; and a third current source coupled between the first terminal of the second transistor and a ground terminal.

This provides the advantage that these current sources can be flexibly designed, for example by transistors.

In a thirteenth possible implementation form of the tunable filter according to any of the eighth to the twelfth implementation forms of the first aspect, the active element is a differential voltage active element, further comprising: a differential first transistor coupled between a differential first input terminal and a differential first internal node of the active element; a differential second transistor coupled between a differential first output terminal and the differential first internal node of the active element; and a differential first stabilization element corresponding to the first stabilization element, wherein the differential first stabilization element is coupled to the differential first internal node of the active element.

This provides the advantage that a differential design is of higher quality and shows improved linearity.

In a fourteenth possible implementation form of the tunable filter according to the thirteenth implementation form of the first aspect, the active element further comprises: a cascode circuit coupled between the second terminal of the first transistor and the second terminal of the differential first transistor.

A cascode circuit provides the advantage of decoupling of the inverse and non-inverse parts resulting in improved linearity and stability.

BRIEF DESCRIPTION OF THE DRAWINGS

Further embodiments of the invention will be described with respect to the following figures, in which:

Fig. 1 shows a circuit diagram illustrating a MFB low pass filter 100;

Fig. 2 shows a circuit diagram illustrating the MFB low pass filter 100 together with electrical components of the OPAMP;

Fig. 3 shows a circuit diagram illustrating the MFB low pass filter 100 including internal capacitances Co;

Figs. 4a, 4b show frequency diagrams of the MFB low pass filter 100 illustrating trade-off between gain bandwidth products versus Cmax/Cmin tuning ranges;

Figs. 5a, 5b correspond to Figs. 4a, 4b and Figs. 5c, 5d show frequency diagrams of a tunable filter according to the disclosure which removes the trade-off between gain bandwidth products versus Cmax/Cmin tuning ranges;

Fig. 6 shows a circuit diagram illustrating a tunable filter 600 according to a first implementation form;

Fig. 7 shows a circuit diagram illustrating a tunable filter 700 according to a second implementation form;

Fig. 8 shows a circuit diagram illustrating a tunable filter 800 according to a third implementation form;

Fig. 9 shows a performance diagram 900 illustrating a tuning range for a tunable filter according to the disclosure; and

Fig. 10 shows performance diagrams 1000a, 1000b illustrating OPAMP cross-over frequency and phase margin for a tunable filter according to the disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings, which form a part thereof, and in which is shown by way of illustration specific aspects in which the disclosure may be practiced. It is understood that other aspects may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present disclosure is defined by the appended claims.

It is understood that comments made in connection with a described device, circuit or system may also hold true for a corresponding method and vice versa. For example, if a specific method step is described, a corresponding device may include a unit to perform the described method step, even if such unit is not explicitly described or illustrated in the figures. Further, it is understood that the features of the various exemplary aspects described herein may be combined with each other, unless specifically noted otherwise.

Fig. 6 shows a circuit diagram illustrating a tunable filter 600 according to a first implementation form. The tunable filter 600 includes an active element 601 that may correspond to the OPAMP 101 described above with respect to Figures 1 to 3. In contrast to the OPAMP 101, the active element 601 additionally includes one or more stabilization elements CP, CF coupled to the internal node D+, D- for providing large gain at cutoff frequency and wide and stable tuning range as described in the following. The one or more stabilization elements may be a first pole capacitance, or a combination of capacitances and resistors.

The active element 601 includes a non-inverse input VIN+, an inverse input VIN-, a non-inverse output VOUT+ and an inverse output VOUT-. The tunable filter 600 further includes load capacitances CL coupled to the active element 601 which may correspond to the capacitances C1 and C2 as described above with respect to Fig. 1.

The active element 601 includes a non-inverse input path between a reference voltage VDD and ground GND including a first (non-inverse) current source MP+, a first (non-inverse) transistor Q1+ and a second current source (non-inverse) Iin+. A control terminal of Q1+ is coupled to the non-inverse input Vin+ of the active element 601. The active element 601 includes an inverse output path between a reference voltage VDD and ground GND including a second (inverse) transistor QF- and a third (inverse) current source Iout-. A control terminal of QF- is coupled to a first (non-inverse) node D+ of the active element 601 which is located between MP+ and Q1+. A first terminal of QF- is coupled to the inverse output VOUT- of the active element. A second terminal of QF- is coupled to the reference voltage VDD. The inverse output VOUT- of the active element 601 is coupled to a load having a (variable) load capacitance CL which determines the location of the secondary poles. The load capacitance CL is an equivalent capacitance associated to capacitance C1 and C2 of Fig.2. The above described components are additionally used in inverse form as described in the following.

The active element 601 further includes an inverse input path between a reference voltage VDD and ground GND including a first (inverse) current source MP-, a first (inverse) transistor Q1- and a second (inverse) current source Iin-. A control terminal of Q1- is coupled to the inverse input Vin- of the active element. The active element 601 includes a non-inverse output path between a reference voltage VDD and ground GND including a second (non-inverse) transistor QF+ and a third (non-inverse) current source Iout+. A control terminal of QF+ is coupled to a first (inverse) node D- of the active element 601 which is located between MP- and Q1-. A first terminal of QF+ is coupled to the first output 121 (VOUT+) of the active element 601. A second terminal of QF+ is coupled to the reference voltage VDD. The non-inverse output VOUT+ of the active element is coupled to the load having the (variable) load capacitance CL which determines the location of the secondary poles.

A capacitance Cs and a resistor Rs are coupled in parallel between the first terminal of Q1+ and the first terminal of Q1-. A further cascode circuit may be coupled between the differential part and the non-differential part of the active element 601.

The first and/or second transistors Q1+, Q1-, QF+, QF- may be realized as bipolar transistors; in this case the control terminal is a base terminal, the first terminal is an emitter terminal and the second terminal is a collector terminal. Alternatively, the first and/or second transistors Q1+, Q1-, QF+, QF- may be realized as Field Effect transistors;

in this case, the control terminal is a gate terminal, the first terminal is a source terminal and the second terminal is a drain terminal.

Note that the active element 601 can be realized as a differential active element or alternatively as a non-differential active element. The differential active element is shown in Fig. 6 while a non-differential active element comprises of half the elements as depicted in Fig. 6, i.e. one first current source MP, one first transistor Q1, one second current source Iin, one third current source Iout, one input and one output without the differentiation of non-inverse and inverse components.

A basic design of the tunable filter 600 can be described using the following words: The tunable filter 600 includes: a filter input VIN+; a filter output VOUT+; at least one feedback loop coupled between the filter output VOUT+ and the filter input VIN+, wherein the at least one feedback loop comprises at least one tunable feedback capacitance C1, C2 which is configured to tune a cut-off frequency fo of the tunable filter; and an active element 601, in particular an operational amplifier (OPAMP), coupled between the filter input and the filter output and configured to drive the at least one tunable feedback capacitance C1, C2, said active element having a transfer function with a primary pole ω_{p1} and at least one secondary pole ω_{p2}, wherein the active element 601 comprises a first pole capacitance CP, CF coupled to a first internal node D+ of the active element 601, wherein the first pole capacitance CP, CF is configured to establish a linear relationship between a location of the primary pole ω_{p1} and a location of the at least one secondary pole ω_{p2} of the active element.

The location of the at least one secondary pole ω_{p2} may change with a tuning of the cut-off frequency fo of the tunable filter; and the first pole capacitance CP, CF may be configured to change the location of the primary pole ω_{p1} in accordance to the change of the at least one secondary pole ω_{p2}. The first pole capacitance CP, CF may be configured to move the location of the primary pole ω_{p1} to higher frequencies when the location of the at least one secondary pole ω_{p2} is tuned to higher frequencies. The first pole capacitance CP, CF may be configured to move the location of the primary pole ω_{p1} to lower frequencies when the location of the at least one secondary pole ω_{p2} is tuned to lower frequencies. The first pole capacitance CP, CF may be a function of the at least one feedback capacitance C1, C2.The primary pole may be associated to an internal node total capacitance of the first internal node, the internal node total capacitance being proportional to the at least one feedback capacitance C1, C2. An internal node total capacitance of the first internal node D+ may be proportional to the first pole capacitance, the first pole capacitance being tunable and configured to be tuned of an amount proportional to the change of the at least one feedback capacitance C1, C2. A proportionality constant of the tuning may be a function of the first pole capacitance CF. The active element 601 may include: a first transistor Q1+ coupled between a first input terminal Vin+ and the first internal node D+ of the active element 601; and a second transistor QF- coupled between a first output terminal VOUT- and the first internal node D+ of the active element 601.

The first transistor Q1+ may include a first terminal, a second terminal and a control terminal, wherein the control terminal of Q1+ is coupled to the first input terminal VIN+ of the active element 601. The second transistor QF- may include a first terminal, a second terminal and a control terminal, wherein the first terminal of QF- is coupled to the first output terminal VOUT- of the active element. The first internal node D+ may be configured to couple the second terminal of Q1+ to the control terminal of QF-. The first pole capacitance CP may be coupled between the first internal node D+ and a reference voltage VDD. The first pole capacitance CP may be variable proportional to a change of a load capacitance CL of a load applied to the tunable filter 600.

The active element 601 may include: a first current source MP+ coupled between the first internal node D+ and a reference voltage GND; a second current source Iin coupled between the first terminal of Q1+ and a ground terminal GND; and a third current source Iout coupled between the first terminal of QF- and a ground terminal GND.

The active element 601 may be a differential voltage active element, further including: a differential first transistor Q1- coupled between a differential first input terminal VIN- and a differential first internal node D- of the active element 601; a differential second transistor QF- coupled between a differential first output terminal VOUT+ and the differential first internal node D- of the active element 601; and a differential first pole capacitance CP, CF corresponding to the first pole capacitance CP, CF, wherein the differential first pole capacitance CP, CF may be coupled to the differential first internal node D- of the active element 601.

The active element 601 may further include a cascode circuit coupled between the second terminal of Q1+ and the second terminal of Q1-.

The above described active element 601 (e.g. OPAMP) may be used in a filter with *variable* operating frequency fo. The tuning of the frequency fo may be performed by changing its capacitances and this change can be modeled (in its simplest form) as a change in the capacitance CL at the output VOUT. The change of capacitance CL moves locations of secondary poles located at nodes VOUT. The tunable filter 600 according to the disclosure includes the following features: (i) the addition of capacitances CP and/or CF and (ii) a method to vary CP and/or CF of an amount proportional to the change of CL. Different embodiments can be derived from the tunable filter 600 by applying the following restrictions: (a) CP is variable and CF is fixed, (b) CP is variable and no CF is used, (c) no CP is used and fixed CF is used, (d) no CP is used and variable CF is used.

The basic principle of the disclosure is described in the following. The input impedance at the base of the voltage follower (the capacitance associated to this node contributes to the capacitance of the primary pole of the OPAMP) can be written as:

$$ZF(s) = \frac{1}{s \cdot (C_\pi + C_F)} + \frac{1}{s \cdot C_L} + \frac{1}{s^2 \cdot C_L \cdot (C_\pi + C_F) \cdot g_m(QF)},$$

where C_π is the base-emitter capacitance of the Bipolar (or alternatively FET) transistor QF and gm(QF) is its transconductance.

The above equation shows that 1) ZF has a negative real part. This is due to simplification of modeling all feedback loops with a single capacitance CL and is not relevant hereinafter. The input capacitance (that contributes to the capacitance of the primary pole) is a function of CL and CF.

If capacitance CP is also taken into account, the total capacitance at the node D (i.e. the primary pole capacitance) can be written as:

$$C_D = C_o + C_P + \frac{(C_\pi + C_F) \cdot C_L}{C_\pi + C_F + C_L}.$$

The above equation can be analyzed in following two cases resulting in the second and third implementation forms as described below with respect to Figures 7 and 8.

Fig. 7 shows a circuit diagram illustrating a tunable filter 700 according to a second implementation form.

The tunable filter 700 corresponds to the tunable filter 600 described above with respect to Fig. 6; however the active element 701 of the tunable filter 700 does not include the stabilization element CF, instead only the stabilization element CP is implemented.

This corresponds to the implementation of no CF and low input capacitance voltage follower, i.e.: $C_F = 0\ \ C_\pi << C_P$. In this case $C_D = C_P + C_o$ and the tracking of the primary pole can be done by varying CP of the same amount as CL.

Fig. 8 shows a circuit diagram illustrating a tunable filter 800 according to a third implementation form.

The tunable filter 800 corresponds to the tunable filter 600 described above with respect to Fig. 6; however the active element 801 of the tunable filter 800 does not include the stabilization element CP, instead only the stabilization element CF is implemented.

This corresponds to the implementation of a fixed value according to C_F and $C_P = 0$. In this case the following relation holds:

$$C_D = C_o + \frac{(C_\pi + C_F)\cdot C_L}{C_\pi + C_F + C_L}.$$

If $C_\pi + C_F = C_L$, then $C_D = C_o + \frac{C_L}{2}$.

The above equation shows that the capacitance at the primary pole is proportional to CL, i.e. when CL changes, same change is applied to CD.

The three implementation forms 600, 700, 800 show the following advantages of the disclosed tunable filter: Since the primary pole is not limited by maximum load capacitance, very large GBW can be achieved when load capacitance is low (i.e. filter is programmed to fo_max). This allows to implement a filter with closed loop approach at fo>700-MHz in an exemplary implementation. At very large fo, G_OPAMP cannot be very high to consider it infinite. The filter shape (i.e. its quality factor) will depend upon

G_OPAMP. Since the primary pole is programmable the following relation holds: G_OPAMP(fo_max) = G_OPAMP(fo_min). Since G_OPAMP is more stable across filter tuning range, filter response (i.e. Quality factor of filter) will be be more uniform across the tuning range.

The disclosed tunable filter designs can be used for all filter with very large tuning range or any closed loop systems with very large different loading capacitances.

Fig. 9 shows a performance diagram 900 illustrating a tuning range for a tunable filter according to the disclosure.

The tunable filter has been realized with a 4th order Low Pass Filter (LPF) with a 1GHz Bandwidth. Performances are shown in Fig. 9. The filter achieves 90-700MHz 1dB Bandwidth tuning range. With such large tuning range, the disclosed tunable filter using adaptive stability compensation allows to have 10GHz Gain*Bandwidth product with 60 degree phase margin and a filter that operates between 90-700MHz.

Fig. 10 shows performance diagrams 1000a, 1000b illustrating OPAMP cross-over frequency and phase margin for a tunable filter according to the disclosure.

BGW 1000a and Phase Margin 1000b of the OPAMP used in the tunable filter according to the disclosure are depicted for the following three cases: (A): Fixed CF, CP=0; (B): Fixed CF and variable CP; (C): fixed CF and CP set at maximum value. The A case yields good results, i.e. the phase margin is kept almost constant across the complete tuning range. The B-case yields the best result in terms of phase margin, i.e. phase margin is inproved when operating frequency is reduced. The C-case is reported as a reference and can be useful in case that a maximum phase margin is needed, regardless of the bandwidth achieved.

While a particular feature or aspect of the disclosure may have been disclosed with respect to only one of several implementations, such feature or aspect may be combined with one or more other features or aspects of the other implementations as may be desired and advantageous for any given or particular application. Furthermore, to the extent that the terms “include”, “have”, “with”, or other variants thereof are used in either the detailed description or the claims, such terms are intended to be inclusive in a manner similar to the term “comprise”. Also, the terms “exemplary”, “for example” and “e.g.” are merely meant as an example, rather than the best or optimal. The terms “coupled” and “connected”, along with derivatives may have been used. It should be understood that these terms may have been used to indicate that two elements cooperate or interact with each other regardless whether they are in direct physical or electrical contact, or they are not in direct contact with each other.

Although specific aspects have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific aspects shown and described without departing from the scope of the present disclosure. This application is intended to cover any adaptations or variations of the specific aspects discussed herein.

Although the elements in the following claims are recited in a particular sequence with corresponding labeling, unless the claim recitations otherwise imply a particular sequence for implementing some or all of those elements, those elements are not necessarily intended to be limited to being implemented in that particular sequence.

Many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the above teachings. Of course, those skilled in the art readily recognize that there are numerous applications of the invention beyond those described herein. While the present invention has been described with reference to one or more particular embodiments, those skilled in the art recognize that many changes may be made thereto without departing from the scope of the present invention. It is therefore to be understood that within the scope of the appended claims and their equivalents, the invention may be practiced otherwise than as specifically described herein.

CLAIMS

1. A tunable filter (600), comprising:

a filter input (VIN);

a filter output (VOUT);

at least one feedback loop coupled between the filter output (VOUT) and the filter input (VIN), wherein the at least one feedback loop comprises at least one tunable feedback capacitance (C1, C2) which is configured to tune a cut-off frequency (fo) of the tunable filter; and

an active element (601), in particular an operational amplifier (OPAMP), coupled between the filter input and the filter output and configured to drive the at least one tunable feedback capacitance (C1, C2), said active element having a transfer function with a primary pole (ω_{p1}) and at least one secondary pole (ω_{p2}),

wherein the active element comprises a first stabilization element, in particular a first pole capacitance (CP, CF), coupled to a first internal node (D) of the active element,

wherein the first stabilization element (CP, CF) is configured to establish a linear relationship between a location of the primary pole (ω_{p1}) and a location of the at least one secondary pole (ω_{p2}) of the active element.

2. The tunable filter (600) of claim 1,

wherein the location of the at least one secondary pole (ω_{p2}) changes with a tuning of the cut-off frequency (fo) of the tunable filter; and

wherein the first stabilization element (CP, CF) is configured to change the location of the primary pole (ω_{p1}) in accordance to the change of the at least one secondary pole (ω_{p2}).

3. The tunable filter (600) of claim 1 or 2,

wherein the first stabilization element (CP, CF) is configured to move the location of the primary pole (ω_{p1}) to higher frequencies when the location of the at least one secondary pole (ω_{p2}) is tuned to higher frequencies.

4. The tunable filter (600) of one of the preceding claims,

wherein the first stabilization element (CP, CF) is configured to move the location of the primary pole (ω_{p1}) to lower frequencies when the location of the at least one secondary pole (ω_{p2}) is tuned to lower frequencies.

5. The tunable filter (600) of one of the preceding claims,

wherein the first stabilization element (CP, CF) is a function of the at least one feedback capacitance (C1, C2).

6. The tunable filter (600) of one of the preceding claims, wherein the primary pole is associated to an internal node total capacitance of the first internal node, the internal node total capacitance being proportional to the at least one feedback capacitance (C1, C2).

7. The tunable filter (600) of claim 4, wherein an internal node total capacitance of the first internal node is proportional to a capacitance of the first stabilization element (CF), the capacitance of the first stabilization element (CF) being tunable and configured to be tuned of an amount proportional to the change of the at least one feedback capacitance (C1,C2).

8. The tunable filter (600) of claim 7, wherein a proportionality constant of the tuning is a function of the capacitance of the first stabilization element (CF).

9. The tunable filter (600) of one of the preceding claims, wherein the active element (OPAMP) comprises:

a first transistor (Q1+) coupled between a first input terminal (Vin+) and the first internal node of the active element; and

a second transistor (QF-) coupled between a first output terminal (Vout-) and the first internal node of the active element.

10. The tunable filter (600) of claim 9,

wherein the first transistor (Q1+) comprises a first terminal, a second terminal and a control terminal, wherein the control terminal of Q1+ is coupled to the first input terminal (Vin+) of the active element,

wherein the second transistor (QF-) comprises a first terminal, a second terminal and a control terminal, wherein the first terminal of QF- is coupled to the first output terminal (Vout-) of the active element; and

wherein the first internal node is configured to couple the second terminal of Q1+ to the control terminal of QF-.

11. The tunable filter (600) of claim 10,

wherein the first stabilization element (CP) is coupled between the first internal node and a reference voltage.

12. The tunable filter (600) of claim 10,

wherein the first stabilization element (CP) is variable proportional to a change of a load capacitance (CL) of a load applied to the tunable filter.

13. The tunable filter (600) of one of claims 9 to 12, wherein the active element (OPAMP) comprises:

a first current source (MP+) coupled between the first internal node and a reference voltage;

a second current source (Io) coupled between the first terminal of Q1+ and a ground terminal; and

a third current source (Iout) coupled between the first terminal of QF- and a ground terminal.

14. The tunable filter (600) of one of claims 9 to 13, wherein the active element (OPAMP) is a differential voltage active element, further comprising:

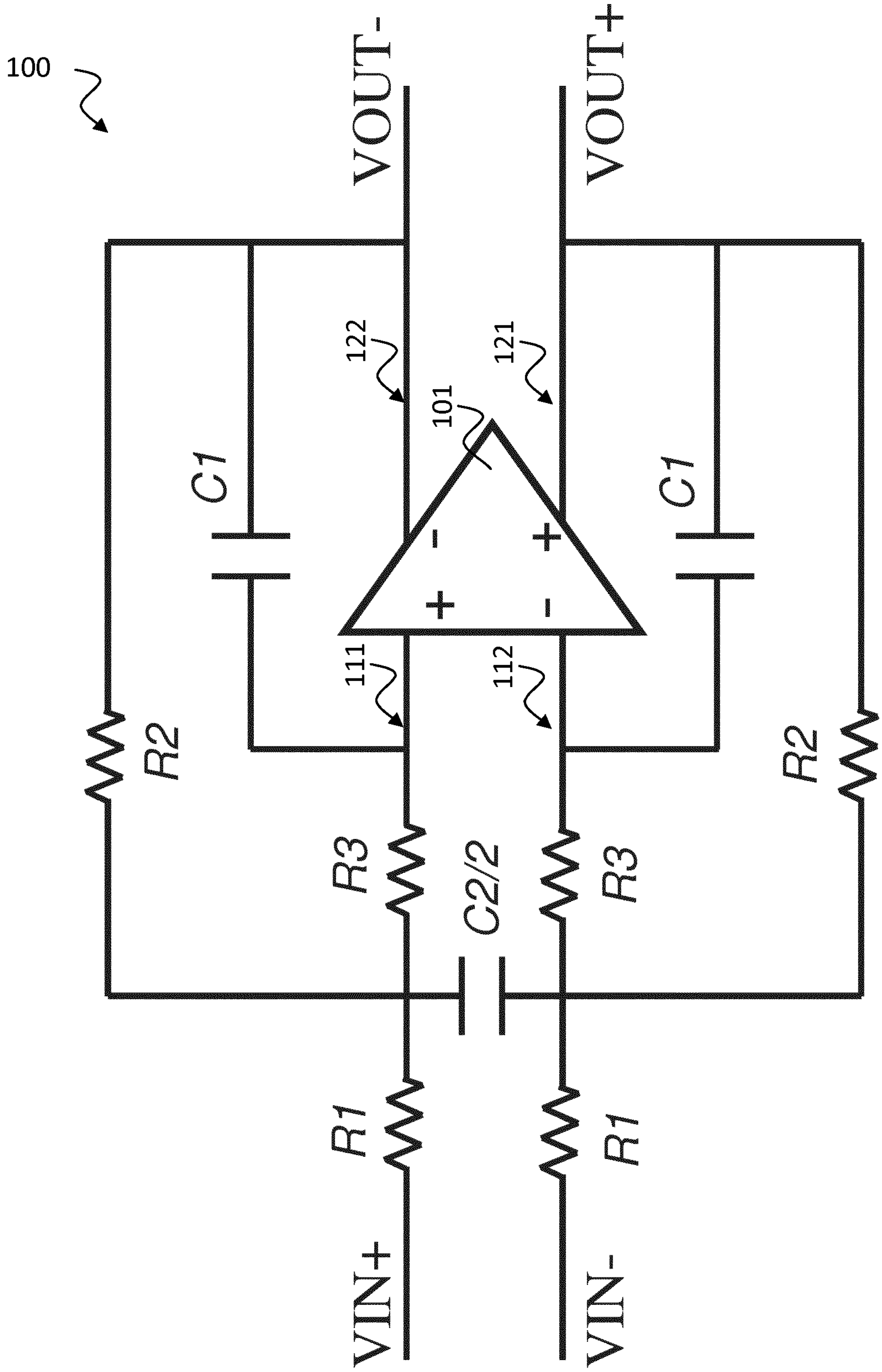
a differential first transistor (Q1-) coupled between a differential first input terminal (Vin-) and a differential first internal node of the active element;

a differential second transistor (QF-) coupled between a differential first output terminal (Vout+) and the differential first internal node of the active element; and a differential first stabilization element (CP, CF) corresponding to the first stabilization element (CP, CF),

wherein the differential first stabilization element (CP, CF) is coupled to the differential first internal node of the active element.

15. The tunable filter (600) of claim 14, wherein the active element (OPAMP) further comprises:

a cascode circuit coupled between the second terminal of Q1+ and the second terminal of Q1-.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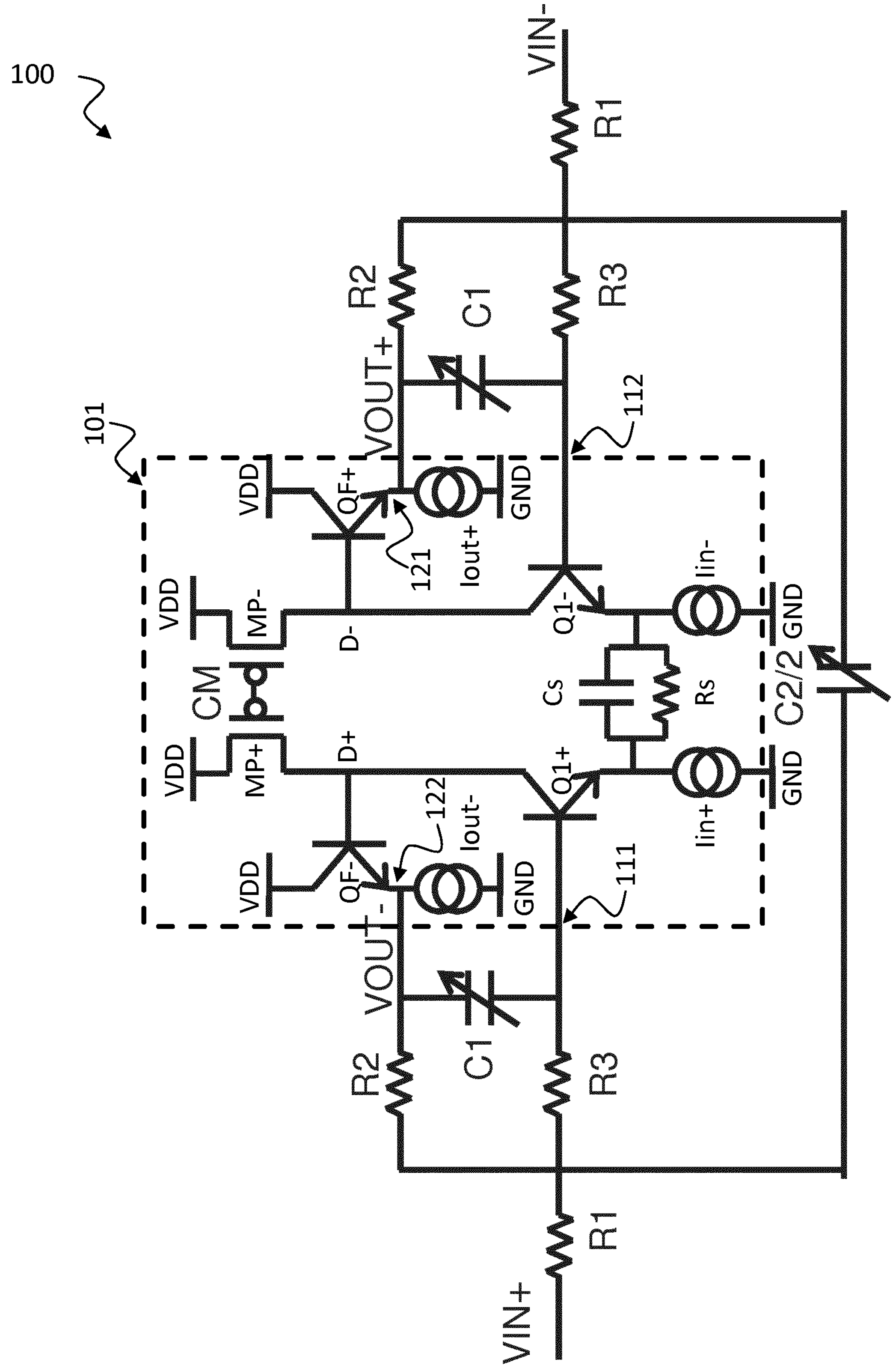
VOUT-
VOUT+
122
121
101
C1
C1
111
112
R2
R2
R3
R3
C2/2
R1
R1
VIN+
VIN-

Fig. 1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101
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R1
R2
R3
C1
VOUT+
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VDD
QF+
Iout+
GND
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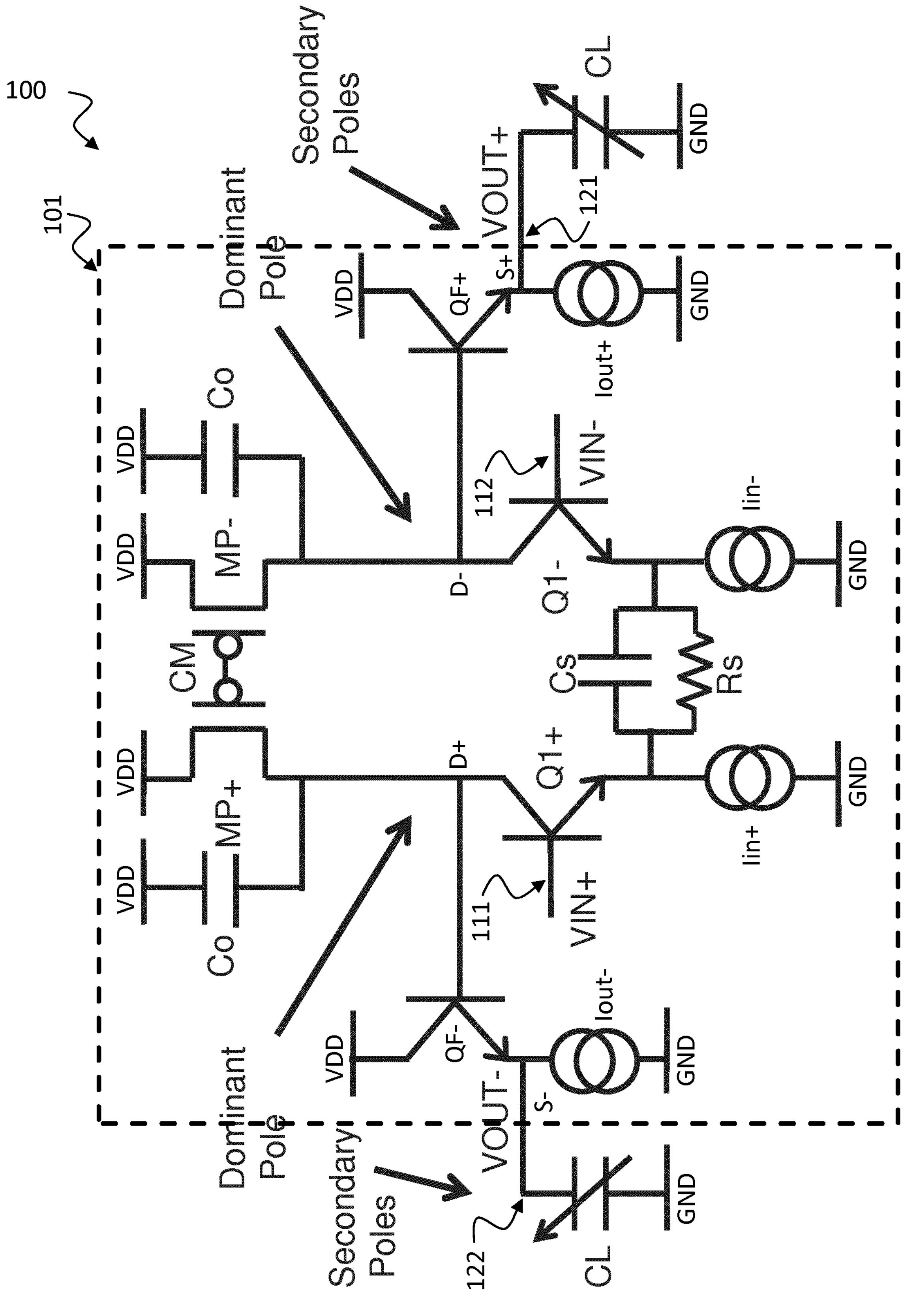
MP-
D-
Q1-
Iin-
CM
Cs
Rs
C2/2
MP+
D+
Q1+
Iin+
122
Iout-
QF-
VOUT-
111
VIN+

Fig. 2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101
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Dominant Pole
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MP-
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D-
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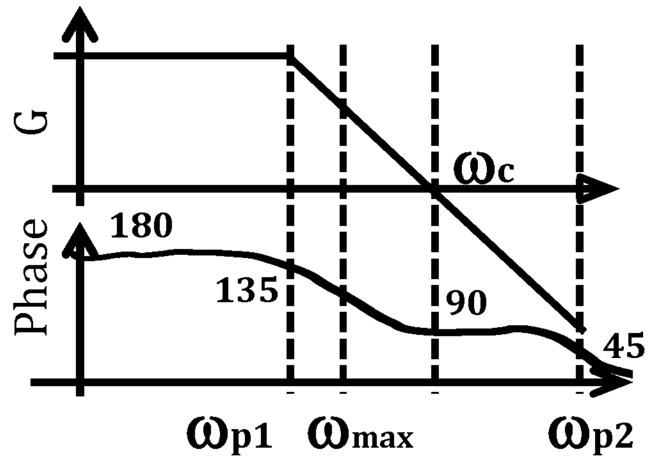
Q1-
Q1+
QF+
QF-
S+
S-
VOUT+
VOUT-
121
122
111
112
VIN-
VIN+
Iin-
Iin+
Iout+
Iout-
Cs
Rs
CL
GND

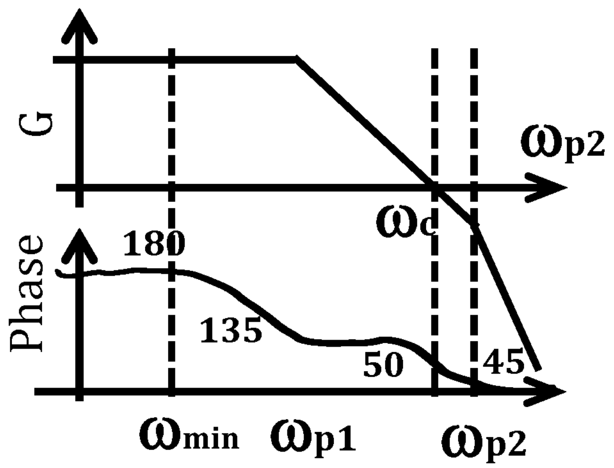
Fig. 3

400a



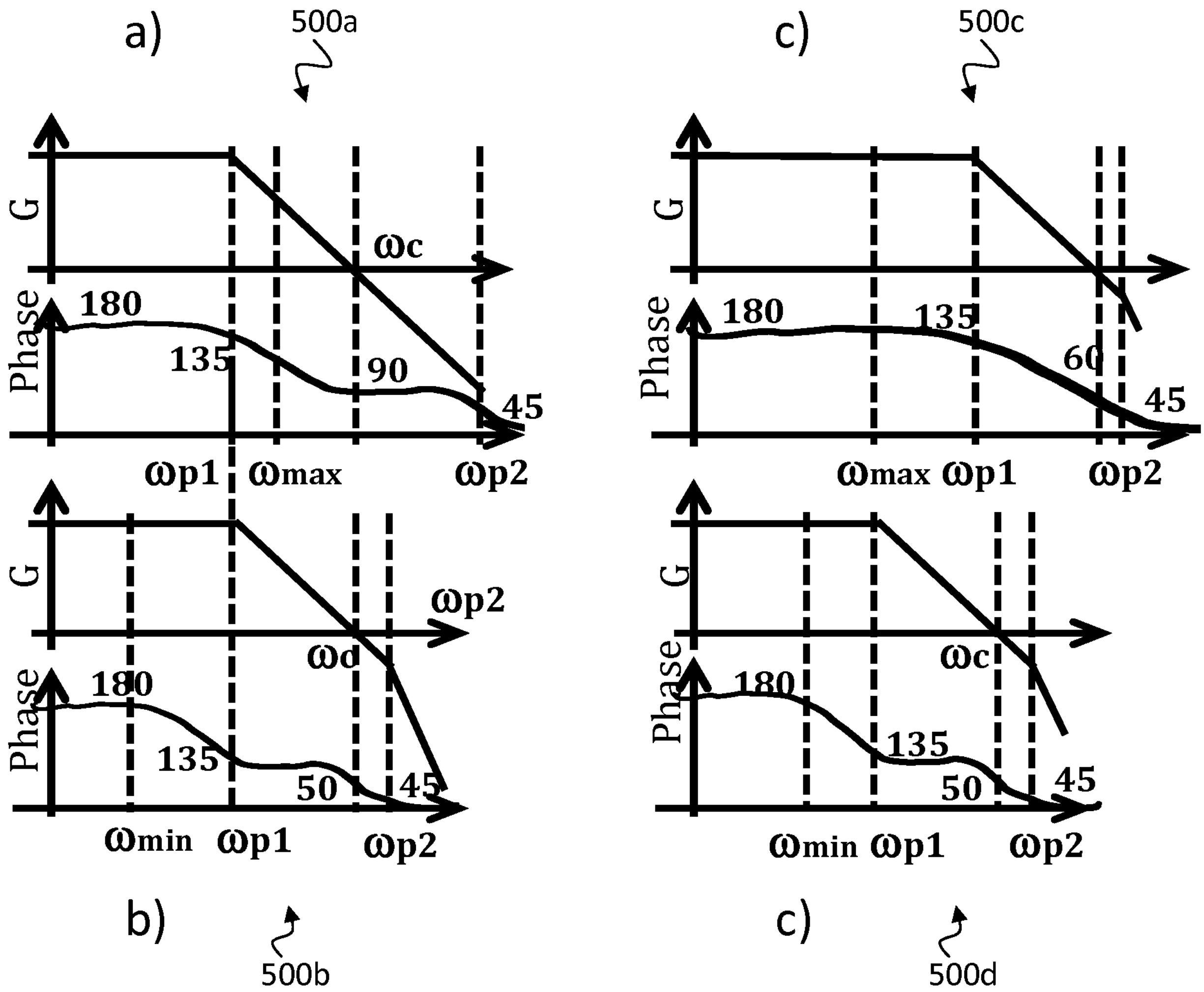
a)

400b



b)

Fig. 4



a)
500a
G
ωc
Phase
180
135
90
45
ωp1
ωmax
ωp2
G
ωp2
ωd
Phase
180
135
50
45
ωmin
ωp1
ωp2
b)
500b
c)
500c
G
Phase
180
135
60
45
ωmax
ωp1
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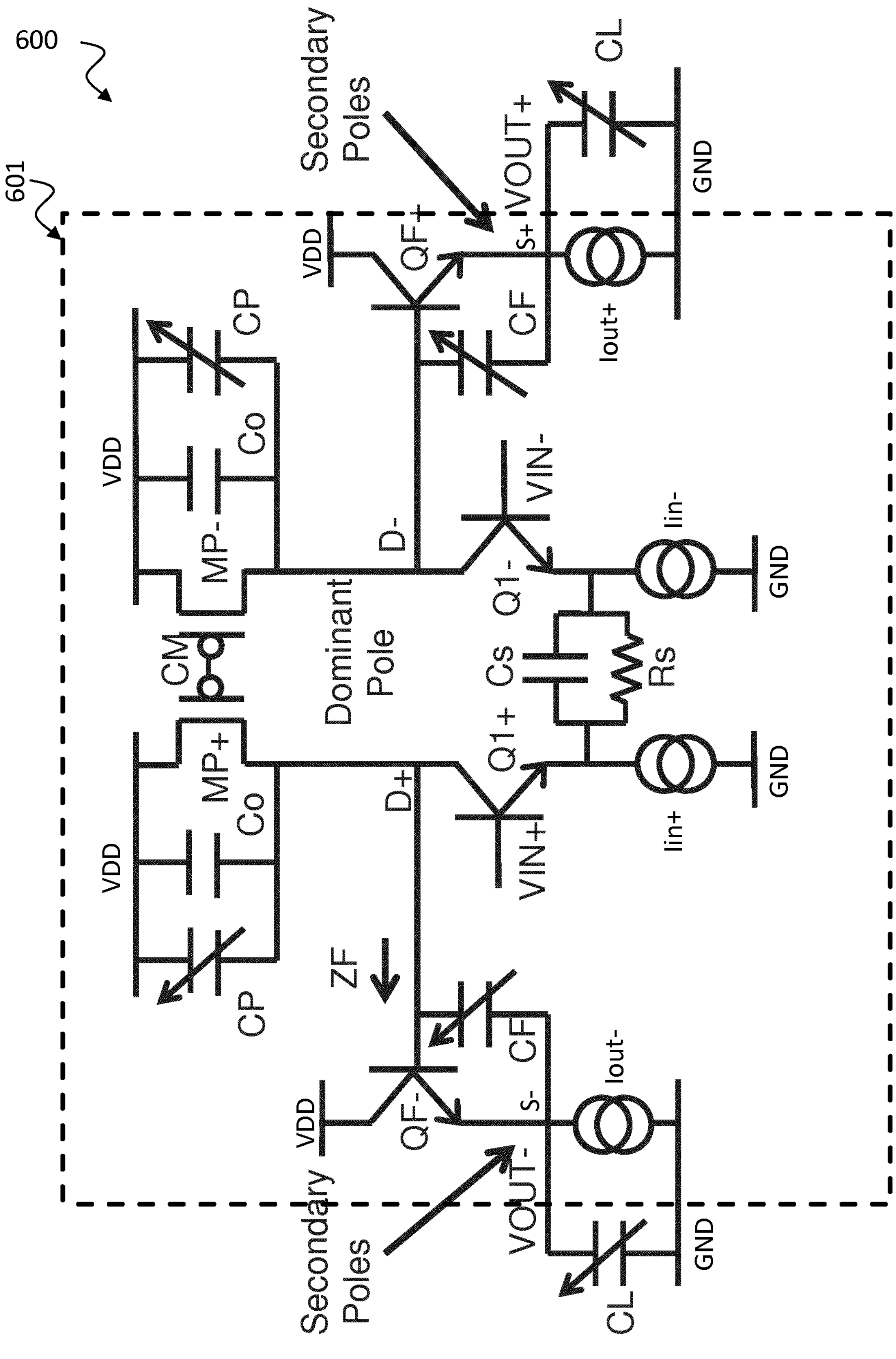
G
ωc
Phase
180
135
50
45
ωmin
ωp1
ωp2
c)
500d

Fig. 5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CL
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VDD
QF+
S+
CF
Iout+
CP
Co
VDD
MP-
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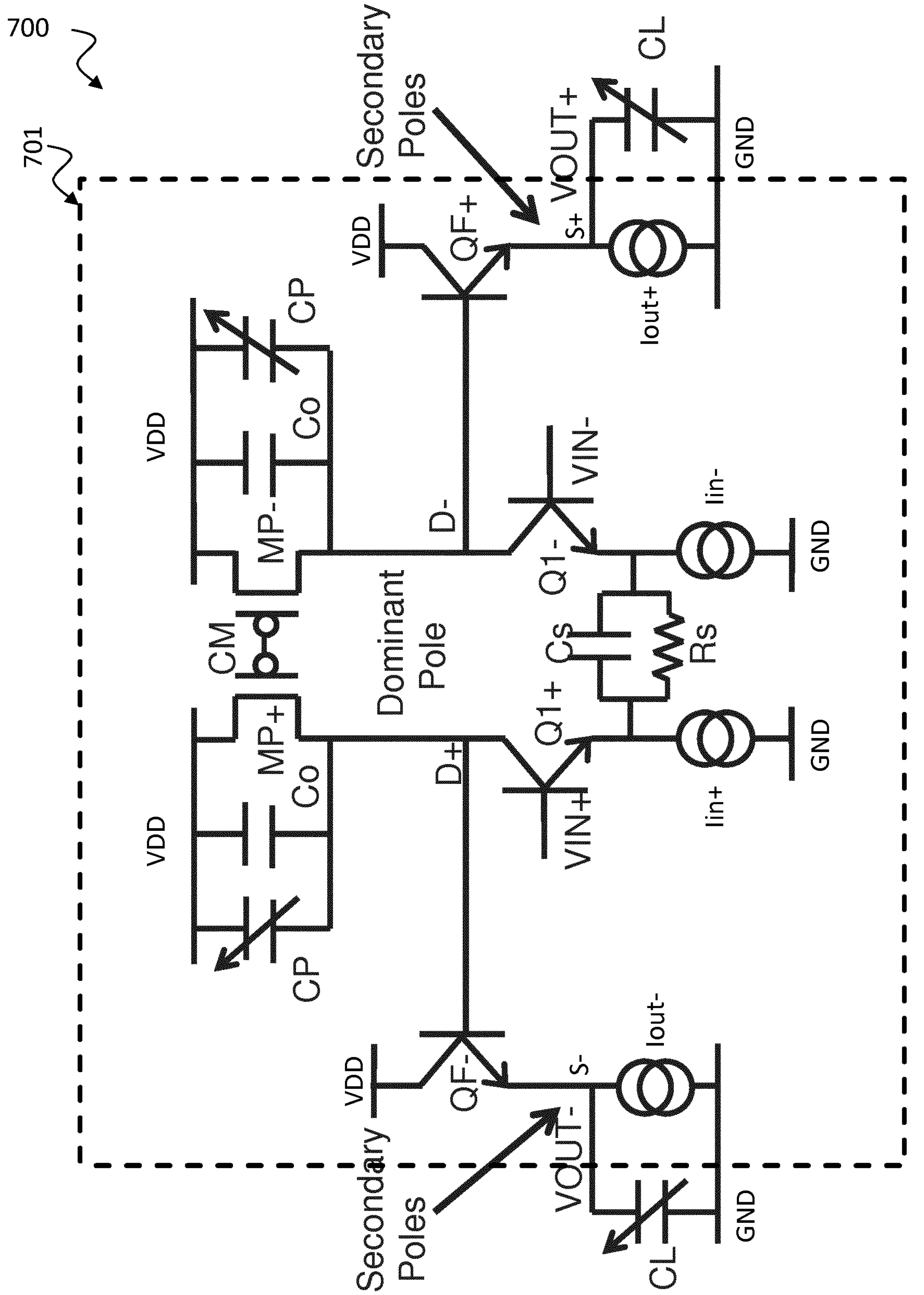
Q1-
Iin-
GND
CM
Dominant Pole
Cs
Rs
Q1+
MP+
Co
D+
VIN+
Iin+
GND
VDD
CP
ZF
CF
QF-
S-
Iout-
VDD
Secondary Poles
VOUT-
GND
CL

Fig. 6


700
701
Secondary Poles
VDD
QF+
S+
VOUT+
CL
GND
Iout+
CP
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MP-
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D-
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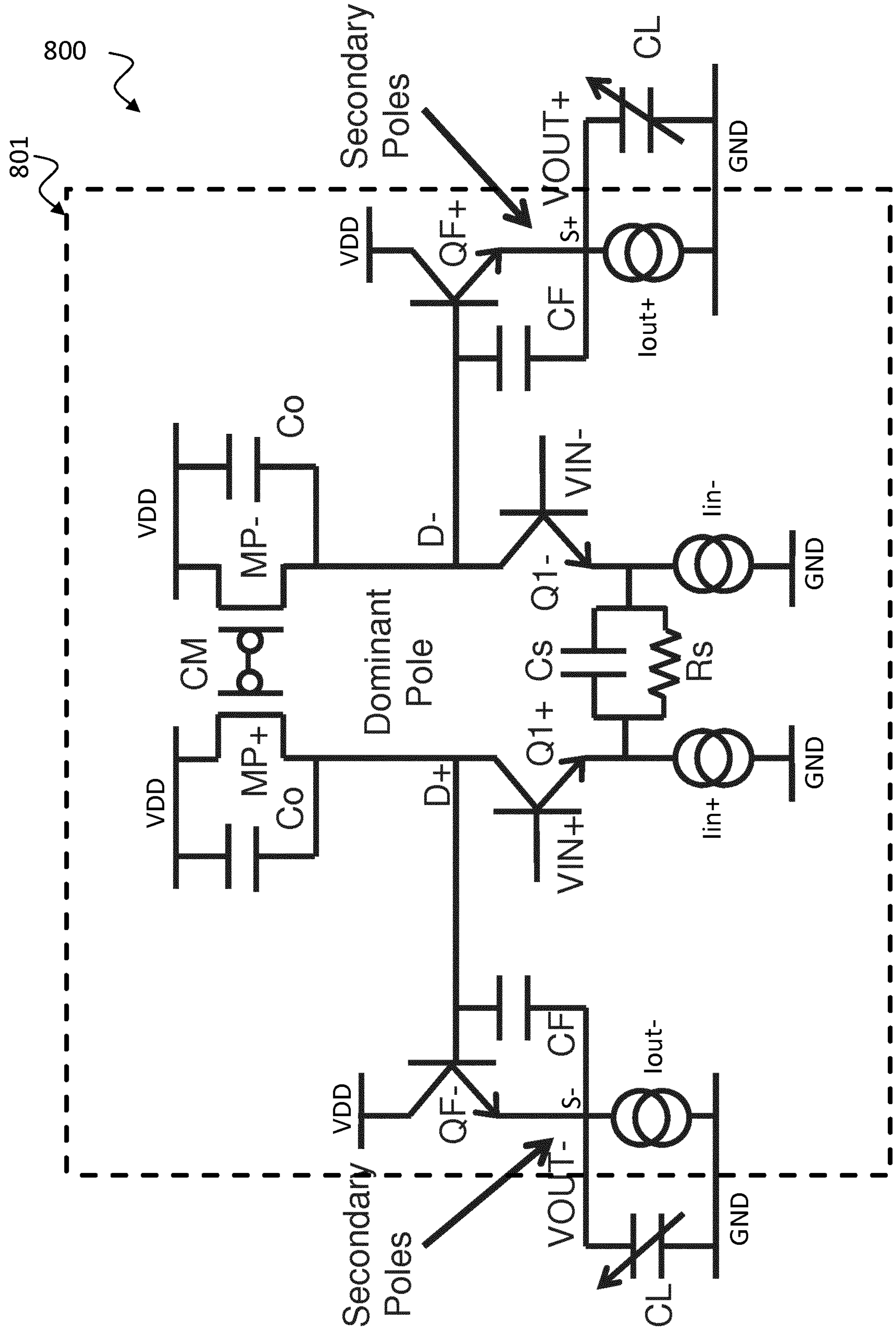
Iin-
GND
Q1-
CM
Dominant Pole
Cs
Rs
Q1+
MP+
D+
VIN+
Iin+
GND
Co
VDD
CP
QF-
S-
Iout-
VOUT-
CL
GND
Secondary Poles

Fig. 7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801
Secondary Poles
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CL
GND
VDD
QF+
S+
CF
Iout+
Co
VDD
MP-
D-
VIN-
Iin-
GND
Q1-
CM
Dominant Pole
Cs
Rs
Q1+
VDD
MP+
Co
D+
VIN+
Iin+
GND
CF
Iout-
VDD
QF-
S-
VOUT-
GND
Secondary Poles
CL

Fig. 8

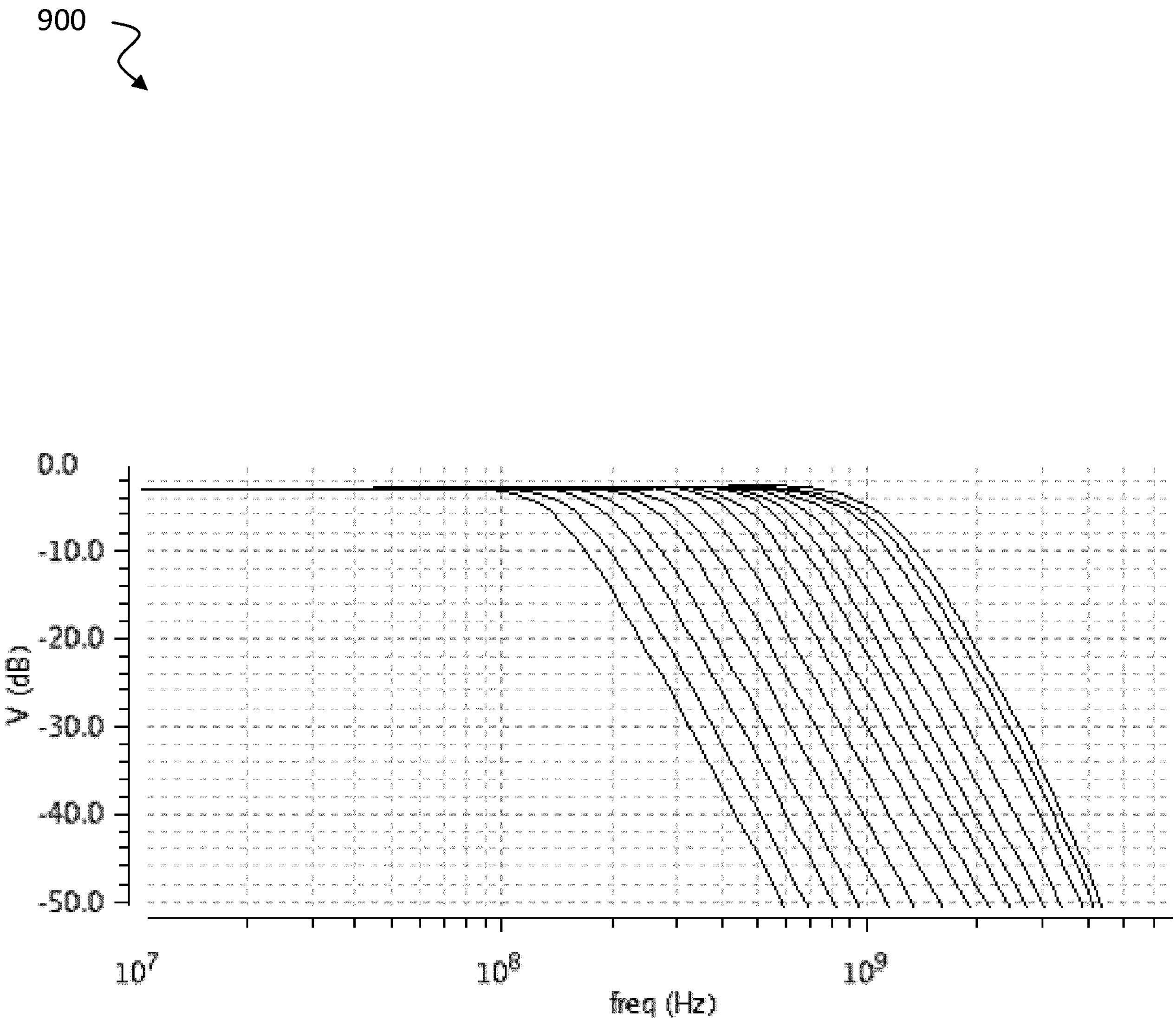
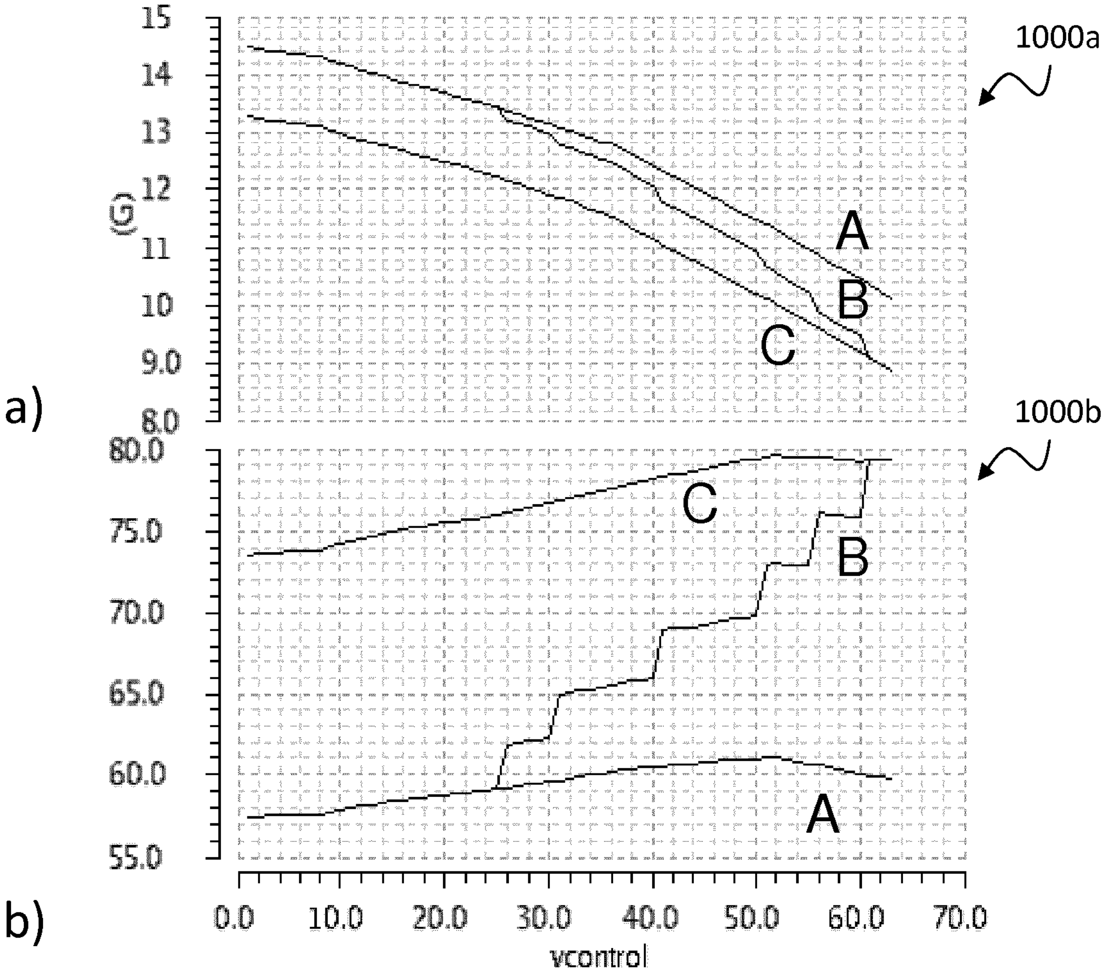


Fig. 9


1000a
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14
13
12
11
10
9.0
8.0
(G)
A
B
C
a)
1000b
80.0
75.0
70.0
65.0
60.0
55.0
C
B
A
b)
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
vcontrol

Fig. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/060769

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03H11/12 H03F1/08
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03H H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MOHAMMED ABDULAZIZ ET AL: "A 3.4mW 65nm CMOS 5 th order programmable active-RC channel select filter for LTE receivers", RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM (RFIC), 2013 IEEE, IEEE, 2 June 2013 (2013-06-02), pages 217-220, XP032443942, DOI: 10.1109/RFIC.2013.6569565 ISBN: 978-1-4673-6059-3	1,9,10, 13-15
A	II. The Amplifier Design ; III. Filter Design; page 217, right-hand column - page 219, left-hand column; figures 1 - 4	2-8,11, 12

X	US 6 618 579 B1 (SMITH MALCOLM H [US] ET AL) 9 September 2003 (2003-09-09)	1,9,10, 13-15
A	column 2, line 53 - column 4, line 18; figures 5 - 8	2-8,11, 12

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 February 2017	14/02/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Trafidlo, Renata

3

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/101279 A1 (GREITSCHUS NORBERT [DE] ET AL) 1 August 2002 (2002-08-01) paragraph [0003] - paragraph [0004]; figures 1 - 3 paragraph [0045] - paragraph [0050]; figures 6 - 8 -----	1-15
A	US 2013/135503 A1 (PARK YU JIN [KR] ET AL) 30 May 2013 (2013-05-30) paragraph [0074] - paragraph [0087]; figures 5, 6 paragraph [0091] - paragraph [0095]; figure 8 -----	1-15
A	US 2008/157874 A1 (LIN HENG-CHIH [TW]) 3 July 2008 (2008-07-03) paragraph [0026] - paragraph [0040]; figures 4 - 11 -----	1-15
A	EP 0 777 319 A1 (SGS THOMSON MICROELECTRONICS [IT]) 4 June 1997 (1997-06-04) abstract column 2, line 10 - column 4, line 52; figures 1 - 3 column 6, line 23 - column 9, line 25; figures 4 - 6 -----	1-15

3

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2016/060769

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
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			JP	2002185288	A	28-06-2002
			US	2002101279	A1	01-08-2002
US 2013135503	A1	30-05-2013	KR	20130059995	A	07-06-2013
			US	2013135503	A1	30-05-2013
US 2008157874	A1	03-07-2008	CN	101222209	A	16-07-2008
			TW	200832896	A	01-08-2008
			US	2008157874	A1	03-07-2008
EP 0777319	A1	04-06-1997	DE	69529828	D1	10-04-2003
			EP	0777319	A1	04-06-1997
			US	5825250	A	20-10-1998