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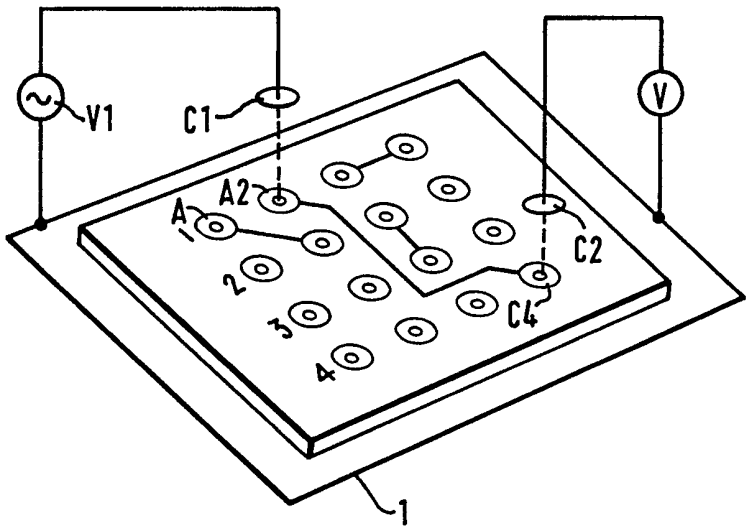
(54) A capacitive method and apparatus for checking connections of a printed circuit board

(57) A first conductive plate (C1) connected to an a.c. voltage source (V1) is placed adjacent and spaced from a terminal (A2) of a printed circuit board. A conductive track between this terminal (A2) and another terminal (C4) is then energised, a signal being obtained by voltmeter (V) as a result of such energisation and capacitive coupling between the terminal (C4) and the voltmeter (V). In this way, the connections of a printed circuit board can be checked using capacitive coupling and without reliance on an ohmic connection.

FIG.3.



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The drawing(s) originally filed was/were informal and the print here reproduced is taken from a later filed formal copy.
The claims were filed later than the filing date within the period prescribed by Rule 25(1) of the Patents Rules 1982

FIG.1.

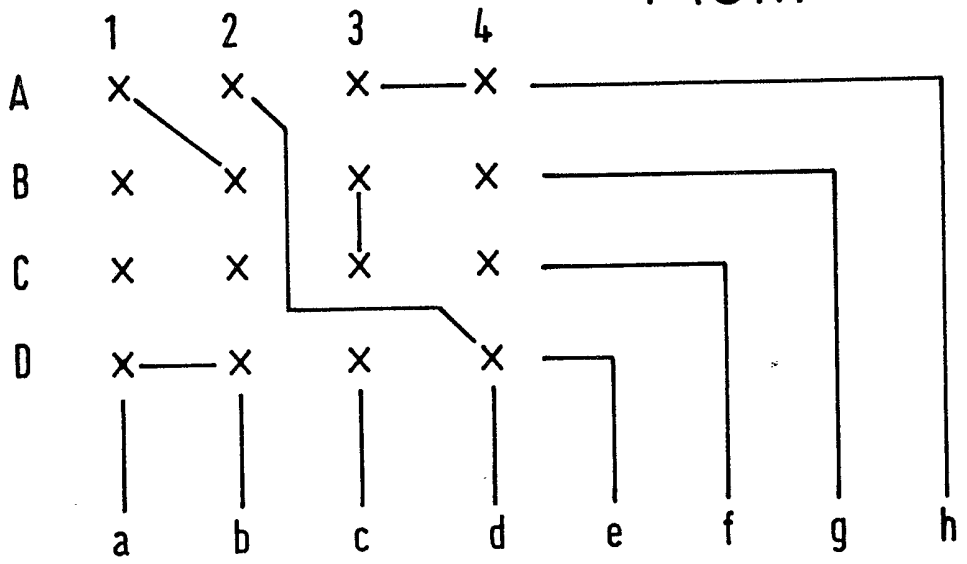
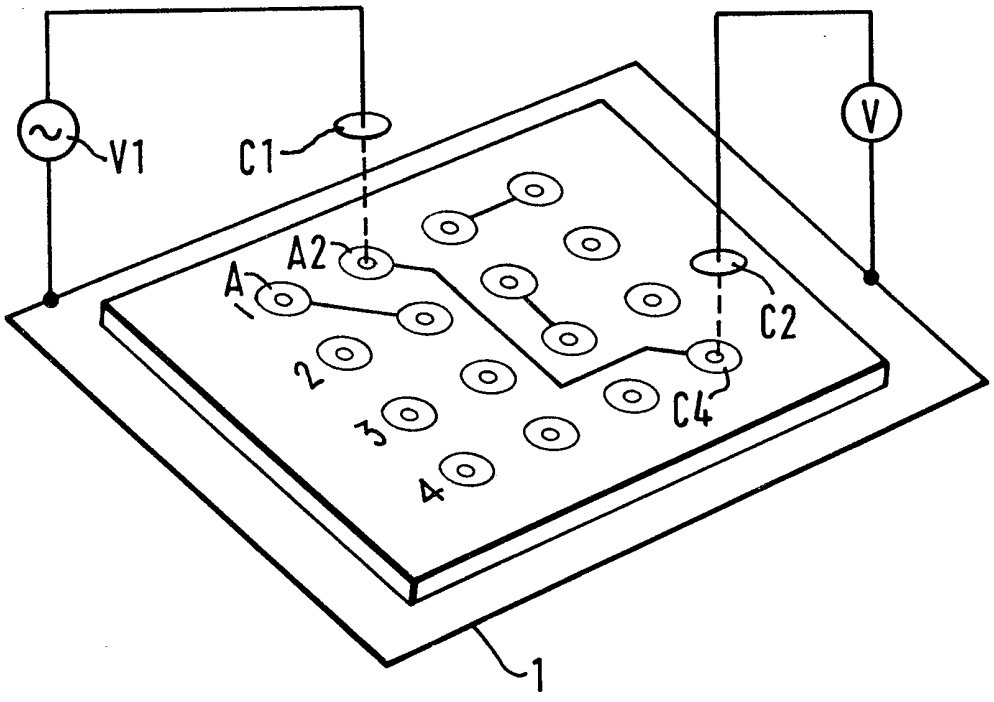


FIG.3.



DRIVE	a	b	c	d	e	f	g	h	BINARY
A1	I							I	129
A2		I						I	130
A3			I					I	132
A4				I				I	136
B1	I						I		65
B2		I					I		66
B3			I				I		68
B4				I			I		72
C1	I					I			33
C2		I				I			34
C3			I			I			36
C4				I		I			40
D1	I				I				17

FIG.2A.

A1	I	I					I	I	195
A2		I		I	I			I	154
A3			I	I				I	140
A4			I	I				I	140
B1	I						I		65
B2	I	I					I	I	195
B3			I			I	I		100
B4				I			I		72
C1	I					I			33
C2		I				I			34
C3			I			I	I		100
C4				I		I			40
D1	I	I			I				19

FIG.2B.

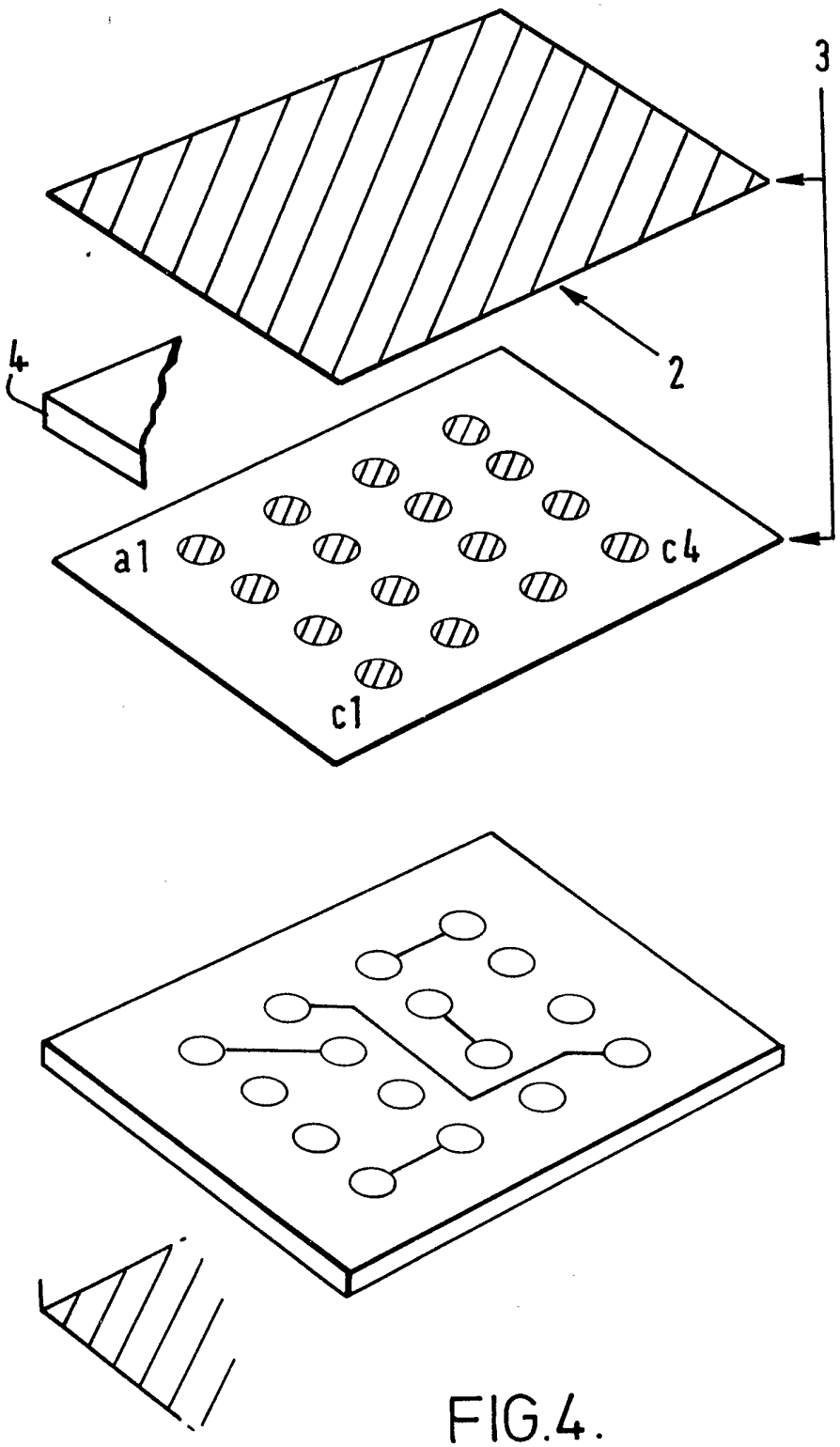


FIG.4.

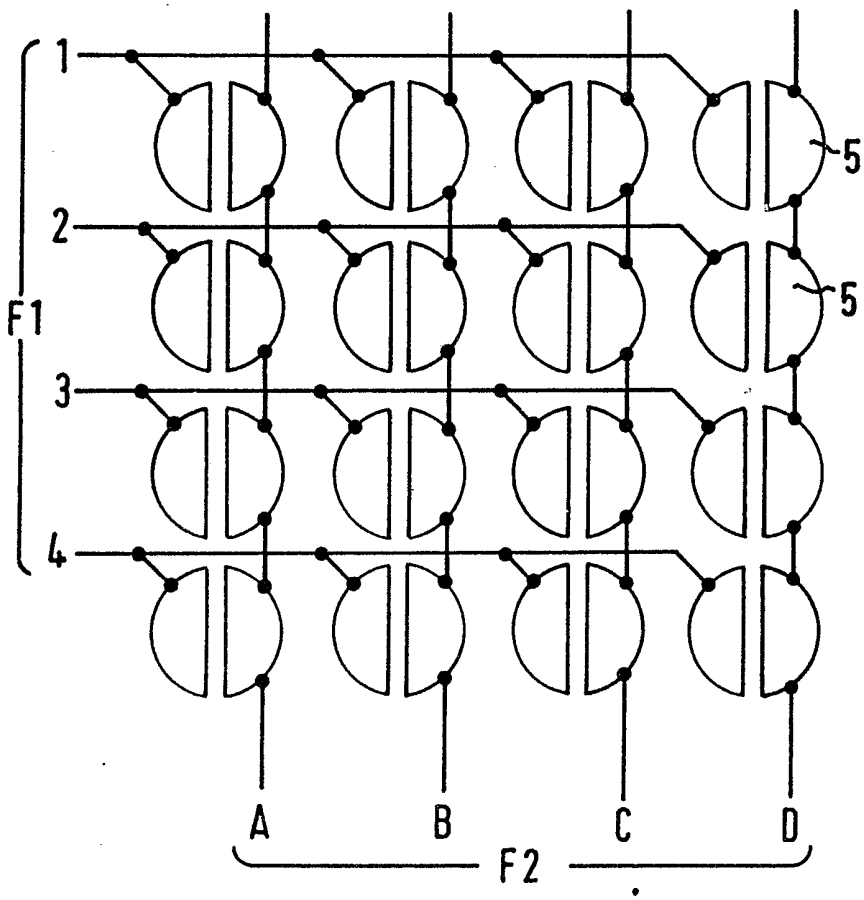


FIG.5A.

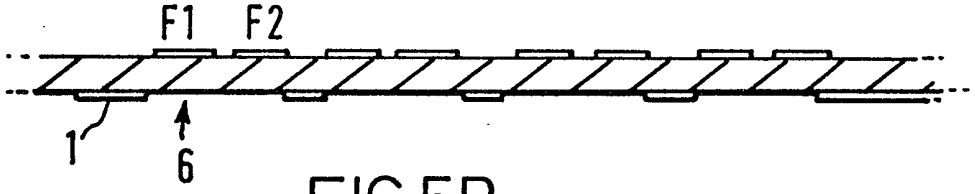


FIG.5B.

FIG.6.

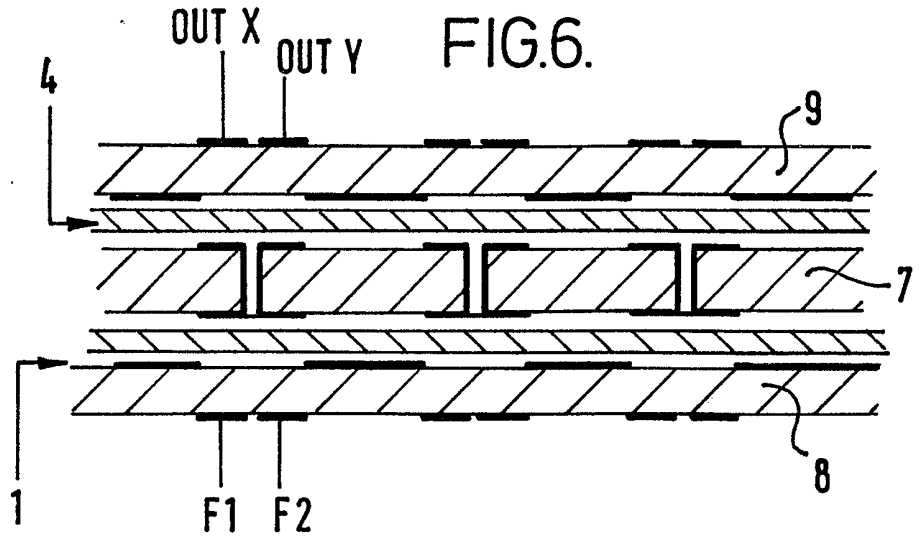
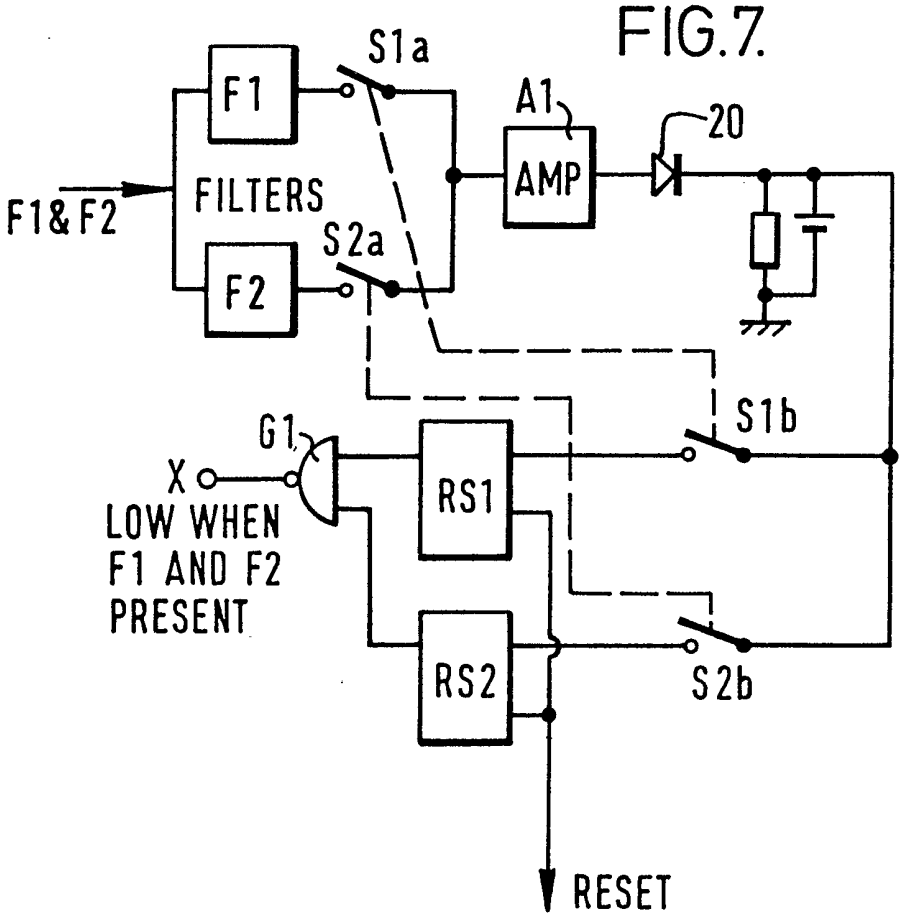

OUT X
OUT Y
4
9
7
8
1
F1
F2

FIG.7.


F1
S1a
A1
20
AMP
F1&F2
FILTERS
S2a
F2
S1b
G1
X
LOW WHEN
F1 AND F2
PRESENT
RS1
RS2
S2b
RESET

SPECIFICATION

A method of and apparatus for checking connections of a printed circuit board

The present invention relates to a method of and apparatus for checking connections of a printed circuit board.

The cost of a bare board tester depends on software and on the maximum number of points. In addition, for each new type of printed circuit board (PCB) to be tested, a new pin jig is required.

A pin jig is an array of spring-loaded pins designed to contact each point to be tested. Such jigs must be jig-drilled to obtain adequate precision, and their cost depends on the number of installed test points. For a PCB manufacturer requiring *per annum* 15–20 jigs to test, say, a 2000 point PCB a considerable capital outlay is involved.

A lower cost method of making the replaceable jig component of the tester would result in a considerable saving for manufacturers.

According to the present invention from one aspect, there is provided a method of checking the connection via a conductive track between first and second terminals of a printed circuit board, wherein a first electrically conductive member connected to a source of alternating voltage is placed adjacent and spaced from the first terminal for electrically energising the conductive track by capacitive coupling between the first terminal and the first member; and a second electrically conductive member is placed adjacent and spaced from the second terminal for obtaining an output signal, as a result of such energisation of the track and its connection of the first and second terminals, by capacitive coupling between second terminal and the second member.

According to the present invention from another aspect, there is provided an apparatus, for carrying out the method described in the preceding paragraph, comprising: a first electrically conductive member which, in use of the apparatus, is placed adjacent and spaced from the first terminal; applying an alternating voltage to the first member for electrically energising the conductive track by capacitive coupling between the first terminal and the first member; a second electrically conductive member which, in use of the apparatus, is placed adjacent and spaced from the second terminal; and means for obtaining an output signal, as a result of such energisation of the track and its connection of the first and second terminals by capacitive coupling between the second terminal and the second member.

For a better understanding of the present invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:–

Figure 1 illustrates how a method according to an embodiment of the present invention may be applied to conventional jigs;

Figures 2A and 2B are tables showing respectively typical signatures, from a connected and from an unconnected PCB;

Figure 3 shows the PCB of Fig. 1 in isometric form with added components;

Figure 4 illustrates the construction of the PCB of Figs. 1 and 3;

Figures 5A and 5B illustrate the connections of pads on a master PCB;

Figure 6 shows the construction of a PCB tester; and

Figure 7 shows one embodiment of a sense amplifier.

In Fig. 1, signature generation is accomplished by sequentially applying a signal to A1, A2, A3, A4, B1, B2, etc. The resultant signature is shown in Fig. 2. Each point is connected to a horizontal row (e - h) AND to a vertical column (a - d) by a diode. Thus, if no links existed on the PCB the signature is as shown in Fig. 2A, which is modified to that shown in Fig. 2B when the PCB is connected.

The points a - h are in practice an 8-bit word, with a binary value as shown in the last column, and are stored in a memory for subsequent comparison with the signature from an untested board. For this system to be cost-effective, a bulk electrically alterable read only memory (EAROM) (for example 2K × 96) must be available for a 2K point system. EAROM is an electrically erasable, hence reusable, memory that retains its data when shut down. The cost of a memory block for a 2K jig is negligible in comparison with the present cost of known jigs.

It can be seen that the above-described principle depends on applying a signal to A1 etc. and detecting its presence on the eight lines a - h. All known systems have used d.c., usually 5V., signals.

The system to be described hereinbelow relies on capacitive coupling to the test area, not on an ohmic connection.

Fig. 3 shows the PCB with tracks. C1 and C2 are small circular discs with a diameter similar to a pad below. Two plates are required, C1 being a transmitter coupled to an r.f. source V1, and C2 being a receiver coupled to a sensitive r.f. volt-meter V. Application of a voltage from source V1 to the capacitor C1 will cause the track from A2 to C4 to become r.f. "live". This state may be detected by positioning C2 above the output pad C4, as shown in Fig. 3.

The choice of frequency is a compromise between a high frequency, with improved coupling between C1 and the pad A2, and a low frequency to reduce points effects which may couple adjacent tracks.

In practice both sides of the PCB will be

covered by ground planes 1 with cut-outs 6 at the pad areas (Fig. 5B) to minimise this fringing. This operation will now be described with reference to Fig. 4. A copper capacitor plate 2 at C4 can be automatically positioned above pad A4 etc. by means of a double sided PCB 3. An important point to note is that the PCB comprising the upper capacitor plate at C4 is in fact using the solder resist mask of the PCB below. A PCB manufacturer therefore has the ability to produce this component at low cost in his own plant. Reference numeral 4 denotes an insulating layer.

It can be seen that both input and output capacitor plates are automatically created at the same time.

The next step is to generate a means of scanning all of the test points and converting the result of this scan into an 8-line signal compatible with the standard logic required by Fig. 1.

This could be done by adopting a modified approach employing two frequencies in an XY matrix, with PCB being employed on the input side, the lower surface is used for detection.

This step will require that the system is only usable with double sided PTH boards. In practice, however, as these high complexity boards are the only ones which would normally be tested this is not a disadvantage.

The preceding description has illustrated in outline a method of capacitive coupling between a fixed upper plate 2 and a PCB 1. Next the r.f. signal must be switched from point to point.

An optimum solution to this problem is found by using two frequencies on an XY grid as shown in Fig. 5A.

A series of adjacent semi circular or other shaped copper pads 5 are etched on a master PCB which is fixed and which constitutes a fundamental part of the basic tester. One half of each pad 5 is connected to a frequency F1 while the other half is connected to a frequency F2. The signals are sequentially injected into lines 1–4 for F1 and A-D for F2.

As an example, for a master jig of 63.5cm square, 250 lines in X (A-D) and 250 lines in Y (1–4) axes are required, when employing a 0.1 pitch.

Each twin pad 5 will be scanned, but only one pad will have both F1 and F2 present. In this manner a complete array of 64K pads may be scanned.

In practice, a memory would direct the XY grid to points where pads existed on the PCB under test, thus saving scanning time. The PCB assembly shown in Fig. 5 is a permanent part of the tester and thus represents a single capital cost only.

The remaining problem is now to detect pads 5 on the PCB 7 under test (Fig. 6) where both F1 and F2 are present. This differs from a conventional d.c. tester where only one signal is required for detection.

Fig. 6 shows the construction of a complete tester showing the bottom PCB 8, as shown in Fig. 5, held, for example, by a vacuum in contact with the PCB7 under test. Finally a second PCB 9 of Fig. 5 type is used as the output sensor, the function of which is described in the next section.

At this point, two options are possible, either to use an upper board containing 250 × 250 sensors as a permanent fixture, with the attendant high cost of sense amplifiers for the r.f. on each of 500 lines, or to create a network connected to the 2K points actually used. The economies of these two options will be considered at a later stage.

The capacitance between upper and lower sections of test points on a jig will be of the order of 0.5 pF. This yields a reactance of 30K at 10 MHz. To use a higher frequency would enable lower impedance sense amplifiers to be employed, but would risk more "jump over" between scanning tracks due to standing wave problems.

To use a lower sense of frequency would entail higher impedance amplifiers with the likely risk of stray coupling.

There is a further reason for the use of frequencies of the order of 10 MHz which is best explained with the description of a possible sense amplifier. It should be noted that a sense amplifier is defined as a system capable of detecting both F1 and F2 at a test point.

Fig. 7 shows one such possible system.

Two filters F1 and F2, with passband characteristics close to 10 MHz, are switched sequentially to an amplifier A1 with a feeding detector 20. If a signal is detected at one frequency either of two RS FLIP-FLOPS RS1, RS2 is set to a high output state. It can be seen that respective second, synchronously operating switches S1a, b; S2a, b route the detector output to either RS1, set by F1, or RS2 set by F2. Only when both are present will the output of a NAND gate G1 fall low.

When the test has been performed on one XY pair of sense lines, a RESET pulses is applied at the next change of address to reset the sense amplifier for a new input.

In a dedicated 2K point system, 96 of these amplifiers will be required (they represent, however, only a single capital cost), hence their price must be kept as low as possible.

The choice of 10 MHz as a nominal sense of frequency has two practical advantages namely:

(i) low cost filters are available at 9 and 10.7 MHz as cheap standard components; and

(ii) on the drive side, 10 MHz signals are easily routed by standard LS series logic gates.

Two separate amplifiers, with associated decoding logic, may become viable depending on the prevailing market.

CLAIMS

1. A method of checking the connection via a conductive track between first and second terminals of a printed circuit board, wherein a first electrically conductive member connected to a source of alternating voltage is placed adjacent and spaced from the first terminal for electrically energising the conductive track by capacitive coupling between the first terminal and the first member; and a second electrically conductive member is placed adjacent and spaced from the second terminal for obtaining an output signal, as a result of such energisation of the track and its connection of the first and second terminals, by capacitive coupling between the second terminal and the second member.

2. A method as claimed in claim 1, wherein the connections via each of a plurality of conductive tracks between respective first and second terminals are checked for a master printed circuit board to produce an output signature representative of the master printed circuit board, the signature being stored in a storage means for subsequent comparison with an output signature of a printed circuit board under test.

3. A method as claimed in claim 1 or 2, the first electrically conductive member being one of a plurality of such members forming an array, each such member comprising first and second parts each part being connectable to a source of voltage at first and second frequencies respectively, in which method the first and second parts of the first electrically conductive members are sequentially connected to the respective voltage sources so that only one member is connected to both the first and second frequency voltage sources, the output signal being obtained at the second electrically conductive member which is connected, via the track between the first and second terminals, energised at both first and second frequencies, by capacitive coupling between the second terminal and the second electrically conductive member, to the one first electrically conductive member.

4. An apparatus for checking the connection via a conductive track between first and second terminals of a printed circuit board, the apparatus comprising: a first electrically conductive member which, in use of the apparatus, is placed adjacent and spaced from the first terminal; means for applying an alternating voltage to the first member for electrically energising the track by capacitive coupling between the first terminal and the first member; a second electrically conductive member which, in use of the apparatus, is placed adjacent and spaced from the second terminal; and means for obtaining an output signal, as a result of such energisation of the track and its connection of the first and second terminals, by capacitive coupling between the second terminal and the second member.

5. An apparatus as claimed in claim 4, comprising first and second electrically conductive components which provide respectively a plurality of such first and second electrically conductive members arranged in an array to check the connections between each of a plurality of such tracks, each electrically conductive member having first and second parts, wherein the means for applying an alternating voltage to each first member consists of means for sequentially applying an alternating voltage at a first frequency to each first part and means for sequentially applying an alternating voltage at a second frequency to each second part for energising one of the tracks at both first and second frequencies, and wherein the means for obtaining an output signal comprises means for providing an output when signals of both first and second frequencies are detected at one of the second electrically conductive members.

6. A method of checking the connection via a conductive track between first and second terminals of a printed circuit board substantially as herein described with reference to the accompanying drawings.

7. An apparatus for checking the connection via a conductive track between first and second terminals of a printed circuit board substantially as herein described with reference to, and as shown in, Figs. 3 to 7 of the accompanying drawings.

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