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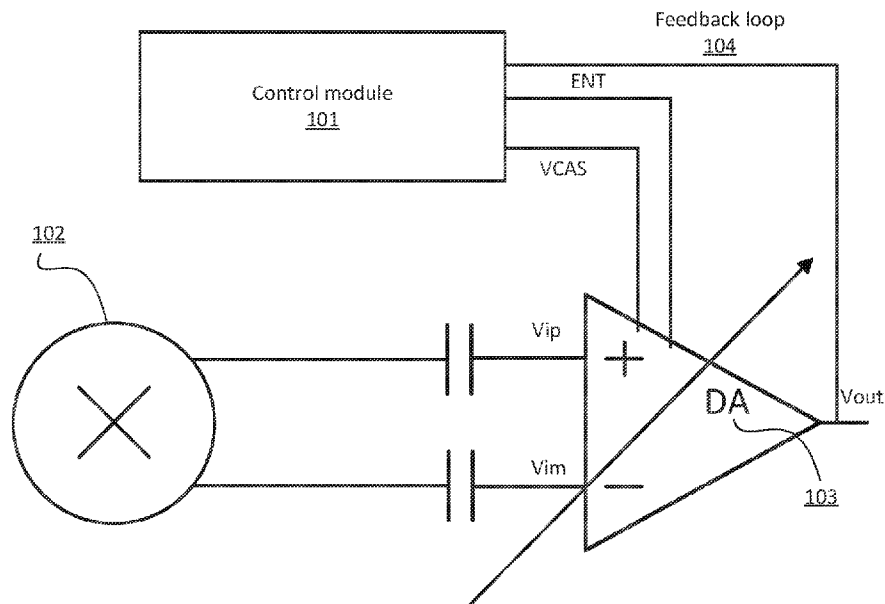


Figure 1

(57) Abstract: The present invention is directed to electrical circuits and methods thereof. In a specific embodiment, an array of differential amplifiers includes a number of amplifier devices configured in parallel relative to a pair of differential inputs and parallel relative to a pair of differential outputs. A total gain of the array of differential amplifiers is based on the number of amplifier devices and their respective auxiliary transistors being turned on. There are other embodiments as well.



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DRIVER AMPLIFIERS WITH DIFFERENTIAL AMPLIFIER ARRAYS

BACKGROUND OF THE INVENTION

[0001] Driver amplifiers are widely used in small signal RF applications. Deployed in many wireless communication systems, such as WLAN, WiFi, Bluetooth, or Cellular networks, the driver amplifier has been required to deliver high performance in gain control and signal noise reduction while keeping power consumption as low as possible. A design objective to save power while still trying to maintain the amplifier gain often causes the issue of output signal noise or phase distortion.

[0002] Therefore, new and improved driver amplifier circuit topologies and corresponding control schemes are desired.

BRIEF SUMMARY OF THE INVENTION

[0003] In a specific embodiment, an array of differential amplifiers includes several amplifier devices configured in parallel relative to a pair of differential inputs and parallel relative to a pair of differential outputs. A total gain of the array of differential amplifiers is based on the number of amplifier devices and their respective auxiliary transistors being turned on. There are other embodiments as well.

[0004] In one aspect, a driver amplifier apparatus is provided. A driver amplifier apparatus includes a first differential input terminal. The apparatus also includes a second differential input terminal. The apparatus also includes a control logic configured to provide a first plurality of control signals and a second plurality of control signals. The first plurality of control signals includes a first control signal. The second plurality of control signals includes a second control signal. The apparatus also includes a first differential output terminal. The apparatus also includes a second differential output terminal. The apparatus also includes an array of differential amplifiers including a first differential amplifier device and a second differential amplifier device, the first differential amplifier device and the second differential amplifier device may include a parallel input configuration and a parallel output configuration. The first differential amplifier device may include: a first input transistor may include a first gate and a first drain, the first gate being coupled to the first differential input terminal; a second input transistor may include a second gate and a second drain, the second gate being coupled to the second differential input terminal; a first output transistor coupled to the first

drain and the first control signal; a second output transist
first control signal; a first auxiliary transistor may include a third gate and a third drain, the
third gate being coupled to the first differential input terminal, the third drain being coupled to
the second drain; a second auxiliary transistor may include a fourth gate and a fourth drain, the
5 fourth gate being coupled to the second differential input terminal, the fourth drain being
coupled to the first drain; and a third auxiliary transistor coupled to the first auxiliary transistor
and the second control signal.

[0005] In another aspect, a driver amplifier apparatus includes a first differential input
terminal. The apparatus also includes a second differential input terminal. The apparatus also
10 includes a first differential output terminal. The apparatus also includes a second differential
output terminal. The apparatus also includes an array of differential amplifiers including a first
differential amplifier device and a second differential amplifier device, the first differential
amplifier device and the second differential amplifier device may include a parallel input
configuration and a parallel output configuration. The first differential amplifier device may
15 include: a first input transistor may include a first gate and a first drain and a first source, the
first gate being coupled to the first differential input terminal; a second input transistor may
include a second gate and a second drain and a second source, the second gate being coupled to
the second differential input terminal; a first output transistor may include a third gate and a
third drain and a third source, the third source being coupled to the first drain, and the third
20 gate being coupled to a first control signal; a second output transistor may include a fourth gate
and a fourth drain and a fourth source, the fourth source being coupled to the second drain, and
the fourth gate being coupled to the first control signal; a first auxiliary transistor may include
a fifth gate and a fifth drain and a fifth source, the fifth gate being coupled to the first
differential input terminal, the fifth drain being coupled to the second drain; a second auxiliary
25 transistor may include a sixth gate and a sixth drain and a sixth source, the sixth gate being
coupled to the second differential input terminal, the sixth drain being coupled to the first
drain; and a third auxiliary transistor may include a seventh gate and a seventh drain and a
seventh source, the seventh drain being coupled to the sixth source, the seventh gate being
coupled to a second control signal.

30 [0006] In a further aspect, a driver amplifier apparatus is provided in which a control logic is
configured to provide either a first signal or a second signal. The first signal includes an
enabling binary signal. The second signal includes a disabling binary signal. The apparatus
also includes an array of N differential amplifier devices, wherein N is an integer. Each
differential amplifier device respectively includes an amplifier unit having a first control

terminal and an auxiliary unit having a second control terminal to a parallel input configuration and a parallel output configuration, and the auxiliary unit is coupled to the amplifier unit and the parallel input configuration. The control logic is configured to set m differential amplifier devices in a first state with the respective first control terminals being supplied with the first signal and the respective second control terminals being supplied with the second signal, and to set n differential amplifier devices in a second state with the respective first control terminals being supplied with the second signal and the respective second control terminals being supplied with the first signal, wherein $m + n \leq N$, $n \geq 1$.

10 [0007] It is to be appreciated that embodiments of the present invention provide many advantages over conventional techniques. Among other things, driver amplifiers according to embodiments of the present invention with multi-sliced differential amplifier cells provide improved AM-PM performance under control schemes designed according to the topology of the individual differential amplifier. Additionally, improved AM-PM performance directly leads to improved error-vector magnitude (EVM), an important metric of driver amplifier performance, even with a smaller number of turned-on differential amplifier cells with flexible gain control and reduced power consumption. Various performance metrics are used to analyze the DA operation under different control schemes, demonstrating many advantages over conventional amplifiers in various RF applications.

20 [0008] Embodiments of the present invention can be implemented in conjunction with existing systems and processes. For example, driver circuits and differential amplifiers according to the present invention can be used in a wide variety of systems and applications, including cellular, WiFi devices, and others. There are other benefits as well.

25 [0009] The present invention achieves these benefits and others in the context of known technology. However, a further understanding of the nature and advantages of the present invention may be realized by reference to the latter portions of the specification and attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

30 [0010] Figure 1 is a simplified diagram illustrating a driver amplifier according to various embodiments of the present invention.

[0011] Figure 2A is a simplified diagram illustrating an exemplary driver amplifier with an array of differential amplifiers according to various embodiments of the present invention.

[0012] Figure 2B is a simplified diagram illustrating an amplifier with an array of differential amplifiers according to various embodiments of the present invention.

5 [0013] Figure 3 is a simplified graph showing the performance of the driver amplifier according to various embodiments of the present invention using gain variation, phase shifting, and error-vector magnitude measurement.

[0014] Figure 4 is a simplified graph showing the performance of the driver amplifier according to various alternative embodiments of the present invention using gain and phase control and error-vector magnitude measurement.

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DETAILED DESCRIPTION OF THE INVENTION

[0015] The present invention is directed to electrical circuits and methods thereof. In a specific embodiment, an array of differential amplifiers includes several amplifier devices configured in parallel relative to a pair of differential inputs and parallel relative to a pair of differential outputs. A total gain of the array of differential amplifiers is based on the number of amplifier devices and their respective auxiliary transistors being turned on. There are other embodiments as well.

15 [0016] The following description is presented to enable one of ordinary skill in the art to make and use the invention and to incorporate it into the context of particular applications. Various modifications, as well as a variety of uses in different applications, will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to a wide range of embodiments. Thus, the present invention is not intended to be limited to the embodiments presented but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

20 [0017] In the following detailed description, numerous specific details are outlined to provide a more thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without necessarily being limited to these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, to avoid obscuring the present invention.

25 [0018] The reader's attention is directed to all papers and documents which are filed concurrently with this specification and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference. All the features disclosed in this specification, (including any accompanying claims,

abstract, and drawings) may be replaced by alternative features for a similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

[0019] Furthermore, any element in a claim that does not explicitly state "means for" performing a specified function, or "step for" performing a specific function, is not to be interpreted as a "means" or "step" clause as specified in 35 U.S.C. Section 112, Paragraph 6. In particular, the use of "step of" or "act of" in the Claims herein is not intended to invoke the provisions of 35 U.S.C. 112, Paragraph 6.

[0020] Moreover, when an element is referred to herein as being "connected" or "coupled" to another element, it is to be understood that the elements can be directly connected to the other element, or have intervening elements present between the elements. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, it should be understood that no intervening elements are present in the "direct" connection between the elements. However, the existence of a direct connection does not exclude other connections, in which intervening elements may be present.

[0021] Please note, if used, the labels left, right, front, back, top, bottom, forward, reverse, clockwise, and counterclockwise have been used for convenience purposes only and are not intended to imply any particular fixed direction. Instead, they are used to reflect relative locations and/or directions between various portions of an object.

[0022] In some embodiments, a driver amplifier apparatus is provided. The apparatus includes a first differential input terminal. The apparatus also includes a second differential input terminal. The apparatus also includes a control logic configured to provide a first plurality of control signals and a second plurality of control signals. The first plurality of control signals includes a first control signal. The second plurality of control signals includes a second control signal. The apparatus also includes a first differential output terminal. The apparatus also includes a second differential output terminal. The apparatus also includes an array of differential amplifiers including a first differential amplifier device and a second differential amplifier device, the first differential amplifier device and the second differential amplifier device may include a parallel input configuration and a parallel output configuration. The first differential amplifier device may include: a first input transistor may include a first gate and a first drain, the first gate being coupled to the first differential input terminal; a second input transistor may include a second gate and a second drain, the second gate being coupled to the second differential input terminal; a first output transistor coupled to the first

drain and the first control signal; a second output transistor
first control signal; a first auxiliary transistor may include a third gate and a third drain, the
third gate being coupled to the first differential input terminal, the third drain being coupled to
the second drain; a second auxiliary transistor may include a fourth gate and a fourth drain, the
5 fourth gate being coupled to the second differential input terminal, the fourth drain being
coupled to the first drain; and a third auxiliary transistor coupled to the first auxiliary transistor
and the second control signal.

[0023] In some examples, implementations may include one or more of the following
features. The first differential amplifier device further may include a fourth auxiliary transistor
10 coupled to the second auxiliary transistor and the second control signal. The third auxiliary
transistor may include a fifth drain and a fifth gate, the fifth gate being coupled to the second
control signal. The fifth drain is directly coupled to the first auxiliary transistor. The fifth drain
is directly coupled to the second auxiliary transistor. The driver amplifier apparatus may
include a fourth auxiliary transistor, the fourth auxiliary transistor may include a sixth drain
15 and a sixth gate, the sixth drain being directly coupled to the second auxiliary transistor, and
the sixth gate being coupled to the second control signal. The first output transistor is turned
off based on the first control signal, and the third auxiliary transistor is turned on based on the
second control signal. The first differential amplifier device is operated in an off mode with
phase correction. The control logic may include a look-up table for generating the first control
20 signal and the second control signal. The driver amplifier apparatus may include a feedback
loop path, the control logic being configured on the feedback loop path and coupled to the first
differential output terminal and the second differential output terminal. The first input
transistor is characterized by a first device area and the first auxiliary transistor is characterized
by a second device area. The second device area is no greater than 80% of the first device area.
25 Implementations of the described techniques may include hardware, a method or process, or
computer software on a computer-accessible medium.

[0024] In further embodiments, a driver amplifier is provided. The driver amplifier includes
a first differential input terminal. The apparatus also includes a second differential input
terminal. The apparatus also includes a first differential output terminal. The apparatus also
30 includes a second differential output terminal. The apparatus also includes an array of
differential amplifiers including a first differential amplifier device and a second differential
amplifier device, the first differential amplifier device and the second differential amplifier
device may include a parallel input configuration and a parallel output configuration. The first
differential amplifier device may include: a first input transistor may include a first gate and a

first drain and a first source, the first gate being coupled
a second input transistor may include a second gate and a second drain and a second source,
the second gate being coupled to the second differential input terminal; a first output transistor
may include a third gate and a third drain and a third source, the third source being coupled to
5 the first drain, and the third gate being coupled to a first control signal; a second output
transistor may include a fourth gate and a fourth drain and a fourth source, the fourth source
being coupled to the second drain, and the fourth gate being coupled to the first control signal;
a first auxiliary transistor may include a fifth gate and a fifth drain and a fifth source, the fifth
gate being coupled to the first differential input terminal, the fifth drain being coupled to the
10 second drain; a second auxiliary transistor may include a sixth gate and a sixth drain and a
sixth source, the sixth gate being coupled to the second differential input terminal, the sixth
drain being coupled to the first drain; and a third auxiliary transistor may include a seventh
gate and a seventh drain and a seventh source, the seventh drain being coupled to the sixth
source, the seventh gate being coupled to a second control signal.

15 [0025] In some examples, implementations may include one or more of the following
features. The seventh drain is coupled to the fifth source and the seventh source is grounded.
The driver amplifier apparatus may include a fourth auxiliary transistor. The fourth auxiliary
transistor may include an eighth gate and an eighth drain and an eighth source, the eighth drain
being coupled to the fifth source, the eighth gate being coupled to the second control signal,
20 and the eighth source being grounded. The driver amplifier apparatus may include a control
logic configured to generate the first control signal for turning on the first output transistor and
the second output transistor. The driver amplifier apparatus may include a control logic
configured to generate the second control signal for turning on the third auxiliary transistor.
Implementations of the described techniques may include hardware, a method or process, or
25 computer software on a computer-accessible medium.

[0026] In yet further embodiments, a driver amplifier apparatus is provided. The driver
amplifier apparatus includes a control logic is configured to provide either a first signal or a
second signal. The first signal includes an enabling binary signal. The second signal includes
a disabling binary signal. The apparatus also includes an array of N differential amplifier
30 devices, wherein N is an integer. Each differential amplifier device respectively includes an
amplifier unit having a first control terminal and an auxiliary unit having a second control
terminal. The amplifier unit is coupled to a parallel input configuration and a parallel output
configuration, and the auxiliary unit is coupled to the amplifier unit and the parallel input
configuration. The control logic is configured to set m differential amplifier devices in a first

state with the respective first control terminals being supplied with the first signal and the respective second control terminals being supplied with the second signal, and to set n differential amplifier devices in a second state with the respective first control terminals being supplied with the second signal and the respective second control terminals being supplied with the first signal, wherein $m + n \leq N, n \geq 1$.

[0027] In some examples, the amplifier unit includes a first input transistor coupled to a first differential input terminal coupled to the parallel input configuration. The amplifier unit also includes a second input transistor coupled to a second differential input terminal coupled to the parallel input configuration. The amplifier unit further includes a first output transistor coupled to the first input transistor, a first differential output terminal coupled to the parallel output configuration, and the first control terminal. The amplifier unit still includes a second output transistor coupled to the second input transistor, a second differential output terminal coupled to the parallel output configuration, and the first control terminal. The auxiliary unit includes a first auxiliary transistor coupled to the first differential input terminal and cross-coupled to the second input transistor. The auxiliary unit also includes a second auxiliary transistor coupled to the second differential input terminal and cross-coupled to the first input transistor. The auxiliary unit still includes a third auxiliary transistor coupled to the second control terminal and both the first auxiliary transistor and the second auxiliary transistor. Other embodiments of this aspect include corresponding computer systems, apparatus, and computer programs recorded on one or more computer storage devices, each configured to perform the actions of the methods.

[0028] In further examples, the control logic associated with the driver amplifier is configured to set k ($k < m$) differential amplifier devices in the first state and l ($l > n$) differential amplifier devices in the second state to enhance system power saving while maintaining a signal error-vector magnitude below a preset value. The control logic is configured to fix the number m of the m differential amplifier devices in the first state while only increasing the number n of the n differential amplifier devices in the second state to reduce phase distortion while lowering a signal error-vector magnitude at least by -4dB and maintaining a nearly constant amplifier gain. Implementations of the described techniques may include hardware, a method or process, or computer software on a computer-accessible medium.

[0029] Figure 1 is a simplified diagram illustrating a driver amplifier according to various embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of the ordinary skills in the art would recognize

many variations, alternatives, and modifications. In vari-

(DA) 103 has a pair of input terminals configured to receive a first input signal V_{ip} (i.e., input signal plus) at the first input terminal (+) and a second input signal V_{im} (i.e., input signal minus) at the second input terminal (-) from a source 102. For example, A difference between

5 the first input signal V_{ip} and the second input signal V_{im} forms a differential input $V_{ip} - V_{im}$. For example, the first input signal and the second input signal have opposite polarity. In the embodiment, the DA is configured as a differential amplifier device to amplify the differential inputs $V_{ip} - V_{im}$ to yield a differential output signal V_{out} with an amplifier gain. In some implementations, for example, the differential output signal can be converted to an output

10 signal at a single output terminal through an inductive coupling load. As described in further detail below, the DA 103 in Figure 1 includes several differential amplifiers (sometimes referred to as "slices") that are configured in parallel, and the number of differential amplifiers that are enabled determines the total amplifier gain of the DA 103. According to various embodiments, the amplifier gain may be variable under controls from two control signals, a

15 first control signal VCAS and a second control signal ENT, generated by a control module 101. For example, the VCAS signal and the ENT signal each include several bits, and each bit can be used to enable or disable a differential amplifier 103. In some embodiments, control module 101 is configured to flexibly use different combinations of the first control signal VCAS and the second control signal ENT to adjust DA 103 operations for gain change, noise

20 reduction, phase correction, or the like. In an embodiment, control module 101 includes a look-up table (LUT)—predetermined to satisfy various performance metrics of the DA—that is used to determine the combination of the two control signals. In some embodiments, the control module 101 is coupled to the output terminal via a feedback path 104 so that the control module 101 can generate the first and the second control signals according to the DA

25 103 performance metric measured in real-time. For example, the DA may be used for driving small signals in various RF applications, such as wireless communication systems (WiFi, Bluetooth, cellular, or the like), with flexibly adjusted gains and improved amplitude-to-phase (AM-PM) characteristics. Accordingly, the control module 101 may include, in various examples, control logic (such as a logic circuit, application specific integrated circuit (ASIC),

30 and/or programmable logic (e.g., a field programmable gate array)), and/or a controller, such as a microcontroller, processor, or other device configured to execute computer readable instructions and perform processes as described herein.

[0030] DAs according to embodiments of the present invention may be suitable for various purposes characterized by different loads, such as coaxial load, inductive coupling, and

35 resistance load, without specific limitation except that load matching is required for tuning

the amplifier gain. The advantages of the DA disclosed in the improvement of several performance metrics. On a system level, the DA may operate by setting the signal error-vector magnitude (EVM) below a certain threshold value with reduced AM-PM distortion. In various implementations, by optimizing circuitry design and control scheme selection, the DA also achieves operation power saving while maintaining gain control flexibility. In some specific embodiments, the DA includes an array of differential amplifier devices incorporated respectively with auxiliary switches. The control module associated with the DA is designed to provide the first control signal VCAS to turn on or off individual differential amplifier devices as well as the second control signal ENT to enable or disable the corresponding auxiliary switches for achieving improved phase correction and additional gain control flexibility. Implementations of the described techniques may include hardware, a method or process, or computer software on a computer-accessible medium. Further details of the DA circuit topology and control scheme are described with reference to Figure 2A and Figure 2B below.

[0031] Figure 2A is a simplified diagram illustrating an exemplary driver amplifier with an array of differential amplifiers according to various embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of the ordinary skills in the art would recognize many variations, alternatives, and modifications.

[0032] As shown, the driver amplifier (DA) is configured as an array of N cells, labeled as $\langle 1 \rangle, \dots, \langle N-1 \rangle$, and $\langle N \rangle$, arranged to have a parallel input configuration and a parallel output configuration. Each cell is configured as an independent differential amplifier device, optionally, with substantially the same topology including a pair of input transistors and a pair of output transistors plus several auxiliary transistors. It is understood that the N cells as shown with corresponding labels might be arranged in any order visually, not being limited to a serial order shown in Figure 2A. Using the first differential amplifier device $\langle 1 \rangle$ as an example, it is configured with a first control terminal 31 coupled to a control module to receive a first control signal VCAS and a second control terminal 32 coupled to the control module to receive a second control signal ENT respectively. The parallel input configuration, as arranged for individual cells, includes a first differential input terminal 11 configured to receive a first input signal V_{ip} and a second differential input terminal 12 configured to receive a second input signal V_{im} , providing a differential input signal $V_{ip}-V_{im}$. For example, V_{ip} and V_{im} have opposite polarities. In various embodiments, each differential amplifier device in the DA may receive the differential input signal with differential phases.

[0033] The first differential amplifier device <1>, as shown in Figure 2A, includes a first differential input terminal 11 and a second differential input terminal 12 respectively outputting a first output signal OP<1> (output "plus") and a second output signal OM<1> (output "minus"). The parallel output configuration of the DA allows each differential amplifier device to contribute the output of individual differential amplifier devices to yield a first output signal OP and a second output signal OM, resulting in a differential output signal OP-OM. Optionally, via an inductive coupling load, an output signal V_{out} on a single output terminal of the DA is obtained from the differential output signal OP-OM. With more differential amplifier devices in the DA being in use, output signal phase distortion may arise. As shown below in more detail, the control module (not explicitly shown in Figure 2A) associated with the DA disclosed herein is configured to implement an effective control scheme for reducing phase distortion. The control module can at least use the first control signal VCAS to control how many (*m*) differential amplifier devices are turned on among the array of *N* differential amplifier devices and use the second control signal ENT to enable a selected number (*n*) of auxiliary devices among the (*N-m*) turned-off differential amplifier devices to make the DA's system-level performance to be optimized in terms of several metrics like a minimum EVM, signal amplitude or phase distortion level, and amplifier gain level required for a certain load, or others.

[0034] In a specific embodiment, as illustrated in Figure 2A, the first differential amplifier device <1> includes a first input transistor 111 coupled to a first output transistor 113, and a second input transistor 112 coupled to a second output transistor 114. The first input transistor 111 has a gate terminal connected to the first differential input terminal 11, a drain terminal coupled to the first output transistor 113, and a source terminal grounded. The first output transistor 113 has a gate terminal connected to the first control terminal 31. The first output transistor 113 also includes a drain terminal connected to the first differential output terminal 21 and a source terminal connected to the drain terminal of the first input transistor 111. The second input transistor 112 includes a gate terminal connected to the second differential input terminal 12, a drain terminal connected to the second output transistor 114, and a source terminal grounded. The second output transistor 114 has a gate terminal connected to the first control terminal 31, a drain terminal connected to a second differential output terminal 22, and a source terminal connected to the drain terminal of the second input transistor 112. The gate terminal of the first input transistor 111 is connected to the first differential input terminal 11 that is supplied with a first input signal V_{ip}. The gate terminal of the second input transistor 112 is connected to the second differential input terminal 12 which is supplied with a second input signal V_{im}. The first control terminal 31 is supplied with a first control signal VCAS<1>

from the control module. The first control signal VCAS-
output transistor 113 and the second output transistor 114. Additionally, the first differential
amplifier device <1> includes a first auxiliary transistor 121 coupled to the second input
transistor 112 and a second auxiliary transistor 122 coupled to the first input transistor 111.
5 The first auxiliary transistor 121 includes a gate terminal connected to the first differential
input terminal 11 and a drain terminal connected to the drain terminal of the second input
transistor 112. The second auxiliary transistor 122 includes a gate terminal connected to the
second differential input terminal 12 and a drain terminal connected to the drain terminal of the
first input transistor 111. Furthermore, the first differential amplifier device <1> includes a
10 third auxiliary transistor 123 connected to the first input transistor 111 and the second control
terminal 32. Moreover, the first differential amplifier device <1> includes a fourth auxiliary
transistor 124 connected to the second input transistor 112 and the second control terminal 32.
Specifically, the gate terminal of the third auxiliary transistor 123 and the gate terminal of the
fourth auxiliary transistor 124 are both connected to the second control terminal 32 supplied
15 with a second control signal ENT<1> from the control module. The third auxiliary transistor
123 and the fourth auxiliary transistor 124 are served as auxiliary switches, which are
controlled by the second control signal ENT<1>, as an enabling signal, to switch on or off.
Optionally, the third auxiliary transistor 123 and the fourth auxiliary transistor 124 can be
implemented using a single auxiliary switch transistor.

20 [0035] As seen in Figure 2A, the gate terminal of the first auxiliary transistor 121 shares the
first differential input terminal 11 with the gate terminal of the first input transistor 111, and
the gate terminal of the second auxiliary transistor 122 shares the second differential input
terminal 12 with the gate terminal of the second input transistor 112. This topology provides a
source degeneration effect in the differential amplifier configuration, reduces the amplifier
25 gain, improves signal error tolerance, and enhances the linearity of the signal amplification. At
the same time, the auxiliary transistors 121 and 122—because their drain terminals are
crossover connected respectively with the drain terminal of the second input transistor 112 and
the drain terminal of the first input transistor 111—also provide a crossover effect to partially
cancel amplifier gain and to reduce non-linear capacitive noise from CGD coupling of
30 transistors. Auxiliary transistors 123 and 124 provide a switch function as their gate terminals
are connected to the second control terminal 32 and controlled by the control module (e.g.,
control logic) to use the second control signal ENT<1> to turn on or off the auxiliary switches.

[0036] As shown in Figure 2A, in various embodiments, all other N cells <2>, ..., <N-1>,
and <N> of the DA are configured in the same topology as the first differential amplifier

device <1>. In general, the first differential amplifier de
the DA and may not be the first one as shown in Figure 2A. All the N differential amplifier
devices of the DA have a parallel input configuration and a parallel output configuration. The
control module (e.g., the control module 101 in Figure 1) is configured to provide an array of
5 first control signals $VCAS<1>$, ..., $VCAS<N-1>$, and $VCAS<N>$ respectively to
corresponding first control terminal 31 of the array of differential amplifiers <1>, ..., <N-1>,
and <N> and also provide an array of second control signals $ENT<1>$, ..., $ENT<N-1>$, and
 $ENT<N>$ respectively to corresponding second control terminal 32 of the array of differential
amplifiers <1>, ..., <N-1>, and <N>. In various implementations, each of the N first control
10 signals or the N second control signals is a binary enabling signal.

[0037] In an embodiment, the DA is operated with the control module configured to
implement a control scheme for achieving certain system-level performance metrics. In the
control scheme, sub-array m cells of the N cells of the DA are selected to be turned on by
setting $VCAS = 1$, $ENT = 0$, and next sub-array $n = X - m$ ($X \leq N$) cells of the DA are set to
15 $VCAS = 0$, $ENT = 1$ while remaining cells are turned off by setting to $VCAS = 0$, $ENT = 0$. In
some embodiments, m is preferred to be as small as possible (i.e., let a minimum number of
cells of the DA be turned on) to save system power consumption while n is preferred to be a
larger value to minimize signal phase distortion and maintain the error-vector magnitude
(EVM) of the DA below a threshold (e.g., -40dB). Optionally, the control module (e.g., the
20 control logic) is configured to select m and n through a built-in look-up table based on various
performance metrics in applications, such as power saving, amplifier gain, gain required for
matching the load, signal amplitude or phase distortion, EVM, etc. The $ENT = 1$ setting for
the next sub-array n cells is particularly used for achieving signal phase control with these cells
being set in an off state by $VCAS = 0$. Any one of these cells with $ENT = 1$, compared to any
25 cell being set to $ENT = 0$, has additional auxiliary transistors enabled in crossover connections
between the differential input terminals and differential output terminals. Because of the cross-
coupling, the non-linear capacitance due to CGD coupling of transistors can be reduced. In an
example, the input capacitance variation is reduced from 17% to 6.9% for a single cell in an off
state. As a result, signal amplitude-to-phase distortion of the DA is reduced and
30 correspondingly the DA's performance is improved with an improved EVM. For the DA with
a sub-array of m differential amplifier devices being set to a first state by two control signals
 $VCAS = 1$, $ENT = 0$, and a sub-array of n differential amplifier devices being set to a second
state by two alternate control signals $VCAS = 0$, $ENT = 1$, the DA can be adjusted by tuning m
and n to perform its best for corresponding application, e.g., to turn on the least number of
35 differential amplifier devices to achieve an improved EVM under a required gain level. In

general, a larger value of m alone may result in a smaller restriction of $X - m$) with fixed m tends to yield a smaller EVM.

[0038] In another embodiment, the control module (e.g., control logic) can be configured to implement a control scheme for providing an additional level of gain control by taking advantage of source degeneration and crossover effects provided by the auxiliary transistors. For example, setting both control signals VCAS and ENT to 1 directly adds an auxiliary unit (consisting of all auxiliary transistors 121, 122, 123, 124 as shown in Figure 2A and a second control terminal 32) to an amplifier unit (consisting of all input transistors 111, 112 and output transistors 113, 114 as shown in Figure 2A and a first control terminal 31) in each differential amplifier device. The auxiliary unit contributes a negative gain on top of the positive gain given by the amplifier unit. Generally, the auxiliary transistors have a smaller device area, e.g., < 80%, than the input transistors. Thus, the negative gain may partially cancel the amplifier gain. By setting a state given by VCAS = 1 and ENT = 1, the gain level maintains a generally linear relationship with the number of differential amplifier devices in this state: the gain level increases corresponding to an increasing number of differential amplifier devices in such a state. By setting a state given by VCAS = 0 and ENT = 1, the gain level still can be affected by the increasing number of differential amplifier devices in DA in such a state, though the gain change may be negligibly small. As used herein, a device area may refer to the two-dimensional area of a substrate occupied by the component and/or device.

[0039] In various embodiments, the control module, implemented for the DA with k differential amplifiers, is configured to make a selection of a combination of the first control signal VCAS and the second control signal ENT out of 2^k bits of binary enabling signals for controlling each of the k differential amplifiers individually. In some alternative embodiments, the control module associated with the DA is configured to provide two signals: the first signal is set to 1 as an enabling signal, and the second signal is set to 0 as a disabling signal. The control module selects an array of m differential amplifier devices by sending the first signal 1 to the first control terminal of the amplifier units and the second signal 0 to the second control terminal of the corresponding auxiliary units. The array of m differential amplifier devices is set in a first state. The control module may also select an array of n differential amplifier devices, with the first control terminal of the amplifier units being supplied with the second signal 0 and the second control terminal of the auxiliary units being supplied with the first signal 1. The array of n differential amplifier devices is set in a second state. For example, the selection of an array of m or n differential amplifier devices in the first or second states may be based on a look-up table pre-stored in the control module. In another example, the section is

based on a feedback path formed between the control module and the DA, as illustrated in Figure 1. The feedback path allows the control module to receive a feedback signal about the DA's performance metric such as phase distortion, EVM, amplifier gain required for matching the load, etc. The control module may make some adjustments in the control signal setting for achieving optimization for the DA operation.

[0040] In Figure 2A, all transistors are shown as NMOS transistors. Yet, the differential amplifier device circuitry in the DA disclosed herein is also suitable for using PMOS transistors to achieve the same functions as claimed herein. In some embodiments, Bipolar junction transistors may be used instead. In various embodiments, the addition of the auxiliary transistors to each cell of the DA compared with conventional DA without using the auxiliary transistors does provide advantages in reducing signal phase distortion and improving EVM. It also allows a smaller number of cells to be turned on with substantially the same amplifier gain, which results in system power saving. Depending on the implementation, the number of transistor devices per cell may depend on the device area availability. For example, auxiliary transistors may be smaller than the main transistors (i.e., first and second input and output transistors) in each cell. Thus, a small device-area cost is always a goal of the DA design. For example, the size of the first auxiliary transistor 121 is implemented with an area that is 80% or smaller relative to that of the first input transistor 111. For the DA disclosed herein to operate in various small signal RF applications, the choice of the load has no limitation. For example, the load can be inductive coupling type, coaxial cable type, or other alternatives.

[0041] Figure 2B is a simplified diagram illustrating an alternative exemplary driver amplifier with an array of differential amplifiers according to various embodiments of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of the ordinary skills in the art would recognize many variations, alternatives, and modifications.

[0042] The driver amplifier (DA) shown in Figure 2B shares a similar topology as the DA shown in Figure 2A. It includes an array of N cells, labeled (1), ..., (N-1), and (N), arranged to have a parallel input configuration and a parallel output configuration. Individual cells (or sometimes referred to as "slices") are configured as a differential amplifier device with the same or substantially similar topology, where each includes a pair of input transistors and a pair of output transistors, plus auxiliary transistors. A pair of input transistors are respectively coupled to a first differential input terminal 11 and a second differential input terminal 12 coupled to the parallel input configuration of the DA. The pair of output transistors are respectively coupled to a first differential output terminal 21 and a second differential output

terminal 22 coupled to the parallel output configuration (e.g., the control module 101 in Figure 1) is coupled to a first control terminal 31 to provide a first control signal VCAS, and coupled to a second control terminal 32 to provide a second control signal ENT respectively for each cell. In various embodiments, the first differential input terminal 11 is configured to receive a first input signal V_{ip} and the second differential input terminal 12 is configured to receive a second input signal V_{im} , thereby the differential input signal being $V_{ip}-V_{im}$, where V_{ip} and V_{im} have opposite polarity. For each cell, the first differential output terminal 21 and the second differential output terminal 22 respectively output a first output signal OP(1) and a second output signal OM(1). The parallel output configuration of the DA allows each differential amplifier device to contribute an output of individual differential amplifier device to yield a first output signal OP and a second output signal OM, resulting in a differential output signal OP-OM of the DA. In an embodiment, the differential output signal is provided as an output signal V_{out} on a single output terminal through an inductive coupling load.

[0043] In a specific embodiment, the first differential amplifier device (1) includes a first input transistor 211 coupled to the first output transistor 213. The first input transistor 211 has a gate terminal that is connected to the first differential input terminal 11. The first input transistor 211 also has a drain terminal coupled to the first output transistor and a source terminal grounded. The first output transistor 213 has a gate terminal that is connected to the first control terminal 31. The first output transistor 213 also has a drain terminal that is connected to the first differential output terminal 21. The first output transistor 213 has a source terminal that is connected to the drain terminal of the first input transistor 211. Additionally, the first differential amplifier device (1) includes a second input transistor 212 coupled to a second output transistor 214. The second input transistor 212 includes a gate terminal connected to the second differential input terminal 22. The second input transistor 212 also has a drain terminal that is coupled to the second output transistor 214 and a source terminal grounded. The second output transistor 214 has a gate terminal that is connected to the first control terminal 31. The second output transistor 214 also has a drain terminal that is connected to a second differential output terminal 22 and a source terminal connected to the drain terminal of the second input transistor 212. The gate terminal of the first input transistor 211 is connected to the first differential input terminal 11 which is supplied with the first input signal V_{ip} . The gate terminal of the second input transistor 212 is connected to the second differential input terminal 12 which is supplied with the second input signal V_{im} . The first control terminal 31 is coupled to the first control signal VCAS(1) from the control module. The first control signal VCAS(1) is for turning on or off the first output transistor 201 and the

second output transistor 202. The two input transistors 2 serve as an amplifier unit controlled by the first control signal VCAS(1) via the first control terminal 31. The first differential amplifier device (1) further includes a first auxiliary transistor 221, a second auxiliary transistor 222, and a third auxiliary transistor 223. The first auxiliary transistor 211 includes a gate terminal that is connected to the first differential input terminal 11 and a drain terminal that is connected to the drain terminal of the second input transistor 212. The second auxiliary transistor 222 has a gate terminal that is connected to the second differential input terminal 12. The second auxiliary transistor 222 also has a drain terminal that is connected to the drain terminal of the first input transistor 211 and a source terminal that is shorted with a source terminal of the first auxiliary transistor 221. Furthermore, the third auxiliary transistor 223 has a gate terminal that is connected to the second control terminal 32. The third auxiliary transistor 223 also includes a drain terminal that is connected to both the source terminals of the first auxiliary transistor 221 and the second auxiliary transistor 212. The third auxiliary transistor 223 further includes a source terminal that is grounded. Specifically, the three auxiliary transistors form an auxiliary unit controlled by the second control signal ENT(1) via the second control terminal 32. Here no additional auxiliary transistor is used, saving more device space and reducing power consumption for operating the DA. Further, each auxiliary transistor is selected with a smaller (e.g., < 80%) device area than the input/output transistors.

20 [0044] In an alternative embodiment, the DA disclosed in Figure 2B can be viewed as an array of N differential amplifier devices with a parallel input configuration and a parallel output configuration. Each of the N differential amplifier devices comprises a first control terminal coupled to an amplifier unit and a second control terminal coupled to an auxiliary unit and is independently controlled by a control module to supply a first control signal and a second control signal via the first control terminal and the second control terminal. The amplifier unit consists of the first/second input transistors coupled to the first/second differential input terminals, and the first/second output transistors coupled to the first/output differential output terminals and gate-connected to the first control terminal. The auxiliary unit consists of all auxiliary transistors cross-connected to the first/second input transistors and coupled to the second control terminal. The control module can determine to set the first control signal to an enabling binary signal and the second control signal to a disabling binary signal. Thus, the amplifier unit and the auxiliary unit of each of the array of N differential amplifier devices may be turned on or off depending on the system-level performance requirements of the DA.

[0045] In an embodiment, the DA disclosed in Figure 1 is being configured to implement a control scheme for achieving certain system-level performance metrics. The control scheme is designed for controlling signal phase shift such that the resulted EVM can be kept under a threshold value by turning on the amplifier unit in each of a smaller number of m cells in the DA with the corresponding auxiliary unit being switched off in those cells. At the same time, the control module enables the auxiliary unit in each of the proper number of $n = (X-m)$ cells in the DA without turning on the corresponding amplifier unit in each of those cells. In some other embodiments, an alternative control scheme is implemented to simply reduce the phase distortion to yield a lower EVM by fixing a sub-array of m cells with each amplifier unit being enabled and auxiliary unit disabled, and by increasing the number n of a sub-array of n cells with each amplifier unit being disabled and auxiliary unit enabled. Of course, other control schemes may also be implemented with this DA design according to the present disclosure.

[0046] Figure 3 is a simplified graph showing the performance of the driver amplifier according to various embodiments of the present invention using gain variation, phase shifting, and error-vector magnitude measurement. These graphs are merely examples, which should not unduly limit the scope of the claims. One of the ordinary skills in the art would recognize many variations, alternatives, and modifications. The driver amplifier (DA) referred to in Figure 3 can be the DA described in Figure 2A or Figure 2B and is operated under control by a control module in various control schemes. Various performance metrics or advantages are demonstrated in some embodiments of the DA configured with an array of 64 differential amplifier devices (like the one shown in Figure 2A or Figure 2B) and the control module configured to provide a first control signal VCAS to either 1 or 0 and a second control signal ENT to either 0 or 1. In pa, the DA used in Figure 3 has m differential amplifier devices being set in a first state defined by supplying the first control signal CAS = 1 to respective amplifier units and the second control signal ENT = 0 to respective auxiliary units, and has $n = 63 - m$ differential amplifier devices being set in a second state defined by supplying the first control signal VCAS = 0 to respective amplifier units and the second control signal ENT = 1 to respective auxiliary units.

[0047] As shown, the top graph shows a relationship between the amplifier gain of the driver amplifier and the number m of the differential amplifier devices in the first state (while having $n = 63 - m$ differential amplifier devices in the second state. Here, as m varies from 24 to 48 ($n = 63 - m$) the amplifier gain increases almost linearly from 12.87 dB to 22.27 dB for driving a small signal (with Pout ranging from -20dBm or less up to 10 dBm or more). When m

becomes lower than such as 36 down to 24, the gain line:

auxiliary unit in each differential amplifier device in the DA, the DA has nearly the same AMAM performance, compared with conventional driver amplifiers without using the auxiliary transistors.

5 [0048] The middle graph of Figure 3 shows a measurement of error-vector magnitude (EVM) at $P_{out} = 6.0$ dBm. As m decreases over 32 down to 28, EVM starts to crossover the -40 dB mark. Generally, a higher EVM means a poorer Amplitude-to-Phase (AM-PM) behavior of the driver amplifier. A certain value of EVM is generally set, such as -40dB, as a performance metric required for the driver amplifier in use. The middle graph shows that the
 10 DA disclosed herein can allow only 30 in the array of 64 differential amplifier devices to be turned on to make the EVM under -40dB. This is improved compared with a typical performance of a conventional driver amplifier with multi-sliced differential amplifiers which requires at least 36 differential amplifiers to be turned on. Less number of turned-on differential amplifiers results in less system power consumption. The DC current at P_{out} 6dBm
 15 can be reduced from 34.9mA to 30mA comparing the DA disclosed herein with the conventional design. The DC current without signal is also reduced by 16%. Additionally, with the same number, e.g., 36, of turned-on unit cells in the DA, AM-PM behavior is also improved. This suggests a control scheme to allow the control module to select a smaller number k ($k < m$) of the k differential amplifier devices set in the first state by $VCAS = 1$,
 20 $ENT = 0$ in the DA, and select a larger number l ($l > n$) of the l differential amplifier devices set in the second state by $VCAS = 0$, $ENT = 1$, such that the system power saving is enhanced while the signal error-vector magnitude still being maintained below the desired level.

[0049] The AM-PM behavior of the driver amplifier can be directly reflected from the phase peaking point shift due to different settings of the driver amplifier. The bottom graph of Figure
 25 3 just shows a plot of the phase (deg) versus P_{out} for varying m from 24, 28, ..., 44, to 48 (and $n = 63 - m$). It shows that the phase peak shifts lower and lower from 3.36 deg down to 0.058 deg. For $m = 36$, the phase peak is 1.2 deg, which is significantly lower than 5.4 deg obtained by the conventional DA with 36 turned-on sliced differential amplifiers but without the auxiliary units in design. The reduction of phase peaking directly results in an improved, i.e.,
 30 lowered error-vector magnitude. This indicates that the DA design and the associated control scheme disclosed herein are particularly advantageous for the AM-PM improvement over the conventional DA in various RF applications.

[0050] The data shown in Figure 3 is merely showing a DA with 64 sliced differential amplifiers and only an isolated few settings for m turned-on cells. But, the performance of the

DA with a larger number, e.g., 128 or others, cells and th
out of the 128 cells in the DA, similar or more advantageous performance metrics can be
presented and covered by the claims of this disclosure.

[0051] Figure 4 is a simplified graph showing the performance of the driver amplifier
5 according to alternative embodiments of the present invention using gain and phase control and
error-vector magnitude measurement. These graphs are merely examples, which should not
unduly limit the scope of the claims. One of the ordinary skills in the art would recognize
many variations, alternatives, and modifications. The driver amplifier (DA) referred to in
Figure 4 can be the DA described in Figure 2A or Figure 2B and is operated under control by a
10 control module in an alternative control scheme. Again, the DA is configured with an array of
64 differential amplifier devices, each differential amplifier device including an amplifier unit
having a first control terminal and an auxiliary unit having a second control terminal. The
amplifier unit is coupled to a parallel input configuration and a parallel output configuration,
and the auxiliary unit is coupled to the amplifier unit and the parallel input configuration. A
15 control module associated with the DA is configured to provide a first signal "1" as an enabling
signal and a second signal "0" as a disabling signal. In particular, the DA used for
measurements shown in Figure 4 has m differential amplifier devices being set in a first state,
i.e., an on state, with respective amplifier units being enabled by supplying the first signal "1"
and the respective auxiliary units being disabled by supplying the second signal "0", and has n
20 $= 63 - m$ differential amplifier devices being set in a second state, i.e., an off state, with
respective amplifier units being disabled by supplying the second signal "0" while respective
auxiliary units being enabled by supplying the first signal "1". In particular, Figure 4 shows
various measurement results of the DA with m being fixed to 40 while n varying from 0, 2, 4,
...,20, to 22.

25 [0052] As shown in Figure 4, the top graph shows amplifier gain variation as n varies from 0
to 22. The result indicates that the amplifier gain is nearly constant with just 0.1dB variation.
As long as the number m is fixed for the sub-array of m differential amplifier devices in the
first state, the amplifier gain of the DA is almost not affected by how many remaining
differential amplifier devices in the second state, Auxiliary unit does contribute a negative
30 gain with the crossover connection with the amplifier unit but it is disabled in the first state.
However, enabling the auxiliary units in the sub-array of n differential amplifier devices,
though not causing AMAM change, does help improve the AM-PM behavior of the DA
disclosed herein under the above control scheme.

[0053] The middle graph of Figure 4 shows the AM-PM control scheme using error-vector magnitude (EVM) measurement. With m fixed to 40, EVM is measured at a condition of operating the DA to have a P_{out} at 6dBm for n varying from 0, 2, ..., to 22. The result shows that by increasing the number n of the n differential amplifier devices in the second state alone, about -4dB of EVM improvement can be obtained. Lower EVM means less signal phase distortion in the DA. This demonstrates one of the advantages of the DA disclosed herein under the alternative control scheme.

[0054] The EVM improvement is directly a result of improved AM-PM performance of the DA under this operation control scheme. As shown in the bottom graph of Figure 4, the AM-PM improvement is demonstrated by phase peaking shift with the changing number n of the n differential amplifier devices in the DA. In the graph, the signal output phase (deg) of the DA is plotted against the output power P_{out} . Multiple curves respectively for n varying from 0 to 22 are plotted in the same graph with non-linear phase peaking shifts near the high-power end. When n increases from 0 to 22, the phase peak drops monotonically from about 3.7 deg to 0.7 deg. In fact, by adding a single differential amplifier device in the off state in the DA, the input capacitance variation is reduced from 17% to 6.9 %, serving as the main cause for the reduction of phase distortion. In other words, the non-linear phase distortion of the DA output can be reduced by fixing the number of cells in the on state while only increasing the number of cells in the off state under the operation control scheme.

[0055] While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. A driver amplifier apparatus comprising:
a first differential input terminal;
a second differential input terminal;
a control logic configured to provide a first plurality of control signals and a second plurality of control signals, the first plurality of control signals including a first control signal, the second plurality of control signals including a second control signal;
a first differential output terminal;
a second differential output terminal; and
an array of differential amplifiers including a first differential amplifier device and a second differential amplifier device, the first differential amplifier device and the second differential amplifier device comprising a parallel input configuration and a parallel output configuration;

wherein the first differential amplifier device comprises:

a first input transistor comprising a first gate and a first drain, the first gate being coupled to the first differential input terminal;
a second input transistor comprising a second gate and a second drain, the second gate being coupled to the second differential input terminal;
a first output transistor coupled to the first drain and the first control signal;
a second output transistor coupled to the second drain and the first control signal;
a first auxiliary transistor comprising a third gate and a third drain, the third gate being coupled to the first differential input terminal, the third drain being coupled to the second drain;
a second auxiliary transistor comprising a fourth gate and a fourth drain, the fourth gate being coupled to the second differential input terminal, the fourth drain being coupled to the first drain; and
a third auxiliary transistor coupled to the first auxiliary transistor and the second control signal.

2. The driver amplifier apparatus of claim 1 wherein the first differential amplifier device further comprises a fourth auxiliary transistor coupled to the second auxiliary transistor and the second control signal.

3. The driver amplifier apparatus of claim 1 wherein the third auxiliary transistor comprises a fifth drain and a fifth gate, the fifth gate being coupled to the second control signal.
4. The driver amplifier apparatus of claim 3 wherein the fifth drain is directly coupled to the first auxiliary transistor.
5. The driver amplifier apparatus of claim 4 wherein the fifth drain is directly coupled to the second auxiliary transistor.
6. The driver amplifier apparatus of claim 4 further comprising a fourth auxiliary transistor, the fourth auxiliary transistor comprising a sixth drain and a sixth gate, the sixth drain being directly coupled to the second auxiliary transistor, the sixth gate being coupled to the second control signal.
7. The driver amplifier apparatus of claim 1 wherein the first output transistor is turned off based on the first control signal, and the third auxiliary transistor is turned on based on the second control signal, the first differential amplifier device operating in an off mode with phase correction.
8. The driver amplifier apparatus of claim 1 wherein the control logic comprises a look-up table for generating the first control signal and the second control signal.
9. The driver amplifier apparatus of claim 1 further comprising a feedback loop path, the control logic being configured on the feedback loop path and coupled to the first differential output terminal and the second differential output terminal.
10. The driver amplifier apparatus of claim 1 wherein the first input transistor is configured to occupy a first device area and the first auxiliary transistor is configured to occupy a second device area, the second device area being no greater than 80% of the first device area.
11. A driver amplifier comprising:
 - a first differential input terminal;
 - a second differential input terminal;
 - a first differential output terminal;
 - a second differential output terminal; and

an array of differential amplifiers including
and a second differential amplifier device, the first differential amplifier device and the second differential amplifier device comprising a parallel input configuration and a parallel output configuration;

wherein the first differential amplifier device comprises:

a first input transistor comprising a first gate and a first drain and a first source, the first gate being coupled to the first differential input terminal;

a second input transistor comprising a second gate and a second drain and a second source, the second gate being coupled to the second differential input terminal;

a first output transistor comprising a third gate and a third drain and a third source, the third source being coupled to the first drain, and the third gate being coupled to a first control signal;

a second output transistor comprising a fourth gate and a fourth drain and a fourth source, the fourth source being coupled to the second drain, and the fourth gate being coupled to the first control signal;

a first auxiliary transistor comprising a fifth gate and a fifth drain and a fifth source, the fifth gate being coupled to the first differential input terminal, the fifth drain being coupled to the second drain;

a second auxiliary transistor comprising a sixth gate and a sixth drain and a sixth source, the sixth gate being coupled to the second differential input terminal, the sixth drain being coupled to the first drain; and

a third auxiliary transistor comprising a seventh gate and a seventh drain and a seventh source, the seventh drain being coupled to the sixth source, the seventh gate being coupled to a second control signal.

12. The driver amplifier apparatus of claim 11 wherein the seventh drain is coupled to the fifth source and the seventh source is grounded.

13. The driver amplifier apparatus of claim 11 further comprising a fourth auxiliary transistor comprising an eighth gate and an eighth drain and an eighth source, the eighth drain being coupled to the fifth source, the eighth gate being coupled to the second control signal, the eighth source being grounded.

14. The driver amplifier apparatus of claim 11 further comprising a control logic configured to generate the first control signal for turning on the first output transistor and the second output transistor.

15. The driver amplifier apparatus of claim 11 further comprising a control logic configured to generate the first control signal for turning off the first output transistor and the second output transistor and generate the second control signal for turning on the third auxiliary transistor.

16. A driver amplifier apparatus comprising:

a control logic configured to provide either a first signal or a second signal, the first signal comprising an enabling binary signal, the second signals comprising a disabling binary signal; and

an array of N differential amplifier devices, wherein N is an integer, each of the N differential amplifier devices respectively comprising an amplifier unit having a first control terminal and an auxiliary unit having a second control terminal, the amplifier unit being coupled to a parallel input configuration and a parallel output configuration, and the auxiliary unit being coupled to the amplifier unit and the parallel input configuration;

wherein the array of N differential amplifier devices and the control logic are configured to set m differential amplifier devices in a first state with the respective first control terminals being supplied with the first signal and the respective second control terminals being supplied with the second signal, and to set n differential amplifier devices in a second state with the respective first control terminals being supplied with the second signal and the respective second control terminals being supplied with the first signal, wherein $m + n \leq N$, $n \geq 1$.

17. The driver amplifier apparatus of claim 16 wherein the amplifier unit comprises:

a first input transistor coupled to a first differential input terminal coupled to the parallel input configuration;

a second input transistor coupled to a second differential input terminal coupled to the parallel input configuration;

a first output transistor coupled to the first input transistor, a first differential output terminal coupled to the parallel output configuration, and the first control terminal;

a second output transistor coupled to the second input transistor, a second differential output terminal coupled to the parallel output configuration, and the first control terminal.

18. The driver amplifier apparatus of claim 16 comprises:
- a first auxiliary transistor coupled to the first differential input terminal and cross-coupled to the second input transistor;
 - a second auxiliary transistor coupled to the second differential input terminal and cross-coupled to the first input transistor, and
 - a third auxiliary transistor coupled to the second control terminal and both the first auxiliary transistor and the second auxiliary transistor.
19. The driver amplifier apparatus of claim 16 wherein the control logic is configured to set k ($k < m$) differential amplifier devices in the first state and l ($l > n$) differential amplifier devices in the second state to enhance system power saving while maintaining a signal error-vector magnitude below a preset value.
20. The driver amplifier apparatus of claim 16 wherein the control logic is configured to fix the number m of the m differential amplifier devices in the first state while only increasing the number n of the n differential amplifier devices in the second state to reduce phase distortion while lowering a signal error-vector magnitude at least by -4dB and maintaining a nearly constant amplifier gain.

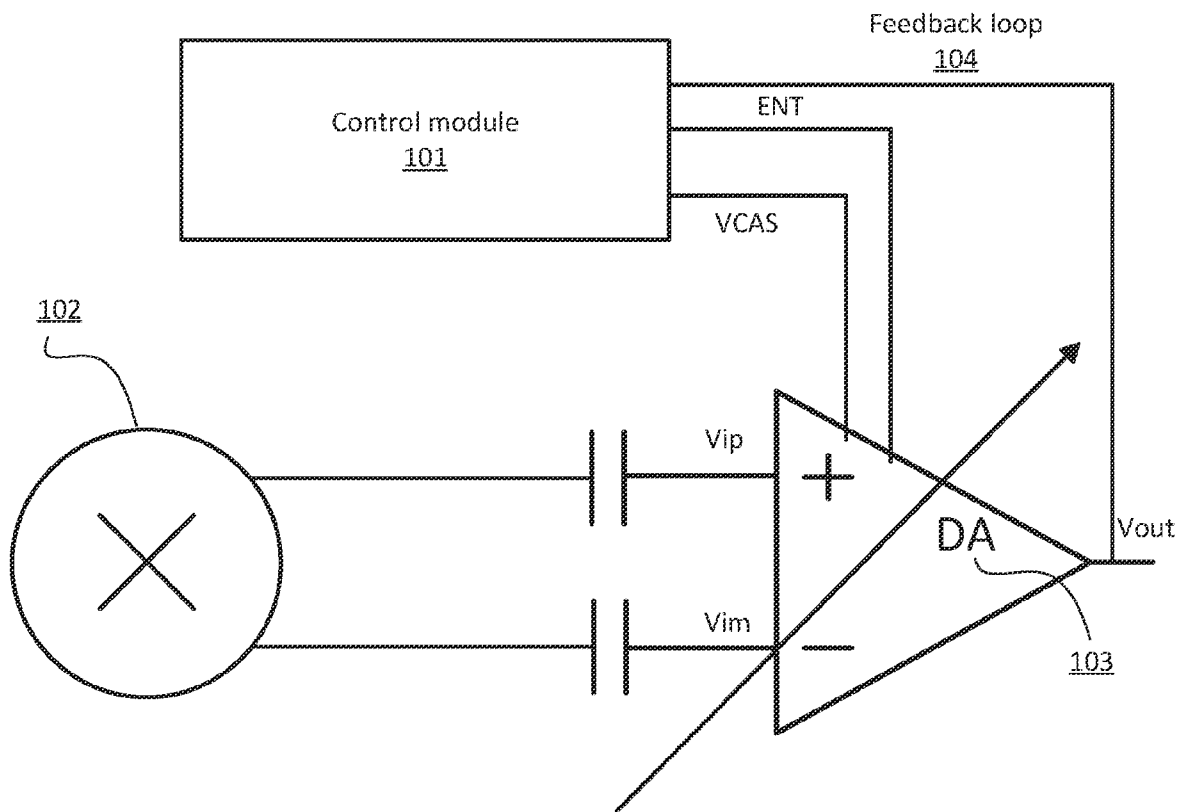
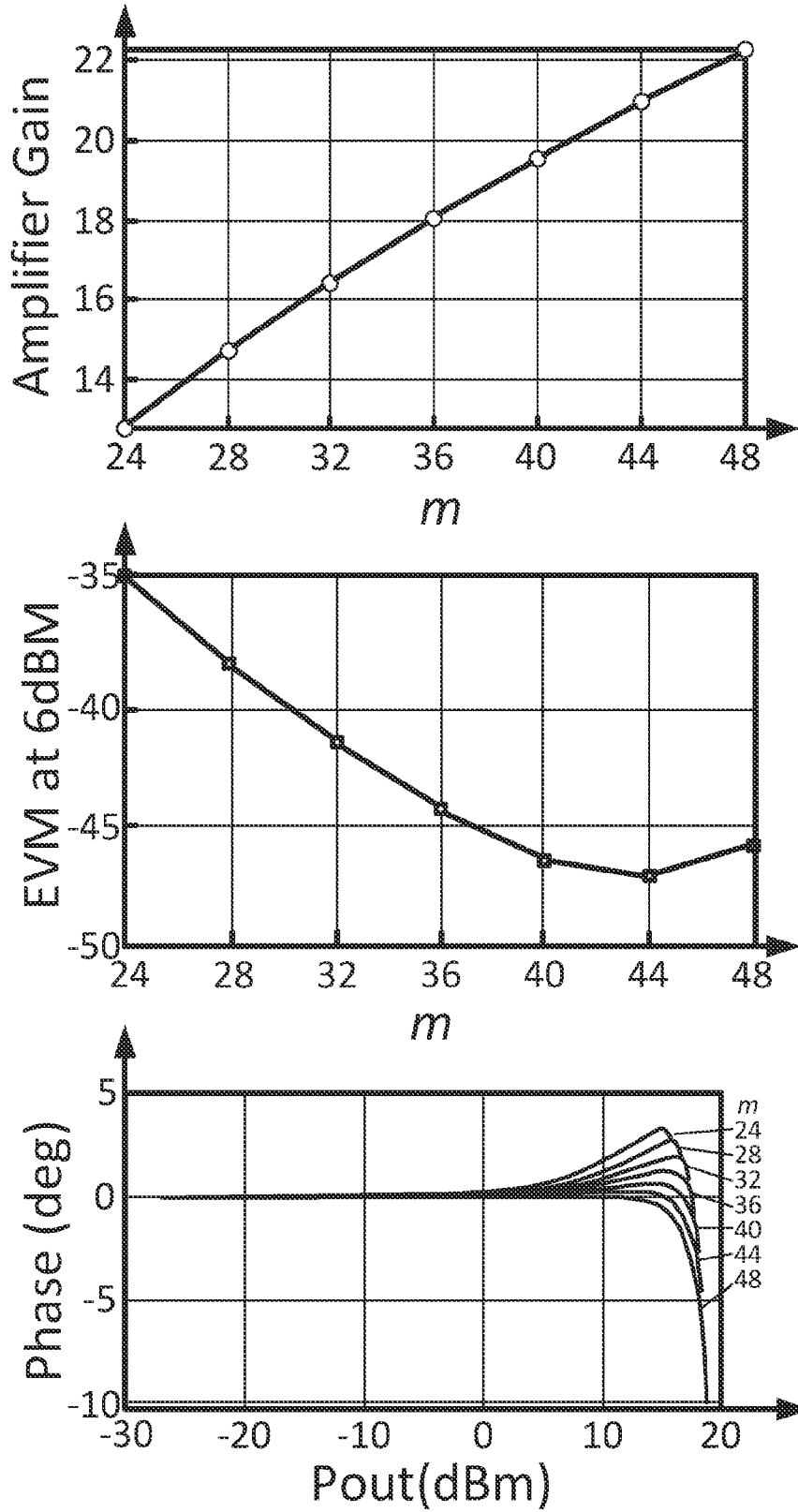
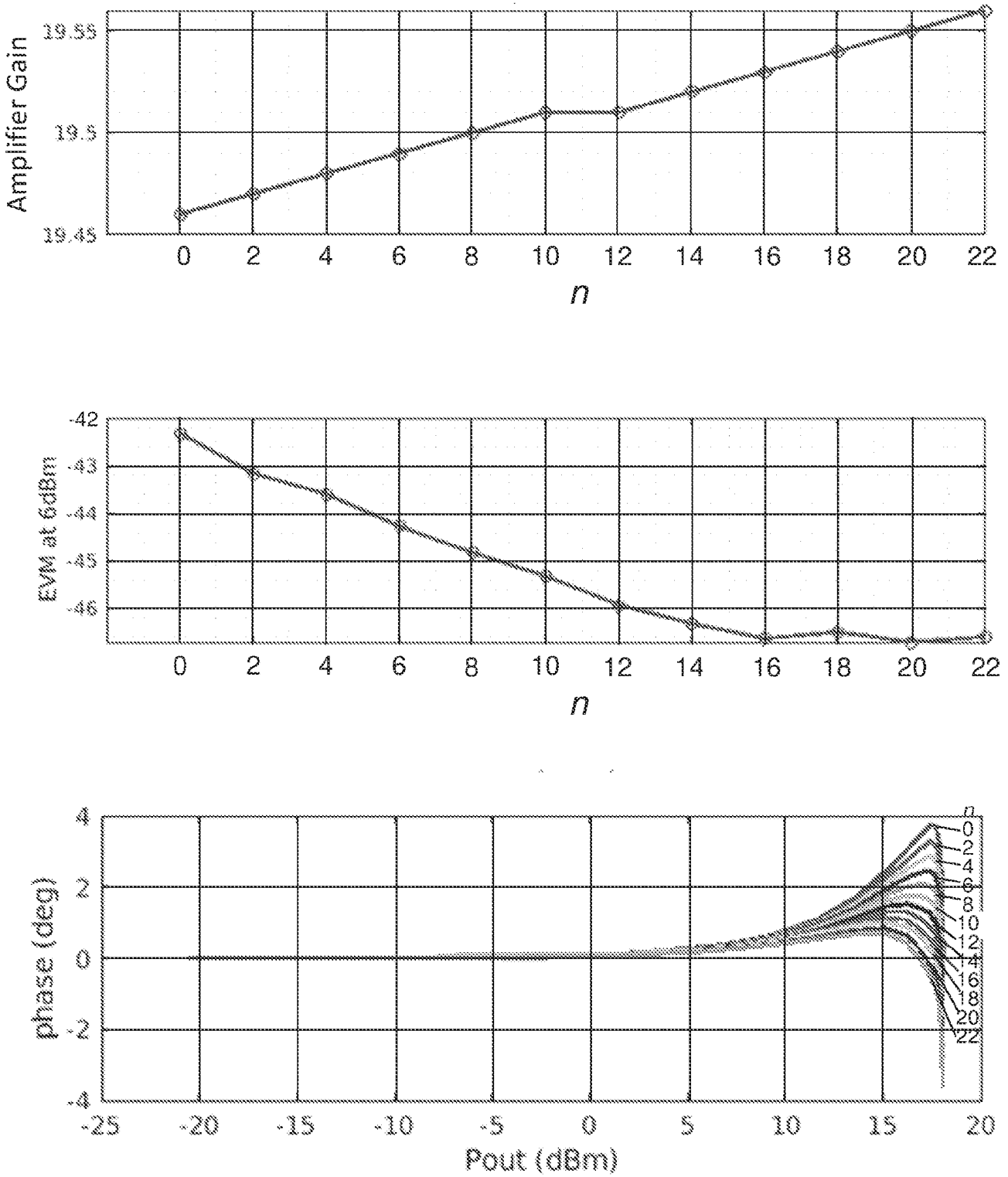


Figure 1



Array of 64 differential amplifiers, $n = 63 - m$

Figure 3



Array of 64 differential amplifiers, $m = 40$, $n = 0, 2, \dots, 22$

Figure 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US22/42922

<p>A. CLASSIFICATION OF SUBJECT MATTER</p> <p>IPC - INV. H03F 3/21; H03F 3/45 (2022.01) ADD. H03F 3/68 (2022.01)</p> <p>CPC - INV. H03F 3/211; H03F 3/45 ADD. H03F 3/68</p> <p>According to International Patent Classification (IPC) or to both national classification and IPC</p>																
<p>B. FIELDS SEARCHED</p> <p>Minimum documentation searched (classification system followed by classification symbols) See Search History document</p> <p>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched See Search History document</p> <p>Electronic database consulted during the international search (name of database and, where practicable, search terms used) See Search History document</p>																
<p>C. DOCUMENTS CONSIDERED TO BE RELEVANT</p> <table border="1"> <thead> <tr> <th>Category*</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>US 2005/0237109 A1 (LALETIN, W) 27 October 2005; paragraphs [0034], [0036] and [0037]</td> <td>1-15</td> </tr> <tr> <td>A</td> <td>US 6,111,468 A (TANISHIMA, H) 29 August 2000; see claims 7-9 and column 1 lines 59-67, column 2 lines 1-7, column 14 lines 62-67, column 15 lines 1-6, column 16 lines 39-47 and 6-67, column 17 lines 1-15, column 21 lines 66-67 and column 22 lines 1-18</td> <td>1-15</td> </tr> <tr> <td>A</td> <td>RU 2439780 C1 (G OBRAZOVATEL NOE UCHREZHDENIE VYSSHEGO PROFESSIONAL NOGO OBRAZOVANIJA JUZHNO ROSSIJSKIJ GU EHKONOMI) 10 January 2012; see claim 1 of the machine translation</td> <td>1-15</td> </tr> <tr> <td>A</td> <td>KR 19990071368 A (FUJITSU CO., LTD.) 27 September 1999; See entire document</td> <td>1-15</td> </tr> </tbody> </table>		Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	A	US 2005/0237109 A1 (LALETIN, W) 27 October 2005; paragraphs [0034], [0036] and [0037]	1-15	A	US 6,111,468 A (TANISHIMA, H) 29 August 2000; see claims 7-9 and column 1 lines 59-67, column 2 lines 1-7, column 14 lines 62-67, column 15 lines 1-6, column 16 lines 39-47 and 6-67, column 17 lines 1-15, column 21 lines 66-67 and column 22 lines 1-18	1-15	A	RU 2439780 C1 (G OBRAZOVATEL NOE UCHREZHDENIE VYSSHEGO PROFESSIONAL NOGO OBRAZOVANIJA JUZHNO ROSSIJSKIJ GU EHKONOMI) 10 January 2012; see claim 1 of the machine translation	1-15	A	KR 19990071368 A (FUJITSU CO., LTD.) 27 September 1999; See entire document	1-15
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<p><input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.</p>																
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<p>Date of the actual completion of the international search</p> <p>30 November 2022 (30.11.2022)</p>	<p>Date of mailing of the international search report</p> <p>FEB 14 2023</p>															
<p>Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300</p>	<p>Authorized officer</p> <p>Shane Thomas</p> <p>Telephone No. PCT Helpdesk: 571-272-4300</p>															

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US22/42922

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
-***-Please See Supplemental Page-***-

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-15

Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

-***-Continued From Box No. III: Observations where unity of invention is lacking-***-

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-15 are directed towards a driver amplifier comprising a first input transistor.

Group II: Claims 16-20 are directed towards a driver amplifier apparatus.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

The special technical features of Group I include at least wherein the first differential amplifier device comprises: a first input transistor comprising a first gate and a first drain, the first gate being coupled to the first differential input terminal; a second input transistor comprising a second gate and a second drain, the second gate being coupled to the second differential input terminal; a first output transistor coupled to the first drain and the first control signal; a second output transistor coupled to the second drain and the first control signal; a first auxiliary transistor comprising a third gate and a third drain, the third gate being coupled to the first differential input terminal, the third drain being coupled to the second drain; a second auxiliary transistor comprising a fourth gate and a fourth drain, the fourth gate being coupled to the second differential input terminal the fourth drain being coupled to the first drain; and a third auxiliary transistor coupled to the first auxiliary transistor and the second control signal, which are not present in Group II.

The special technical features of Group II include at least wherein the array of N differential amplifier devices and the control logic are configured to set m differential amplifier devices in a first state with the respective first control terminals being supplied with the first signal and the respective second control terminals being supplied with the second signal, and to set n differential amplifier devices in a second state with the respective first control terminals being supplied with the second signal and the respective second control terminals being supplied with the first signal, wherein $m + n \leq N$, $n \geq 1$, which are not present in Group I.

The common technical features shared by Groups I-II are a driver amplifier apparatus comprising: a control logic configured to provide either a first signal or a second signal, an array of N differential amplifier devices, wherein N is an integer, each of the N differential amplifier devices respectively comprising an amplifier unit having a first control terminal and an auxiliary unit having a second control terminal, the amplifier unit being coupled to a parallel input configuration and a parallel output configuration.

However, these common features are previously disclosed by US 2005/0237109 A1 to Laletin. Laletin discloses a driver amplifier apparatus comprising: a control logic configured to provide either a first signal or a second signal, an array of N differential amplifier devices, wherein N is an integer (a plurality of driver amplifiers, each equipped with a small valued resistor in series with its output, are configured in a parallel array controlled by a global control signal. Each of the slave amplifiers is accompanied by a servo integrator amplifier that forces the slave amplifier's output voltage to track the output voltage of the designated master amplifier over a limited range of frequencies that includes D, Para. 18), each of the N differential amplifier devices respectively comprising an amplifier unit having a first control terminal and an auxiliary unit having a second control terminal (Differential amplifier 400 operates as a servo integrator means, to force the output voltage of slave amplifier 300 to track the output voltage of master amplifier 200, in the following manner. The non-inverting input 406 of servo amplifier 400 is connected through optional resistor 401 to the output 208 of amplifier 200, while the inverting input 407 of amplifier 400 is connected through optional resistor 403 to output 306 of amplifier 300. Thence, output 408 of amplifier 400 is connected to resistor 302 to convey feedback to amplifier 300, Para. 47), the amplifier unit being coupled to a parallel input configuration and a parallel output configuration (Output 108 is the controlling signal for parallel amplifier array 500, which is configured for a non-inverting transfer function. In the conventional manner, resistor 102 is connected between non-inverting input 106 and local ground 600, while resistor 104 completes the negative feedback connection between output 500 and inverting input 107, Para. 63).

Since the common technical features are previously disclosed by the Laletin reference, these common features are not special and so Groups I-II lack unity.