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(54) Title of the Invention: **A Pixel**

Abstract Title: **Reading a pixel by increasing the reset input, source follower, transfer gate or charge transfer node voltages**

(57) A pixel arrangement and method of use, comprising a photodiode 12, a reset transistor 18 controlled by a reset input voltage RST, a transfer gate transistor 14 controlled by a transfer gate voltage TG, configured to transfer charge from the photodiode to a charge transfer node (SN) 22 when in use and a source follower transistor 16 controlled by the node voltage and coupled to a source follower voltage when in use. During a read operation, at least one identified voltage is increased, the identified voltage being a reset input voltage, source follower voltage, transfer gate voltage or transfer charge node voltage. Further a read transistor 20 may be included, controlled during reading by a read voltage set to a read value, which may have a time period exceeding the period during which the identified voltage is increased. Preferably, during the read operation, the transfer gate voltage signal is changed from a lower first voltage level to an intermediate voltage level and then from the intermediate voltage to a second higher voltage. The reverse may also occur, for example, second, intermediate first voltage sequence. The reset signal may be pulsed at the beginning of the read operation and at the same time as the read voltage is set to the read value. A capacitor 32 coupled to the charge transfer node may be configured to increase the voltage on the node during a read.

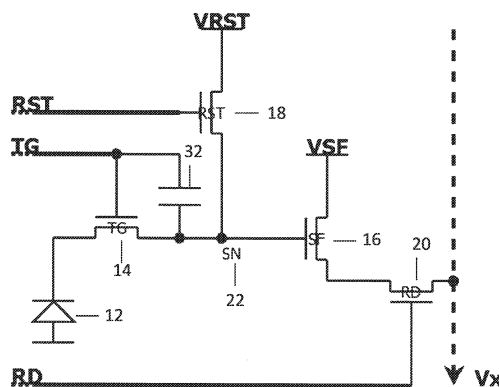


Figure 9

Figure 1

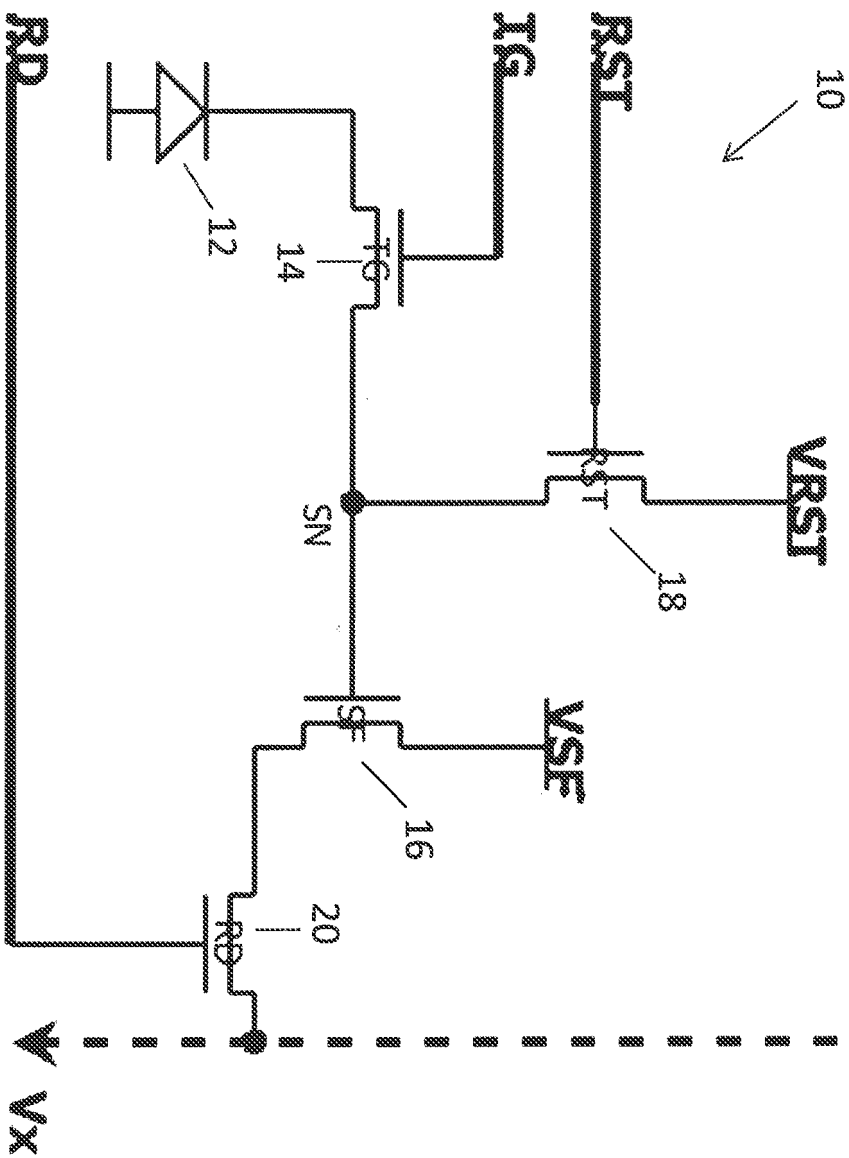


Figure 2

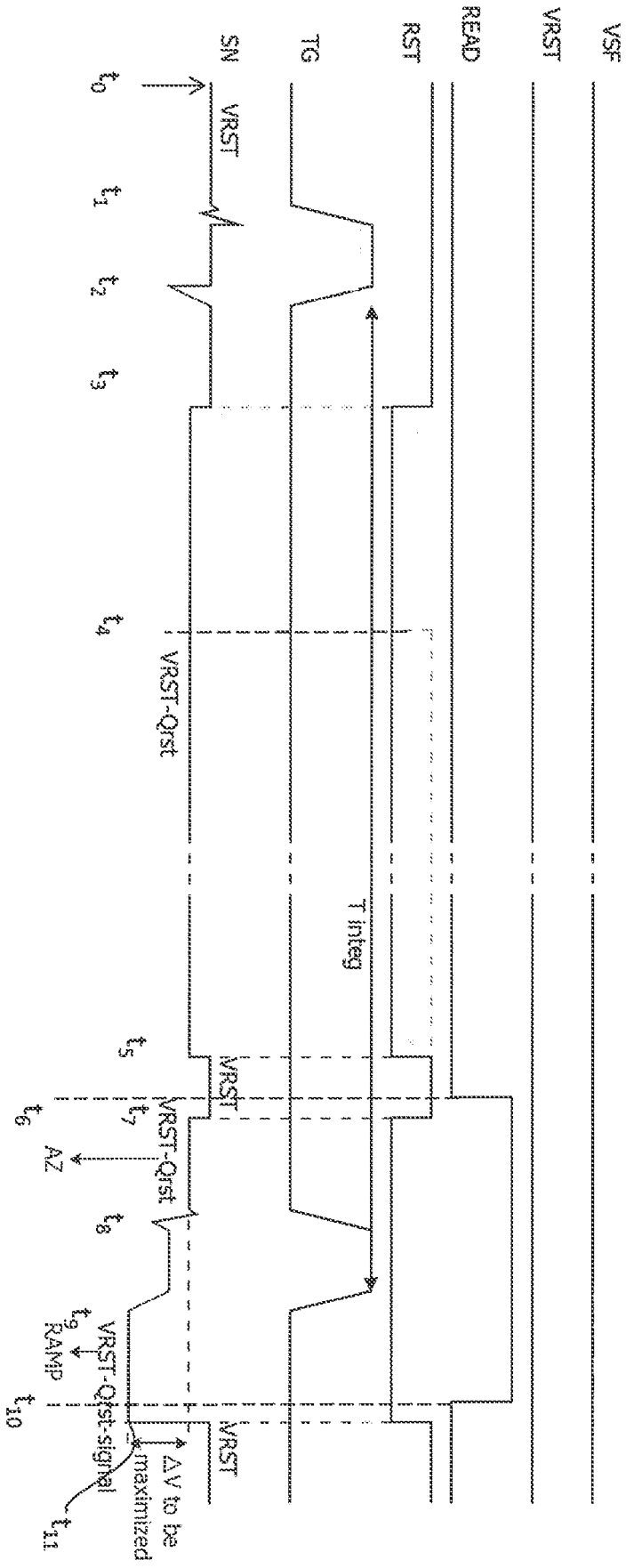


Figure 4

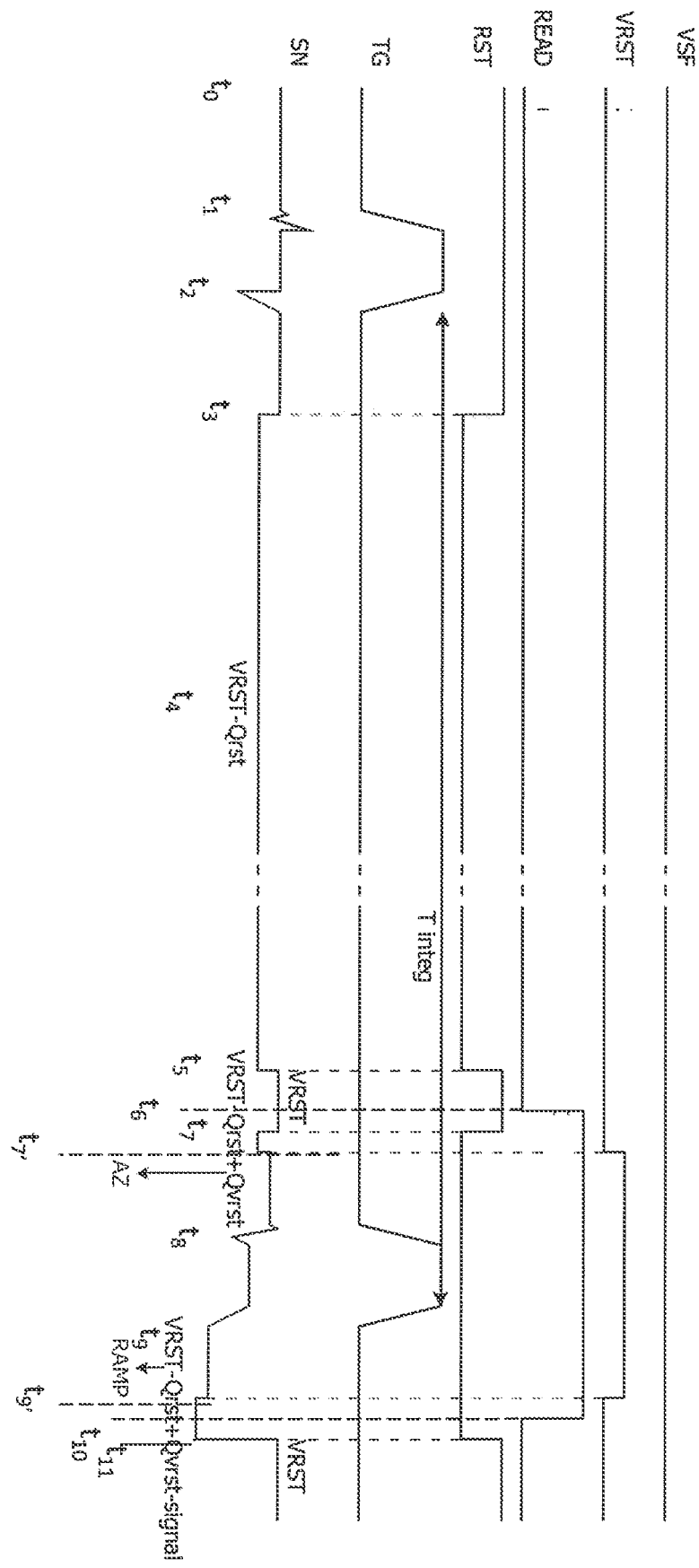


Figure 5

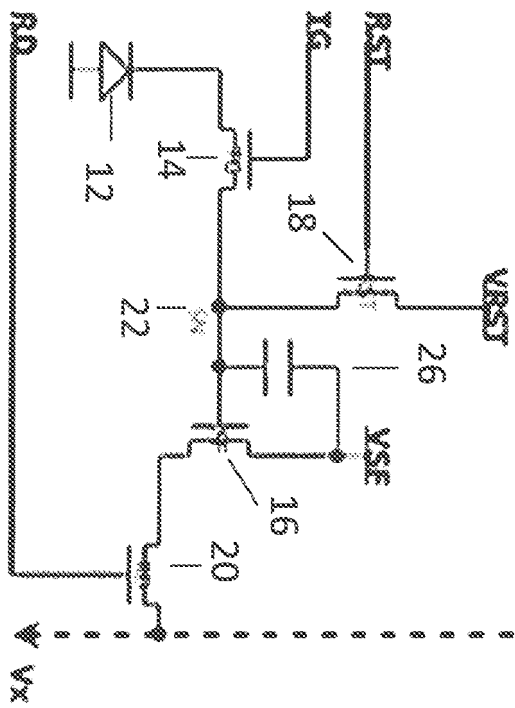


Figure 6

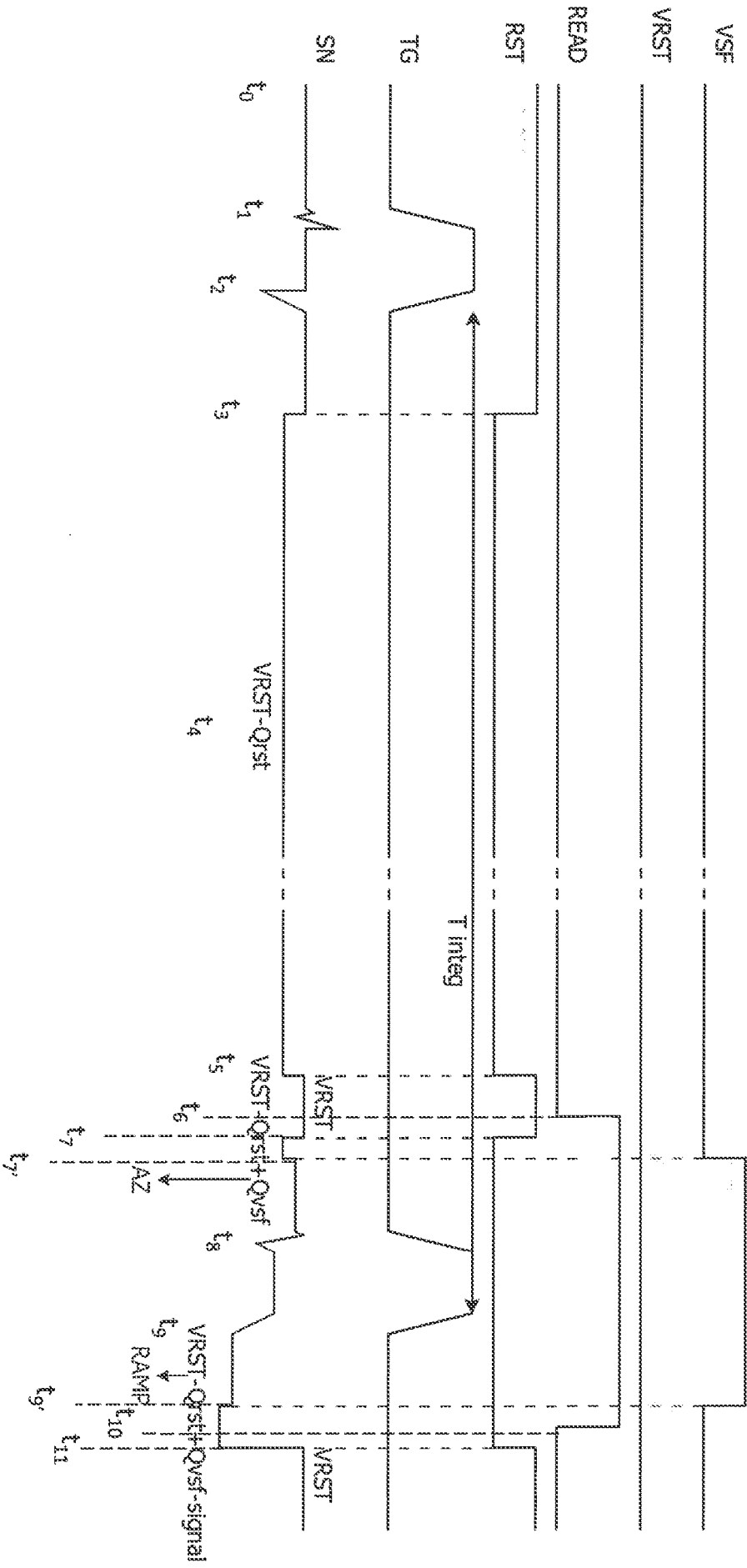


Figure 7

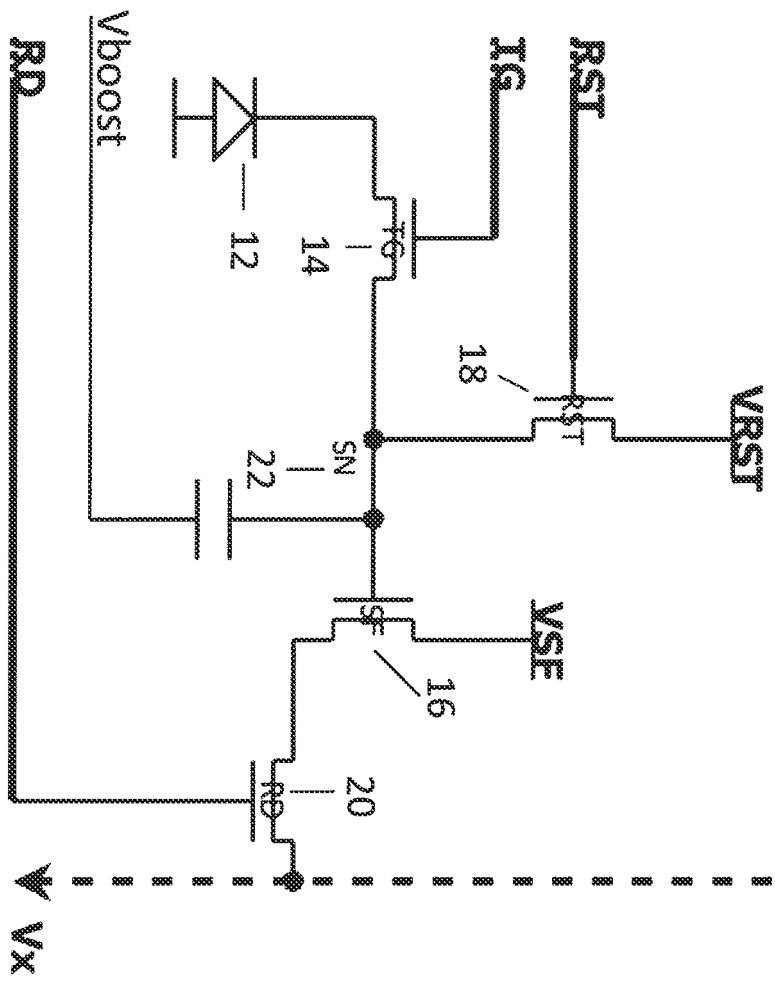


Figure 8

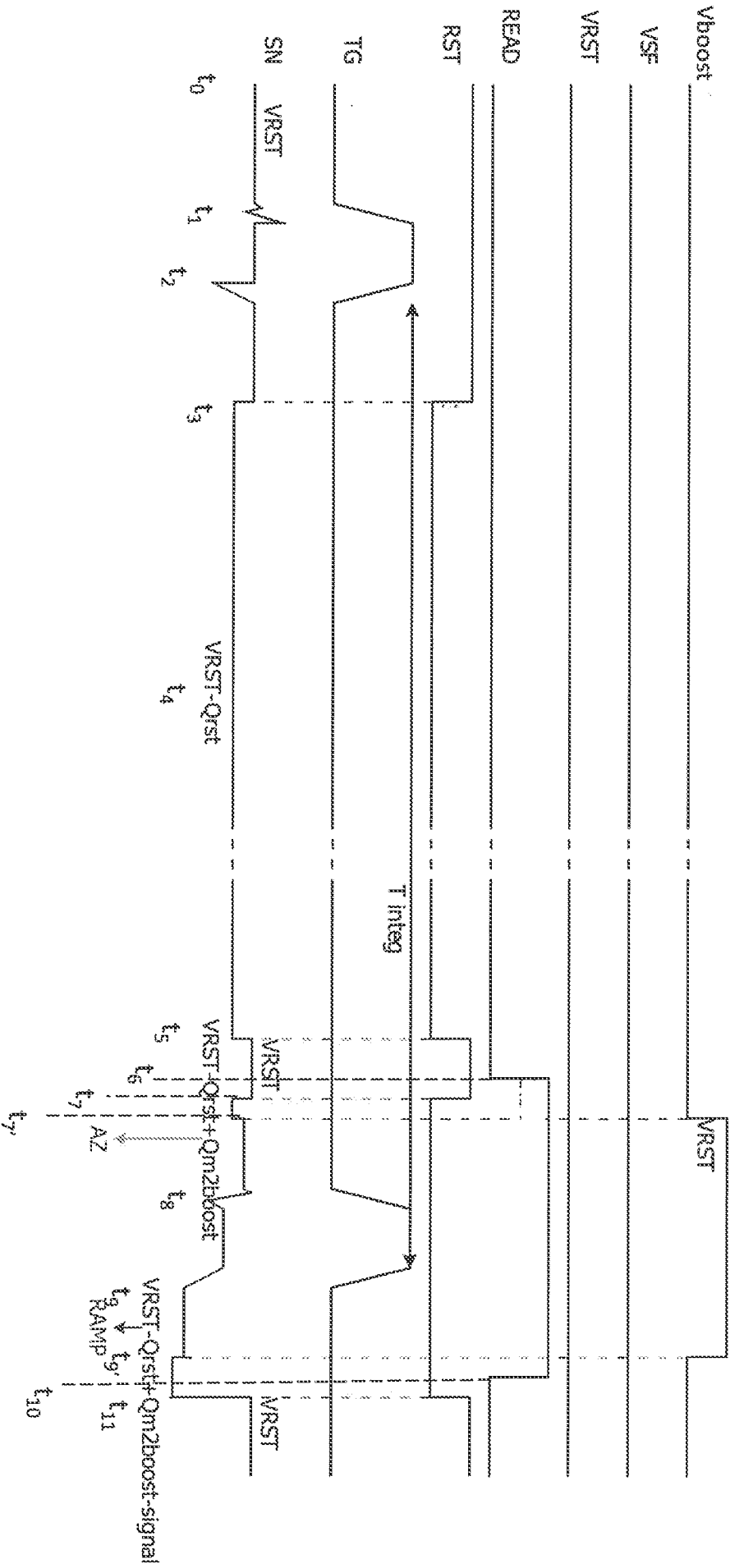


Figure 9

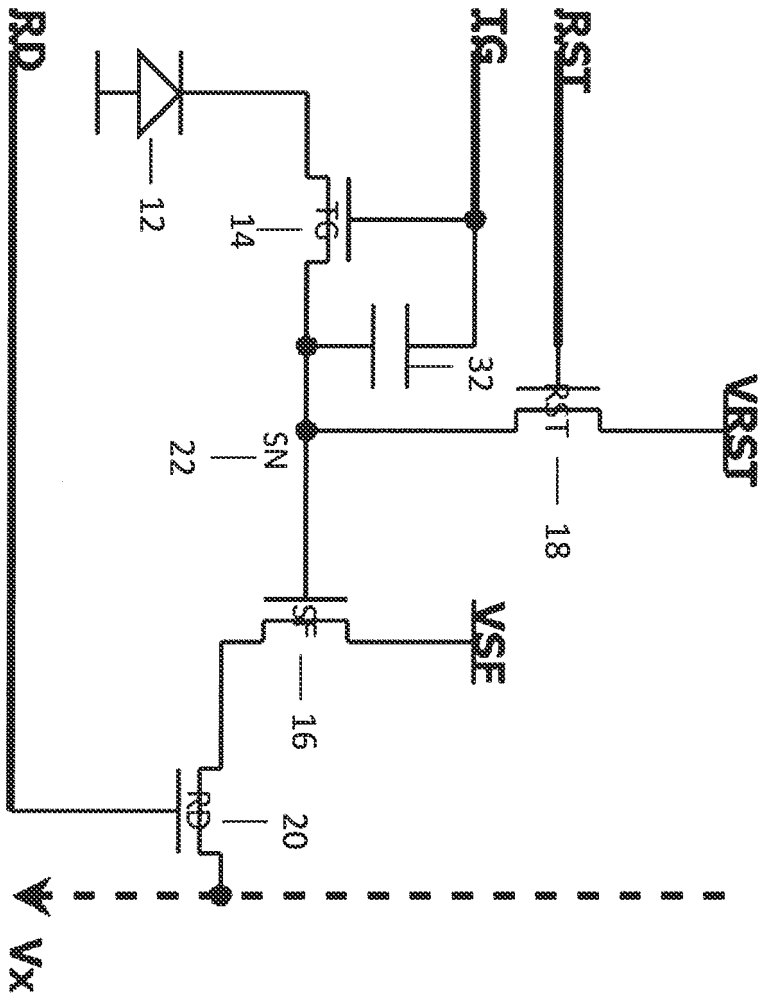


Figure 10

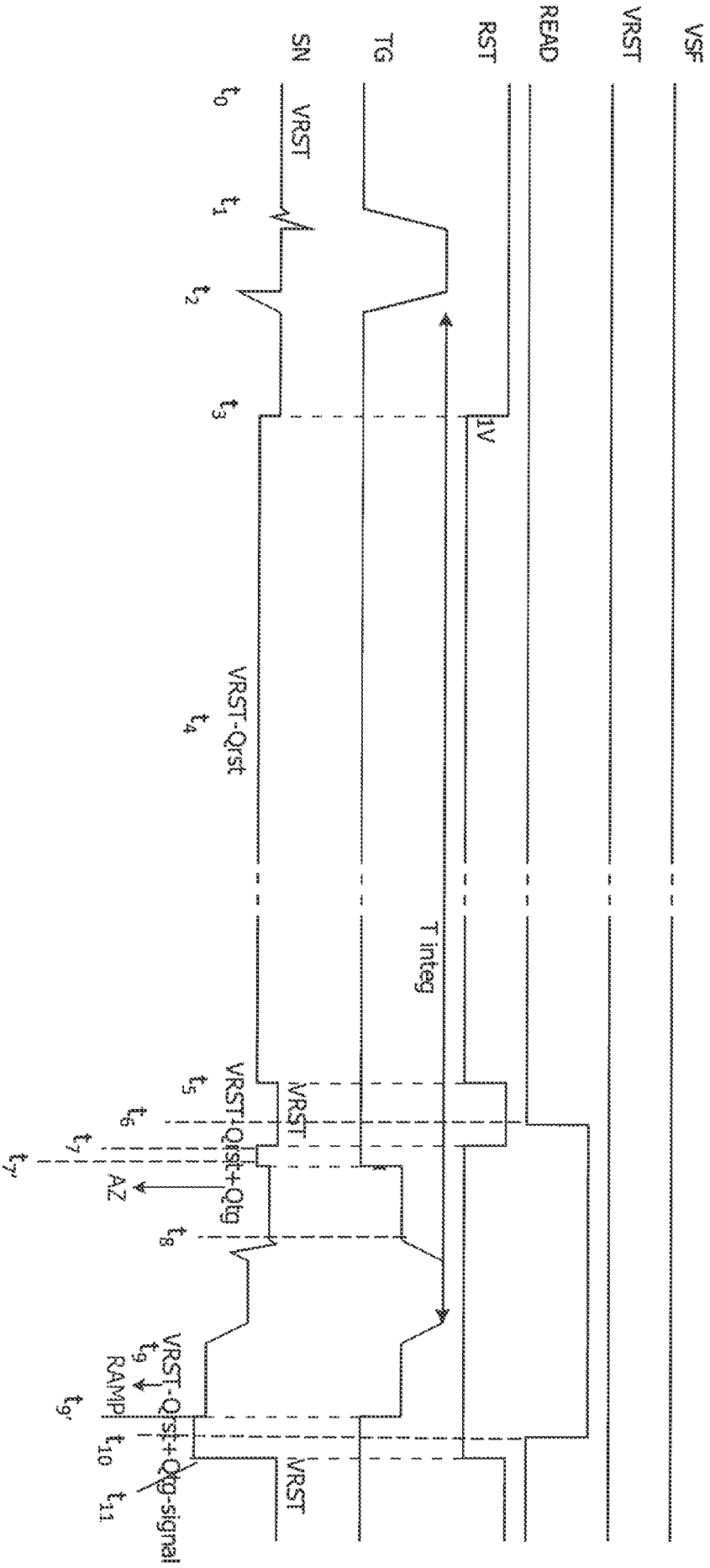


Figure 11

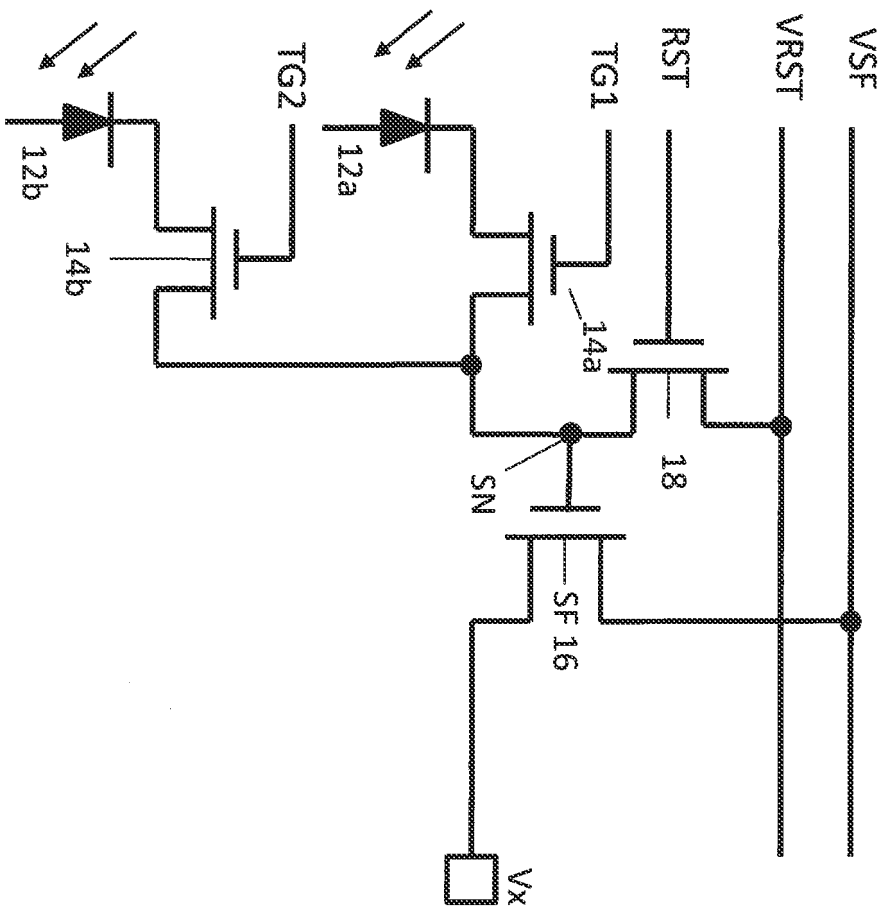


Figure 12

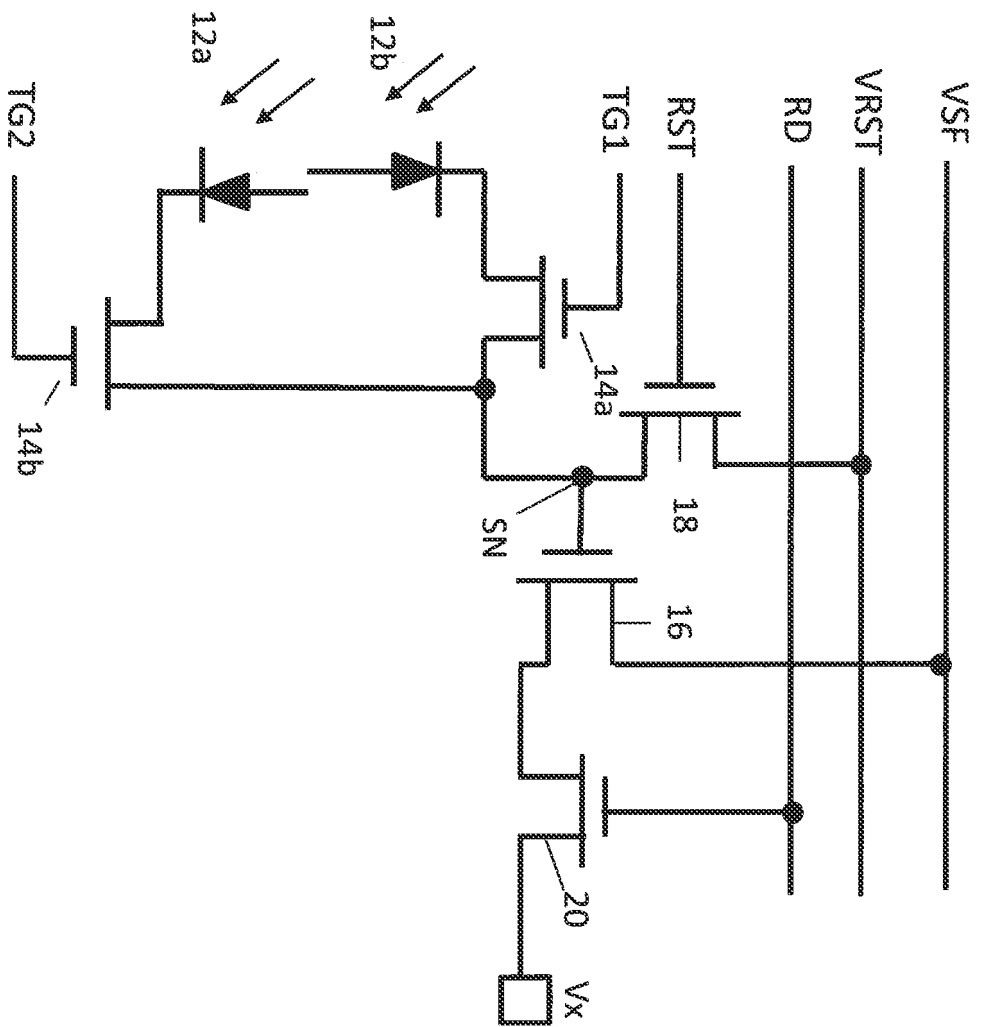


Figure 13

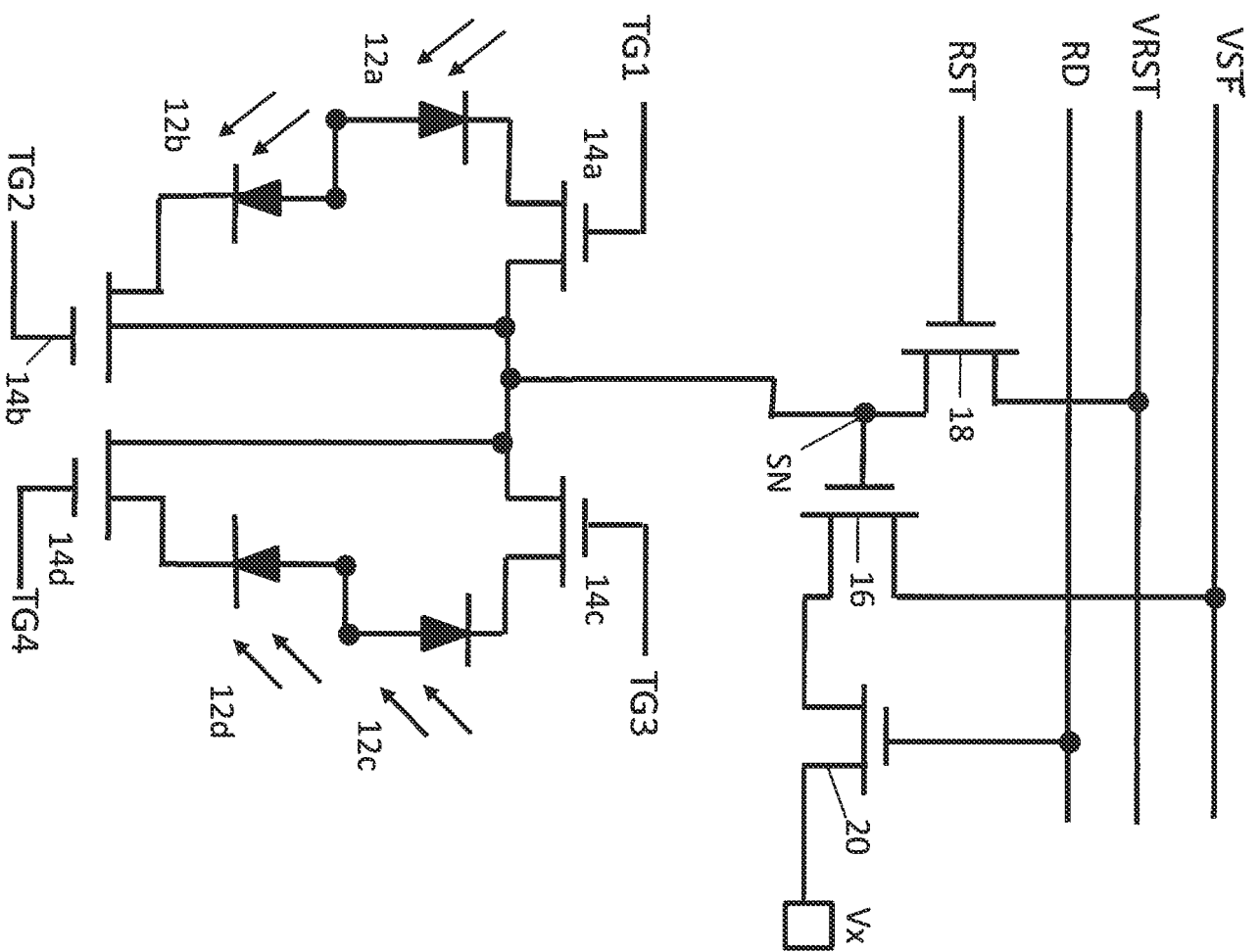
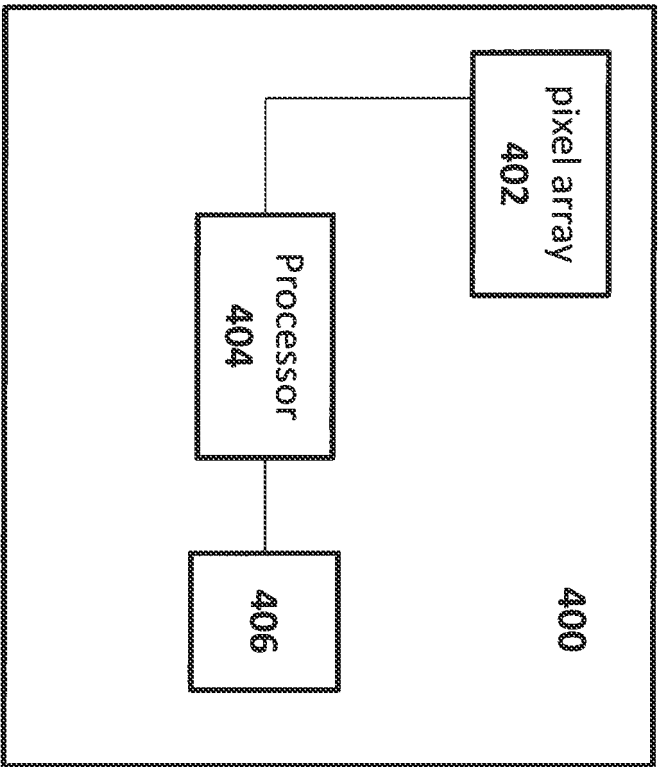


Figure 14



A PIXEL

Some embodiments relate to a pixel and in particular but not exclusively to a pixel structure for use in an array of pixels.

Image sensors using photodiode pixels, typically implemented in CMOS architecture, are well known. Such image sensors in many applications may have the image sensitive element and the image processing circuitry embodied in a single chip which can be manufactured using CMOS techniques.

According to an aspect, there is provided an pixel arrangement comprising: at least one photodiode; at least one reset transistor configured to be controlled by a reset signal and coupled in use to a reset input voltage; a transfer gate transistor for each photodiode configured to transfer charge from the photodiode to a node in use, said transfer gate transistor configured to be controlled by a transfer gate voltage, and at least one source follower transistor configured to be controlled by the voltage on the node and coupled in use to a source follower voltage, wherein during a read operation, at least one voltage is increased, said increased voltage being one or more of a said reset input voltage, said source follower voltage, said transfer gate voltage and a voltage on said node.

The arrangement may comprise at least one read transistor configured to be controlled by a read voltage, wherein during a read operation said read voltage has a read value.

At least one voltage may be increased for a period which is shorter than a period during which said read voltage has said read value.

The transfer gate voltage may in use be increased during a read operation, said transfer gate signal being changed from a first voltage level to an intermediate voltage level and then from the intermediate voltage level to a second voltage level during the read operation, the intermediate voltage level being intermediate the first and second voltage levels.

The first voltage level may be lower than said second voltage level.

The transfer gate voltage may then be changed from the second voltage level to the intermediate voltage to the first voltage level during the read operation.

The reset signal is pulsed at a beginning of said read operation

In use said reset signal may be pulsed and said read voltage may be changed to said read value while said reset signal is pulsed.

The arrangement may comprise a capacitor, said capacitor coupled to said node and in use configured to increase said voltage on said node during said read operation.

The pixel arrangement may provide one or more pixels.

An integrated circuit may comprise an arrangement described above.

Reference is now made by way of example only to the accompanying drawings in which:

Figure 1 shows a first example of a 4T (four transistor) pixel;

Figure 2 shows a timing diagram for the pixel of Figure 1;

Figure 3 shows a second example of a 4T (four transistor) pixel;

Figure 4 shows a timing diagram for the pixel of Figure 3;

Figure 5 shows a third example of a 4T (four transistor) pixel;

Figure 6 shows a timing diagram for the pixel of Figure 5;

Figure 7 shows a fourth example of a 4T (four transistor) pixel;

Figure 8 shows a timing diagram for the pixel of Figure 7;

Figure 9 shows a fifth example of a 4T (four transistor) pixel;

Figure 10 shows a timing diagram for the pixel of Figure 9;

Figure 11 shows a two transistor pixel;

Figure 12 shows a 2.5 transistor pixel;

Figure 13 shows a 1.75 transistor pixel; and

Figure 14 shows a device

A CMOS image sensor has a pixel array. Figure 1 shows a common pixel architecture, based on what is known as a 4T (four transistor) pixel 10. The pixel 10 comprises a photodiode 12, a transfer gate transistor 14, a source follower transistor 16, a reset transistor 18 and a read transistor 20. These transistors act to reset, expose and then read out data from the photodiode. The transfer gate transistor 14 is controlled by a signal TG, the reset transistor 18 is controlled by a signal RST and the readout transistor 20 is controlled by the read signal RD. The source follower transistor 16 has its gate tied to a sense node 22.

In more detail, the reset transistor 18 receives the reset signal RST at its gate, its drain is connected to a voltage VRST and its source is connected to the sense node 22. The source follower transistor 16 has its drain connected to a source follower supply voltage VSF and its source connected to the drain of the read transistor 20. The read signal RD is coupled to the gate of the read transistor 20.

The source of the read transistor 20 provides the output voltage V_x . The transfer gate transistor 14 has its gate coupled to the control signal TG. The drain of the transfer gate transistor is connected to the sense node 22 whilst its source is connected to the photodiode 12.

The transistors typically operate with a pinned photodiode structure and Correlated Double Sampling (CDS) to remove "kTC" noise associated with the reset operation. In Correlated Double Sampling, the output of the pixel is measured twice: once in a reset condition (in this case at "black level" when the only level change is resultant from noise) and once in a condition including the signal (which still includes the "black level" noise). The value measured from the signal condition is then subtracted from the reset condition so as to remove the "black level" noise offset. The double sampling operation also removes fixed noise sources such as variation in the threshold voltage of the source follower transistor.

The pixel needs to have appropriate voltage levels applied at defined time intervals. The voltage levels of the control signal TG (to transfer the pixel signal level to the sense node), RESET (to reset the sense node and photodiode) and READ (to select the pixel to the V_x line) as well as the pixel power supply (providing VRST and VSF), should comprise little noise, since any noise may couple directly to the sense node or column parallel output voltage level V_x and corrupt the image data.

The amount of charge that a photodiode can collect before saturating is known as the full well. It is desirable to have a large full well so that many photons can be collected from the incoming illumination and the imaging range extended. During the pixel read operation the collected charge is transferred to the sense node which causes a downward voltage change (of which the magnitude is determined by the capacitance on the sense node). A large voltage change per electron transferred (known as conversion factor) is desirable to maximise the signal swing but if the transferred charge is large, the full voltage swing may not be achieved. Limitations can come from one or more of the following (but are not limited to):

1. A requirement to have a sense node voltage above the pinning voltage of the photodiode. If the sense node voltage is too low, full charge transfer will not occur and signal will be lost.
2. Limited swing available on the V_x column. If the sense node voltage is too low the source follower may not be able to correctly buffer the sense node voltage.

The V_x voltage lower limit may be dictated by the column current source which requires a voltage drop to operate correctly.

It is thus desirable in some embodiments to maximise the blk level of the sense node. This blk level is the voltage after the RESET transistor has been turned OFF and before the TG signal is pulsed. It may be desirable to maximise the change in the sense node and V_x voltage.

The reset signal will typically vary between the low and high levels.

Reference is made to Figure 2 which shows the voltage of the different signals over time.

The voltage VSF is held at a first voltage V . The reset voltage VRST is held at second voltage V .

Initially, at time t_0 , the read signal RD is held at third, non-read voltage V . In the time period t_0 to t_1 , the signal TG is at a fourth voltage which may be a negative voltage in some embodiments.. At time t_1 , the TG signal is taken up to fifth voltage which is higher than the fourth voltage and then back down to the fourth voltage at time t_2 . The voltage on the SN is initially VRST. There will be corresponding voltage spike in the voltage on node SN corresponding to the signal TG toggling up to the fifth voltage level. There is a corresponding downward spike when the voltage TG is returned back to the fourth voltage level.

The RST signal is initially at a sixth voltage and is then dropped at time t_3 to a seventh voltage level. In some embodiments, the RST signal is optionally returned to the sixth voltage level at time t_4 . From time t_3 to t_5 , the voltage on the SN is VRST-Qrst. The integration period in this embodiment is from time t_2 to time t_9 .

At time t_5 the RST signal and just beyond at time t_6 the READ signal are respectively raised to higher voltage levels, that is the sixth voltage level in the case of the RST signal and a eighth voltage level in the case of the READ signal. This starts the read period of the pixel. The RST signal is then set to its low level, the seventh voltage level at time t_7 . Again, the voltage on the SN node will drop to VRST-Qrst.

At time t_8 the TG signals increase to the fifth voltage which turns on the TG device causing a positive coupling onto the sense node. The upward coupling will be in opposition to any downward voltage shift caused by the charges transferred from the photodiode. When the TG voltage toggles back down at time t_9 , the voltage on

the SN node couples downward reversing the previous upward kick. The voltage is VRST-Qrst-signal.

At time t10 and t11 the column voltage has been converted by an on-chip ADC so the read signal is set to the lower voltage, the third voltage, and the RST signal set to the higher voltage, the sixth voltage to disable the pixel. The voltage on the node SN will increase to VRST. ΔV represents the signal voltage. It is this voltage which some embodiments aim to maximise.

In this example, the signal RST is low during the integration time. In other arrangements, this signal could be high during the integration time.

Reference is now made to Figure 3 which shows a second example of a 4T pixel. It should be appreciated that those parts which are the same as in Figure 1 are referred to with the same reference number. In this arrangement, a capacitor 24 is provided in parallel with the reset transistor 18. This capacitor may be capacitance inherent in the arrangement. In some embodiments, the capacitance may be increased by the way in which the pixel is constructed. Otherwise the arrangement is as shown in Figure 1.

Reference is now made to Figure 4 which shows the corresponding timing for the circuitry of Figure 3. It should be appreciated that there is a correspondence in the events at times t0, t1, t2, t3, t4, t5, t6, t7, t8, t9, t10, and t11 between Figures 2 and 4. Accordingly, these events will not be described again.

At time t7' (between times t7 and t8), the voltage VRST is increased to a ninth voltage level until time t9' (between times t9 and t10) when it is returned to the second voltage level. The voltage on the node SN will be VRST-Qrst+Qvrst at time t7'. VRST is returned to the second level before the read voltage drops to the third voltage level. However, it should be appreciated that the voltage between times t9 and t9' on the SN node will be VRST-Qrst+Qvrst-signal. There will thus be more headroom available for signal as compared to Figure 2. To improve the effect of boosting, the capacitor 24 can be increased in size.

Reference is made to Figures 5 and 6 which show another embodiment. Figure 5 shows the circuitry. The circuitry is as shown in Figure 1 but a capacitor is shown between VSF and the node SN. This capacitor is referenced 26 and may be inherent and optionally augmented by a metal arrangement in the layout.

Figure 6 shows the timing for the circuit of Figure 5. It should be appreciated that there is a correspondence in the events at times t0, t1, t2, t3, t4, t5, t6, t7, t8, t9,

t10, and t11 between Figures 2 and 6. Accordingly, these events will not be described again and the differences with respect to the timing of Figure 2 will now be discussed. The voltage VSF voltage is held at a tenth voltage level which is lower than the first voltage level of Figure 2. The VSF voltage is increased up to the first voltage level at time t7' (between time t7 and t8) and reduced back to tenth voltage level at time t9' (between time t9 and t10). This timing is the same as used in the arrangement of Figures 3 and 4 with respect of the increasing of the voltage VRST, but for the VSF voltage. The voltage on the node SN at times t9 to t9' is $VRST - Qrst + Qvsf$ -signal. Again, the headroom available for signal is increased with respect to the arrangement of Figure 1.

Reference is made to Figures 7 and 8 which show another embodiment. The circuitry is shown in Figure 7 and differs from the arrangement of Figure 1 in that a capacitor 27 is shown between the sense node SN and a boost voltage, referred to Vboost. The capacitor is provided by the layout of metal. The timing associated with this arrangement is shown in Figure 8.

Figure 8 shows the timing for the circuit of Figure 7. It should be appreciated that there is a correspondence in the events at times t0, t1, t2, t3, t4, t5, t6, t7, t8, t9, t10, and t11 between Figures 2 and 8. Accordingly, these events will not be described again and the differences with respect to the timing of Figure 2 will now be discussed. The Vboost signal follows the same pattern as the VRST of Figure 4. The Vboost signal voltage varies between an eleventh voltage and a higher twelfth voltage. The twelfth voltage level may be the second voltage level of VRST. At time t7', Vboost increases from the eleventh voltage level to the twelfth voltage level and decreases back to the eleventh voltage level at time t9'

The voltage on the node SN at times t9 to t9 is $VRST - Qrst + QVboost$ -signal. Again, the headroom for signal is increased with respect to the arrangement of Figure 1.

Reference is made to Figure 9 where a capacitor 32 is shown between TG and the node SN. The capacitor is inherent in some embodiments and in other embodiments may be augmented by metal of the layout. The timing associated with this arrangement is shown in Figure 10.

Figure 10 shows the timing for the circuit of Figure 9. It should be appreciated that there is a correspondence in the events at times t0, t1, t2, t3, t4, t5, t6, t7, t8, t9, t10, and t11 between Figures 2 and 10. Accordingly, these events will not be

described again and the differences with respect to the timing of Figure 2 will now be discussed. The TG signal can now be set to three different voltage levels. This permits both boosting and charge transfer to be controlled from the same signal – TG. The boosting operation is shown in Figure 10 at time t17' where the TG voltage is increased from a fourth voltage to an intermediate voltage level between the fourth and fifth voltage levels. The intermediate voltage may vary depending on how much boosting is required and/or what the process defines to be the maximum level that does not transfer charge to the sense node from the photodiode. After the boost has been applied, the blk level is sampled at node Vx. The transfer pulse on TG is made between t8 and t9. The difference from previous embodiments is that the TG voltage starts at the intermediate voltage level at time t8 and returns to the intermediate voltage level at time t9. The TG voltage level decreases from the intermediate level to the fourth voltage level at time t9'.

In this embodiment, the voltage on node SN between times t7' and t8 is $VRST - Q_{rst} + Q_{tg}$. Q_{tg} is the charge on the capacitor 27. This is also the blk sampling period.

The voltage on the node SN at times t9 to t9' is $VRST - Q_{rst} + Q_{tg}$ -signal. This is the signal sampling period. Again, the headroom available for signal is increased with respect to the arrangement of Figure 1.

As mentioned previously, it is desirable to have a low capacitance on the node SN to have a high conversion factor. Figure 9 and Figure 10 have described an arrangement in which the inherent overlap capacitance of the TG transistor can be used to boost the sense node voltage.

The above described embodiments have used four n-type transistors. It should be appreciated that in other embodiments, the transistors may be p type transistors or a mix of at least one n type transistor and at least one p type transistors.

The about embodiments have been described in relation to a 4T pixel. It should be appreciated that embodiments may be used with other structures of pixels. By way of example, reference is made to Figure 11 which shows a 2T pixel. In the arrangement shown in Figure 11, there are four transistors which are used to provide two pixels, thus giving two transistors per pixel. In the arrangement shown in Figure 11, a first photo diode 12a and a second photo diode 12b are shown. Each of these diodes is coupled to a respective transfer gate transistor 14a and 14b. A single reset

transistor 18 is used for both of the pixels. Likewise, a single source follower transistor 16 is shown. In this arrangement, there is no read transistor. It should be appreciated that in the arrangement of Figure 11, one or more of the following may occur:

- the VRST voltage may be controlled as shown in Figure 4;

- the VSF voltage may be controlled as shown in Figure 6;

- a boost voltage can be applied to a capacitor as described in relation to Figure 7 and 8;

- the TG voltage can be controlled as described in relation to Figure 10.

Reference is made to Figure 12 which shows a 2.5 T pixel. Five transistors are used to provide two pixels giving 2.5 transistors per pixel. The arrangement is as described in relation to Figure 11 but with the addition of the read transistor 20. One or more of the voltages can be boosted as described previously.

Reference is made to Figure 13 which shows a 1.75T pixel. In this arrangement, there were seven transistors providing four pixels, giving 1.75 transistors per pixel. There are four photodiodes 12a, 12b, 12c and 12d. Each photodiode is provided with a respective transfer gate transistor 14a, 14b, 14c and 14d. A single reset transistor 18, source follower transistor 16 and read transistor 20 are provided. Again, any of the voltages previously described as having been boosted can be boosted in the arrangement of Figure 13.

Whilst examples of 2T, 1.75T and 2.5T arrangements have been shown, it should be appreciated that this is by way of example only. Other embodiments may be used with other transistor structures, for example 5T etc.

The above described embodiments have been described in relation to MOS transistors. It should be appreciated that in other embodiments, different types of transistors have been used.

Some embodiments may be provided in a device 400 such as shown in Figure 14. The device 400 may comprise any one of arrangements as previously described which are referenced 402. An output from the pixel array may be provided to a processor 404. The output of the processor may control for example a display 406 and allow the captured image to be displayed,

It should be appreciated that the device may be any suitable device. By way of example only and without limitation, that device may be a mobile telephone, smart phone, tablet, computer, camera or the like

Various embodiments with different variations have been described here above. It should be noted that those skilled in the art may combine various elements of these various embodiments and variations. Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

CLAIMS:

1. A pixel arrangement comprising:
 - at least one photodiode;
 - at least one reset transistor configured to be controlled by a reset signal and coupled in use to a reset input voltage;
 - a transfer gate transistor for each photodiode configured to transfer charge from the photodiode to a node in use, said transfer gate transistor configured to be controlled by a transfer gate voltage, and
 - at least one source follower transistor configured to be controlled by the voltage on the node and coupled in use to a source follower voltage,wherein during a read operation, at least one voltage is increased, said increased voltage being one or more of a said reset input voltage, said source follower voltage, said transfer gate voltage and a voltage on said node.
2. An arrangement as claimed in claim 1, comprising at least one read transistor configured to be controlled by a read voltage, wherein during a read operation said read voltage has a read value.
3. An arrangement as claimed in any preceding claim, wherein said at least one voltage is increased for a period which is shorter than a period during which said read voltage has said read value.
4. An arrangement as claimed in any preceding claim, wherein said transfer gate voltage is in use increased during a read operation, said transfer gate signal being changed from a first voltage level to an intermediate voltage level and then from the intermediate voltage level to a second voltage level during the read operation, the intermediate voltage level being intermediate the first and second voltage levels.
5. An arrangement as claimed in claim 4, wherein said first voltage level is lower than said second voltage level.
6. An arrangement as claimed in claim 4 or 5, wherein said transfer gate voltage is then changed from the second voltage level to the intermediate voltage to the first voltage level during the read operation.

7. An arrangement as claimed in any preceding claim, wherein said reset signal is pulsed at a beginning of said read operation
8. An arrangement as claimed in claim 2 or any claim appended thereto wherein in use said reset signal is pulsed and said read voltage is changed to said read value while said reset signal is pulsed.
9. An arrangement as claimed in any preceding claim, comprising a capacitor, said capacitor coupled to said node and in use configured to increase said voltage on said node during said read operation.
10. An arrangement as claimed in any preceding claim, wherein said pixel arrangement provides one or more pixels.
11. An integrated circuit comprising an arrangement as claimed in any preceding claim.



Application No: GB1314288.0

Examiner: Dr Dilwyn Williams

Claims searched: All

Date of search: 17 January 2014

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1-7, 10 and 11	US2005/0083421 A1 (BEREZIN) - Figure 3 and 5 (Variable Saturation control voltage Vtx) paragraph 28 and all of the document
X	1-7,10 and 11	US2008/0093534 A1 (MHEEN) Figure 5A, 5B Paragraphs 82-84 and all of the document
X	1-2, 7 and 10-11 at least	WO99/52273 A1 (KOZLOWSKI)- Figures 4-6 and 9 and all of the document
X	1-3 and 9-11 at least	US2005/0121519 A1 (SHINOHARA) - Figures1-6 : in particular features in figure 3 (SO->Node 12, FD->node4 & Cap(17)) paragraphs 47 -54.
X	1-7, 9-11 at least	US2006/0261431 A1 (KIM) - Figures 2-4, and all of the document
X	1-2, 10 and 11 at least	US6043478 A (WANG) figure 4 and 6, (Feature VC variable). All of the document
X	1-2 and 9-11 at least	US2011/0216231 A1 (FOWLER) - Figure 8 feature 52,53 paragraph 25.
X	1-3, 7-8, 10-11	US2011/0042551 A1 (HA) - Figures 2-4 and 7, (see features 110, Rx) paragraphs 17-42 and all of the document.

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^X :



Worldwide search of patent documents classified in the following areas of the IPC

H01L; H04N

The following online and other databases have been used in the preparation of this search report

WPI, EPODOC, INSPEC , Full English text TXTE

International Classification:

Subclass	Subgroup	Valid From
H01L	0027/146	01/01/2006
H04N	0005/30	01/01/2006
H04N	0005/335	01/01/2011