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(71) Applicant: PACTEL CORPORATION [US/US]; 2999 Oak Road, Mailstop 800, Walnut Creek, CA 94596 (US).

(72) Inventor: LEE, William, Chien-Yeh ; 55 Montecito Drive, Corona Del Mar, CA 92625 (US).

(74) Agents: McCUBBREY, J., Bruce et al.; McCubbrey, Bartels, Meyer & Ward, Suite 2700, One Post Street, San Francisco, CA 94104-5231 (US).

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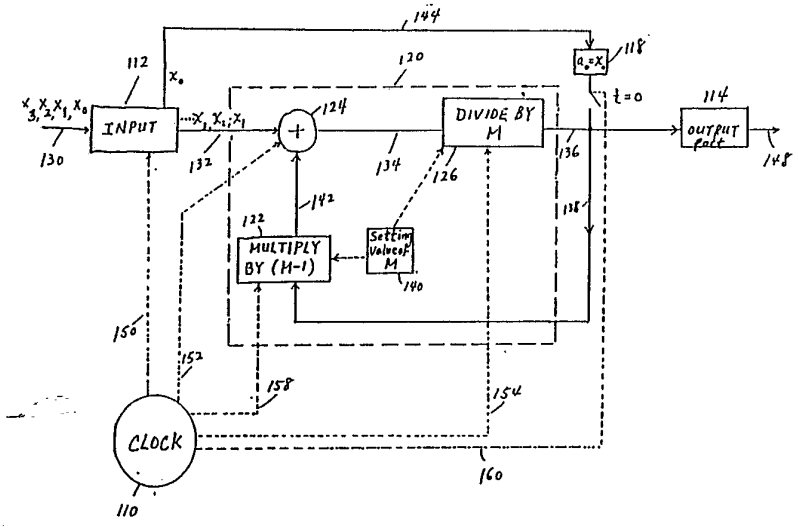

(57) Abstract

A real-time signal averaging circuit (120) is disclosed. The averaging circuit includes a signal input port (112) for receiving an input signal (130); the input signal representing a value x^n which is to be averaged by the averaging circuit. The averaging circuit uses a register (122) for temporarily storing and updating a previous average value a^p which was output from the averaging circuit. An averaging circuit is connected to the signal input port and the register. The averaging circuit provides a weighted average value a^n of the value x^n represented by the input signal and of the previous average value a^p stored in the register. The average value a^n is defined as the sum $((M-1)a^p + x^n)$ divided by M, where M is a predetermined positive number greater than 1. The averaging circuit provides to the register the average value a^n. Finally, the circuit includes an output port (114) for generating an output signal representing the average value a^n. The output signalling port is connected to the averaging circuit. A clock (110) generates the necessary timing signals.

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A REAL-TIME RUNNING AVERAGING DEVICE

Field of the Invention

The present invention relates to real-time devices, and more specifically to real-time devices for calculating an average of values represented by a signal.

Background of the Invention

Mobile radio (electronic) devices often are required to adapt to changes in their environment or to vary the output which they are to produce in a nearly instantaneous manner. This has led to an increased reliance upon real-time evaluation of data representing physical quantities. "Real-time" here refers to the fact that the evaluation is performed at essentially the same time as the data is acquired. Real-time systems typically require very rapid processing of data as that data is obtained. Non-real-time evaluation occurs at some time long after the data is obtained. For example, when a mobile unit is requesting a service, a response from the system to the mobile unit takes a long time; the time lag in processing the data can cause the results to be obsolete by the time those results are obtained.

The information processing limitations of the electronic hardware involved with a particular device help determine the operational capacity and maximum processing speed of that device. Hence minimization of hardware complexity and increases in hardware response time are critical to evaluation of data for those applications.

One example of such a time-critical application is found in the field of cellular telephones. Cellular mobile telephones (mobile units) must receive signals broadcast from the cell site transmitters. The mobile telephones are often themselves

in motion. This motion leads to changes in the strength of the signals received by the mobile unit. Cellular telephone networks attempt to maintain an acceptable signal level at each site, and switch the signal to a new cell when the average signal received from the mobile unit becomes weak, i.e. below the acceptable level. This switching may be accomplished by comparing the intensity of the average value of the signals from different cells and selecting that signal which is strongest.

Determination of the average value is presently accomplished in the following manner. The receiver measures the signal intensity at a number of points, for example twenty, and stores these values in a memory. The values are then added and the sum is divided by the number of stored values. This yields the mean (average) value of the signal intensity. Typically, the next average is obtained by discarding the oldest stored value, replacing it with a new value, and performing the averaging computations just described. This leads to a smoother transition of the computed average over time, and utilizes a fixed memory capacity.

This method is not ideal for real-time operations such as are used in cellular telephone systems. It requires memory devices for storing these values to be averaged. This complicates the hardware of the system and slows the averaging process. More importantly, it yields the average value as of the moment that is halfway between the newest and the oldest data value. In the example given above, the average value represents the value at the time midway between the 10th and 11th data value. Thus if instantaneous data were being sampled once every second, the average obtained is actually the average value as of a point in time ten seconds prior to the most recent data value measured. This does not include the delay caused by actually performing the calculations themselves.

This physical delay is a serious problem for cellular telephone networks. In addition, the lag in the computed average value is large enough to adversely affect the reliability of the comparisons based upon those averages, which

are not valid for use for real-time comparisons among them. This lag increases as the number of points sampled increases. Thus the more precise the average, the older it is and thus less reliable. This is only compensated for by increasing the sampling rate of the device, which often is accompanied by severe increases in cost.

It would therefore be desirable to perform an averaging which yields a more timely result, and one which minimizes the hardware complexity of the average processing device. Also, while the example given relates to cellular telephone networks, it is clear that similar problems may arise in a variety of applications which involve real-time averaging of data to smooth out fluctuations.

Broadly, it is an object of the present invention to provide an improved real-time signal averaging device.

It is a further object of the present invention to provide a real-time signal averaging circuit which generates an output which represents the average value of data at a time close to the time at which the new data are obtained.

It is a still further object of the present invention to provide a real-time signal averaging circuit which requires no memory hardware.

These and other objects of the present invention will be apparent to those skilled in the art from the following detailed description of the invention and the accompanying drawings.

Summary of the Invention

The present invention comprises a real-time signal averaging circuit. The averaging circuit includes clock means for generating timing signals. The averaging circuit also includes signal input means for receiving an input signal. The input signal represents a value x_n which is to be averaged by the averaging circuit. The averaging circuit further includes register means for temporarily storing and updating a previous average value a_p which was output from the averaging circuit. Averaging means are connected to the clock means, the signal input means and the register means. The averaging means provides in response to the timing signals a weighted average value a_n of the value x_n represented by the input signal and of the previous average value a_p stored in the register means. The average value a_n is defined as the sum $((M-1)a_p + x_n)$ divided by M, where M is a predetermined positive number greater than 1. The averaging means provides to the register means the average value a_n. Finally, the circuit includes output signalling means for generating an output signal representing the average value a_n. The output signalling means is connected to said averaging means.

Alternative embodiments are disclosed for circuits in which the value is represented digitally, wherein the register means is a digital data register, and in which the value is represented by an analog amplitude, wherein the register means is a sample and hold device. Also, in the preferred embodiment of the present invention, the previous value a_p is the immediately previous average value a_{n-1}.

The present invention also includes a method of producing an average value of a signal in real-time. The method includes obtaining timing signals from a clock means. Next a previous average value a_{n-1} is input into a register means. An input signal representing a value x_n to be averaged is then received. Then a weighted

average value a_n of the previous average value a_{n-1} and the value x_n represented by said input signal is provided in response to the timing signals. The weighted average value a_n is defined as the sum $((M-1)a_{n-1} + x_n))$ divided by M, where M is a predetermined positive number greater than 1. Finally an output signal is generated representing the weighted average value a_n.

As for the circuit described above, there are corresponding alternative implementations of the present method. The value may be represented digitally, in which case the register means is again a digital register, or an analog magnitude device.

Brief Description of the Drawings

Figure 1 illustrates a signal being sampled at discrete points separated by uniform time intervals.

Figure 2 is a flow chart illustrating the preferred implementation of the method of the present invention.

Figure 3 is a block diagram representation of an implementation of an averaging circuit according to the present invention.

Figure 4 is a schematic diagram of a circuit according to the present invention for averaging digital signals.

Figure 5 is a schematic diagram of a circuit according to the present invention for averaging analog signals.

Figure 6 is a block diagram representation of a comparison circuit according to the present invention.

Figure 7 is a schematic diagram of a circuit according to the present invention for comparing the averaging values of a plurality of digital signals.

Figure 8 is a schematic diagram of a circuit according to the present invention for comparing the averaging values of a plurality of analog signals.

Detailed Description of the Invention

The advantages provided by the present invention are best understood in light of the prior art method. Therefore a brief explanation of the method of the prior art is required. A signal to be averaged is sampled at regular intervals. The times at which these samples were obtained are referred to as t_0, t_1, ... t_n, where there are n+1 data points sampled. The values of these data points are denoted as x_0, x_1, ... x_n. While these signal values are said to represent the values to be averaged, this does not mean that there must be an encoding of external data into signal form. The signal may be inherently characterized by the values to be averaged.

The average value obtained by the prior art method is:

$$a_n = \frac{1}{n} \sum_{i=0}^{n-1} (x_i) \qquad (1)$$

This type of average is referred to as an arithmetic mean, or simply a mean.

Figure 1 illustrates an example of how such a sampling is undertaken. A signal 1 is shown plotted on a graph, where vertical distance represents the value of the signal and the horizontal distance represents time. The labelled circles represent the signal values x_0, x_1, ... sampled at the times t_0, t_1, ... A specified number of these values are added and the sum is divided by that number of values. Hence, for 15 points, the mean is equal to $(x_0 + x_1 + ... + x_{14}) / 15$.

Typically, these n+1 values are stored in a memory device. The next subsequent mean would be obtained by discarding x_0 and replacing it with x_{n+1}. The summation would then be performed by summing the values x_1 to x_{n+1}. This allows for summation using a continuing adding process using an adder and with a memory for storing the n+1 most recent values. Such a procedure, utilized for each time sampled, acts to smooth out the values of the means thus obtained. This helps eliminate noise and minimizes the possibility of dramatic swings in the average values obtained by the procedure.

It should be noted that the term "memory" is used herein to describe devices for storage of values which are to be statically maintained during the calculation of several average value. In the specific example given above each memory location retains its value for 15 average value calculations. This is where the data itself is stored. The term "register", by contrast, is used herein to describe devices for storage of values which are to be maintained only until used a single time, and then are replaced with a new value. Registers would be used to temporarily store data until it is utilized and replaced during the next average value calculation.

The method described above may be better understood by again referring to Figure 1. A first set 4 of 15 data points which are averaged at time t_{14} is shown. Also, a second set 5 of 15 data points which are averaged at time t_{15}. Since the processor only looks at n+1 points out of many that have been taken, it is said

that the processor is looking at a "window" of values. This refers to the fact that this appears to be a slice on a graph of time plotted against sampled values. The n+1 points move on the graph in the direction of increasing time. Hence set 4 is to the left of the later set 5. This is known as "sliding" the "window".

Unfortunately, as described above, the mean does not provide an accurate representation of the average at the time t_n. Instead, it actually represents the average value at the time $t_{n/2}$, which is the time halfway between t_0 and t_n. Using the example in Figure 1, the mean is actually effective as of time t_7, not t_{14}.

This can present problems in real-time applications, as the time $t_{n/2}$ may be sufficiently remote from the time t_n that the mean will have changed significantly. In the example in Figure 1, the average value at t_7 is clearly different than that at t_{14}. Hence it may be necessary to obtain the mean at the time t_n.

To obtain the average at time t_n, one must know the values for times after t_n. This presents no problem in non-real time applications, since the later values are obtained and the processing is performed at a time remote from the sampling. Unfortunately, real-time applications require processing prior to obtaining these later values. Hence it is impossible to obtain a mean for t_n in a real-time application.

Therefore it may be necessary to utilize an alternative averaging process to the mean-generating process described above. The present invention reveals a different method of generating an average, one which minimizes the need for memory and which provides an average which can be effective at a time far later than that of the prior art.

The present invention provides a running average of the signal value. Each subsequent average is a weighted average of the new data point and the previous data points. For the preferred embodiment of the present invention, given

the previous average value a_{n-1}, the new average value a_n is generated by the following formula:

$$a_n = \frac{(M-1)\,a_{n-1} + x_n}{M} \qquad (2)$$

where M is greater than 1. It can be shown that this equation is equivalent to the equation:

$$a_n = \frac{1}{M}\sum_{i=0}^{n} \left(\frac{M-1}{M}\right)^i x_{n-i} \qquad (3)$$

Here it is obvious that $0 < (M-1)/M < 1$. Therefore as i gets larger, the factor $((M-1)/M)^i$ gets smaller. This factor corresponds to the weight which x_{n-i} is given in the average a_n. Hence the method of the present invention weighs those values which are sampled later more heavily than those taken earlier. This results in an average value which more closely approximates the average at t_n than the mean generating method of the prior art.

It should be noted that the weight of the previous values of the signal depends solely upon the choice of M and the time interval between the time when the average is performed (t_n) and the time when that value was sampled, (t_{n-i}). As M gets smaller, more recent points are weighted more heavily. As the weights accorded to recent values are increased, the effective time of the average becomes closer to the time t_n.

Unfortunately, there are disadvantages to weighting the more recent values very heavily. Such weighting reduces the smoothing effect that the averaging provides to the data. In practical terms, heavily increasing the weights of recent data

values produces a similar effect to that caused by diminishing the number of sample points in the mean generating method.

Hence there is a tradeoff when selecting weights for recent values between providing more timely responses and providing accurate responses. Thus a desired M should be chosen in light of the specific needs of the application in which this method is implemented. For example, for the case of a moving cellular telephone, values of M = 2 or M = 3 may be satisfactory.

The method of the present invention does not require a memory device, since in the preferred embodiment only a register is required to hold the previous value of the average, a_{n-1}. This can lead to a significant decrease in the complexity of the hardware necessary to obtain the average over the prior art.

In the preferred embodiment described above, a_n replaces a_{n-1}. This is not necessary for all embodiments. The average value may be calculated based upon some time interval which is an integer i times the sampling time. This may be desired in cases where the sampling occurs faster than the circuit can produce the average. In such cases the undesired samples may be neglected while every i^{th} sample is averaged. The previous average value may then be denoted as a_p, to prevent confusing the indices of the average and the samples x_n.

Hence the method of the present invention provides an effective average which is effectively closer in time to the time when the averaging is performed than the methods of the prior art. In addition, a significant decrease in hardware complexity can be achieved.

The preferred implementation of the method of the present invention is illustrated in Figure 2. First, the operational parameters are set at 10. This includes setting the value of M and obtaining the initial value of the input signal, x_0, received

by an input port. Also, at $t = t_0$ there is no previous average value. Thus the value x_0/M is assigned to a_0 and is read into a register which temporarily holds the average value. Initialization is completed by setting a counter n to 0 at 12.

The method may be implemented as follows. The most recent value of the average, a_n, is retrieved at 14. The average value may be temporarily stored in a register separate from the arithmetic unit, or may be stored in the arithmetic unit itself. Next, the value $(M-1)a_n$ is computed by the arithmetic unit at 16. The counter n is then incremented at 18. The next value of the input signal, x_n, is read at 20. The value x_n is then summed at 22 with the output of step 16. It should be noted that the value of n has been incremented, and therefore the result obtained at 16 is actually $(M-1)a_{n-1}$. Hence the result of step 22 is $(M-1)a_{n-1} + x_n$. The result of step 22 is then divided by M at 24. This yields the new average value $a_n = [(M-1)a_{n-1} + x_n] / M$, which is available for retrieval at 14 for the next iteration.

It is possible to implement the preferred method without the initialization steps, i.e. without steps 10 and 12. If these steps are ignored, and the register is initially set to zero, then an error is introduced into a_n. The size of this error is:

$$Err = \left(\frac{M-1}{M}\right)^n \frac{x_0}{M} \qquad (4)$$

Therefore the fractional error is given by:

$$\frac{Err}{x_0} = \frac{1}{M}\left(\frac{M-1}{M}\right)^n \qquad (5)$$

For a typical small value, M = 3, the fractional error is less than 0.01 when n = 9. The fractional error is reduced to less than 0.001 after n = 15. For M = 2, the fractional error is less than 0.01 when n = 6, and is less than 0.001 after n =

9. Therefore it is clear that if M is small then the effects of the error diminishes rapidly. There may be applications for which the effects of the resulting error are outweighed by the benefits of the resulting decrease in hardware complexity. In such cases initialization may be omitted.

The manner in which the present invention can be implemented as an apparatus can best be understood in light of the preferred embodiment. Figure 3 is a block diagram of an implementation of an averaging circuit according to the present invention. A clock 110 is provided for generating timing signals which control the timing of the operations accomplished by the circuit. These signals may be such that different signals operate to control different elements of the circuit, or all elements may be controlled by the same signal. The signal only need be utilized to control some element of the circuit.

First, a signal input port 112 receives on input line 130 an input signal which is to be averaged. The input signal represents a value x_n which is to be averaged by said averaging circuit, where the subscript n indicates a measure of the time at which the signal is received. The representation may be accomplished in a variety of manners know to the art, including but not limited to digital representation and amplitude modulation. The choice of representation schemes is then matched to the hardware which implements the averaging. This will be discussed in greater detail below.

Next, input port 112 responds to timing signals on input port clock control line 150 to transmit the signal value at discrete time intervals corresponding to integer values of n as described above. These signals x_n are transmitted on input port transmission line 132 to the averaging circuit 120. Averaging circuit 120 is connected to clock 110 and is responsive to timing signals transmitted on timing lines 152, 154 and 158, as discussed below.

Averaging circuit 120 generates an average value a_n from the value x_n and the previous average value a_{n-1}. The previous average value a_{n-1} is received from previous average retrieval line 138 which is connected to an output port setting line 136. Averaging circuit 120 acts to add x_n to (M-1) times the previous average value a_{n-1}, and then divides the sum by M to yield the average value a_n. M may be set in the multiplier 122 and the divider 126 by a setting device 140. The role of the weighting factor M is discussed in greater detail above.

In the preferred embodiment illustrated in Figure 3, averaging circuit 120 receives the previous average value a_{n-1} from previous average input line 138 and stores it temporarily in multiplying circuit element 122. Multiplying circuit element 122 acts in response to timing signals on timing line 158 to generate a signal which represents the value $(M-1)a_{n-1}$. The output signal from multiplying circuit element 122 is transmitted on multiplier output line 142 to adding circuit element 124. Adding circuit element 124 acts in response to timing signals on timing line 152 to generate a signal representing the sum of the value corresponding to the output of multiplying circuit element 122 ($(M-1)a_{n-1}$) and that of the input signal value x_n. The output of adding circuit element 124 is transmitted via adder output line 134 to dividing circuit element 126. Dividing circuit element 126 acts in response to timing signals on timing line 154 to generate a signal representing the value obtained by dividing the value represented by the output of adding circuit element 124 by M. The value thus obtained is the average value a_n.

The resulting signal representing the average a_n is then transmitted on output port transmission line 136 to an output port 114. Output port 114 is connected to output line 148 to allow the average a_n to be accessed by external circuits.

At the time t_0, it is desirable to utilize a different process in order to initialize the system, as described above. In the preferred embodiment of the present

invention, this is implemented by connecting input port 112 to an initialization circuit 118 via an initialization line 144. Initialization circuit 118 responds to timing signals from clock 110 on initialization timing line 160 to read the value x_0/M into memory 116 at time t_0. The value x_0/M is then transmitted to previous average input line 138 and output port setting line 136.

One implementation of a circuit according to the present invention is illustrated in Figure 4. The input signal is a digital signal, wherein several individual binary voltage values together comprise a signal. This signal represents the value x_n.

A clock 210 generates timing signals which control the timing of the operations accomplished by the circuit. As noted above, these signals may be such that different signals operate to control different elements of the circuit, or all elements may be controlled by the same signal. In addition, not every signal need be utilized to control some element of the circuit.

A signal input port 212 receives on input line 230 a digital input signal which is to be averaged. Signal input port may be implemented as a digital buffer. The input signal represents a value x_n which is to be averaged by the averaging circuit, as described above.

Input port 212 responds to timing signals on input port clock control line 250 to transmit the signal value at discrete time intervals as described above. These signals x_n are transmitted on input port transmission line 232 to the averaging circuit 220. Averaging circuit 220 is connected to clock 210 and is responsive to timing signals transmitted on timing lines 252, 254 and 258, as discussed below.

Averaging circuit 220 generates an average value a_n from the value x_n and the previous average value a_{n-1}. The previous average value a_{n-1} is received from

previous average retrieval line 238 which is connected to an output port setting line 236. The previous average value may be stored in a standard digital register, as described below. Averaging circuit 220 acts to add x_n to (M-1) times the previous average value a_{n-1}, and then divides the sum by M to yield the average value a_n. The role of the weighting factor M is discussed in greater detail above.

Averaging circuit 220 receives the previous average value a_{n-1} from previous average retrieval line 238 and stores it temporarily in multiplying circuit element 222. Multiplying circuit element 222 acts in response to timing signals on timing line 258 to generate a signal which represents the value $(M-1)a_{n-1}$. If (M-1) is known to always be a power of two, then the multiplying circuit may be implemented as a single digital shift register, considerably simplifying hardware implementation. It may otherwise include a standard digital register and a digital multiplier. Such multipliers are well known in the art.

The output signal from multiplying circuit element 222 is transmitted on multiplier output line 242 to adding circuit element 224. Adding circuit element 224 acts to generate a signal representing the sum of the value corresponding to the output of multiplying circuit element 222 ($(M-1)a_{n-1}$) and that of the input signal value x_n.

The output of adding circuit element 224 is transmitted via adder output line 234 to dividing circuit element 226. Dividing circuit element 226 acts in response to timing signals on timing line 254 to generate a signal representing the value obtained by dividing the value represented by the output of adding circuit element 224 by M. If M is known to always be a power of two, then dividing element 226 may be implemented as a single digital shift register. It may otherwise include a standard digital register and a digital divider. Such dividers are well known in the art. The value thus obtained is the average value a_n.

The resulting signal representing the average a_n is then transmitted on output port transmission line 236 to an output port 214. Output port 214 may be implemented as a digital output buffer. Output port 214 is connected to output line 248 to allow the average a_n to be accessed by external circuits.

At the time t_0, it is desirable to utilize a different process in order to initialize the system, as described above. In the preferred embodiment of the present invention, this is implemented by connecting input port 212 to an initialization circuit 218 via an initialization line 244. Initialization circuit 218 responds to timing signals from clock 210 on initialization timing line 260 to read the value x_0/M into memory 216 at time t_0. The value x_0/M is then transmitted to previous average input line 238 and output port setting line 236.

An alternative implementation to the circuit of Figure 3 according to the present invention is illustrated in Figure 5. The input signal is an analog signal, wherein the voltage value of the signal represents the value x_n.

A clock 310 generates timing signals which control the timing of the operations accomplished by the circuit. As noted above, these signals may be such that different signals operate to control different elements of the circuit, or all elements may be controlled by the same signal. In addition, not every signal need be utilized to control some element of the circuit.

A signal input port 312 receives on input line 330 an analog input signal which is to be averaged. Signal input port may be implemented as an analog sample-and-hold circuit. The instantaneous voltage value of the input signal represents a value x_n which is to be averaged by the averaging circuit, as described above.

Input port 312 responds to timing signals on input port clock control line 350 to transmit the signal value at discrete time intervals as described above. These signals x_n are transmitted on input port transmission line 332 to the averaging circuit 320. Averaging circuit 320 is connected to clock 310 and is responsive to timing signals transmitted on timing lines 352, 354 and 358, as discussed below.

Averaging circuit 320 generates an average value a_n from the value x_n and the previous average value a_{n-1}. The previous average value a_{n-1} is received from memory output line 340 which is connected to a sample-and-hold (S/H) device 316. S/H device 316 may be a standard sample-and-hold circuit. Averaging circuit 320 acts to add x_n to (M-1) times the previous average value a_{n-1}, and then divides the sum by M to yield the average value a_n. The role of the weighting factor M is discussed in greater detail above.

Averaging circuit 320 receives the previous average value a_{n-1} from S/H device 316 via output line 340. Multiplying circuit 322 acts to generate in response to timing signals on timing line 356 a signal which represents the value $(M-1)a_{n-1}$. Multiplying circuit 322 may be implemented as a standard op-amp with a gain of M-1, as shown. The gain of op-amp 370 is set by the ratio of resistors 372 and 374, i.e. $(M-2)R_4 / R_4$, or (M-2). The gain of such an op-amp is the ratio of the resistances plus one. Hence the gain is (M-1). Op-amp 370 acts to multiply the amplitude of the signal.

The output signal from multiplying circuit 322 is transmitted on multiplier output line 342 to adding circuit 324. Adding circuit 324 acts to generate a voltage representing the sum of the output voltage multiplying circuit 322 ($(M-1)a_{n-1}$) and that of the input signal value x_n on input port transmission line 332. The value on input port transmission line 332 is changed in response to timing signals on timing line 250 to S/H device 312.

Adding circuit 324 may use resistors 376 and 378 to average the voltage between the inputs. The average is an arithmetic mean as the values of resistors 376 and 378 is the same, e.g. R_1. The op-amp 380 has a gain of two because the ratio of the resistances between resistors 382 and 384 is R_2 / R_2 or 1, and the gain of such an op-amp is the ratio of the resistances plus one. The output of op-amp 380 is a pure sum of the voltages, as twice the mean average of two values is the sum of those values. In addition, op-amp 380 acts as a driver for subsequent stages.

The output of adding circuit element 324 is transmitted via adder output line 334 to dividing circuit 326. Dividing circuit element 326 acts to divide the voltage representing the value obtained by dividing the value represented by the output of adding circuit 324 by M. Dividing element 326 may be implemented as a resistor-based voltage divider circuit as shown, where the output voltage is based upon the values of resistors 386 and 388 and is $(M-1)R_3 / ((M-1)R_3 + R_3)$, or M. The value thus obtained is the average value a_n.

The resulting signal representing the average a_n is then transmitted on output port transmission line 336 to an output port 314. Output Port 314 may be implemented as an analog sample-and-hold circuit. Output port 314 is connected to output line 348 to allow the average a_n to be accessed by external circuits. In addition, the average value a_n is transmitted on input line 338 to memory 316, which responds to a timing signal from clock 310 transmitted on transmission line 356 to store the new average value a_n.

An example of an application of the averaging method of the present invention is illustrated in Figure 6. Figure 6 is a flow chart for a method of comparing the average values of j distinct signals in real-time. Timing signals are obtained from a clock, which controls the sequence of steps.

The j average values of the j signals at every instant are obtained by the method described above for calculating the averages by the present invention. The j previous average values $a_{k,p}$, where $0 \leq k \leq j - 1$ and p is the index of the immediate previous average value, are read into j memory devices at 610. An input signal representing a value $x_{k,n}$ to be averaged is received at j input ports at 612. A weighted average value $a_{k,n}$ of the previous average value $a_{k,p}$ and the value $x_{k,n}$ represented by the corresponding input signal is provided at 614 in response to the timing signals. The weighted average value is defined as the sum $((m-1)a_{k,p} + x_{k,n})$ divided by M, where M is a predetermined positive number greater than 1. Next j output signals representing each of j said weighted average value $a_{k,n}$ are transmitted at 616 to a comparison device. Finally, the j weighted average values $a_{k,n}$ are compared at 618.

It is important to note that this method may include initialization steps such as those discussed above regarding Figure 2. This initialization would occur at step 610, as initialization essentially provides a prior average value. Such initialization may be less critical in cases such as this implementation, where the error of multiple averaging should not disrupt the comparison being provided.

Although the method described indicates simultaneous processing at each stage of the averaging process, there may be some flexibility in the precise timing of each step. The critical requirement is that the averages for all j averaging circuits be complete at the time when the comparison is initiated.

This method may be implemented in a circuit, as illustrated in Figure 7. A comparison circuit for real-time comparison of j distinct signal values, said comparison circuit would require a clock circuit 710 for generating timing signals. This circuit may be constructed from multiple clocks, and may appear as j individual circuit clocks.

The circuit would include j real-time signal averaging circuits 700, each of said signal averaging circuits being represented by an positive number label k, $0 \leq k \leq j - 1$. These circuits would be identical to the circuit disclosed above. The k^{th} signal averaging circuit 702 includes a k^{th} signal input port 712 for receiving the k^{th} one of the j input signals. The input signal received at k^{th} signal input port 712 represents a value $x_{k,n}$ which is to be averaged by k^{th} signal averaging circuit 702. The k^{th} memory 716 stores a previous average value $a_{k,p}$ which was output from k^{th} signal averaging circuit 702.

The k^{th} averaging subcircuit 720 is connected to clock 710, k^{th} signal input port 712 and k^{th} memory 716. The k^{th} averaging subcircuit 720 provides in response to the timing signals an average value $a_{k,n}$. This average is defined as the sum $((M-1)a_{k,p} + x_{k,n})$ divided by M, where M is a predetermined positive number greater than 1. Hence average value $a_{k,n}$ is the weighted average of the value $x_{k,n}$ represented by the k^{th} input signal received at k^{th} signal input port 712 and of the previous average value $a_{k,p}$ stored in k^{th} memory 716. The k^{th} averaging subcircuit 720 provides to k^{th} memory 716 the average value $a_{k,n}$. Finally, k^{th} output port 714 is connected to k^{th} averaging subcircuit 720 to generate on k^{th} averaging circuit output line 718 a k^{th} one of j output signals, thereby representing the average value $a_{k,n}$.

The j output signals are then compared by an appropriate comparison subcircuit 770 connected to each of the j signal averaging circuits 702 by one of the j averaging circuit output lines 718.

As discussed above regarding Figure 4, these j averaging subcircuits may be designed to include initialization circuitry.

This comparison circuit may be implemented in a variety of manners corresponding to the variety of methods of representing signal values, as discloses above. The input signals may be digital signals representing the values $x_{k,n}$. In such

a case the digital k^{th} averaging circuits 702 may be constructed as illustrated in Figure 4 and discussed above. The j output signals of these averaging circuits 702 would be digital signals representing the weighted average values $a_{k,n}$. Memory 716 could be implemented as a digital data registers. Comparison subcircuit 770 may be implemented as a simple digital calculation circuit.

In the alternative, the input signals may be analog signals whose amplitudes represent the values $x_{k,n}$. In such a case the analog k^{th} averaging circuits 702 may be constructed as illustrated in Figure 5 and discussed above. The j output signals of these averaging circuits 702 would be analog signals representing the weighted average values $a_{k,n}$. Memory 716 could be implemented as a sample-and-hold-circuit, and comparison subcircuit 770 may be implemented as a simple analog comparator.

Each element in the above described embodiments can be constructed by means of components well known in the appropriate electronic art. Those skilled in those arts can readily design numerous alternative implementations of these embodiments. In addition, other methods of representing data values may be utilized.

There has been described herein an improved real-time averaging circuit. Various modifications to the present invention will become apparent to those skilled in the art from the foregoing description and accompanying drawings. Accordingly, the present invention is to be limited solely by the following claims.

WHAT IS CLAIMED IS:

1. A real-time signal averaging circuit comprising: clock means for generating timing signals; signal input means for receiving an input signal, said input signal representing a value x_n which is to be averaged by said averaging circuit; register means for storing a previous average value a_p which was output from said averaging circuit; averaging means connected to said clock means, said signal input means and said register means, said averaging means providing in response to said timing signals a weighted average value a_n of said value x_n represented by said input signal and of said immediately previous average value a_p stored in said register means, said average value a_n being defined as the sum $((M-1)a_p + x_n)$ divided by M, where M is a predetermined positive number greater than 1, said averaging means providing to said register means said average value a_n; and output signalling means for generating an output signal representing said average value a_n, said output signalling means being connected to said averaging means.

2. The averaging circuit of Claim 1 wherein said input signal is a digital signal representing said value x_n, said output signal is a digital signal representing said average value a_n, and wherein said register means comprise a data digital register.

3. The averaging circuit of Claim 1 wherein said input signal is an analog signal whose amplitude represents said value x_n, and said output signal is an analog signal whose amplitude represents said average value a_n and said register means comprise an analog sample and hold device.

4. The averaging circuit of Claim 1 wherein said previous average value a_p is the immediately previous average value a_{n-1}.

5. A method of producing an average value of a signal in real-time, said method comprising: obtaining timing signals from a clock means; inputting to a register means a previous average value a_p; receiving an input signal representing a value x_n to be averaged; providing in response to said timing signals a weighted

average value a_n of said previous average value a_p and said value x_n represented by said input signal, said weighted average value a_n being defined as the sum $((M-1)a_p + x_n))$ divided by M, where M is a predetermined positive number greater than 1; and generating an output signal representing said weighted average value a_n.

6. The method of Claim 5 wherein said previous average value is the immediately previous average value a_{n-1}.

7. A comparison circuit for real-time comparison of j distinct signal values, said comparison circuit comprising: clock means for generating timing signals; j real-time signal averaging circuits, each of said signal averaging circuits being represented by an positive number label k, $0 \leq k \leq j - 1$, the k^{th} of said signal averaging circuits comprising: a k^{th} signal input means for receiving the k^{th} one of said j input signals, said one of said input signals representing a value $x_{k,n}$ which is to be averaged by said k^{th} averaging circuit; the k^{th} one of j register means for storing a previous average value $a_{k,p}$ which was output from said k^{th} signal averaging circuit; a k^{th} one of j averaging means, said k^{th} averaging means being connected to said clock means, said k^{th} signal input means and said k^{th} register means, said k^{th} averaging means providing in response to said timing signals an average value $a_{k,n}$ defined as the sum $((M-1)a_{k,p} + x_{k,n})$ divided by M, where M is a predetermined positive number greater than 1, said average value $a_{k,n}$ being the weighted average of said value $x_{k,n}$ represented by said k^{th} input signal and of said previous average value $a_{k,p}$ stored in said k^{th} register means, said k^{th} averaging means providing to said k^{th} register means said average value $a_{k,n}$; and a k^{th} output signalling means connected to said k^{th} averaging means for generating a k^{th} one of j output signals representing said average value $a_{k,n}$; and comparison means for comparing the j values represented by said j output signals.

8. The averaging circuit of Claim 7 wherein said input signals are digital signals representing said values $x_{k,n}$, said output signals are digital signals representing said weighted average values $a_{k,n}$, and wherein said register means comprise digital data registers.

9. The averaging circuit of Claim 7 wherein said input signal is an analog signal whose amplitudes represent said values $x_{k,n}$, and said output signals are analog signals whose amplitudes represent said average values $a_{k,n}$.

10. A method of comparing the average values of j distinct signals in real-time, said method comprising: obtaining timing signals from a clock means; obtaining the j average values of said j signals by inputting to j register means the j previous average values $a_{k,n-1}$, where $0 \leq k \leq j - 1$, inputting an input signal representing a value $x_{k,n}$ to be averaged, providing in response to said timing signals a weighted average value $a_{k,n}$ of said previous average value $a_{k,n-1}$ and said value $x_{k,n}$ represented by said input signal, where said weighted average value is defined as the sum $((m-1)a_{k,n-1} + x_{k,n})$ divided by M, where M is a predetermined positive number greater than 1, and outputting j output signals representing each of j said weighted average value $a_{k,n}$; and comparing said j weighted average values $a_{k,n}$.

AMENDED CLAIMS

[received by the International Bureau on 1 February 1993 (01.02.93); original claims 1-10 replaced by amended claims 1-10 (3 pages)]

1. A real-time signal averaging circuit comprising: clock means for generating timing signals; signal input means for receiving an input signal, said input signal representing a value x_n which is to be averaged by said averaging circuit; register means for storing a previous average value a_p which was output from said averaging circuit; averaging means connected to said clock means, said signal input means and said register means, said averaging means providing in response to said timing signals a weighted average value a_n of said value x_n represented by said input signal and of said immediately previous average value a_p stored in said register means, said average value a_n being defined as the sum $((M-1)a_p + x_n)$ divided by M, where M is a predetermined positive number greater than 1, said averaging means providing to said register means said average value a_n; and output signalling means for generating an output signal representing said average value a_n, said output signalling means being connected to said averaging means.

2. The averaging circuit of Claim 1 wherein said input signal is a digital signal representing said value x_n, said output signal is a digital signal representing said average value a_n, and wherein said register means comprise a data digital register.

3. The averaging circuit of Claim 1 wherein said input signal is an analog signal whose amplitude represents said value x_n, and said output signal is an analog signal whose amplitude represents said average value a_n and said register means comprise an analog sample and hold device.

4. The averaging circuit of Claim 1 wherein said previous average value a_p is the immediately previous average value a_{n-1}.

5. A method of producing an average value of a signal in real-time, said method comprising: obtaining timing signals from a clock means; inputting to a register means a previous average value a_p; receiving an input signal representing a value x_n to be averaged; providing in response to said timing signals a weighted average value a_n of said previous average value a_p and said value x_n represented by said input signal, said weighted average value a_n being defined as the sum

$((M-1)a_p + x_n))$ divided by M, where M is a predetermined positive number greater than 1; and generating an output signal representing said weighted average value a_n.

6. The method of Claim 5 wherein said previous average value is the immediately previous average value a_{n-1}.

7. A comparison circuit for real-time comparison of j distinct signal values, said comparison circuit comprising: clock means for generating timing signals; j real-time signal averaging circuits, each of said signal averaging circuits being represented by an positive number label k, $0 \leq k \leq j - 1$, the k^{th} of said signal averaging circuits comprising: a k^{th} signal input means for receiving the k^{th} one of said j input signals, said one of said input signals representing a value $x_{k,n}$ which is to be averaged by said k^{th} averaging circuit; the k^{th} one of j register means for storing a previous average value $a_{k,p}$ which was output from said k^{th} signal averaging circuit; a k^{th} one of j averaging means, said k^{th} averaging means being connected to said clock means, said k^{th} signal input means and said k^{th} register means, said k^{th} averaging means providing in response to said timing signals an average value $a_{k,n}$ defined as the sum $((M-1)a_{k,p} + x_{k,n})$ divided by M, where M is a predetermined positive number greater than 1, said average value $a_{k,n}$ being the weighted average of said value $x_{k,n}$ represented by said k^{th} input signal and of said previous average value $a_{k,p}$ stored in said k^{th} register means, said k^{th} averaging means providing to said k^{th} register means said average value $a_{k,n}$; and a k^{th} output signalling means connected to said k^{th} averaging means for generating a k^{th} one of j output signals representing said average value $a_{k,n}$; and comparison means for comparing the j values represented by said j output signals.

8. The comparison circuit of Claim 7 wherein said input signals are digital signals representing said values $x_{k,n}$, said output signals are digital signals representing said weighted average values $a_{k,n}$, and wherein said register means comprise digital data registers.

9. The comparison circuit of Claim 7 wherein said input signal is an analog signal whose amplitudes represent said values $x_{k,n}$, and said output signals are analog signals whose amplitudes represent said average values $a_{k,n}$.

10. A method of determining and comparing the average values of j distinct signals in real-time, said method comprising: obtaining timing signals from a clock means; obtaining the j average values of said j signals by inputting to j register means the j previous average values $a_{k,n-1}$, where $0 \leq k \leq j - 1$, inputting an input signal representing a value $x_{k,n}$ to be averaged, providing in response to said timing signals a weighted average value $a_{k,n}$ of said previous average value $a_{k,n-1}$ and said value $x_{k,n}$ represented by said input signal, where said weighted average value is defined as the sum $((m-1)a_{k,n-1} + x_{k,n})$ divided by M, where M is a predetermined positive number greater than 1, and outputting j output signals representing each of j said weighted average value $a_{k,n}$; and comparing said j weighted average values $a_{k,n}$.

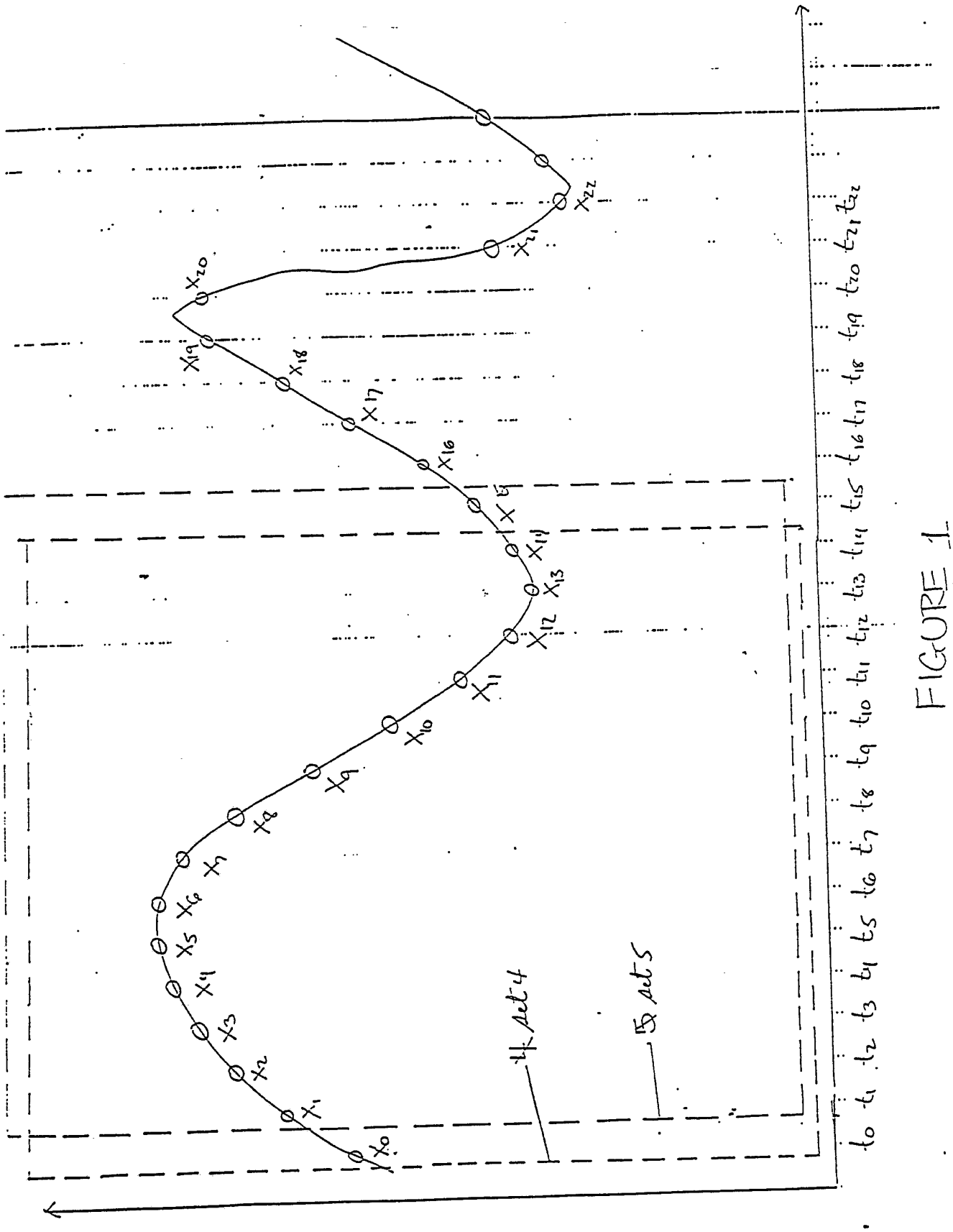

x0 x1 x2 x3 x4 x5 x6 x7 x8 x9 x10 x11 x12 x13 x14 x15 x16 x17 x18 x19 x20 x21 x22
t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16 t17 t18 t19 t20 t21 t22
4 Acts
5 Acts

FIGURE 1

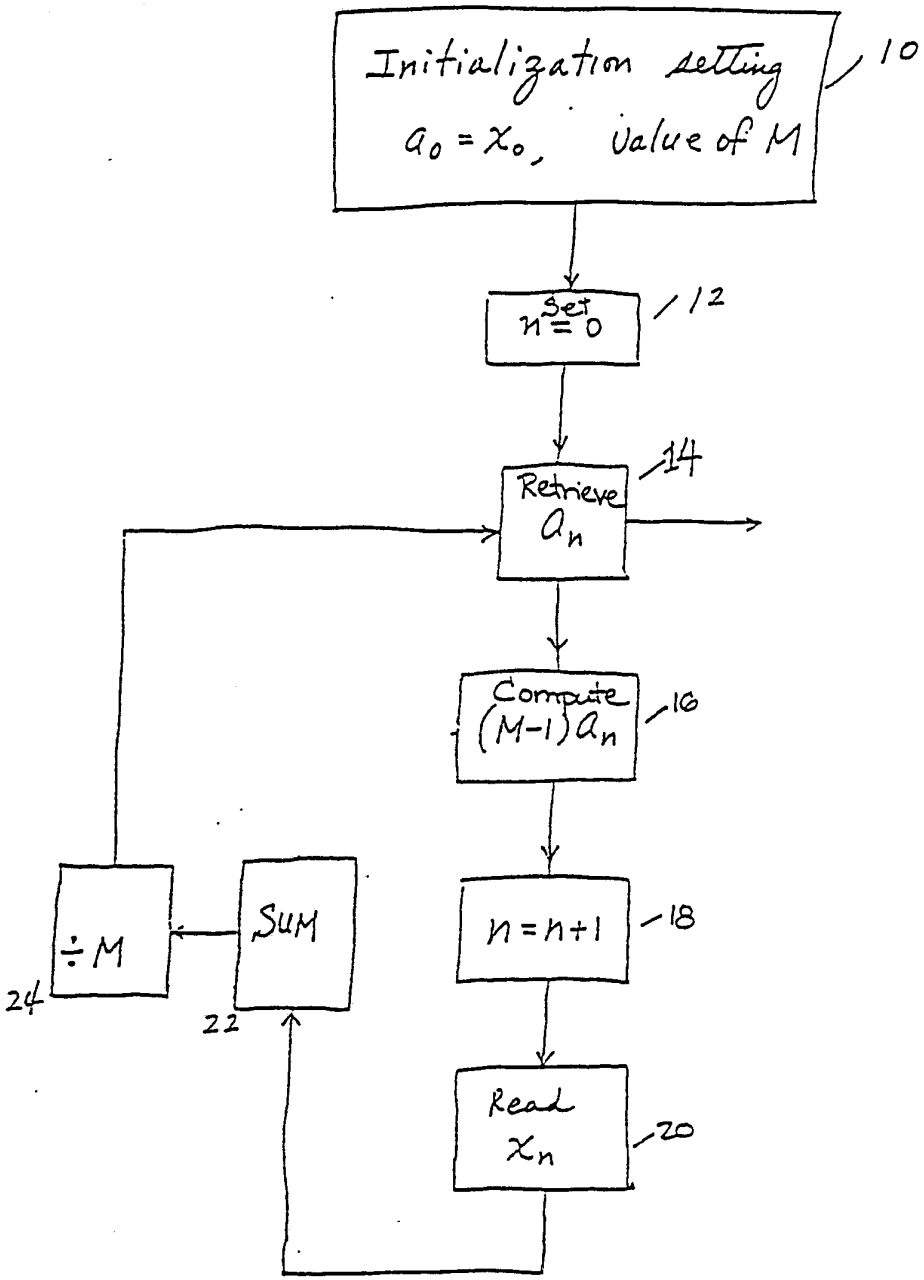

Initialization setting
$a_0 = x_0$, Value of M
10
$n \overset{Set}{=} 0$
12
Retrieve a_n
14
Compute $(M-1)a_n$
16
$n = n+1$
18
Read x_n
20
SUM
22
$\div M$
24

Figure 2

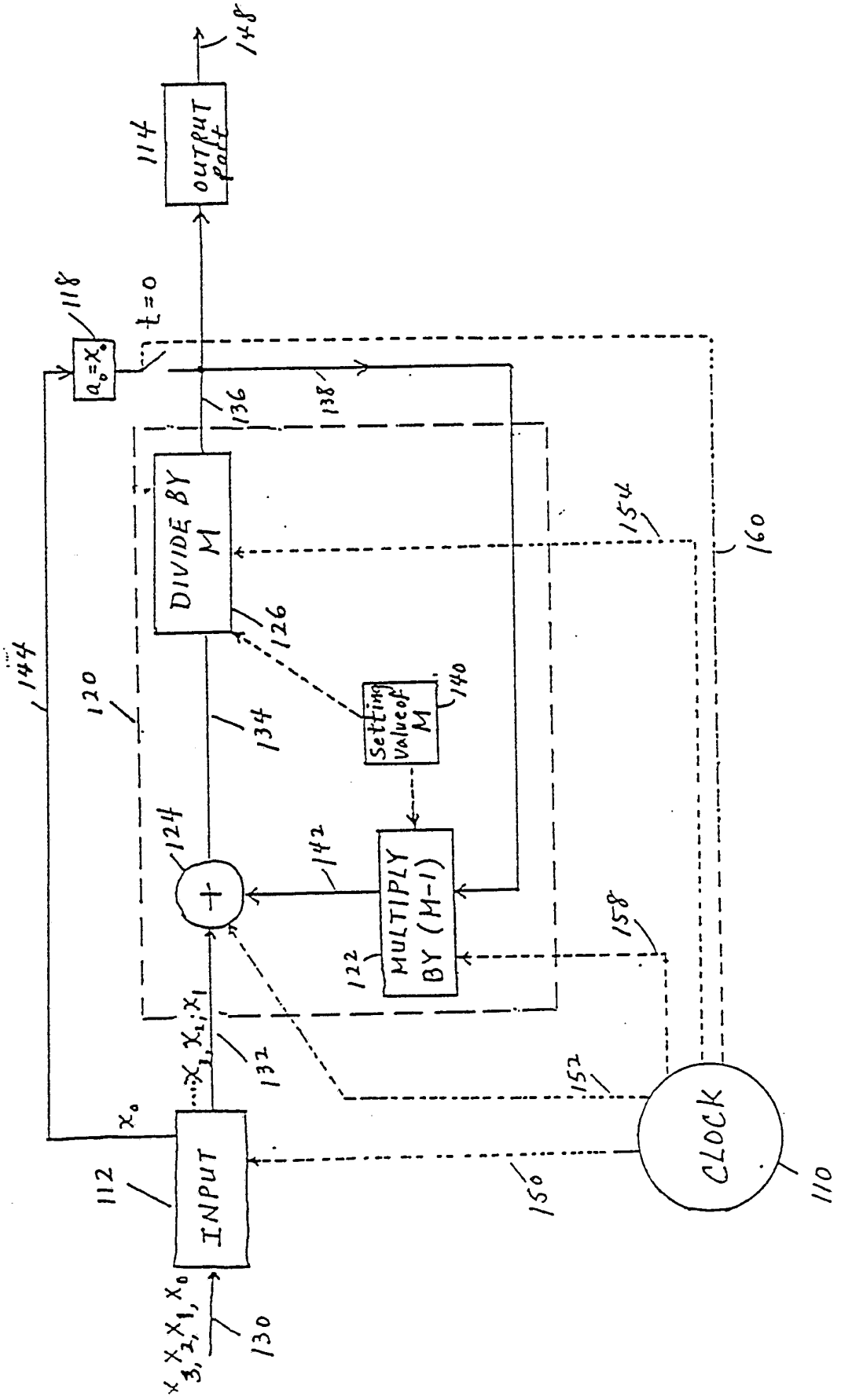

148
114
OUTPUT path
118
$a_0 = X_0$
t = 0
136
138
DIVIDE BY M
154
160
126
144
120
134
140
Setting Value of M
124
142
MULTIPLY BY (M-1)
122
158
$X_1, X_1; X_1$
132
X_0
152
112
INPUT
CLOCK
150
110
X_3, X_2, X_1, X_0
130

FIG 3

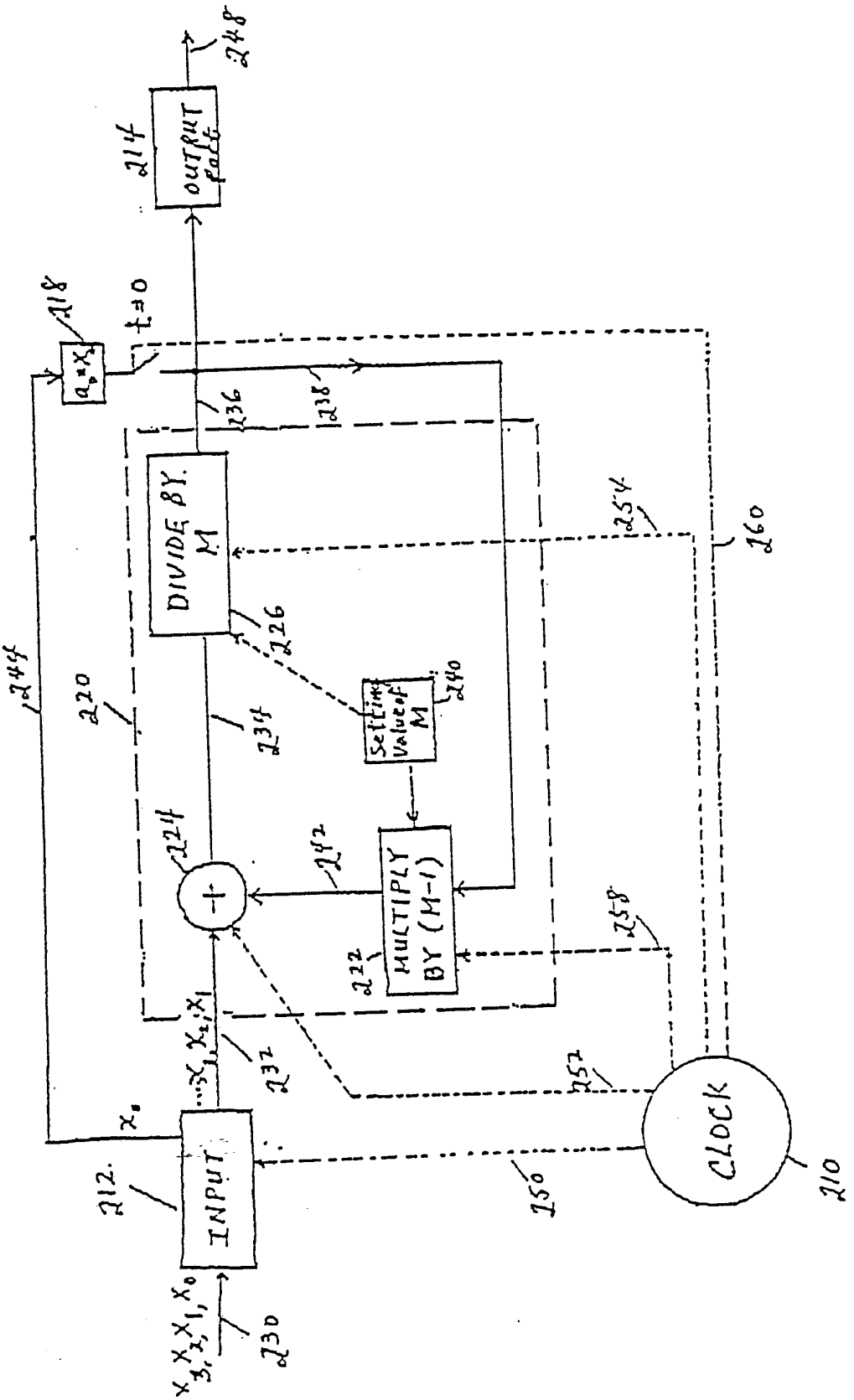
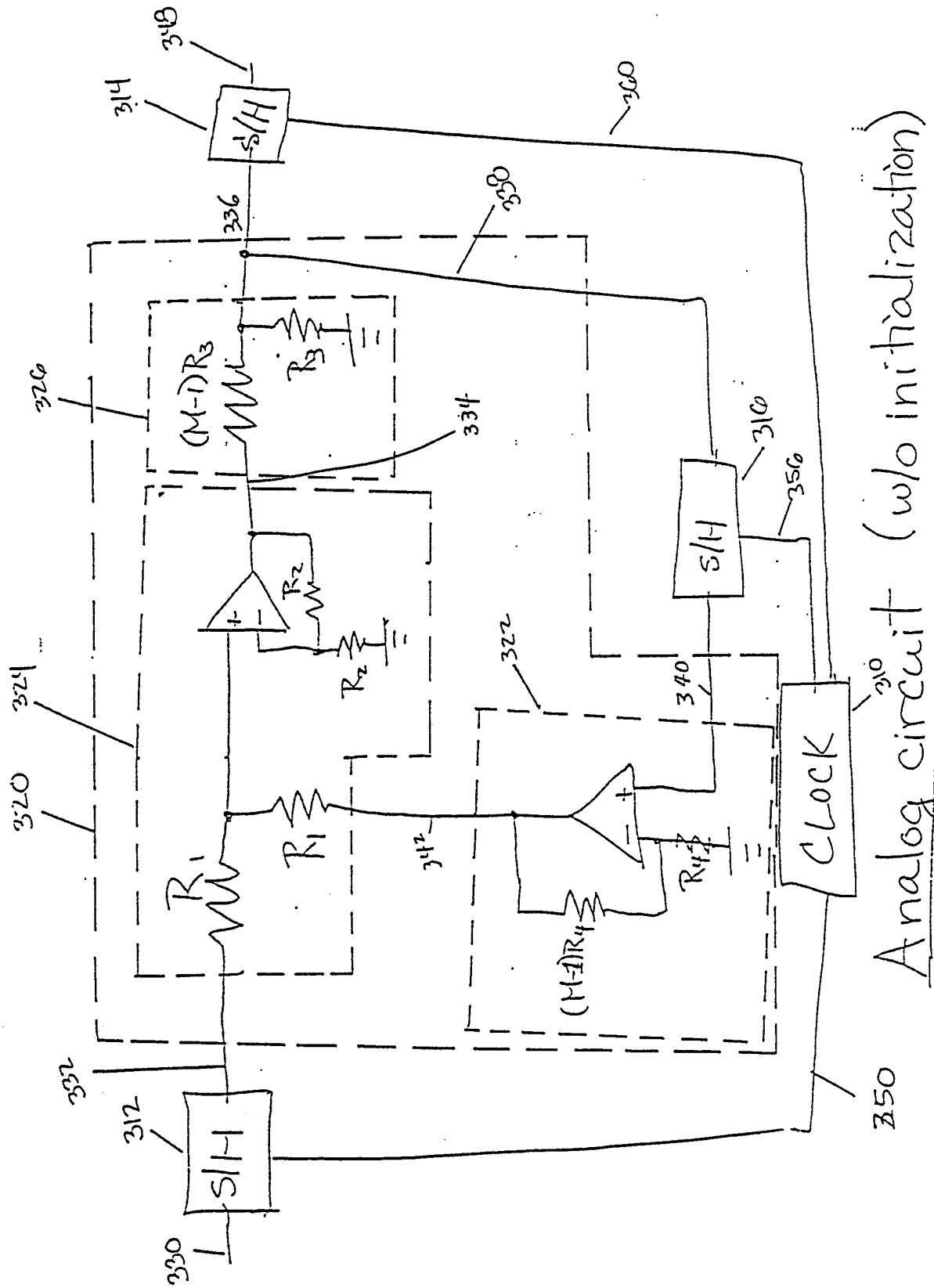

248
OUTPUT Data
214
t=0
218
$a_0 * X_0$
236
238
DIVIDE BY M
254
160
244
220
226
234
Setting Value of M
240
224
242
MULTIPLY BY (M-1)
222
258
$X_0 X_1 X_2 \ldots$
232
252
X_0
212
INPUT
150
CLOCK
210
$X_0, X_1, X_2, X_3 \ldots$
230

FIG 4



Analog circuit (w/o initialization)

FIGURE 5

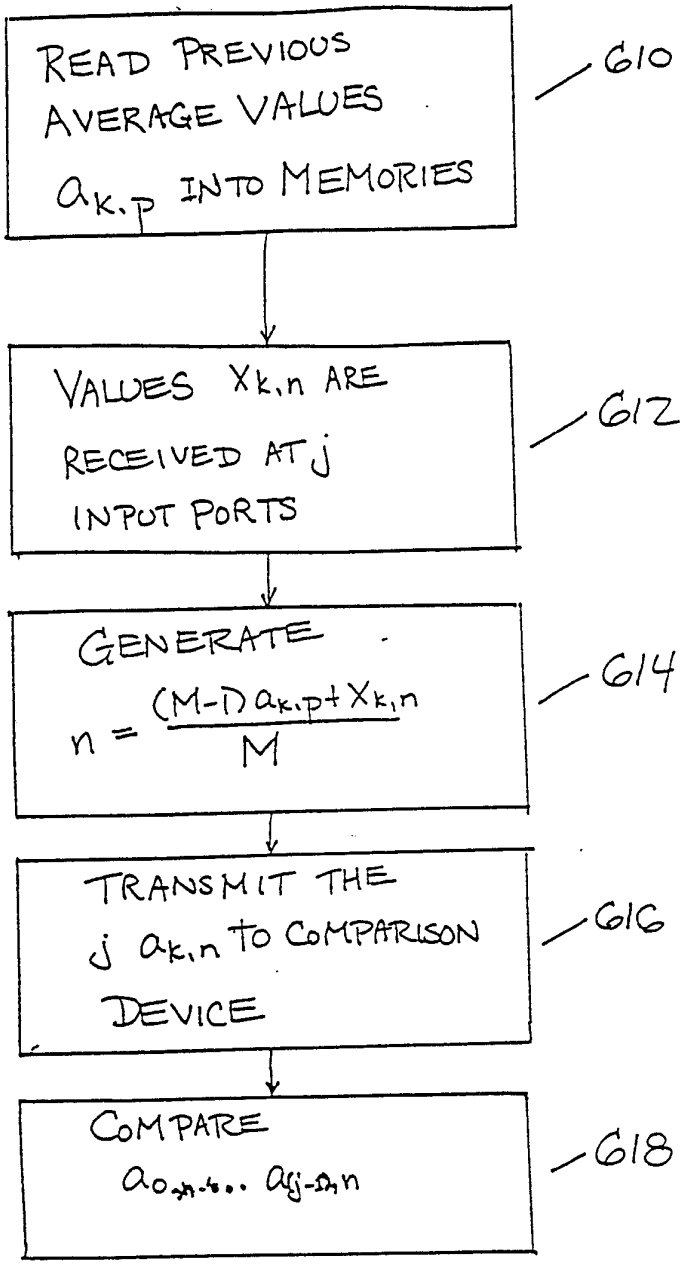

READ PREVIOUS AVERAGE VALUES $a_{k,p}$ INTO MEMORIES
610
VALUES $X_{k,n}$ ARE RECEIVED AT j INPUT PORTS
612
GENERATE $n = \frac{(M-1)a_{k,p}+X_{k,n}}{M}$
614
TRANSMIT THE j $a_{k,n}$ TO COMPARISON DEVICE
616
COMPARE $a_{0,n}$ ... $a_{j-1,n}$
618

FIGURE 6

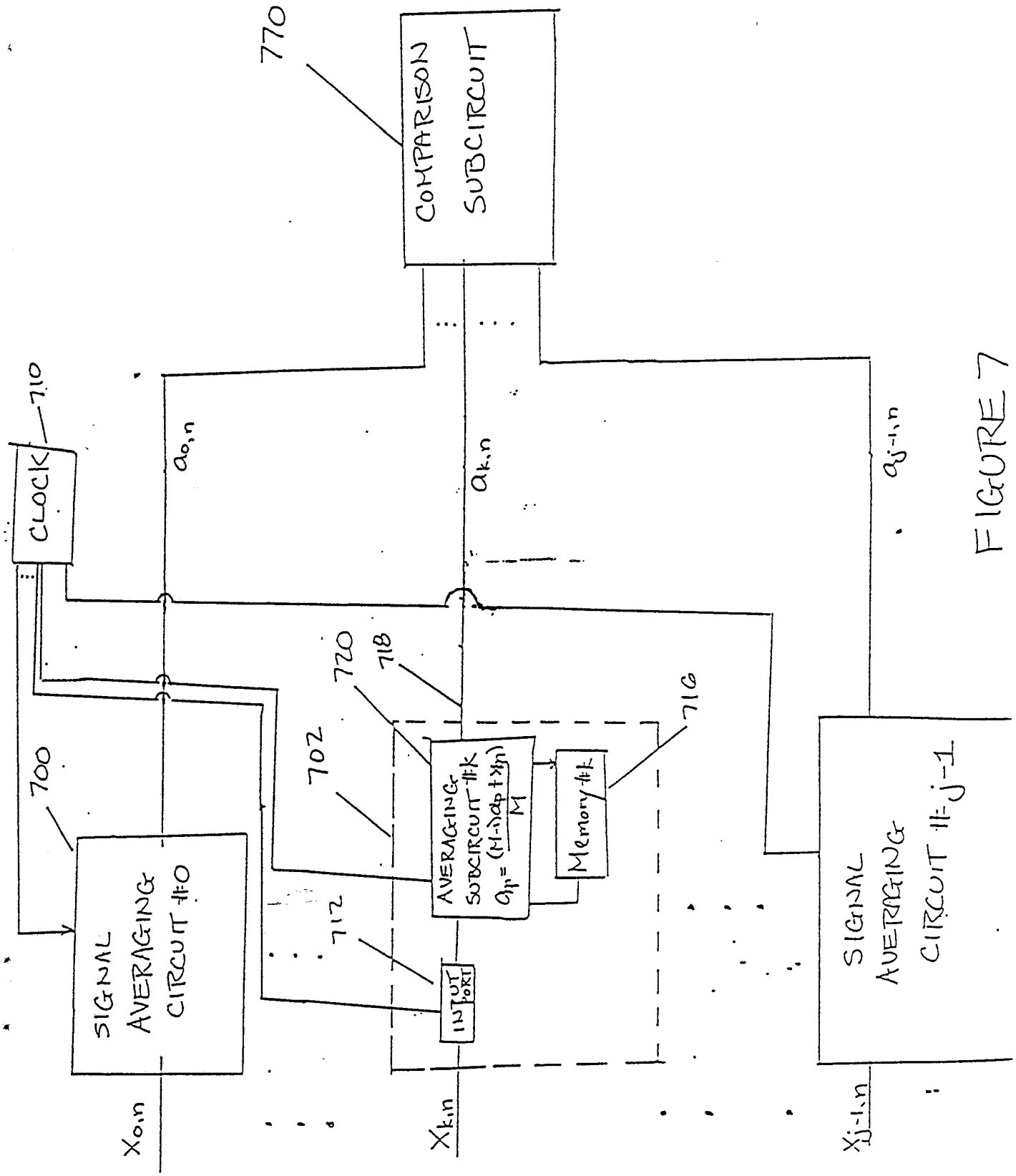

770
COMPARISON SUBCIRCUIT
710
CLOCK
$a_{0,n}$
$a_{k,n}$
$a_{j-1,n}$
700
SIGNAL AVERAGING CIRCUIT #0
702
720
718
716
AVERAGING SUBCIRCUIT #k
$a_{k,n} = \frac{(N-1)a_{k,n-1} + x_{k,n}}{N}$
Memory #k
712
INPUT PORT
SIGNAL AVERAGING CIRCUIT #j-1
$x_{0,n}$
$x_{k,n}$
$x_{j-1,n}$

FIGURE 7

INTERNATIONAL SEARCH REPORT

PCT/US92/08242

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G06F 7/38
US CL :364/734,811
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 364/734,811

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US,A, 4,054,786 (Vincent) 18 October 1977.	1-2 & 4-6 3 & 7-10
X Y	US,A, 3,478,328 (Schillinger) 11 November 1969.	1-2 & 4-6 3 & 7-10
A	US,A, 4,551,817 (Ishikawa) 05 November 1985.	1-10
A	US,A, 4,193,118 (Nash et al.) 11 March 1980.	1-10
A	US,A, 4,789,953 (Gerrath) 06 December 1988.	1-10

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 04 NOVEMBER 1992	Date of mailing of the international search report 14 DEC 1992
Name and mailing address of the ISA/ Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer DAVE MALZAHN Telephone No. (703) 308-1587

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/08242

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,D	US,A, 5,068,818 (Uramoto et al.) 26 November 1991.	1-10
A	US,A, 3,809,874 (Dozzetti et al.) 07 May 1974.	1-10