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(54) **METHOD OF PROGRAMMING AND ERASING MULTI-LEVEL FLASH MEMORY**

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(76) Inventors: **TSO-HUNG FAN**, Taipei Hsien (TW);
Chih-Chieh Yeh, Hsinchu (TW);
Tao-Cheng Lu, Hsinchu (TW)

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Correspondence Address:

J.C. Patents
Suite 250
4 Venture
Irvine, CA 92618 (US)

(57) **ABSTRACT**

A programming method of the multi-level flash memory comprises shooting a programming voltage that is increasing upwards stepwise each time into the gate of the multi-level flash memory, and following, shooting a program verify voltage that is decreasing downwards to program a multi-level in the multi-level flash memory and shooting an additional programming voltage into the multi-level flash memory after the last program verify voltage is shot. An erasing method of the multi-level flash memory comprises shooting an erasing voltage that is decreasing downwards stepwise each time into a gate of the multi-level flash memory, and following, shooting a erase verify voltage that is increasing upwards to erase a multi-level in the multi-level flash memory and shooting an additional voltage into the multi-level flash memory after the last erase verify voltage is shot.

(21) Appl. No.: **11/616,770**

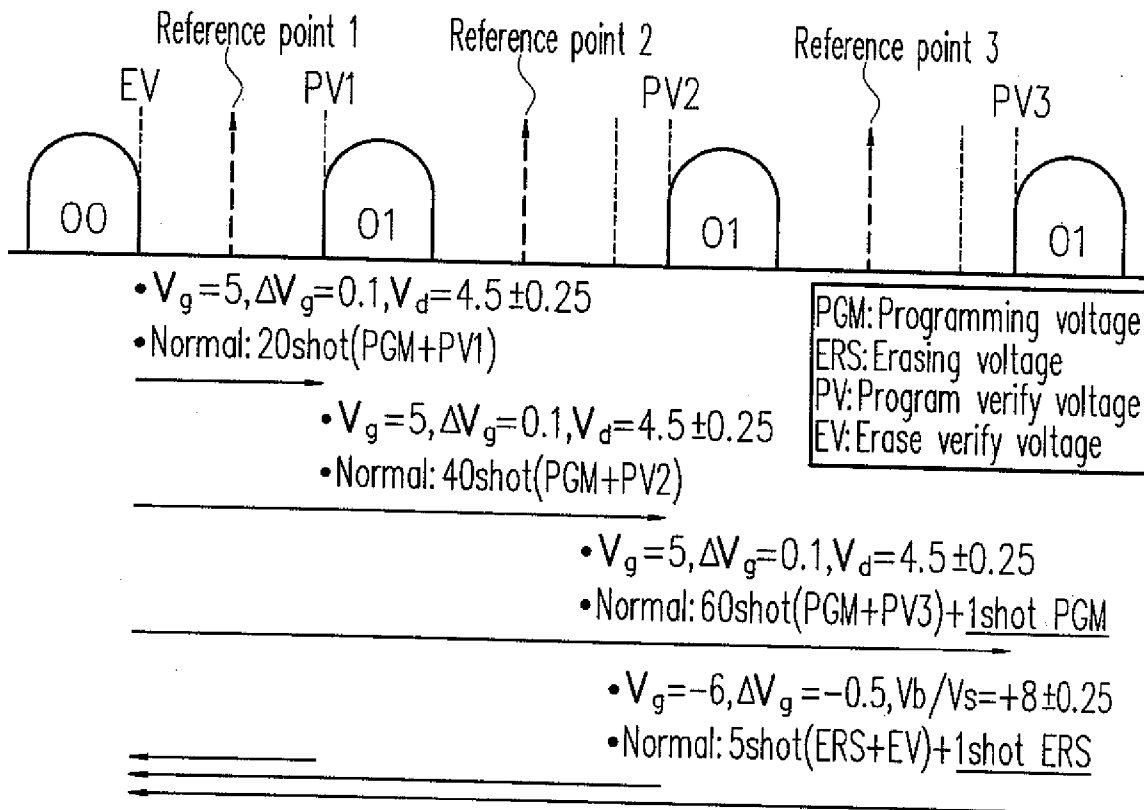
(22) Filed: **Dec. 27, 2006**

Related U.S. Application Data

(60) Continuation of application No. 11/198,684, filed on Aug. 4, 2005, now Pat. No. 7,173,849, which is a division of application No. 10/065,761, filed on Nov. 15, 2002, now Pat. No. 6,958,934.

(30) **Foreign Application Priority Data**

Jan. 17, 2002 (TW)..... 91100639



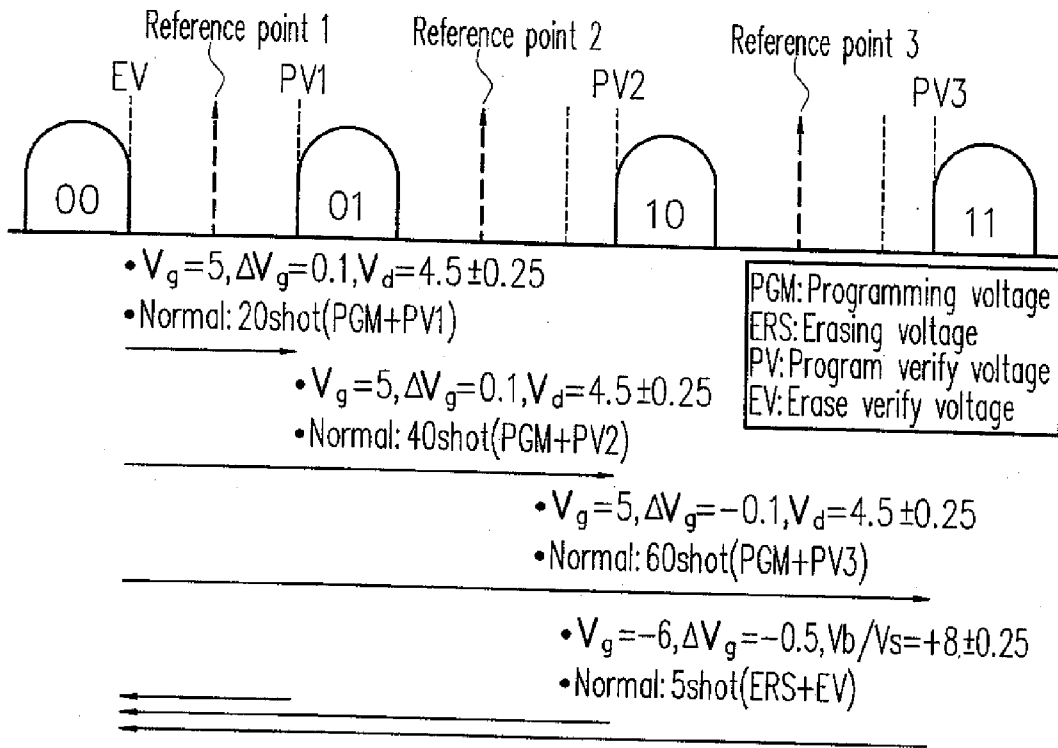


FIG. 1

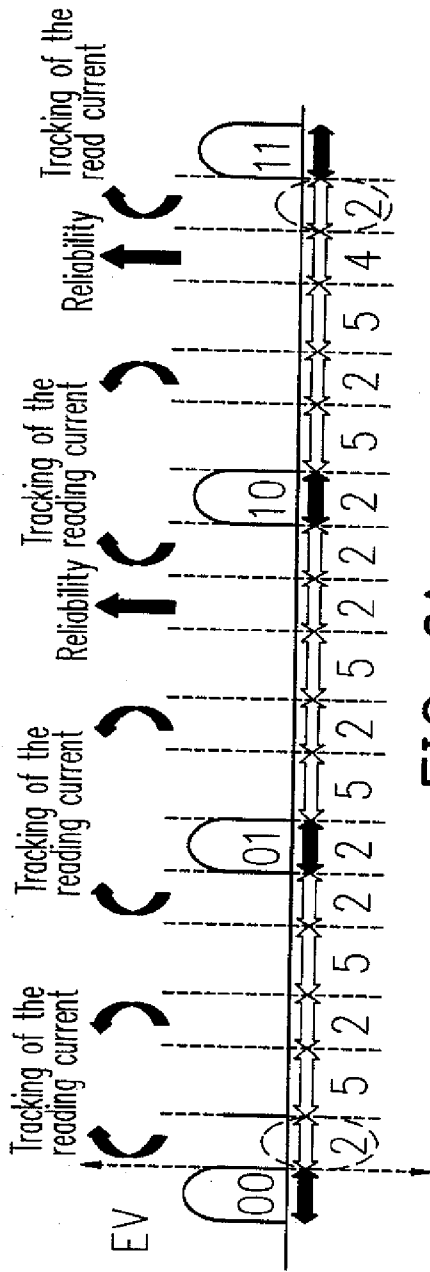


FIG. 2A

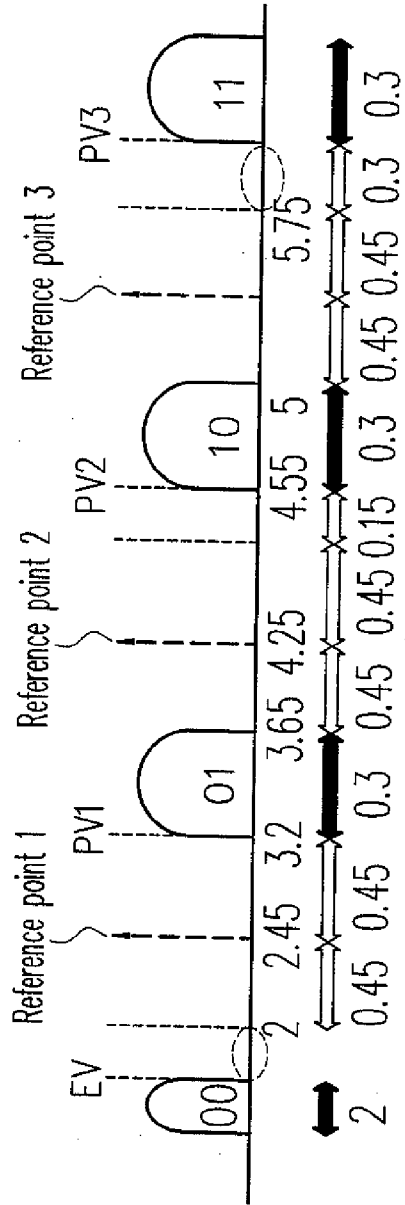


FIG. 2B

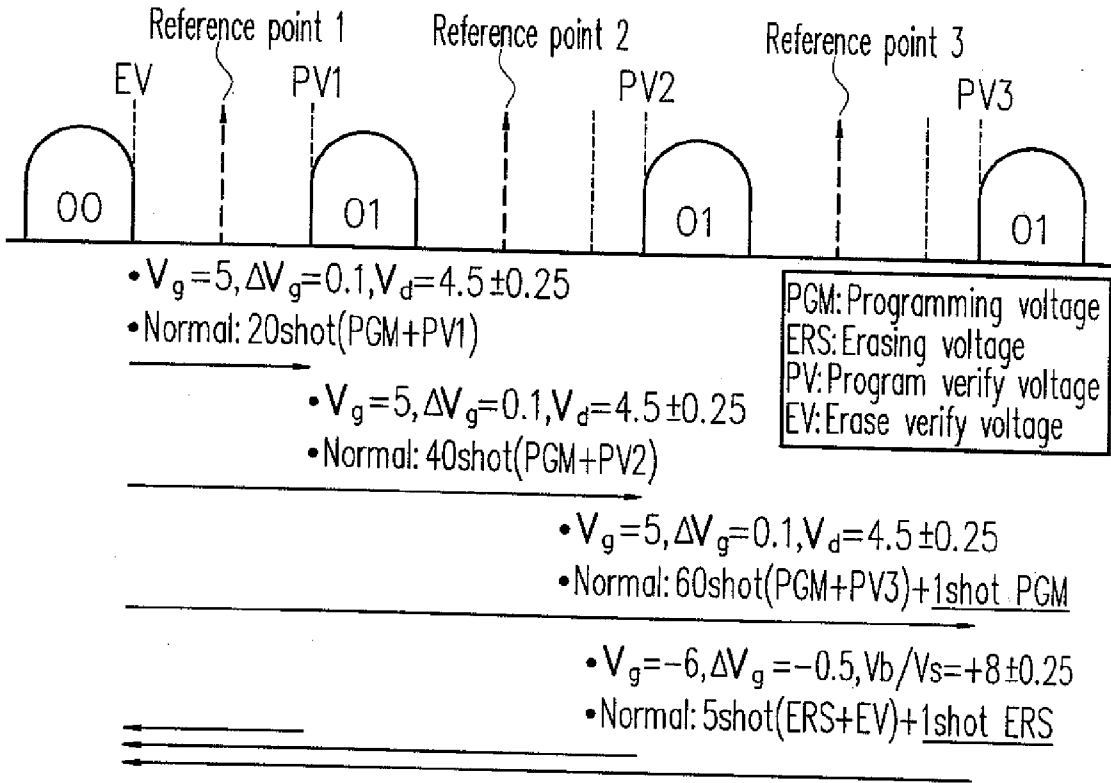


FIG. 3

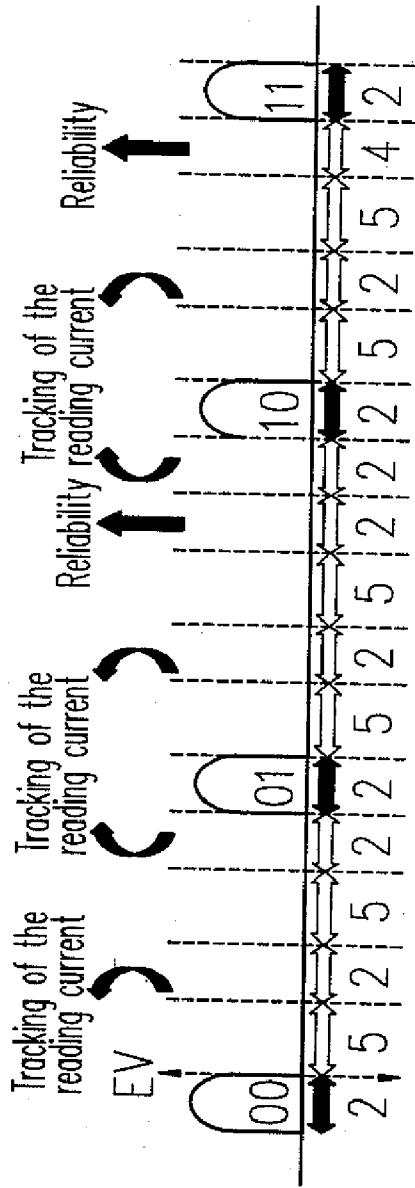


FIG. 4A

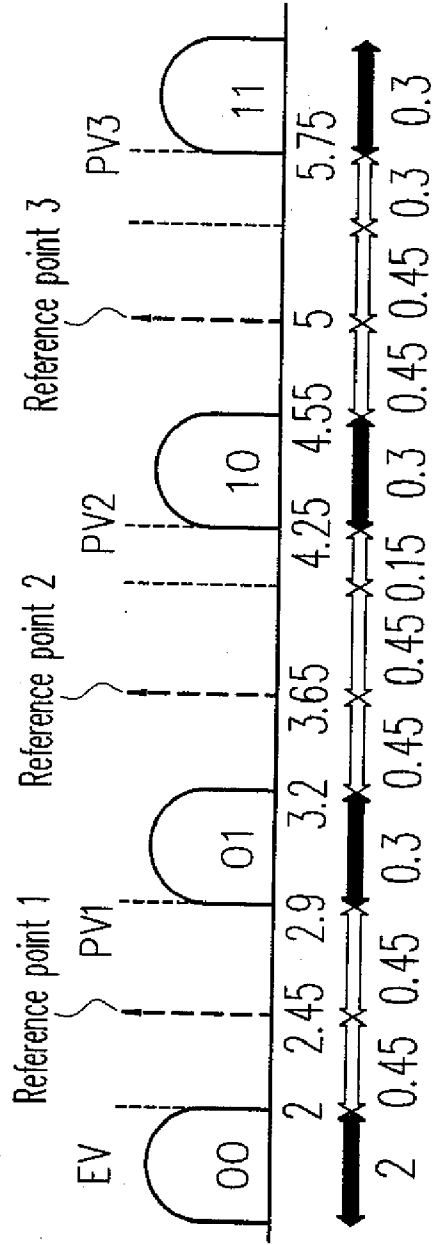


FIG. 4B

METHOD OF PROGRAMMING AND ERASING MULTI-LEVEL FLASH MEMORY

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the priority benefit of Taiwan application serial no. 91100639, filed Jan. 17, 2002.

BACKGROUND OF THE INVENTION

[0002] 1. Field of Invention

[0003] The present invention generally relates to a programming and erasing method of flash memory, and more particularly, to a programming and erasing method of multi-level flash memory.

[0004] 2. Description of Related Art

[0005] In the process of programming and erasing a flash memory bit, in order to have the flash memory describe the binary state and the trinity state, or state, (00, 01, 10, 11 state or 000, 001, 010, 011, 100, 101, 110, 111 state, or . . . state), the means of changing the gate voltage of the flash memory periodically is commonly used to limit the number of the gate voltage shooting times, so that the channel of the flash memory is able to generate the channel hot electrons, and the state when the channel hot electrons are injected to the floating gate via the channel can be different. For example, in order to have multi-level flash memory that represents the binary state describing the multi-level state of the binary bit, its floating gate must have the capacity to store electrons with four different electron distribution states. When the flash memory represents the 00 state value, there is an electron distribution corresponding to the 00 state value stored in the floating gate.

[0006] The conventional programming method of the flash memory is: when the flash memory programs from state 00 to 01, 10 or 11 state, the gate voltage V_g is shot into the gate of the flash memory. The gate voltage V_g is increased by 0.1 volt every time it is shot into the gate (i.e. ΔV_g is 0.1 volt), and is sustained for about 150 ns every time. The programming of flash memory to the 01 or 10 or 11 states from 00 state is determined by the number of times the gate voltage V_g is shot into gate. Where a program verify voltage is carried by the programming voltage in each operation.

[0007] When the flash memory is erased to 00 state from 01 or 10 or 11 state, the gate voltage V_g is decreased by 0.5 volt every shot into the gate (i.e. ΔV_g is -0.5 volt), and is sustained for about 100~500 μ s every time. The number of times the gate voltage V_g is shot into the gate to erase to 00 state from 01 or 10 or 11 states. Where an erase verify voltage is carried by the erasing voltage in each operation.

[0008] Referring to FIG. 1, when the flash memory is programmed to 01 state from 00 state, the gate voltage V_g initially at S volts, and ΔV_g of 0.1 volt, the source voltage of ground, and the drain voltage V_d of 4.5 ± 0.25 volt are shot 20 times. When the flash memory is programmed to 10 state from 00 state, the gate voltage V_g initially at 5 volts, and ΔV_g of 0.1 volt, the source voltage of ground, and the drain voltage V_d of 4.5 ± 0.25 volt are shot for 40 times. When the flash memory is programmed to 11 state from 00 state, the gate voltage V_g initially at 5 volts, and ΔV_g of 0.1 volt, the source voltage of ground, and the drain voltage V_d of

4.5 ± 0.25 volt are shot for 60 times. In addition to the different number of shot times respectively corresponding to the different states, the last gate voltage V_g shot is the program verify voltage PV, and all the shots including the second to last V_g shot before the very last shot is the program voltage PGM.

[0009] When the flash memory performs an erase operation from 01 or 10 or 11 state to 00 state, the source voltage V_s and the bulkvoltage V_b of $+8 \pm 0.25$ volt, the gate voltage V_g initially -6 volts with ΔV_g is -0.5 volt are shot 5 times.

[0010] FIG. 2A and FIG. 2B show the distribution of the reading current I_r and the initial voltage V_t when the programming and erasing of the flash memory are finished and the flash memory state is determined. During programming of the multi-flash memory, if the sense margin in each tracking of the reading current is not high enough misjudgments of the multi-flash memory will easily occur. The problem is more likely to happen at the lowest state or highest state. As shown in FIG. 2A, the tracking of the reading current I_r is distributed in all the 00, 01, 10 and 11 states, and the reliability interval exists in between the tracking of the reading current I_r . The sense margin of each state comprises the partial range of the corresponding tracking of the reading current I_r . The reliability interval for separating each tracking of the reading current I_r is quite narrow. Furthermore, the reliability interval also limits the increase of the sense margin, and so engenders errors, especially when the flash memory is in 00 or 11 state. In FIG. 2B, the voltage interval of the operation initial voltage V_t for determining the state of the flash memory is also too narrow, so as to easily engender errors especially when the flash memory is in 00 or 11 state.

SUMMARY OF THE INVENTION

[0011] In view of this, the present invention provides a programming method of the multi-level flash memory for decreasing the tracking range of the reading current I_r and decreasing the voltage range of the operation initial voltage V_t . As a result fewer errors occur when judging the multi-level flash memory to provide correct segmentation of the multi-flash memory using the same number of states in a smaller tracking range of the reading current when designing the judgment of the multi-level flash memory.

[0012] The present invention provides a programming method of the multi-level flash memory, comprising: comprising shooting a stepwise increasing upwards programming voltage into to the gate of the multi-level flash memory to change the state of the multi-flash memory. An additional programming shot is performed after the multi-flash reaches the highest state.

[0013] The present invention further provides an erasing method of the multi-level flash memory, comprising: shooting a stepwise decreasing downwards erasing voltage into the gate of the multi-level flash memory to clear the state of the multi-level flash memory. An additional erasing shot is performed after the last erase shot during any state of the multi-level flash.

[0014] In summary, the present invention increases the potential of the programming voltage of the multi-level flash memory and decreases the potential of the erasing electron of the multi-level flash memory by adding one additional

programming voltage and one additional erase voltage, so that when the multi-level flash memory is programmed, a smaller reading current tracking range and a smaller voltage tracking range of the operation initial voltage are provided, thus fewer errors occur.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention. In the drawings,

[0016] FIG. 1 schematically shows a conventional programming and erasing method of the flash memory;

[0017] FIG. 2A shows the conventional reading current tracking diagram of the flash memory;

[0018] FIG. 2B shows the conventional initial voltage tracking diagram when the flash memory is read;

[0019] FIG. 3 schematically shows the programming and erasing method of the flash memory of the preferred embodiment according to the present invention;

[0020] FIG. 4A schematically shows the reading current tracking diagram of the preferred embodiment according to the present invention; and

[0021] FIG. 4B schematically shows the initial voltage tracking diagram when the flash memory of the preferred embodiment according to the present invention is read.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] The present invention applies the gate voltage to the gate of the flash memory and applies the drain voltage to the drain of the flash memory. The source is grounded, and the voltage value of the gate voltage shot into the gate is increased upward stepwise, so that the hot electrons in the flash memory channel are injected and stay in the floating gate of the flash memory via the channel. The electrons in the floating gate are provided with different electron distribution due to different gate voltage shot times to represent flash memory having different states. When the method is applied to a full program of the flash memory, an additional program verify voltage is shot into the gate of the flash memory. That is, if 20 voltage shots are needed for the flash memory to program the state value of 01, 20 programming voltages and one additional gate voltage is shot. When multi-flash memory of the present invention erases the flash memory, the gate voltage is applied to the gate of the flash memory, or the source voltage is applied to the source of the flash memory and is $+8\pm 0.25$ volt, and the bulkvoltage is applied to the base of the flash memory, and the drain is floating. The voltage value of the gate voltage that is shot into the gate is decreased downward stepwise, so that the electrons in the floating gate of the flash memory are ejected. Eventually no electrons exist in the floating gate, so that the multi-level flash memory is erased. Furthermore, when a full erase of the flash memory is performed, an additional voltage is shot into gate voltage after the completion of the erase operation.

[0023] The present invention adds one additional programming voltage when the highest state is programmed into the flash memory and adds one additional erase voltage when the flash memory is erased. FIG. 3 schematically shows the sketch map of the programming and erasing method of the flash memory of the preferred embodiment according to the present invention. The flash memory is programmed to 01 state from 00 state, the source of the flash memory remains grounded, and the drain voltage V_d is 4.5 ± 0.25 volt, the gate voltage V_g starts from 5 volts, and is increased upwards by $\Delta V_g=0.1$ volt after performing 20 shots wherein 19 are programming voltage PGM and the last is programming confirmation voltage PV1.

[0024] The flash memory is programmed to 10 state from 00 state, the source of the flash memory remains ground, and the drain voltage V_d is 4.5 ± 0.25 volt, the gate voltage V_g initially 5 volts, and is increased upward by $\Delta V_g=0.1$ volt stepwise after performing 40 shots wherein 39 are PGM shots and a last programming confirmation voltage PV2 is shot.

[0025] The flash memory is programmed to 11 state from 00 state, the source of the flash memory remains grounded, and the drain voltage V_d is 4.5 ± 0.25 volt, the gate voltage V_g initially 5 volts, and is increased upward by $\Delta V_g=0.1$ volt each time after 61 shots wherein 59 are PGM shots and one confirmation voltage PV3 are shot, and an additional one time of PGM shot.

[0026] The flash memory performs an erase operation from state 11 to state 00, the drain is floating at the present state and the source voltage V_s or the V_b is $+8\pm 0.25$ volt, the gate voltage V_g starts from -6 volts and is decreased downward by $\Delta V_g=-0.5$ volt each time after performing 6 erase voltage shots, wherein four are ERS shots, one is an erase confirmation voltage EV, and an additional erase voltage.

[0027] The increase in the number of shooting times of the programming voltage PGM into the flash memory is not limited by the highest state value. A programming voltage PGM can be increased after the last program verify voltage PV is shot when programming anyone value.

[0028] A major characteristic of the present invention is that in the programming process of the flash memory, one additional programming voltage PGM shot is added after the last program verify voltage PV is shot. In the erasing process of the flash memory, one additional erase voltage ERS shot is added after the last erase voltage ERS and erase verify shot.

[0029] The programming and erasing method of the flash memory of the preferred embodiment according to the present invention is able to obtain the reading current tracking diagram of the flash memory after the flash memory has been programmed, and the initial voltage tracking diagram of the flash memory when the flash memory is read. Please refer to FIG. 4A and FIG. 4B respectively, which respectively correspond to FIGS. 2A and 2B. As shown in FIG. 4A and comparing to FIG. 2A, the tracking of the reading current I_r of the flash memory in the 11 state is removed (the dot line portion), and the tracking of the reading current I_r of the flash memory is removed when 00 state is programmed to 11 state due to the additional shot of programming voltage. This ensures that the reading current

at state 11 is precisely within design limits. As a result, the removed segment in state 11 is originally used for error tolerance but now is no longer needed.

[0030] Similar to shooting an additional voltage during programming, an additional erase voltage is also shot during the erase of the multi-flash memory from state 11 to state 00. This ensures that the reading current in state 00 is precisely within the design limits. The removed segment in FIG. 2A is used for error tolerance but now is no longer needed.

[0031] The precise reading current in state 00 and state 11 due to the additional shot of program and erase voltage during programming and erasing of the multi-flash memory allows the tracking of reading current of the multi-flash memory in state 00 and state 11 to decrease. As a result, the exact state 00 and state 01 can be accurately determined.

[0032] Referring to FIG. 4B and comparing to FIG. 2B, FIG. 4B eliminated the segments represented in dotted lines in FIG. 2B. The initial operating voltage is decreased when the multi-flash memory changes state from 00 to 01 and 10 and 11. The additional shot of program and erase voltage during programming and erasing of the multi-flash memory reduces the initial operating voltage between state changes from 00 and 01, and 10 and 11. As a result, the exact state 00 and state 11 can be accurately determined.

[0033] Moreover, the present invention can be applied to the programming of any state of the flash memory, that is, the present invention is not limited to the programming of the highest value.

[0034] In summary, the present invention multi-level adds one additional programming voltage and one additional erase voltage respectively during the programming and erasing of the multi-level flash memory, the tracking of the reading current and the tracking of the initial voltage are decreased. The reduced reading current and initial voltage

can accurately determine the state of the multi-flash memory. Therefore, when the multi-level flash memory is programmed, a bigger sense margin can be provided, so that fewer errors occur.

[0035] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.

1-5. (canceled)

6. An erasing method of a flash memory comprising a floating gate, comprising:

applying an erasing voltage to draw charges out of the floating gate and change a state of the flash memory to an erased state; and

applying an additional erasing voltage to the flash memory after the erasing voltage is applied, wherein the additional erasing voltage is capable of adjusting the erased state of the flash memory.

7. The erasing method of claim 6, wherein the flash memory comprises a multi-level flash memory.

8. The erasing method of claim 7, wherein the erased state of the multi-level flash memory is a state of a lowest value of the multi-level.

9. The erasing method of claim 6, wherein the flash memory comprises a binary flash memory.

10. The erasing method of claim 6, wherein the erasing voltage is applied multiple times.

11. The erasing method of claim 10, wherein electrons are drawn out of the floating gate by the erasing voltage and the erasing voltage is decreased downward stepwise each time.

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