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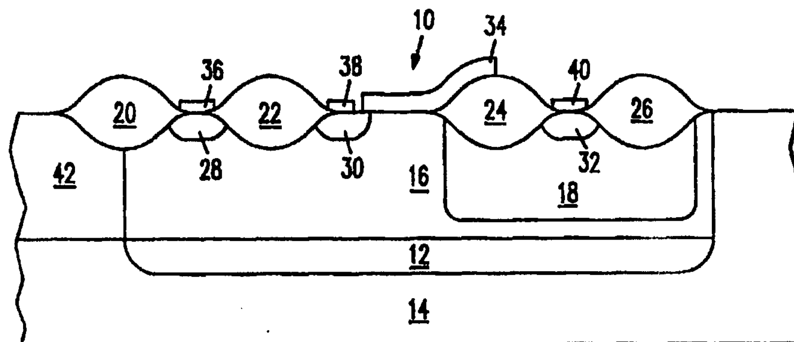

(57) Abstract

A low-voltage 0.8-micron CMOS process is modified by implanting arsenic or phosphorus during epitaxy in a p-type substrate (14) starting material to increase the depth of selected n-well areas (16) for the purpose of producing high-voltage transistors on the same substrate in the same CMOS process. Implanting boron in a p-field extension area (18) through partially formed field oxide insulators (24, 26) so that the diffusion of boron beyond the p-field extension area (18) is minimized, achieves a similar result. That is, breakdown and punch-through voltages are increased. Together, these make CMOS transistors which operate at a higher voltage range than either innovation alone.

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HIGH-VOLTAGE CMOS TRANSISTORS FOR A STANDARD CMOS PROCESS

Background of the Invention

1. Field of the Invention

The present invention relates to an apparatus of high-voltage (over 6 volts) transistors and diodes on the same substrate and made in the same process as
5 ordinary 5-volt CMOS (Complementary Metal Oxide Semiconductor) circuits and to a process for making the apparatus. More particularly, but not by way of limitation, the present invention allows logic circuitry to be fabricated in existing CMOS processes, while allowing interfacing to high-voltage circuits on the same silicon substrate.

10 2. Discussion

High-voltage capability has important applications in consumer electronics, automotive and other markets where many existing devices such as motors, transducers and actuators operate on high voltages. The present invention allows the logic circuitry to operate on power-saving low voltage while allowing the entire
15 device to be fabricated on a single silicon chip in an otherwise conventional CMOS process. For the purpose of this discussion, low voltage is a voltage of 6 volts and less, while high voltage is a voltage of over 6 volts.

Conventional CMOS logic integrated circuits (hereinafter CMOS chips) operate between 2.4 and 5 volts. The range of power supply voltages at which the
20 chip can operate is known as the operating voltage range. Typically a given chip can simply be powered with any power supply selected between 1.2 and 5 volts and the logic will operate with a logic low of 0 volts and logic high of the selected power supply voltage. Typically for battery-operated devices and other devices where a minimum of power consumption is desirable, the lowest possible voltage
25 is used. Although the use of this low voltage minimizes the power consumed, existing physical devices such as motors, transducers, and actuators operate

advantageously at higher voltages. Moreover, the trend is toward CMOS chips that operate at even lower voltages while these other components stay at their fixed voltages, and may even operate more efficiently at higher voltages.

The areas in which high-voltage CMOS chips will be useful are numerous. Applications in LCD active matrix technology, linear amplifiers, voltage translators, switching regulators, computer interfaces including the ubiquitous RS-232 interface and in computer disk drive read/write circuits are in need of this innovation. Numerous other applications will suggest themselves when the device becomes commercially available and thereby well-known. In short, any application which involves operating voltages outside of the presently limited range will benefit from the device. Moreover, as the geometry of the CMOS chips continues to shrink in size, the operating voltage range will be in even lower voltages which will greatly increase the need for the present invention.

As an example, an automobile may have a microprocessor controller that drives a 12-volt motor. For the purpose of this example, assume the motor does a particular physical task and therefore requires the same power output of 120 Watts, regardless of supply voltage. If the motor draws 10 Amperes of current through connections that through age and neglect have a resistance of 0.1 ohms, the power consumed in these connections is 10 Watts. On a 24-volt system, a motor of the same locomotive power would draw only 5 Amperes, dissipating only 2.5 Watts as heat. Similarly on a 6-volt system, the power dissipated as heat would be 40 Watts, a substantial fraction of the motor's power of 120 Watts. The ratio of power wasted to power consumed for the 6, 12, and 24-volt systems is, respectively, 33%, 8%, and 2%. This illustrates how a widely used system, the electrical system of automobiles, is unlikely to go to any lower voltage because of increasing inefficiency in the system as the voltage is decreased.

CMOS chips, on the other hand, have become more efficient at lower voltages. The 4000B series CMOS operates between 5 and 15 volts and has been widely used for over twenty years. However, it accomplishes its high-voltage range by using much larger transistors than are used in current CMOS submicron geometries. As device size was reduced and new CMOS series introduced, the operating voltage range dropped until today, as an example, the 4-bit National

Semiconductor COP424C CMOS microcontroller draws 3.5 milliwatts when operated at 5 volts, but only 0.29 milliwatts at 2.4 volts. Unfortunately for the car manufacturers, the upper limit of the supply voltage for this microcontroller is only 6 volts. Moreover, as modern fabrication techniques reduced device size, the typical maximum operating voltage has decreased. Using a 6-volt controller on a 12-volt system presently requires surrounding the chip with various external interface transistors at additional cost.

The additional transistors, required for the purpose of interfacing to the high voltage circuitry, became necessary as the same CMOS device miniaturization that decreased voltage and power requirements also decreased the depth of the semiconductor wells thereby decreasing the punch-through and breakdown voltages, giving rise to the lowered maximum operating voltages. The punch-through voltage of a CMOS gate is the voltage applied across the source and drain which, in and of itself and without regard to the voltage on the gate, causes significant current flow through the source and drain. Because the current flows without regard for the voltage on the gate of the device, the device is no longer functional. Moreover, the power dissipated by the device in such a condition typically destroys the device. The punch-through voltage is therefore the measure of how great a voltage can be switched by a given transistor. The breakdown voltage is analogously defined as the voltage between the gate and drain or between the gate and source which causes significant current flow through the gate. Insomuch as a CMOS transistor has an insulated gate, this too represents a breakdown of the transistor's function.

In a diode, which has only one junction, only the breakdown voltage is defined. The breakdown voltage is the voltage which reverse-biases the diode and causes significant current to flow through the diode. Unless the current is limited by external means, catastrophic overheating and subsequent destruction of the diode occurs. Because the diode has only one junction, punch-through voltage is not defined for the diode. Consequently, throughout this application, where the term punch-through occurs, the term is understood as applying only to transistors and its application to diodes is a nullity.

The punch-through and breakdown voltages in an integrated circuit are functions of the physical three-dimensional geometry of the circuit. If the resultant electric field within a device exceeds certain bounds, catastrophic electrical breakdown occurs based on the electric field and the device geometry. The geometry is controlled by the extent to and rate at which various dopants diffuse into a given substrate. Such dopants include boron, phosphorus, and arsenic.

The relative diffusion rates of the various dopants are important factors in determining the final device geometry. Different dopants diffuse at different rates and because diffusability is a steep function of temperature, the depth of diffusion is not a linear function of the time for which and temperature to which the wafer is heated. Because of this nonlinearity, heating the wafer twice for the same cumulative time does not produce the same depth of diffusion as heating the wafer once. Therefore, although the various thermal cycle times are stated and are in fact done to accomplish a particular task, the effect on the diffusion of the dopant is also a key issue in the ultimate placement of the doped regions. Consequently, final device geometry depends to a large extent on the overall sequence of events comprising the manufacture of the chip.

A need exists for, and the present invention is directed toward, a process that overcomes these shortcomings of the current CMOS apparatus of the conventional low voltage CMOS process and allows high-voltage devices to be fabricated on existing low-voltage submicron CMOS production lines.

Summary of the Invention

In the present invention, a low-voltage 0.8-micron CMOS process is modified by implanting a selected dopant during epitaxy in a p-type substrate starting material to increase the depth of selected n-well areas for the purpose of producing high-voltage transistors on the same substrate in the same CMOS process.

The present invention is accomplished by growing an epitaxial layer on a selected substrate, and implanting a dopant type into the epitaxial layer at a selected time during growth of the epitaxial layer to produce an implant zone to increase the breakdown and punch-through voltages. Next, a negatively doped n-well region is produced within the epitaxial layer, and a layer of field oxide is

grown at selected sites on the epitaxial layer. The next step is implanting source and drain regions within the n-well region with such regions separated by the field oxide for electrical insulation. Finally, a polysilicon gate is deposited between the source and drain regions.

5 In one embodiment of the present invention, the dopant type is arsenic which is implanted after completion of about 90 percent of the epitaxial layer. In another embodiment, the dopant type is phosphorus which is implanted after, or near, the completion of the growth of the epitaxial layer.

An object of the present invention is to provide high-voltage CMOS
10 transistors and diodes on the same substrate and manufactured in the same process as low-voltage CMOS transistors.

Another object of the present invention is to eliminate at the circuit board level, extra interface integrated circuits (ICs) by providing for translation to high-voltage on a low-voltage CMOS IC.

15 Yet another object of the present invention is to enable the high-voltage transistors needed to interface with liquid crystal and other displays and line drivers for RS-232 and other interface to be manufactured in the same process and in the same substrate as low-voltage CMOS transistors.

Another object is to provide such advantages in other interface circuits such
20 as those found in disc drives.

Other objects, features and advantages of the present invention will become apparent from the following detailed description when read together with the drawings and appended claims.

Brief Description of Drawings

25 FIG. 1 depicts a transistor made according to the present invention.

FIG. 2 is an arsenic implant in an epitaxial layer.

FIG. 3 shows exposed twin well pad oxide before removal of photoresist.

FIG. 4 depicts a step of local oxidation of silicon wherein boron is implanted.

30 FIG. 5 depicts the completion of local oxidation of silicon after the boron implant is made.

Detailed Description

As an example of the present invention, FIG. 1 depicts a cross-sectional view of a high-voltage transistor 10 made in a low-voltage 0.8-micron CMOS process. Selected transistors in the low-voltage 0.8-micron CMOS process are
5 modified to be high-voltage transistors by implanting arsenic 12 during epitaxy in a p-type silicon substrate 14 to increase the depth of an n-well 16. The present invention differs from the prior art in that the arsenic implant 12 increases the punch-through and breakdown voltages of the particular high-voltage transistor implanted. Alternatively, phosphorus may be used instead of arsenic in the arsenic
10 implant 12. However, for the sake of clarity, only "arsenic implant 12" is discussed and is not referred to as a "phosphorus implant 12." The arsenic implant 12 thus effects a high-voltage transistor on silicon that otherwise operates on low voltage. Another difference with the prior art is a p-field extension area 18 which is made by implanting boron. The shape of the p-field extension area 18 is
15 such that the effective cross-sectional area of the conductor does not constrain the electric field as in previous designs. The arsenic implant 12 and the boron p-field extension area 18 each operate separately and independently to raise the breakdown and punch-through voltages. Moreover, they operate in conjunction to raise the breakdown and punch-through voltages over the value that would exist
20 with either operating alone.

As in the case of the transistor 10, this diode in the present invention differs from the prior art in that the arsenic implant 12 increases the breakdown voltage of the particular high-voltage diode implanted. The arsenic implant 12 thus effects a high-voltage diode on silicon that otherwise operates low voltage.
5 Another difference with the prior art is the p-field extension area 18 which is made by implanting boron. The shape of the p-field extension area 18 is such that the effective cross-sectional area of the conductor does not constrain the electric field as in the previous designs. The arsenic implant 12 and the boron p-field extension 18 each operate separately and independently to raise the breakdown voltage.
10 Moreover, they operate in conjunction to raise the breakdown voltage over the value that would exist with either operating alone. A similar effect is achieved using phosphorus instead of arsenic in the arsenic implant 12.

As in the prior art, this device includes the p-field extension area 18 and areas of field oxide 20, 22, 24 and 26. Diffusion area 28 is an n^+ diffusion area
15 that provides an ohmic contact to the n-well 16. P^+ diffusion area 30 is in the n-well 16, so is the source (also 30) of the transistor 10. P^+ diffusion area 32, in the p-field extension area 18 is an ohmic contact for the drain (also 32) of the transistor 10. A polysilicon gate 34 is provided. A metallic n-well contact 36, typically titanium and tungsten, is provided for the n-well 16. Only a small part of
20 the metallic n-well contact 36 is shown because in an actual chip the metal would be used to connect the high voltage transistor 10 to other transistors or bonding pads. Similarly, metallic contact 38 connects the source 30 and metallic drain contact 40 connects the drain 32 to other devices on the chip or to bonding pads. P-wells 42 are optionally present and serve primarily to fully illustrate the
25 fabrication process.

In addition to depicting a transistor, the device in FIG. 1 can also be used as a diode. This diode is called the drain diode because one terminal, the anode is in common with the drain 40 of the transistor 10. The diode has its anode at the metallic drain contact 40 and its cathode at the n^+ diffusion area 28 which provides
30 an ohmic contact to the n-well 16. Used as a diode, current flows through the metallic contact 40, the p^+ diffusion area 32, the p-field extension area 18, the n-well 16, the arsenic implant 12, the n^+ diffusion area 28, and the metallic n-well

contact 36.

Having described a preferred embodiment of the present invention, an example process for fabricating it will now be given for the purpose of explanation. The process begins with a p^+ type substrate with crystallographic orientation <100> (not shown). In FIG. 2, a layer 14A of silicon approximately 22 μm thick is grown epitaxily on the substrate. This epitaxial layer of silicon 14A is not yet the full thickness of the p-type silicon substrate 14 in the other figures. For transistors especially selected to be high-voltage transistors, a special mask is used to implant arsenic only on regions in the epitaxy which will become high-voltage n-wells later in the process. The arsenic implant is done through a thin layer of oxide 46 in FIG. 2 whose thickness is about 120 Å. The oxide was formed during part of the epitaxial process. To do the arsenic implant, a layer of photoresist 48 is applied, masked to open areas to be implanted with arsenic, exposed to ultraviolet (UV) light, and developed in a suitable organic solvent. The solvent washes away the resist in areas to be implanted with arsenic.

In the exposed areas, arsenic is then implanted at an energy of 160 KeV using an ion implanter. Implantation continues until a dose of about 1×10^{13} to 1×10^{14} atoms per cm^2 is reached in the preferred embodiment of the invention. The photoresist is then removed. The arsenic implant 12 is driven in by heating at 1000°C for 21 minutes. The thin layer of oxide 46 is then etched off.

Again by way of example, computer simulation reveals that useful high voltage devices may be obtained with arsenic implanted to dose in the range of from about 1.0×10^{13} atoms per cm^2 to about 1.0×10^{14} atoms per cm^2. Moreover, concentrations over that range may yield desirable results. The remaining photoresist 48 is stripped off. Referring now to FIG. 3, the remaining steps to achieve this configuration will be given. Epitaxy is continued on the p-type silicon substrate 14 until a thickness of approximately 1.8 μm additional substrate is applied. This additional substrate makes up n-well 16 and p-type silicon substrate 42A which will later become p-well 42. Twin well pad oxide 50 is grown to a depth of about 450 Å and then a layer of silicon nitride 52 (Si_3N_4 or after this simply nitride) or other suitable mask material is deposited to a depth of about 1350 Å.

As an alternative to the arsenic implant phosphorus may be used. However, due to the greater diffusion rate of phosphorus, it must be implanted a little later in the process than the arsenic. Specifically, instead of implanting arsenic, the epitaxy is completed or nearly completed. Then, as described, the
5 remaining photoresist 48 is removed. Again referring to FIG. 3, the twin well pad oxide 50 is grown to a depth of about 450 Å. Phosphorus is implanted at an energy of between 140 KeV to 200 KeV or higher at a dose sufficient to achieve and ultimate concentration in the range of 1×10^{16} to 1×10^{17} atoms per cm^3. The nitride 52 or other mask is then deposited to a depth about 1350 Å and the
10 phosphorus is driven in by heating for about 11 hours at a temperature suitable to achieve the above concentration. The remaining process is the same whether arsenic or phosphorus is used.

Photoresist 54 is then applied and exposed to light through the ion implantation mask to expose the nitride over areas selected to become n-wells 16.
15 The exposed nitride is then removed with a suitable etchant such as hydrofluoric acid (HF). Phosphorus ions having a kinetic energy of 140 KeV are then implanted to a dose of about 4.5×10^{12} atoms per cm^2. FIG. 3 depicts the relevant part of the silicon wafer at this point in the process. The photoresist 54 is then stripped. The nitride mask remains to be used in the local oxidation of silicon
20 (LOCOS). The oxide is then grown to a depth of about 5000 Å by exposure to 1200° C dry heat. The nitride 52 is cleaned off. The p-type silicon substrate 42A are then implanted with BF_2 at an energy of 150 KeV to a dose of 2.7×10^{12} atoms per cm^2.

Continuing the process, p-type silicon substrate 42A became a p-well
25 during implantation. The oxide is then selectively etched back such that oxide 2400 Å thick remains over the n-well 16 and oxide 1850 Å thick remains over the p-well 42. The n-well 16 and p-well 42 are then driven in. That is, the wafer is heated to 1150°C for sufficient time to increase the depth of the n-well 16 to 1.8 μm and the depth of the p-well 42 to 2.0 μm. The difference in depths is largely
30 attributable to the differences in the diffusion rates of the respective dopants.

Turning now to FIG. 4, the following additional steps are done to achieve it. As before, the p-type silicon substrate 14, arsenic implant 12, n-well 16, and

p-well 42 are shown. New features are 200 Å composite pad oxide 50, 1850 Å composite nitride 52, and photoresist 54. The steps to form these new features are: deposit the 200 Å of composite pad oxide 50 and the 1850 Å of composite nitride 52; spin on a layer of photoresist 54; expose the photoresist 54 using a
5 mask to achieve the pattern shown; develop the photoresist 54; etch the nitride 52; clean off the photoresist 54; etch the composite pad oxide 50; grow about half (3250 Å) a field oxide 56; spin on a layer of photoresist 54; and expose it using a p-field extension mask; develop the photoresist 54. A p-field extension area 18 is implanted using BF_2 at an energy of 140 KeV to a dose of 5.5×10^{13} atoms per
10 cm^2. The present situation of the silicon is illustrated in FIG. 4. The photoresist 54 is removed and the remaining field oxide 56A is next grown to about 6500 Å, as shown in FIG. 5 as field oxide 56A.

To accomplish the remaining fabrication to complete the transistor 10 shown in FIG. 1, the process is similar to that used in existing CMOS technology.
15 The composite nitride 52 and composite oxide 50 are etched away. Next 200 Å gate oxidation is formed and a V_t implant is done. That is, boron is implanted using BF_2 at an energy of 25 KeV to a dose of 1.5×10^{12} atoms per cm^2. The effect on the transistor 10 is to allow an independent adjustment of the threshold voltage V_t.

20 The next step in the process is to form the polysilicon gate 34 in FIG. 1. This is done by depositing 4000 Å of polysilicon. Resist is then spun on the front side of the wafer. The polysilicon is then etched in a plasma process and the backside oxide is then removed by a buffered etchant. The frontside resist is then removed. The polysilicon is doped by phosphorous to a concentration of 1×10^{20}
25 to 1×10^{21} atoms per cm^2, and deglazed by hydrofluoric acid (HF) with a concentration of 10:1 for 2 minutes. The polysilicon is then etched by the usual resist, mask, expose, develop, etch, remove resist sequence. The polysilicon gate 34 is now formed as depicted in FIG. 1. Seal oxidation to seal the poly at the sides and to protect the surface of the silicon is then performed to a thickness of
30 80Å by exposing the wafer to 900°C dry heat for 50 minutes.

Next the n^+ diffusion areas 28 and the two p^+ diffusion areas 30 and 32 are formed. The drain contact is formed by the technique known as lightly doped drains (LDD). The LDD blocking mask is then used to block everything in FIG. 1 except for the substrate which becomes the n^+ diffusion areas 28.
5 Phosphorous ions are implanted at an energy of 50 KeV to a dose of 2.3×10^{13} atoms per cm^2. At this point the ohmic contact has an n-doping. After this step 2000 Å spacers are formed by oxidation of the silicon. The spacers are then etched back for the purpose of completing LDD. The n^+ blocking mask is then used to expose only the n^+ ohmic contact to arsenic ions implanted at an energy of
10 40 KeV to a concentration of 3.0×10^{15} atoms per cm^2. The resist is removed and oxidation, known as poly oxidation is done to a depth of 150 Å. Next another mask is used to expose the two areas that become p^+ diffusion areas 30 and 32. These are doped with BF_2 ions at an energy of 45 KeV to a dose of 4.5×10^{15} atoms per cm^2. The resist is then removed.

15 The next major step in the process is dielectric deposition. First 500 Å of undoped plasma oxide is deposited. Then borophosphosilicate glass (BPSG) is deposited to a depth of 6000 Å. The glass is reflowed by heating to a temperature of 900°C for a time suitable to achieve the desired profile. Cap deposition is formed by oxidizing to a depth of 2000 Å.

20 The final step in the process is to form the metallic contacts 36, 38, and 40. The contact cuts are made using the contact mask. Next a layer of titanium (Ti) is deposited to a depth of 1000 Å. Titanium nitride (TiN) is formed to a depth of about 150 Å and titanium silicide ($TiSi_2$) is also formed to a thickness of 300 Å. Tungsten (W) is then deposited to a depth of 7500 Å. The combined metal layer
25 is then masked and etched to form metallic contacts 36, 38, and 40, completing the formation of the silicon structure in FIG. 1.

Although the above description combines the arsenic implant and the boron p-field extension, the combination is for the purpose of example. Extensive computer simulation was used to model the above example. The example was then
30 implemented in silicon and found to work in substantially the manner predicted. The same simulation shows that the arsenic implant alone increases the breakdown and punch-through voltages. The simulation further shows that the boron p-field

extension increases the breakdown and punch-through voltages.

By the way of further example, but not by way of limitation, at least three types of transistors may be made by way of this invention. These transistors are first, the transistor of the above example which contains both boron and arsenic; 5 second, a transistor having an arsenic implant without a boron p-field extension; and third, a transistor having a boron p-field extension without an arsenic implant. These three types of transistors may readily be combined on the same silicon substrate along with a fourth, low voltage CMOS transistor. Similarly, at least three types of diodes may be made by way of this invention. These diodes are 10 first, the diode of the above example which contains both boron and arsenic; second, a diode having an arsenic implant without a boron p-field extension; and third, a diode having a boron p-field extension without an arsenic implant. These three types of diodes may readily be combined on the same silicon substrate along with a fourth, low voltage CMOS diode. In addition, any of the three different 15 types of diodes and three different types of transistors may be combined in any combination on the same chip along with low-voltage diodes and low-voltage transistors.

The above description makes clear that the present invention is well adapted to carry out the objects and to attain the ends and advantages mentioned herein as 20 well as those inherent in the invention. While presently preferred embodiments of the invention have been described for purposes of this disclosure, the fact is understood that numerous changes may be made which will readily suggest themselves to those skilled in the art and which are encompassed within the spirit of the invention disclosed and as defined in the appended claims.

What is claimed is:

1. A process for increasing the operating voltage range of a group of selected individual CMOS transistors and diodes in a CMOS process, the process comprising:

growing an epitaxial layer on a selected substrate;

5 implanting a first dopant type into the epitaxial layer at a selected time during epitaxial growth in the group of selected transistor sites after epitaxy to produce an implant zone to increase the breakdown and punch-through voltages;

negatively doping an n-well region substantially within the epitaxial

10 layer;

growing a layer of field oxide at selected sites on the epitaxial layer;

implanting source and drain regions within the n-well region with the source and drain separated by the field oxide for electrical insulation; and

15 depositing a polysilicon gate between the source region and drain region.

2. The process of claim 1 wherein the first dopant type is arsenic.

3. The process of claim 2 wherein the first dopant type is implanted after completion of about 90% of the epitaxial layer.

4. The process of claim 1 wherein the first dopant type is phosphorus.

20 5. The process of claim 4 wherein the first dopant type is implanted substantially at the completion of the epitaxial layer.

6. The process of claim 1 wherein the step of growing the field oxide comprises growing first and second portions of the field oxide layer and wherein the process further comprises:

implanting boron to form a p-field extension area following the growing of
5 the first portion of field oxide so that the diffusion of the boron beyond the p-field extension area is minimized to increase the breakdown and punch-through voltages in the group of transistor and diode sites; and

wherein growing the second portion of the field oxide at selected sites on
10 the epitaxial layer following the step of implanting boron.

7. The process of claim 6 wherein the first dopant type is arsenic.

8. The process of claim 7 wherein the first dopant type is implanted after completion of approximately 90% of the epitaxial layer.

9. The process of claim 6 wherein the first dopant type is phosphorus.

15 10. The process of claim 9 wherein the first dopant type is implanted at substantially the completion of the epitaxial layer.

11. The apparatus of a CMOS integrated circuit with an increased operating voltage range of a selected group of individual CMOS transistors 10 and diodes achieved by the use of a low-voltage CMOS integrated circuit, the apparatus comprising:

5 an epitaxial layer on a selected substrate, the selected individual CMOS transistor and diode sites implanted with a first dopant type at a selected time during growth of the epitaxial layer to form an implant zone in the epitaxial layer to increase the breakdown voltage by minimizing subsequent diffusion of the implanted first dopant;

10 an n-well region 16 doped substantially within the epitaxial layer;
field oxide insulators at selected sites on the epitaxial layer;
a diffusion area forming the drain region in the n-well region;
a diffusion area forming the source region in the n-well region; and
a polysilicon gate between the source region and the drain region.

15 12. The apparatus of claim 11 wherein the first dopant type is arsenic.

13. The apparatus of claim 12 wherein the first dopant type is implanted after completion of approximately 90% of the epitaxial layer.

14. The apparatus of claim 11 wherein the first dopant type is phosphorus.

20 15. The apparatus of claim 14 wherein the first dopant type is implanted substantially at the completion of the epitaxial layer.

16. The apparatus of claim 11 wherein a p-field extension area is formed by implanting boron through partially formed field oxide insulators so that the diffusion of the boron beyond the p-field extension area is minimized to
25 increase the breakdown and punch-through voltages in the group of transistor and diode sites.

17. The apparatus of claim 16 wherein the first dopant type is arsenic.

18. The apparatus of claim 17 wherein the first dopant type is implanted after completion of about 90% of the epitaxial layer.

19. The apparatus of claim 16 wherein the first dopant type is
5 phosphorus.

20. The apparatus of claim 19 wherein the first dopant type is implanted substantially at the completion of the epitaxial layer.

21. The apparatus of a CMOS integrated circuit with an increased operating voltage range of a group of selected individual CMOS transistors and diodes achieved by the use of a low-voltage CMOS integrated circuit, the apparatus comprising:

5 an epitaxial layer on a selected substrate;
an n-well region doped substantially within the epitaxial layer;
field oxide insulators at selected sites on the epitaxial layer;
a p-field extension area formed in the selected individual transistor and diode sites of the group of transistors and diodes by implanting
10 boron through partially formed field oxide insulators so that the diffusion of the boron beyond the p-field extension area is minimized to increase the breakdown and punch-through voltages in the group of transistor and diode sites;
a diffusion area forming the drain region in the n-well region;
15 a diffusion area forming the source region in the n-well region; and
a polysilicon gate between the source region and the drain region.

22. The apparatus of claim 21 wherein arsenic is implanted after completion of about 90% of the epitaxial layer.

23. A process for increasing the operating voltage range of a group of selected individual CMOS transistors and diodes in a CMOS process, the process comprising:

growing an epitaxial layer on a selected substrate;

5 negatively doping an n-well region substantially within the epitaxial layer;

growing a portion of the field oxide at selected sites on the epitaxial layer;

implanting boron to form a p-field extension area so that the diffusion of the boron beyond the p-field extension area is minimized to increase

10 the breakdown and punch-through voltages in a second group of transistor sites;

growing the remaining portion of the field oxide at selected sites on the epitaxial layer;

implanting source and drain regions within the n-well region with the

15 source and drain separated by the field oxide for electrical insulation; and

depositing a polysilicon gate between the source region and drain region.

24. The process of claim 23 wherein arsenic is implanted after completion of about 90% of the epitaxial layer.

20 25. The process of claim 23 wherein phosphorus is implanted at substantially the completion of the epitaxial layer.

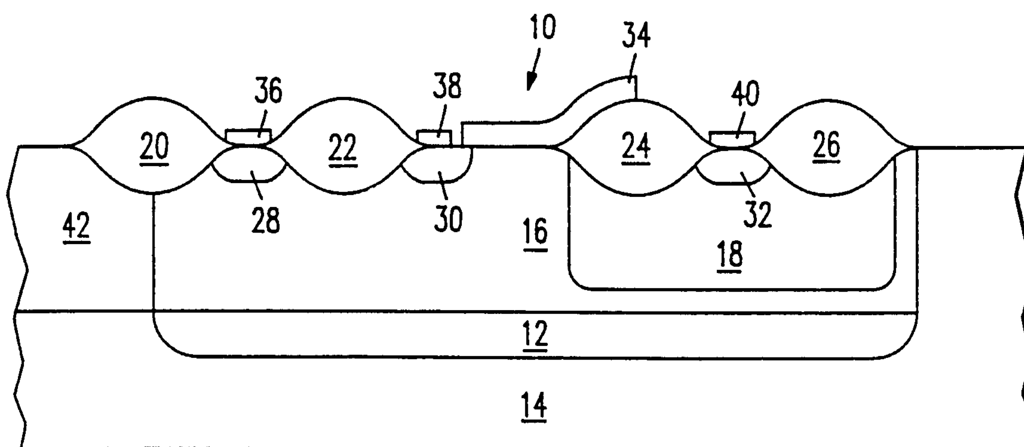

FIG. 1

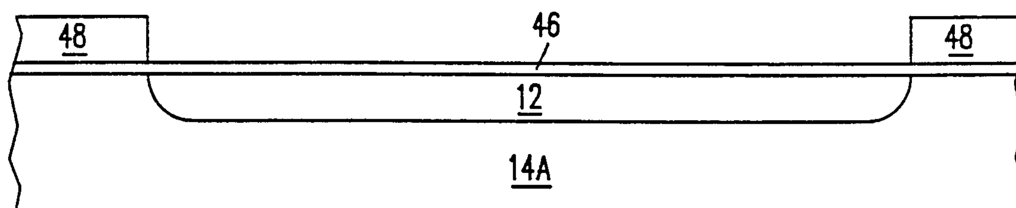

FIG. 2

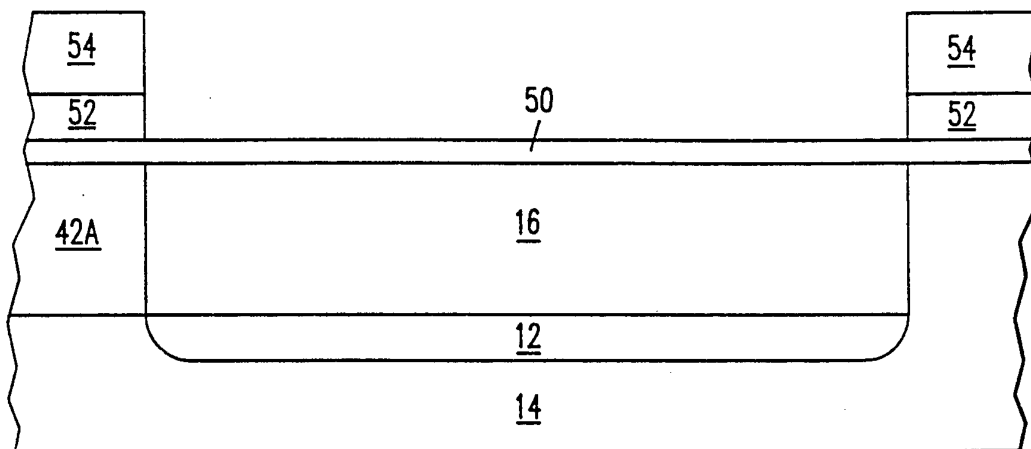

FIG. 3

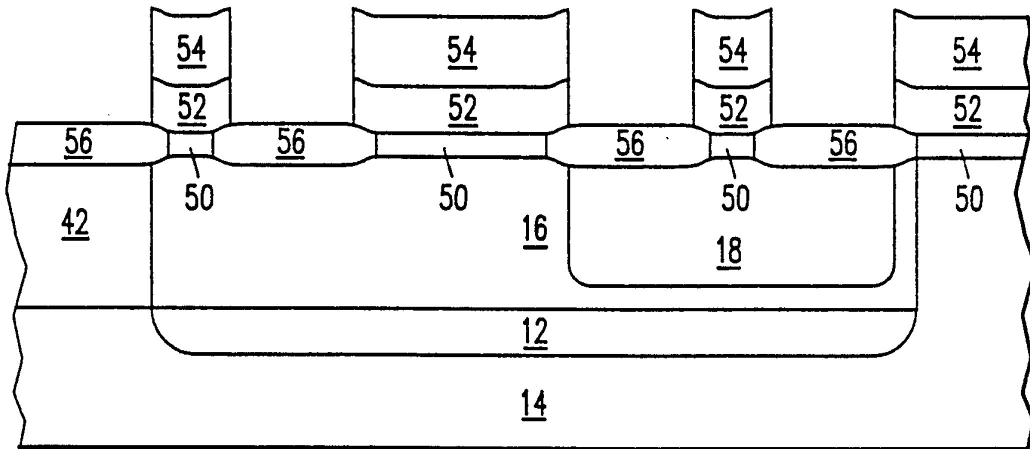

FIG. 4

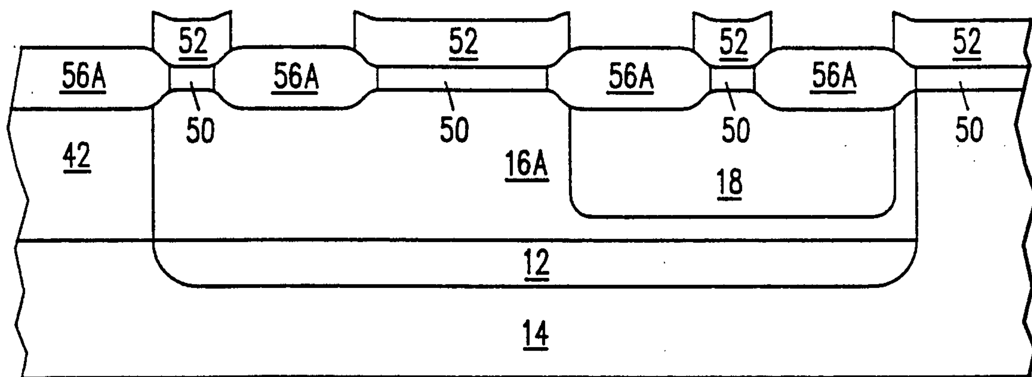

FIG. 5

INTERNATIONAL SEARCH REPORT

Intern. al Application No
PCT/US 94/10843

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/82 H01L21/336 H01L21/266 H01L29/78 H01L27/092

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	EP,A,0 248 988 (SIEMENS AKTIENGESELLSCHAFT) 16 December 1987 see column 4, line 26 - column 5, line 21; figures ---	11-15 1-10, 16-25
Y	EP,A,0 387 999 (DELCO ELECTRONICS CORP) 19 September 1990 see column 7, line 38 - line 56; figures 2C-2E see column 8, line 40 - line 51 ---	1-10, 16-25
A	FR,A,2 675 311 (SAMSUNG ELECTRONICS CORP) 16 October 1992 see abstract; figures --- -/--	1-26

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
21 December 1994	30.12.94

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Sinemus, M

INTERNATIONAL SEARCH REPORT

Intern al Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol.ED-33, no.12, December 1986, NEW YORK US pages 2016 - 2024 GILLES THOMAS ET AL. 'High-Voltage Technology Offers New Solutions for Interface Integrated Circuits' see abstract; figures 1,5	1-26
A	PATENT ABSTRACTS OF JAPAN vol. 14, no. 336 (E-953) 19 July 1990 & JP,A,02 112 271 (OLYMPUS OPTICAL CO LTD) 24 April 1990 see abstract	1-26
A	PATENT ABSTRACTS OF JAPAN vol. 14, no. 380 (E-965) 16 August 1990 & JP,A,02 138 756 (MITSUBISHI ELECTRIC CORP) 28 May 1990 see abstract	1-26
A	US,A,5 229 308 (XEROX CORP) 20 July 1993 see abstract; figures	6-10, 16-25
A	EP,A,0 331 223 (SGS-THOMSON MICROELECTRONICS) 6 September 1989 see column 2, line 33 - line 51; figures 1-3	6-10, 16-25
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 201 (E-336) 17 August 1985 & JP,A,60 066 461 (MATSUSHITA DENKI SANGYO K.K.) 16 April 1985 see abstract	6-10, 16-25
A	PATENT ABSTRACTS OF JAPAN vol. 5, no. 197 (E-86) (869) 15 December 1981 & JP,A,56 118 366 (HITACHI SEISAKUSHO K.K) 17 September 1981 see abstract	6-10, 16-25

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
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US-A-5229308	20-07-93	NONE		
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