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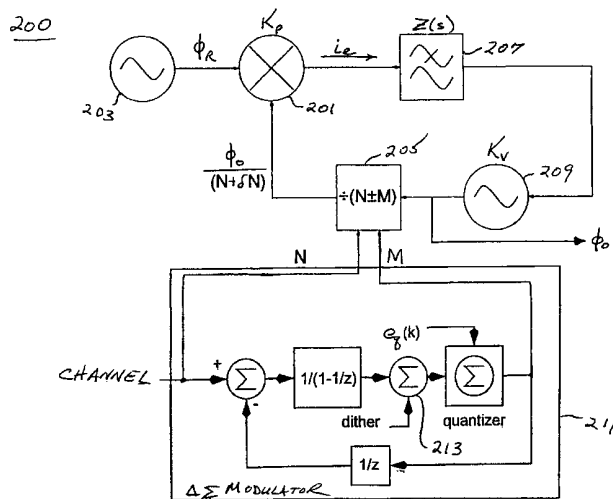
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- (71) Applicant (for all designated States except US): TELEFONAKTIEBOLAGET LM ERICSSON (publ) [SE/SE]; S-126 25 Stockholm (SE).
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- (72) Inventors; and
- (75) Inventors/Applicants (for US only): MATTISSON, Sven [SE/SE]; Östenväg 3, S-237 36 Bjärred (SE). HAGBERG, Hans [SE/SE]; Grynbodgatan 16, S-211 33 Malmö (SE). NILSSON, Magnus [SE/SE]; Flygelvägen 241, S-224 72 Lund (SE).

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(54) Title: LINEAR DEAD-BAND-FREE DIGITAL PHASE DETECTION



(57) Abstract: A phase-locked loop (200) includes a phase detector (201), a loop filter (207), a voltage controlled oscillator (209) and a frequency divider (205) arranged such that the phase detector generates a phase detector output signal as a function of a phase difference between the reference clock signal and the feedback signal; the loop filter (207) generates a frequency control signal from the phase detector output signal (Po); the voltage controlled oscillator (209) generates a phase-locked loop output signal that has a frequency that is controlled by the frequency control signal; and the frequency divider generates the feedback signal from the phase-locked loop output signal. The phase-locked loop further includes one or more circuit elements that maintain an operating point of the phase detector such that, for a predetermined range of both positive and negative phase differences between the reference clock signal and the feedback signal, the output signal is generated as a substantially linear function of the phase difference between the reference clock signal and the feedback signal.



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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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INTERNATIONAL SEARCH REPORT

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 049 233 A (SHURBOFF CARL L) 11 April 2000 (2000-04-11) column 3, line 47 -column 6, line 28 column 7, line 41 -column 8, line 6 figures 5-9,11	1,3,4, 13,15,16
Y	---	5,7,17, 19
X	US 5 631 582 A (FUJIKAWA AKIO) 20 May 1997 (1997-05-20) column 4, line 32 -column 5, line 16; figures 8,9	1,6,8, 13,18,20
Y	---	5,7,17, 19
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Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,  
Fax: (+31-70) 340-3016

Authorized officer

Balbinot, H

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>US 5 103 191 A (WERKER HEINZ) 7 April 1992 (1992-04-07)</p> <p>column 2, line 26 -column 3, line 31; figure 1</p> <p style="text-align: center;">---</p>	<p>1,2, 9-14,21, 22</p>
X	<p>D. P. TURNER: "Phase Locked Loop Phase Adjustment" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 15, no. 7, December 1972 (1972-12), pages 2080-2081, XP002104823 ISSN: 0018-8689 the whole document</p> <p style="text-align: center;">----</p>	<p>1,2, 9-14,21, 22</p>
X	<p>US 4 818 950 A (RANGER MICHAEL H) 4 April 1989 (1989-04-04)</p> <p>column 4, line 60 -column 5, line 47; figures 1,2C</p> <p style="text-align: center;">-----</p>	<p>1,2, 9-14,21, 22</p>

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Information on patent family members

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