



- (51) **International Patent Classification:**
B66B 1/46 (2006.01) *H01H 1/00* (2006.01)
- (21) **International Application Number:**
PCT/US2010/036994
- (22) **International Filing Date:**
2 June 2010 (02.06.2010)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (71) **Applicant (for all designated States except US):** OTIS ELEVATOR COMPANY [US/US]; Ten Farm Springs Road, Farmington, CT 06032 (US).
- (72) **Inventor; and**
- (75) **Inventor/Applicant (for US only):** XING, Gang [CN/CN]; Room 501, #35, 1000 Yuntai Road, Pudong, Shanghai 200123 (CN).
- (74) **Agent:** DORR, Blake, I.; Cantor Colburn LLP, 20 Church Street, 22nd Floor, Hartford, CT 06103 (US).
- (81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO,

DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

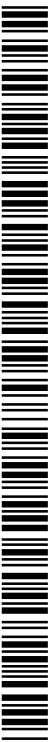
(84) **Designated States (unless otherwise indicated, for every kind of regional protection available):** ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

— with international search report (Art. 21(3))



WO 2011/152823 A1

(54) **Title:** SWITCH DETECTION SYSTEM

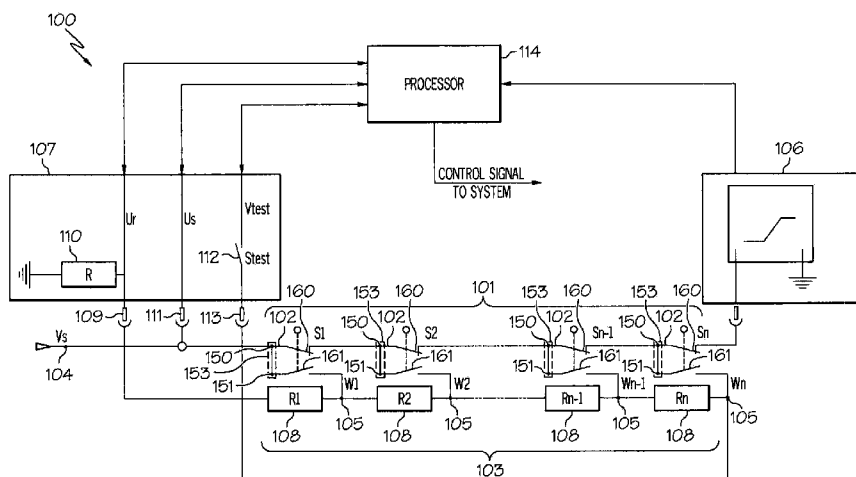


FIG. 1

(57) **Abstract:** A switch detection system (100) includes a first switch (102) having a pole node (153), a normally closed contact (160), and a normally open contact (161), the pole node (153) of the first switch (102) connected to a voltage source node (104), a second switch (102) having a pole node (153), a normally closed contact (160) and a normally open contact (161), the pole node (153) of the second switch (102) connected to the normally closed contact (160) of the first switch (102), a voltage detector (106) connected to the normally closed contact (160) of the second switch (102), a first resistor (108) connected to the normally open contact (161) of the first switch (102), and a second resistor (108) connected to the normally open contact (161) of the second switch (102).

SWITCH DETECTION SYSTEM

BACKGROUND OF THE INVENTION

[0001] The subject matter disclosed herein relates to control systems, particularly switch detection systems for elevator and escalator control systems.

[0002] Switch detection systems may include a plurality of switches electrically connected to a control system. A switch detection system may be used to determine whether a switch in the system has been actuated and identify which particular switch has been actuated.

[0003] The determination and identification of an actuated switch may be used to control a system such as, for example, an elevator or escalator system.

BRIEF DESCRIPTION OF THE INVENTION

[0004] According to one aspect of the invention, a switch detection system includes a first switch having a pole node, a normally closed contact, and a normally open contact, the pole node of the first switch connected to a voltage source node, a second switch having a pole node, a normally closed contact and a normally open contact, the pole node of the second switch connected to the normally closed contact of the first switch, a voltage detector connected to the normally closed contact of the second switch, a first resistor connected to the normally open contact of the first switch, a second resistor connected to the normally open contact of the first switch and the normally open contact of the second switch, and a processor having a first connection connected to the pole node of the first switch and a second connection connected to the first resistor.

[0005] According to another aspect of the invention, a method for determining an actuated switch in a system includes receiving an indication from a voltage detector that the voltage detector is not detecting a voltage, measuring a voltage in a circuit, the circuit including at least one switch and at least one resistor connected in series, determining the resistance of the circuit, dividing the resistance of the circuit with the known resistance of the at least one resistor to determine a number of resistors in series in the circuit, associating the number of resistors in series in the circuit with a number of corresponding switches in the circuit, identifying an actuated switch in the system responsive to associating the number of resistors in series in the circuit with the number of corresponding switches in the circuit, outputting a signal indicating the identified actuated switch.

[0006] According to yet another aspect of the invention, a switch detection system includes a first switch having a pole node, a normally closed contact, and a normally open contact, the pole node of the first switch connected to a voltage source node, a second switch having a pole node, a normally closed contact and a normally open contact, the pole node of the second switch connected to the normally closed contact of the first switch, a first resistor connected to the normally open contact of the first switch, and a second resistor connected to the normally open contact of the first switch and the normally open contact of the second switch.

[0007] These and other advantages and features will become more apparent from the following description taken in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWING

[0008] The subject matter, which is regarded as the invention, is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0009] FIG. 1 illustrates an exemplary embodiment of a switch detection system.

[0010] The detailed description explains embodiments of the invention, together with advantages and features, by way of example with reference to the drawings.

DETAILED DESCRIPTION OF THE INVENTION

[0011] FIG. 1 illustrates an exemplary embodiment of a switch detection system 100. The system 100 includes switches (S1-Sn) 102 in a switch array 101 that may include any number (n) of switches 102. In the illustrated embodiment, each switch 102 includes a first pole 150 and a second pole 151 connected to form a single pole node 153, a normally closed contact 160, and a normally open contact 161. The contacts are arranged such that when the normally closed contact 160 is opened, the normally open contact 161 is closed. The pole nodes 153 of the switches 102 and normally closed contacts 161 of the switches are connected in series between a voltage source (Vs) node 104 and a voltage detector 106. Similar (or substantially identical) resistors (R1-Rn) 108 are arranged in series in a resistor array 103. Each of the resistors 108 is paired with a corresponding switch 102 such that the system 100 includes n number of switches and resistors. The array 103 includes nodes (W1-Wn) 105 arranged between the resistors 108 (the node Wn is arranged at the end of the series of resistors 108); each node 105 connects each resistor 108 to the normally open contact 161

of the paired switch 102. A switch identifier circuit 107 includes a node 109 that is connected to the R1 resistor 108, a node 111 that is connected to the voltage source node 104, and may include a node 113 that is connected to the Wn node 105. The 109 terminal is connected to a resistor 110 that is connected to ground. The terminal 113 may be connected to a voltage source (V_{test}) via a test switch (S_{test}) 112. A processor 114 may be communicatively connected to the switch identifier circuit 107 and the voltage detector 106.

[0012] In operation, when each of the normally closed contacts 160 of the switches 102 are in the closed position, the voltage detector 106 detects the voltage from the voltage source node 104. The voltage detector 106 may send a signal to the processor 114 indicating that a voltage is detected from the voltage source node 104. When a switch 102 for example, switch S2 102, is actuated, the normally closed contact 160 of the switch S2 102 is opened, and the normally open contact 161 of the switch S2 102 is closed. The electrical connection between the voltage source node 104 and the voltage detector 106 is disconnected, and the voltage detector 106 will not detect a voltage. The voltage detector 106 may send a signal to the processor 114 that indicates that no voltage is detected. The closing of the normally open contact 161 of the switch S2 102 results in a current path that flows from the voltage source node 104 through the (closed) normally closed contact 160 of switch S1 102, the (closed) normally open contact 161 of switch S2 102, the resistor R2 108, the resistor R1 108, and the node 109 to the processor 114. The processor 114 senses the voltage source (V_s) at the voltage source node 104 (at the node 111) and the resistance voltage (V_r) at the node 109. Since the resistors 108 have similar resistance, $V_r = V_s / (n + 1)$. Solving for n, $n = V_s / V_r - 1$, where n is the number of resistors 108 connected in series when a switch 102 is actuated (the normally open contact 161 is closed and the normally closed contact 160 is open). Since each switch 102 is paired with a resistor 108, the actuated switch may be identified.

[0013] In the above example, the actuation of the switch S2 102 results in a loss of voltage to the voltage detector 106. The voltage detector 106 sends a signal to the processor 114. The processor 114 detects the voltages V_s and V_r and solves the above equation for n. The resultant $n = 2$ indicates that there are two resistors (R1 and R2) connected in series. Since each resistor 108 is paired with a switch 102, $n = 2$ indicates that the switch S2 102 has been actuated. The indication of a particular actuated switch 102 may be used by the processor 114 to control associated systems, such as for example, an elevator or escalator system. For example, the processor 114 may output a control signal to control visual, audio, or other non-textual indicators in the system, or may output a control signal to control mechanical elements of the system such as, elevator cars.

[0014] The Stest switch 112 may be used to test the system. If the normally closed contacts of the switches 102 are closed, the Stest switch 112 may be closed and voltage may be applied across the resistor array 103. If the system 100 is operating properly, the total resistance of the resistor array 103 (R_t), where $R_t = \sum R_n$ should be detected. The processor 114 may compare the R_t to a threshold resistance value. If R_t is less than the threshold, the processor may indicate a failure in the system, by for example, outputting a failure message to an operator, lighting a failure indicator light (not shown), or performing control logic associated with the failure.

[0015] While the invention has been described in detail in connection with only a limited number of embodiments, it should be readily understood that the invention is not limited to such disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Additionally, while various embodiments of the invention have been described, it is to be understood that aspects of the invention may include only some of the described embodiments. Accordingly, the invention is not to be seen as limited by the foregoing description, but is only limited by the scope of the appended claims.

CLAIMS:

1. A switch detection system (100) comprising:

a first switch (102) having a pole node (153), a normally closed contact (160), and a normally open contact (161), the pole node (153) of the first switch (102) connected to a voltage source node (104);

a second switch (102) having a pole node (153), a normally closed contact (160) and a normally open contact (161), the pole node (153) of the second switch (102) connected to the normally closed contact (160) of the first switch (102);

a voltage detector (106) connected to the normally closed contact (160) of the second switch (102);

a first resistor (108) connected to the normally open contact (161) of the first switch (102);

a second resistor (108) connected to the normally open contact (161) of the first switch (102) and the normally open contact (161) of the second switch (102); and

a processor (114) having a first connection connected to the pole node (153) of the first switch (102) and a second connection connected the first resistor (108).

2. The system of claim 1, wherein the system further includes a third switch (112) connected to the processor (114) and to the normally open contact (161) of the second switch (102).

3. The system of claim 1, wherein the voltage detector (106) is operative to detect a voltage and send an indication that a voltage is detected to the processor (114).

4. The system of claim 1, wherein the first resistor (108) and the second resistor (108) have a similar resistance.

5. The system of claim 1, wherein the first resistor (108) and the second resistor (108) have the same resistance.

6. The system of claim 1, wherein the processor (114) is operative to:

receive a signal from the voltage detector (106), the signal indicative that the voltage detector (106) is not detecting a voltage;

determine a voltage across the first connection of the processor (114) and the second connection of the processor (114);

determine a voltage drop across the connections of the processor (114); and

calculate a number of resistors (108) in series between the first connection of the processor (114) and the second connection of the processor (114).

7. The system of claim 2, wherein the processor is operative to:

close the third switch (112);

apply a voltage across the first resistor (108) and the second resistor (108);

measure the total resistance of the first resistor (108) and the second resistor (108);

compare the measured resistance of the first resistor (108) and the second resistor (108) with a threshold resistance; and

indicate a failure responsive to determining that the measured resistance is less than the threshold resistance.

8. A method for determining an actuated switch in a system (100), the method comprising:

receiving an indication from a voltage detector (106) that the voltage detector is not detecting a voltage;

measuring a voltage in a circuit, the circuit including at least one switch (102) and at least one resistor (108) connected in series;

determining the resistance of the circuit;

dividing the resistance of the circuit with the known resistance of the at least one resistor (108) to determine a number of resistors (108) in series in the circuit;

associating the number of resistors (108) in series in the circuit with a number of corresponding switches (102) in the circuit;

identifying an actuated switch (102) in the system responsive to associating the number of resistors (108) in series in the circuit with the number of corresponding switches (102) in the circuit;

outputting a signal indicating the identified actuated switch (102).

9. A switch detection system comprising:

a first switch (102) having a pole node (153), a normally closed contact (160), and a normally open contact (161), the pole node (153) of the first switch (102) connected to a voltage source node (104);

a second switch (102) having a pole node (153), a normally closed contact (160) and a normally open contact (161), the pole node (153) of the second switch (102) connected to the normally closed contact (160) of the first switch (102);

a first resistor (108) connected to the normally open contact (161) of the first switch (102); and

a second resistor (108) connected to the normally open contact (161) of the first switch (102) and the normally open contact (161) of the second switch (102).

10. The switch detection system of claim 9, wherein the system further comprises a processor (114) having a first connection connected to the pole node (153) of the first switch (102) and a second connection connected the first resistor (108).

11. The switch detection system of claim 9, wherein the system further comprises a voltage detector (106) connected to the normally closed contact (160) of the second switch (102).

12. The system of claim 9, wherein the system further includes a third switch (112) connected to the processor (114) and to the normally open contact (161) of the second switch (102).

13. The system of claim 11, wherein the voltage detector (106) is operative to detect a voltage and send an indication that a voltage is detected to the processor (114).
14. The system of claim 9, wherein the first resistor (108) and the second resistor (108) have a similar resistance.
15. The system of claim 9, wherein the first resistor (108) and the second resistor (108) have the same resistance.
16. The system of claim 10, wherein the processor is operative to:
- determine a voltage across the first connection of the processor (114) and the second connection of the processor (114);
 - determine a voltage drop across the connections of the processor (114); and
 - calculate a number of resistors (108) in series between the first connection of the processor (114) and the second connection of the processor (114).
17. The system of claim 16, wherein the processor (114) is operative to receive a signal from a voltage detector (106), the signal indicative that the voltage detector (108) is not detecting a voltage prior to determining a voltage across the first connection of the processor (114) and the second connection of the processor (114).
18. The system of claim 12, wherein the processor is operative to:
- close the third switch (112);
 - apply a voltage across the first resistor (108) and the second resistor (108);
 - measure the total resistance of the first resistor (108) and the second resistor (108);
 - compare the measured resistance of the first resistor (108) and the second resistor (108) with a threshold resistance; and
 - indicate a failure responsive to determining that the measured resistance is less than the threshold resistance.

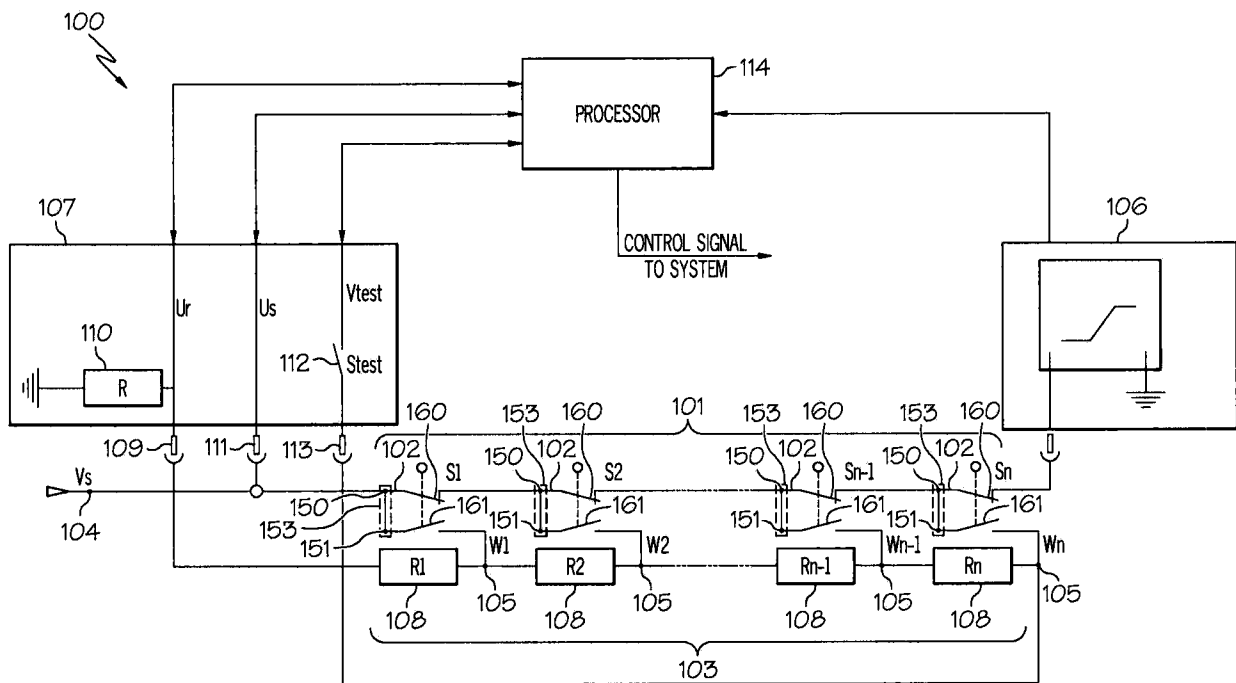




FIG. 1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/036994

A. CLASSIFICATION OF SUBJECT MATTER		
<i>B66B 1/46(2006.01)i, H01H 1/00(2006.01)i</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) B66B 1/46; H03M 1/66; B66B 1/14; B66B 3/00		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: "switch", "identify", "detection", "array", "resistor"		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	KR 10-1999-0054777 A (LG ELECTRO COMPONENTS CO.,) 15 July 1999 See figure 2 and claim 1.	9,14-15 1-8,10-13,16-18
A	KR 10-1999-0084698 A (SAMSUNG ELECTRONICS CO., LTD.) 06 December 1999 See figure 1.	1-18
A	JP 11-343075 A (HITACHI BUILDING SYSTEMS CO., LTD.) 14 December 1999 See claim 1 and figure 1.	1-18
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 18 MARCH 2011 (18.03.2011)		Date of mailing of the international search report 18 MARCH 2011 (18.03.2011)
Name and mailing address of the ISA/KR  Korean Intellectual Property Office Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140		Authorized officer CHO, Choon Geun Telephone No. 010)3380-8015 

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2010/036994

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-1999-0054777 A	15.07.1999	None	
KR 10-1999-0084698 A	06.12.1999	None	
JP 11-343075 A	14.12.1999	None	