

**FuseSoc** - cores never been so  
much fun

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# Who am I?



Olof Kindgren  
@OlofKindgren

Android crashes on boot when running from SD card

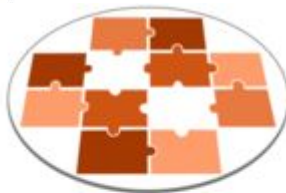


12:17 AM - 21 Mar 2017

11,564 Retweets 15,819 Likes



143 12K



**FOSSi**  
Foundation



Portland Oregon



May 4-5 2019



RISC-V SoftCPU Contest: Winners

- 1<sup>st</sup> Place: Charles Papon with VexRiscv  
- Awarded \$6,000 USD
- 2<sup>nd</sup> Place: Antti Lukats with Engine-V was  
- Awarded \$3,000 USD, a [Splash Kit](#) and an [iCE40 UltraPlus MDP](#)
- 3<sup>rd</sup> Place: Changyi Gu with PulseRain Reindeer  
- Awarded \$1,000 USD, a [PolarFire Evaluation Kit](#) and an [iCE40 UltraPlus Breakout Board](#)
- Creativity Prize: Olof Kindgren with SERV  
- Awarded \$3,000 USD



antmicro



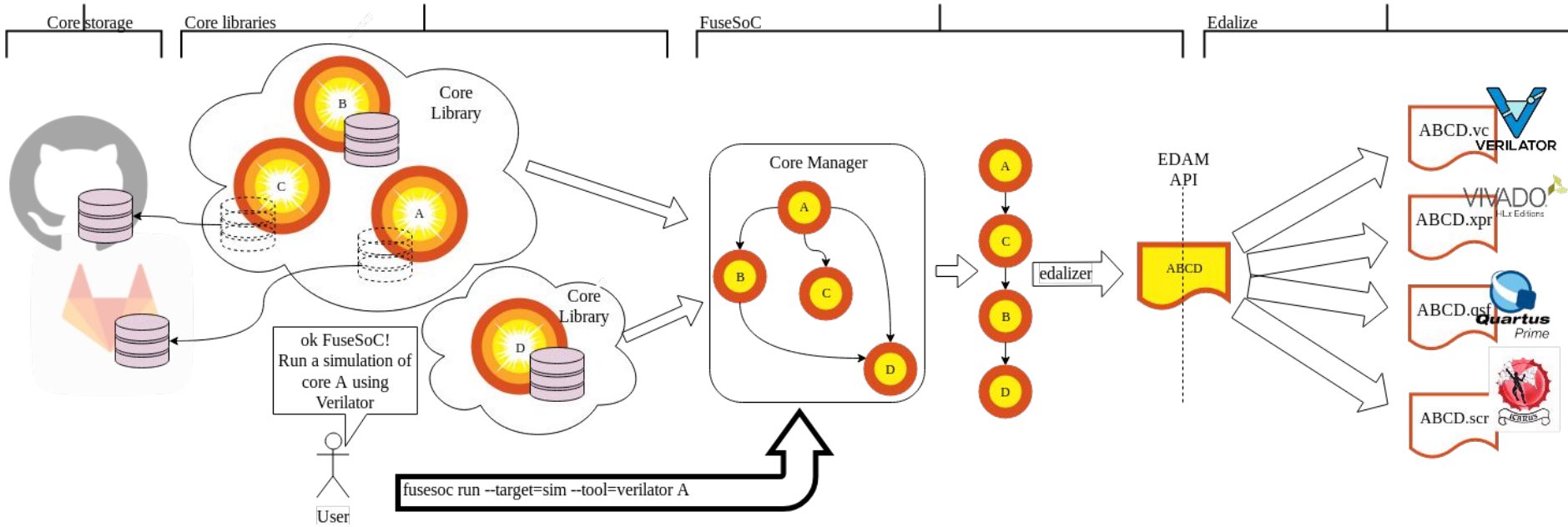
qamcom

# What is FuseSoc?

FuseSoC is a package manager...

...and a build tool for HDL

# What is FuseSoC?



FuseSoC is a package manager...

...and a build tool for HDL

# Why use FuseSoc?

Increase portability

Reduce maintenance

*“Focus on your core business, not your cores”*

# FuseSoC is

the most used package manager

non-intrusive

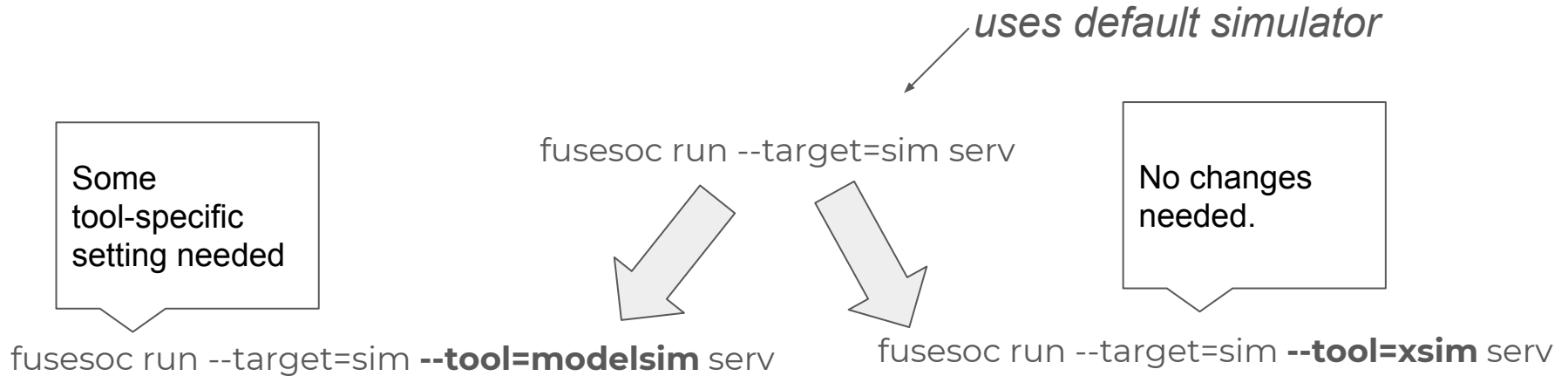
modular

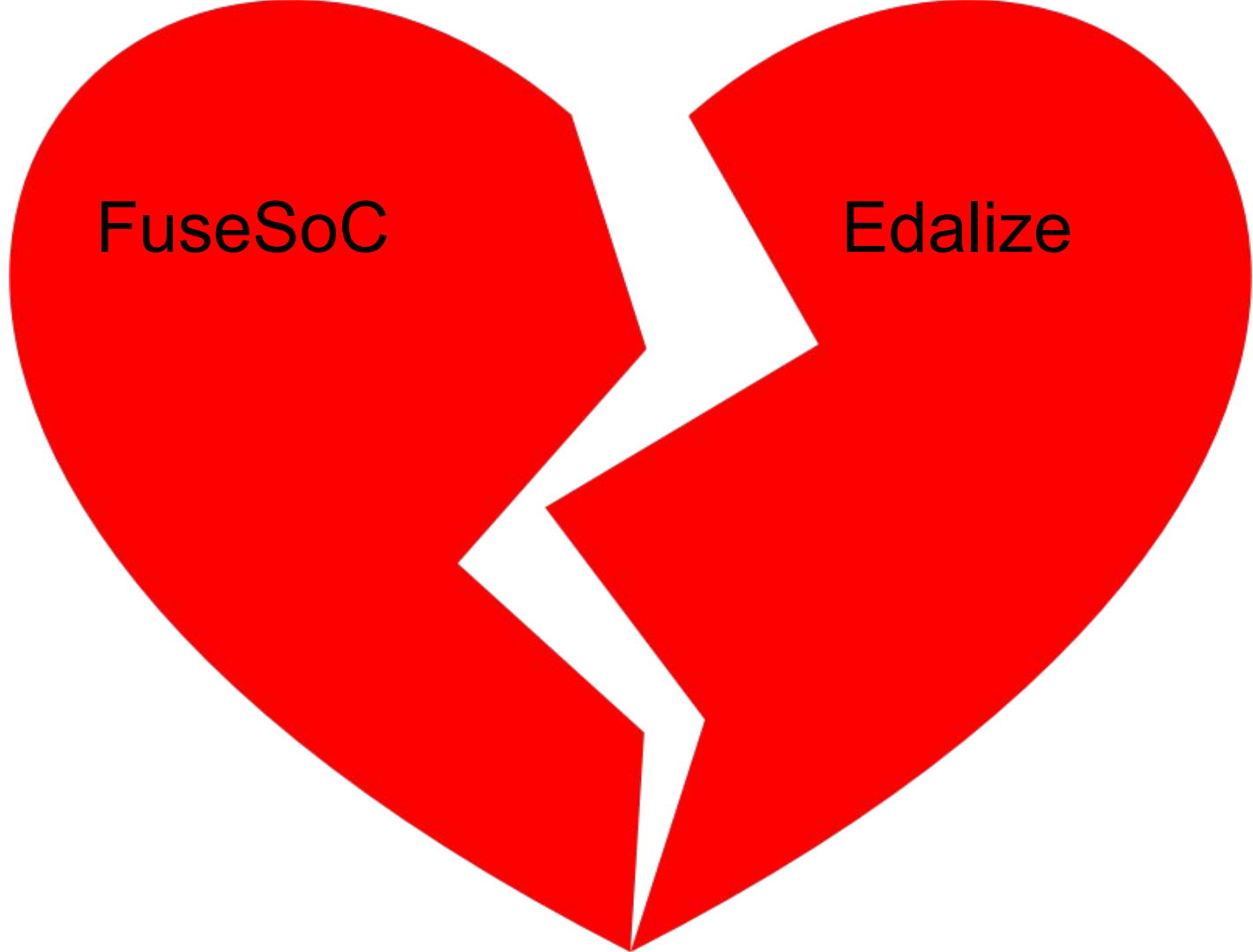
extendable

resourceful

battle-proven

# Case : Target different tools

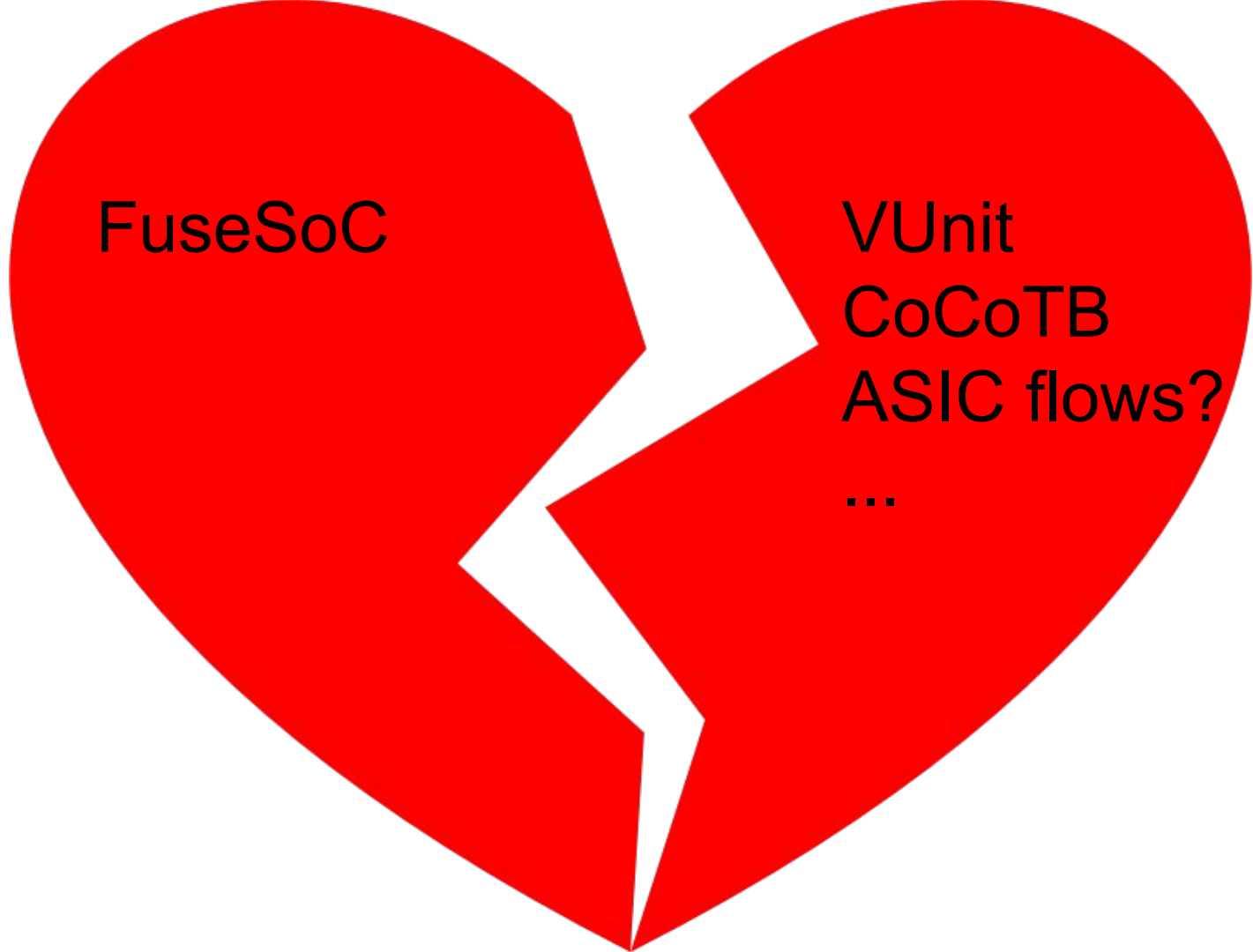




FuseSoC

Edalize





FuseSoC

VUnit  
CoCoTB  
ASIC flows?  
...



Kactus2

MyHDL

Migen

CLaSH

IceStudio

...

Edalize

# Tomorrow

- Generators
- Formal verification
- Use flags



# Future

- **Librecores integration**
- **Edalize everywhere**
- **Industry standard - World domination**

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Anyone?

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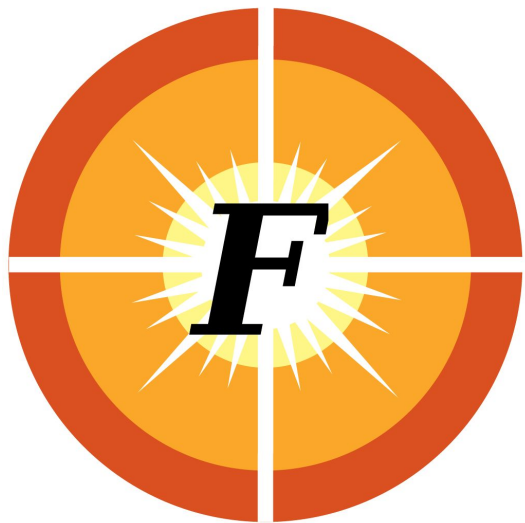
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**That's it folks!**

<https://github.com/olofk/fusesoc>

<http://fusesoc.net>

<https://gitter.im/librecores/fusesoc>

**Don't miss...**



# Core description files (example)

**name** : `::picorv32:0-r1`

## **filesets:**

rtl:

files: [picorv32.v]

file\_type : *verilogSource*

tb:

files: [testbench.v]

file\_type : *verilogSource*

tb\_verilator:

files: [testbench.cc : {file\_type : *cppSource*}]

## **parameters:**

firmware: {datatype : file, paramtype : plusarg}

COMPRESSED\_ISA:

datatype : str

default : 1

paramtype : vlogdefine

## **targets:**

default:

filesets: [rtl]

test:

default\_tool: icarus

filesets: [rtl, tb, "tool\_verilator? (tb\_verilator)"]

parameters: [COMPRESSED\_ISA, firmware]

toplevel:

- "tool\_verilator? (picorv32\_wrapper)"

- "!tool\_verilator? (testbench)"

# supported tools

- Synthesis/P&R support with icesstorm, ise, quartus, trellis, vivado
- Simulations with ghdl, icarus, isim, modelsim, rivierapro, vcs, verilator, xsim
- Linting with spyglass, verilator
- In the works
  - Lattice Diamond, icecube2, radiant
  - ncsim
  - Formal verification with symbiosys