

Chapter 13

Serial Interfacing

Expected Outcomes

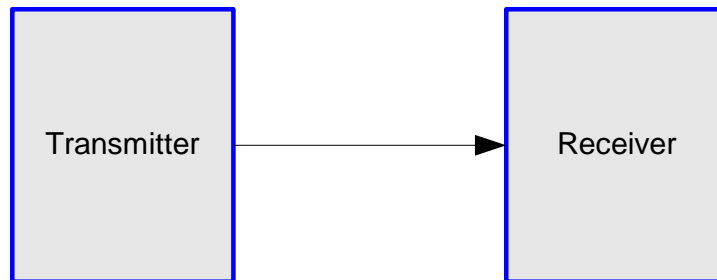
- Explain the fundamental idea of operation of serial interface
- List and describe type of serial interface
- Identify the serial interface characteristic such as data framing and baud rate
- Explain and describe the role line driver in serial interface
- Write a program using serial interface

Introduction

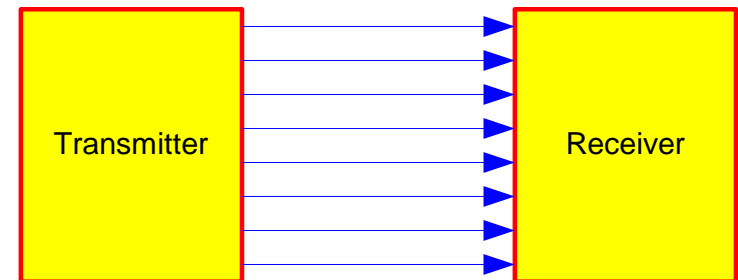
- Computers transfer data in two ways
 - **Parallel**
 - **Serial**
- Parallel data transfers often 8 or more lines are used to transfer data to a device that is only a few feet away such as printers and hard disks
- Parallel requires a short amount of time to transfer data
- However, the distance of the devices are limited and impractical to be used in a long distance
- The parallel is complex to be designed and prone to error
- In serial method, the data is sent one bit at a time

Parallel vs Serial

- Computers transfer data in two ways
 - Parallel
 - Serial



Serial Communication



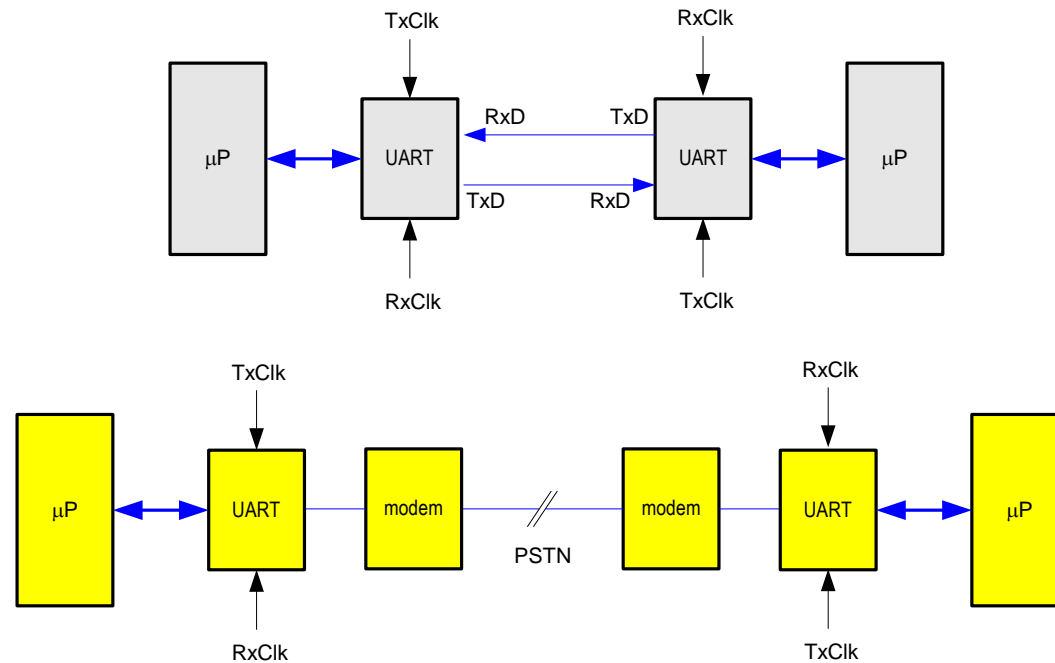
Parallel Communication

Serial Communication

- Serial data communication uses two methods
 - **Asynchronous**
 - **Synchronous**
- The synchronous transfers a block of data (characters) at a time, thus requiring the transmitter and receiver to have the same clock system
- The asynchronous transfers a single byte at a time
- For a small system, normally asynchronous method is preferred as the design is simple and cheap
- Specialized chips are designed for both method: **UART** (Universal Asynchronous Receiver and Transmitter) and **USART**
- M68000 family peripheral – **MC68681 DUART**
- M6800 family peripheral - **MC6850 ACIA**

UART

- Some of the possible connections



DUART 68681

■ The MC68681 (dual universal asynchronous receiver/transmitter) is part of M68000 peripheral using asynchronous bus structure

■ Features

- 2 independent full-duplex asynchronous channels
- Maximum data transfer rate up to 1 MB/s
- Programmable data format
- Programmable channel mode
- Independent programmable baud rate
- Versatile interrupt system
- Multi-function 16-bit programmable counter/timer
- Multi-function 8-bit output port and etc...

ACIA 6850

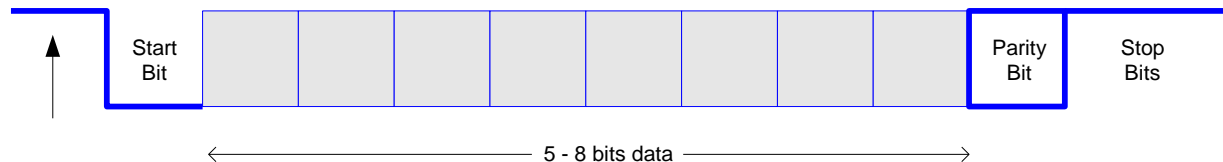
- Alternatively, M6800 family peripheral such as ACIA 6850 can be used in serial transmission
- **Asynchronous Communication Interface Adapter (ACIA 6850)** is widely used due to cost and simplicity

■ Features

- Data lines (D0-D7)
- Chip selects (CS0,CS1 and CS2*)
- Enable (E)
- Read and Write (R/W*)
- Register Select (RS)
- Received Data (RxD) and Transmit Data (TxD)
- Transmit Clock (TxClk) and Receive Clock (RxClk)
- Modem Control Line (CTS*, RTS*, DCD*)

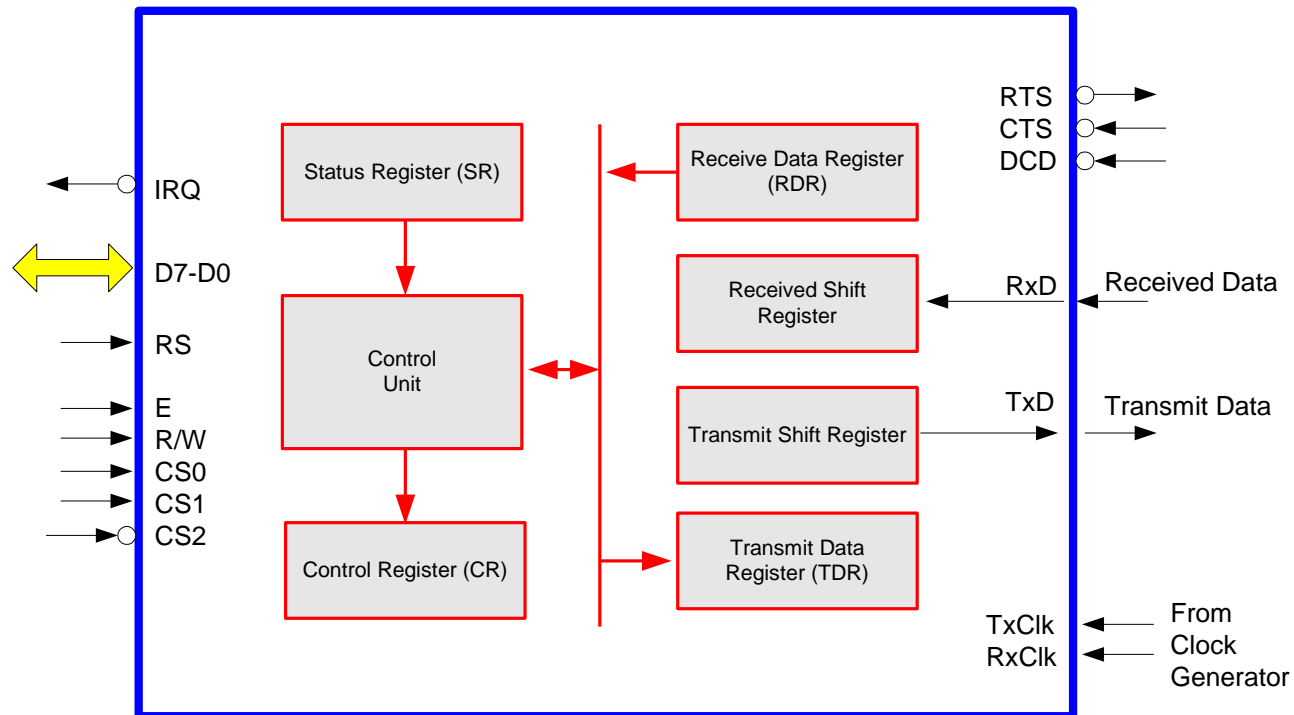
Data Framing

- Before transmission each character must be framed
- Data framing for asynchronous method
- **1 start bit**
 - Always “0” to indicate the beginning of character
- **5-8 bits data**
 - It begins with LSB
- **1 parity bit (optional)**
 - Can be odd or even parity depending on the programmer
- **1 or more stop bits**
 - Always “1” to indicate the end of character



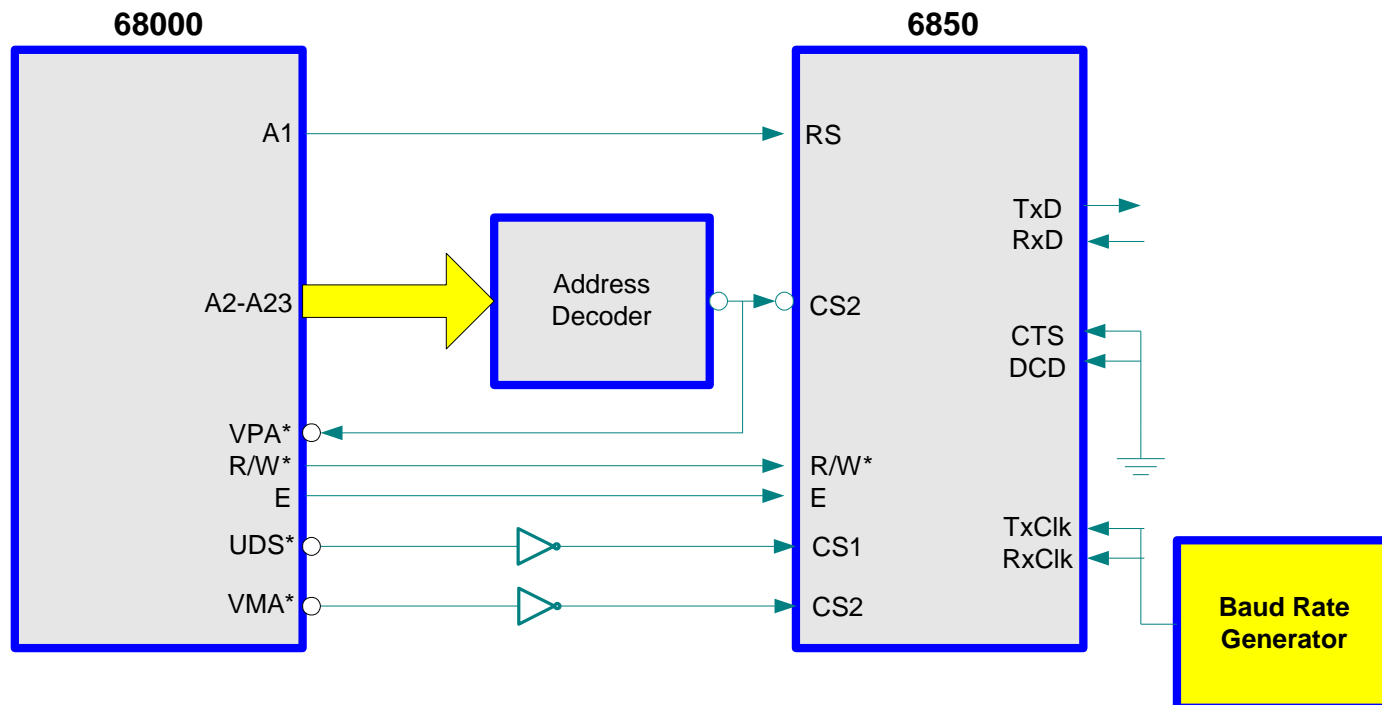
ACIA 6850

Internal architecture of ACIA 6850



ACIA 6850

- **Baud rate generator circuit** : Baud rate generator chips such as MC14411 or oscillator circuit



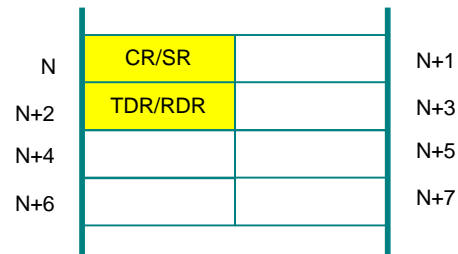
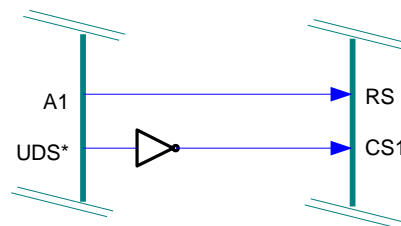
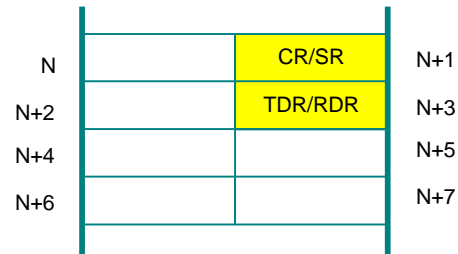
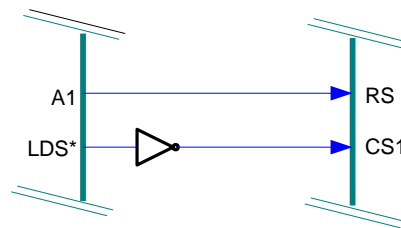
Registers

- There are 4 registers
 - **Control Register (CR)**
 - **Status Register (SR)**
 - **Transmit Data Register (TDR)**
 - **Receive Data Register (RDR)**

RS	R/W	Name	Register
0	0	CR	Control Register
0	1	SR	Status register
1	0	TDR	Transmit Data Register
1	1	RDR	Receive Data Register

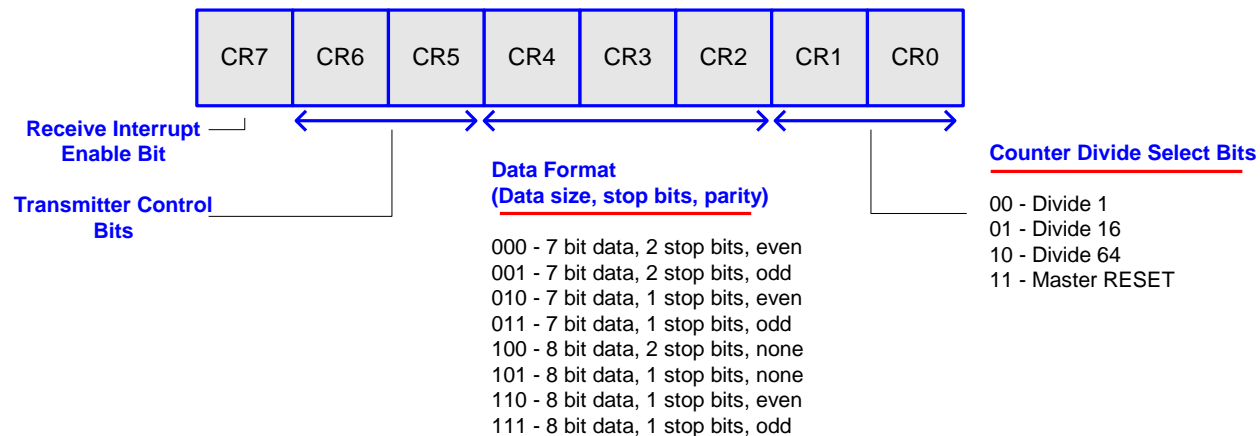
Registers

- The address register depends on
 - Address decoder
 - UDS*/LDS*



Control Register

- The control register (CR) controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output

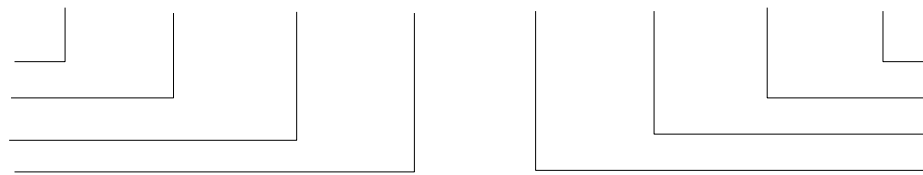


Status Register

- Information on the status of ACIA is available by reading the Status Register (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
IRQ	PE	OVRN	FE	CTS	DCD	TDRE	RDRF

Interrupt Request
Parity Error
Overrun Error
Framing Error



Receive Data register Full
Transmit Data Register Empty
Data Carrier Detect
Clear to Send

Programming ACIA 6850

- ACIA must be initialize in order to operate properly
- Four parameter must be set between transmitter and receiver
 - Data rate
 - Number of bits
 - Type of parity
 - Number of stop bits

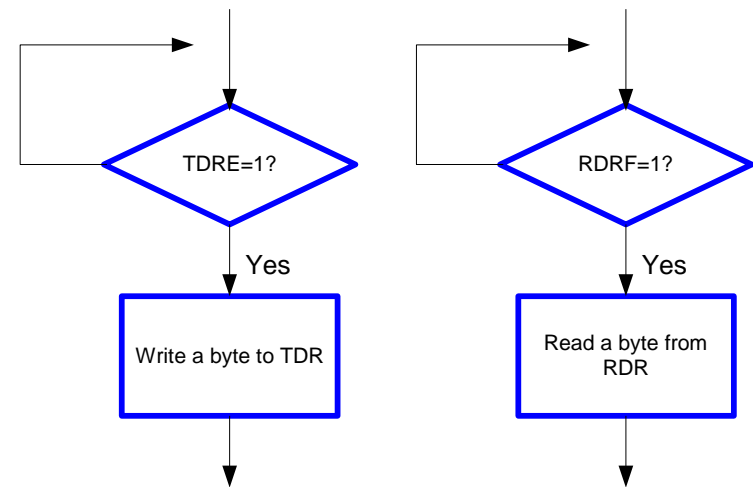
Programming ACIA 6850

- **Example:** Write a routine to initialize ACIA with the following characteristic; 8 bits, 1 stop bit, no parity. Assume clock frequency is 153.6 kHz

```
INIT MOVE .B    #3, ACIACR          ; RESET
      MOVE .B    #15, ACIACR        ; Set CR
      MOVE .W    #400, D0           ; Delay
LOOP  SUBQ .W    #1, D0
      BNE        LOOP
      RTS
```

Programming ACIA 6850

- In order to transmit or receive data, TDRE and RDRF must be monitored
- If TDR is empty, TDRE is set, allowing new data to be transmitted
- Similarly, if RDR is full, RD is set and a new data must be read



Programming ACIA 6850

- **Example:** Write a routine to send a character 'A' continuously

```
SCAN BTST.B #1,ACIASR    ;TDRE = 1?
    BEQ  SCAN            ;No, scan again
    MOVE.B #'A',ACIADR   ;Load 'A' into DR
    BRA  SCAN            ;Repeat sending
    RTS
```

Programming ACIA 6850

- **Example:** Read a byte from Data Receive register and store in D0

```
SCAN BTST.B #0,ACIASR ; Read Status Register
      BEQ  SCAN        ; RDRF=0,scan again
      MOVE.B ACIADR,D0 ; Store a byte in D0
      RTS
```

Line Driver

- The 6850 provides two pins (T_{xD} and R_{xD}) to be used specifically to transfer and receive data serially
- Since the pins are TTL compatible, they require line driver to allow data to be transmitted at a longer distance
- The most common line drivers are RS-232, RS422 and RS423
- However, RS-232 (EIA 232) is widely used as it is the simplest and the cheapest line driver
- Some examples of the ICs that provide the EIA-232 line driver are MAX 233, MAX 232, MC145407 or a pair of MC1488/MC1489

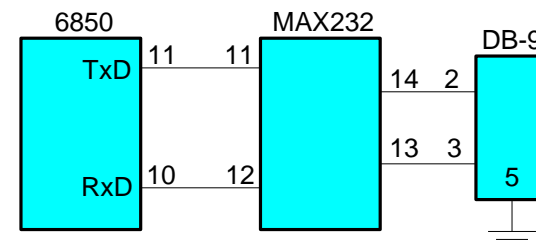
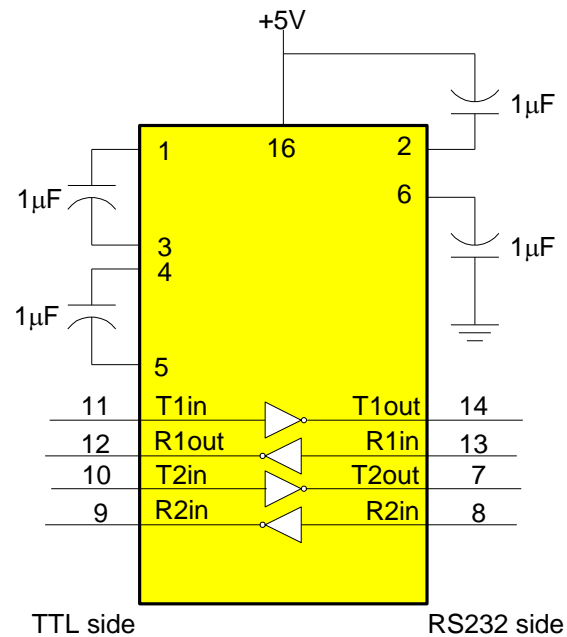
EIA-232

- Widely used for serial interface standard
- Logic “1” is represented by -30 to -25 V and logic “0” is +3 to +25 V allowing the communication to be up to 10 meter
- There are two type of RS232 connectors; DB-25 and DB-9

Pin	Description	Pin	Description
1	Data Carrier Detect (DCD)	6	Data Set Ready (DSR*)
2	Received Data (RxD)	7	Request To Send (RTS*)
3	Transmitted Data (TxD)	8	Clear To Send (CTS*)
4	Data Terminal Ready (DTR)	9	Ring Indicator (RI)
5	Signal Ground (GND)		

EIA-232

■ MAX232 internal architecture



Baud Rate

- To ensure a proper communication, the baud rate of the system must match the baud rate of the PC's COM port
- The baud rate for the system depends on baud rate generator (T_xClk and R_xClk)

Standard baud rate

110

150

300

600

1200

2400

4800

9600

19200

28800

Self-Test

■ Exercise

Explain the advantage of using serial transmission compare to parallel transmission

■ Exercise

Describe the important of using line driver such as EIA232 or RS422

■ Exercise

What is the difference between MAX232 and MAX233?

■ Exercise

State and elaborate the pin requirement for asynchronous transmission

Self-Test

■ Exercise

Briefly explain the procedure for sending a byte of data using ACIA 6850

■ Exercise

State and explain bits (TDRE and RDRF) in status register

■ Exercise

What is the difference between synchronous and asynchronous transmission

■ Exercise

A $1024 \times 512 \times 16$ -grey-level image is to be transmitted to a printer using serial communication at the rate of 19.6 kbps. The data format is one start bit, 8 data bit and one stop bit. How long does it takes to transmit the image?