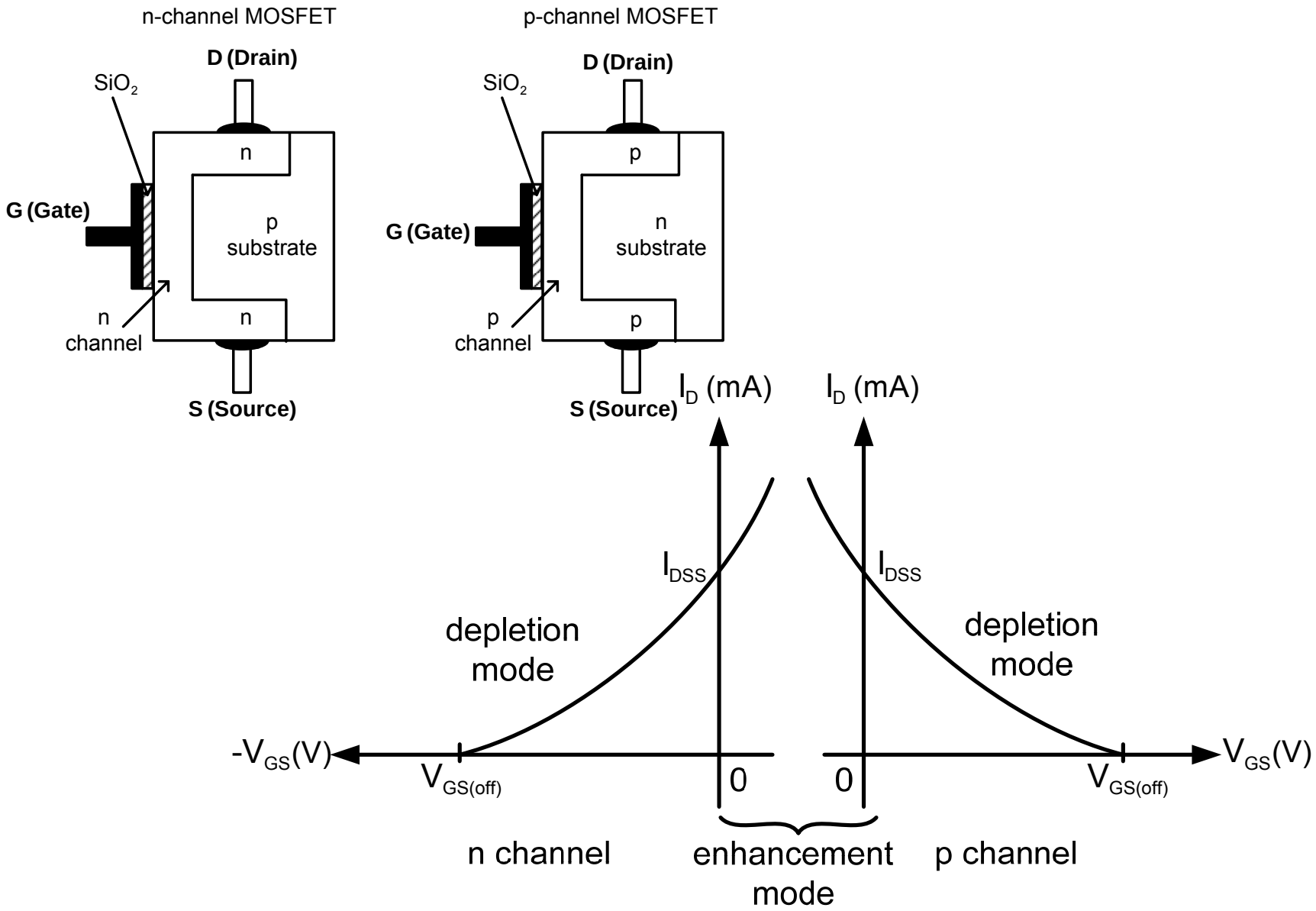
CLASS 25

D-MOSFET OPERATION AND BIASING,
E-MOSFET OPERATION AND BIASING

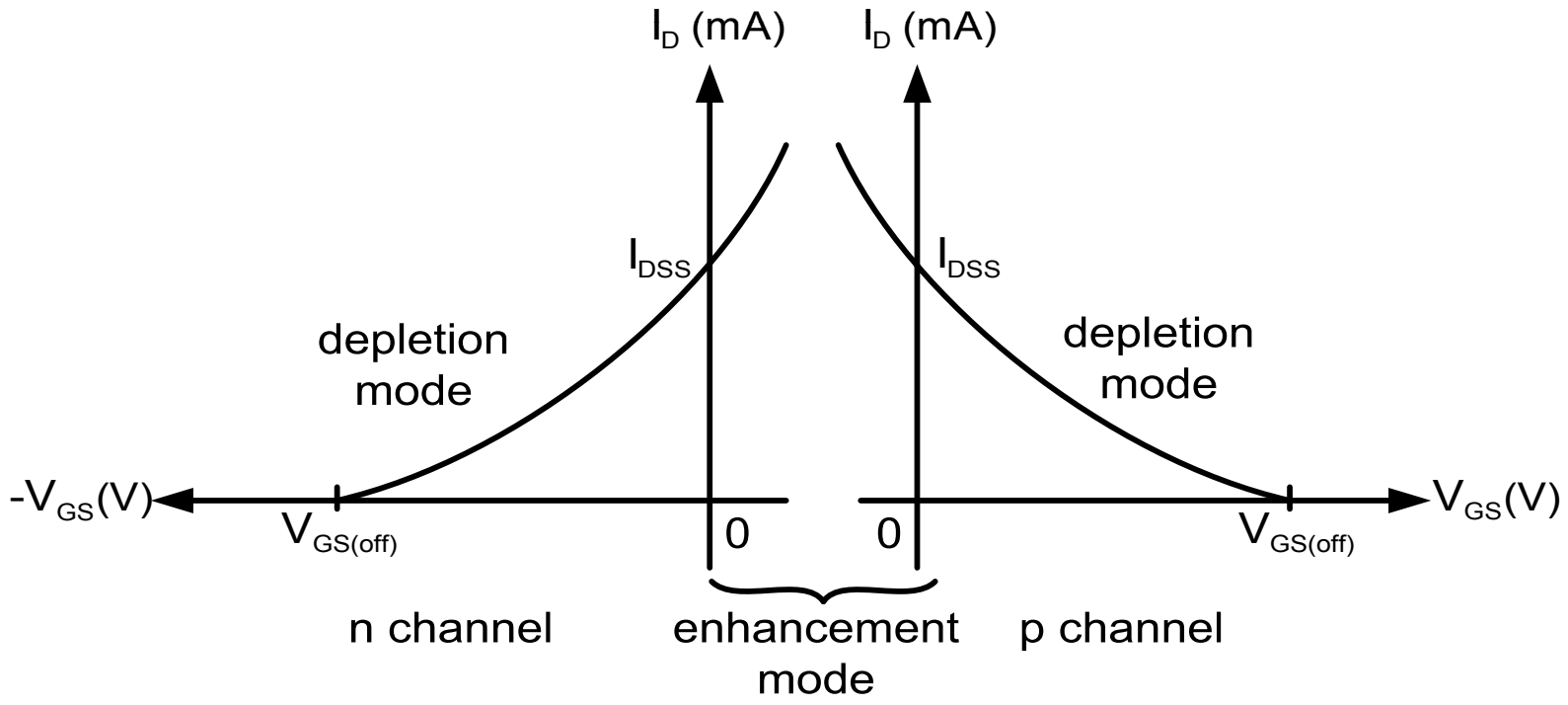
D-MOSFET transfer characteristic



D-MOSFET can operate with either positive or negative gate voltages. The point on the curves where $V_{GS} = 0$ corresponds to I_{DSS}. The point where $I_D = 0$ corresponds to $V_{GS(off)}$. As with the JFET, $V_{GS(off)} = -V_p$. The square-law expression for the JFET curve,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

also applies to the D-MOSFET curve.



Example

For a certain D-MOSFET, I_{DSS} = 10 mA and $V_{GS(off)}$ = -8 V.

(a) Is this an n-channel or a p-channel?

(b) Calculate I_D at V_{GS} = -3 V.

(c) Calculate I_D at V_{GS} = 3 V.

Solution

(a) This is an n-channel D-MOSFET as the $V_{GS(off)}$ is negative.

(b) $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = 10\ m\left[1 - \frac{(-3)}{(-8)}\right]^2 = 3.91\,mA$$

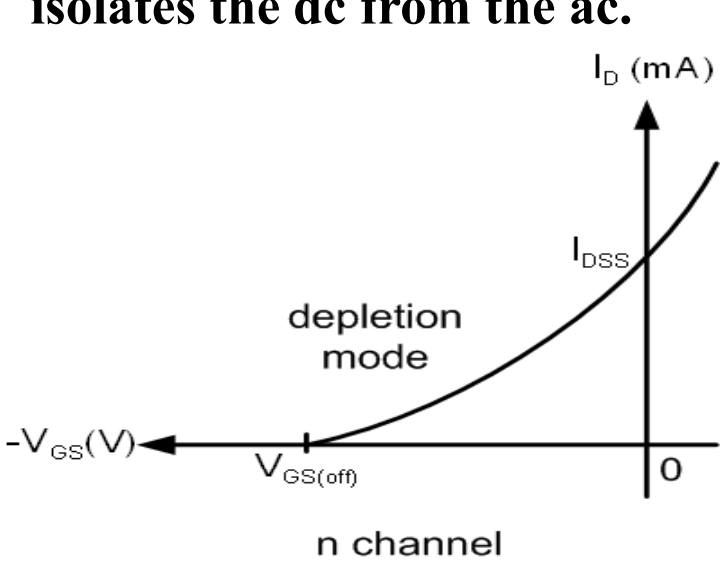
(c) $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = 10\ m\left[1 - \frac{(3)}{(-8)}\right]^2 = 18.91\,mA$$

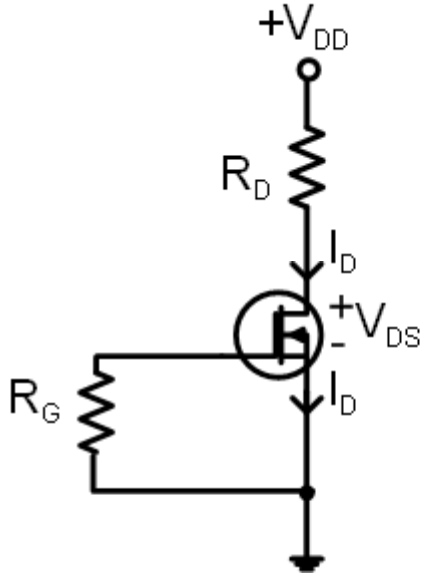
From the answers for (b) and (c), it is observed that if V_{GS} is negative, $I_D < I_{DSS}$. This is the operation of the n-channel D-MOSFET in the depletion mode. If the V_{GS} is positive, $I_D > I_{DSS}$ and this indicates that the transistor is operating in its enhancement mode.

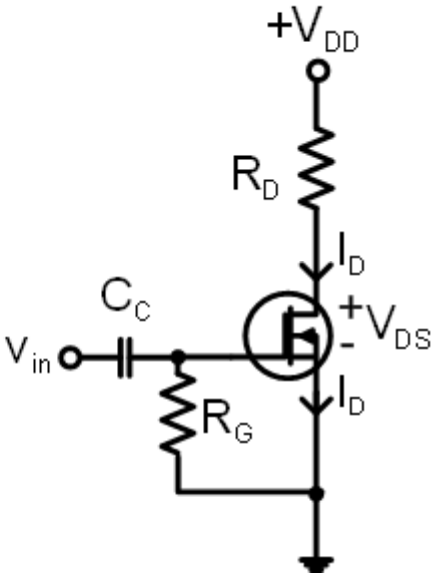
D-MOSFET Bias – Zero bias

As the D-MOSFET can be operated with either positive or negative values of V_{GS}, a simple bias method is to set $V_{GS} = 0$ so that an ac signal at the G varies the G-S voltage above and below this 0 V bias point.

- **$V_S = 0$ and $V_G = 0$ as $I_G = 0$. Hence, $V_{GS} = 0$. For $V_{GS} = 0$, $I_D = I_{DSS}$.**
- **$V_{DS} = V_{DD} - I_D R_D = V_{DD} - I_{DSS} R_D$**
- **The purpose of the R_G is to accommodate an ac signal input by isolating it from ground. Since there is no dc gate current, R_G does not affect the zero G-S bias. C_C is the coupling capacitor which isolates the dc from the ac.**

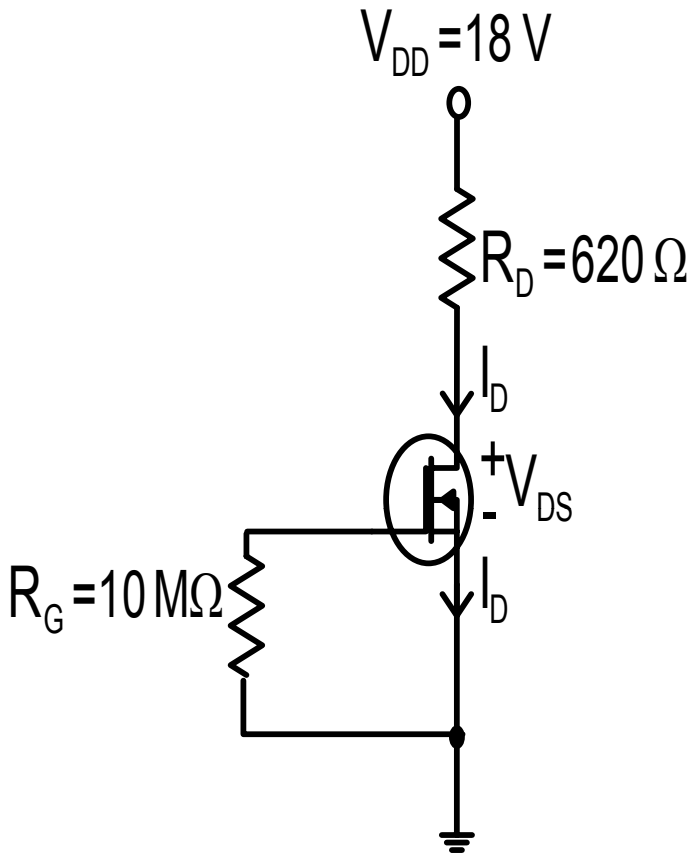






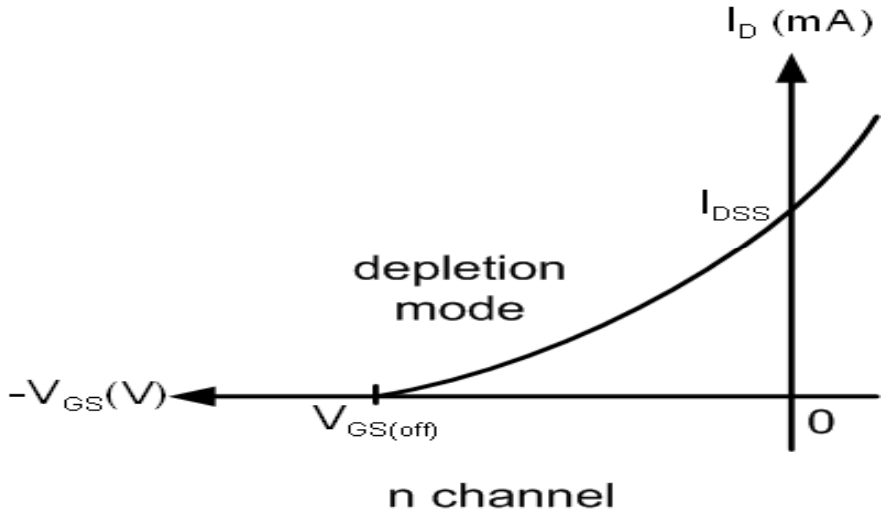
Example

Determine V_{DS} for the shown circuit. The MOSFET data sheet gives $V_{GS(off)}$ = -8 V and I_{DSS} = 12 mA.



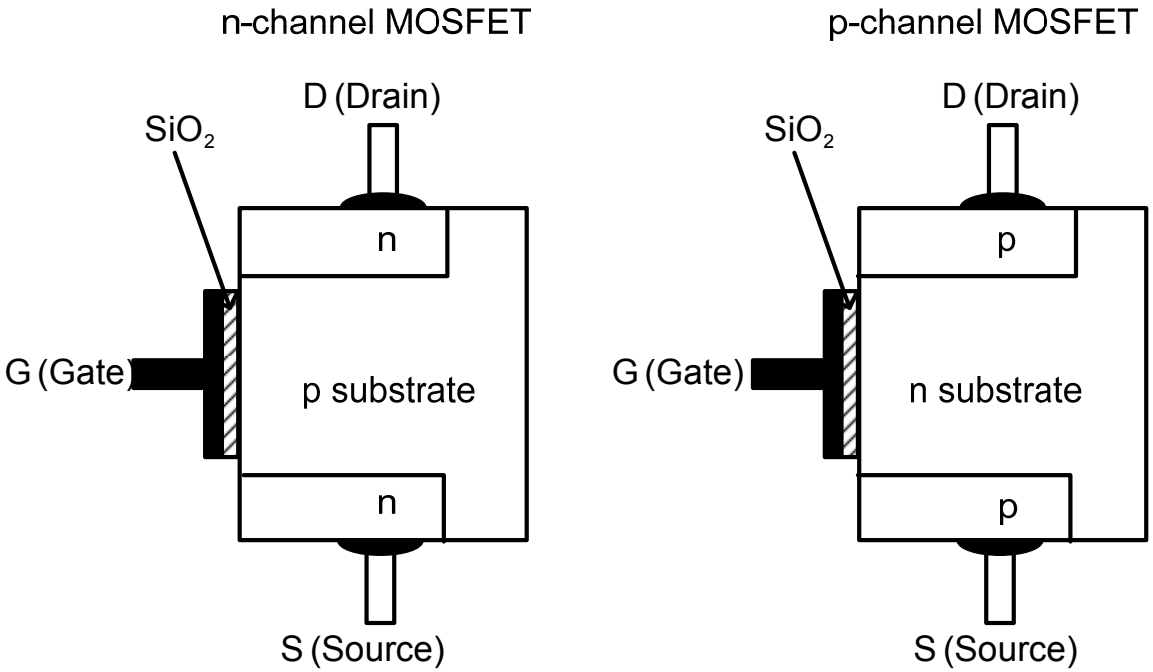
Solution

- **$I_D = I_{DSS}$ = 12 mA.**
- **$V_{DS}=V_{DD}-I_{DSS}R_D=18–12m(620)=10.56V.$**

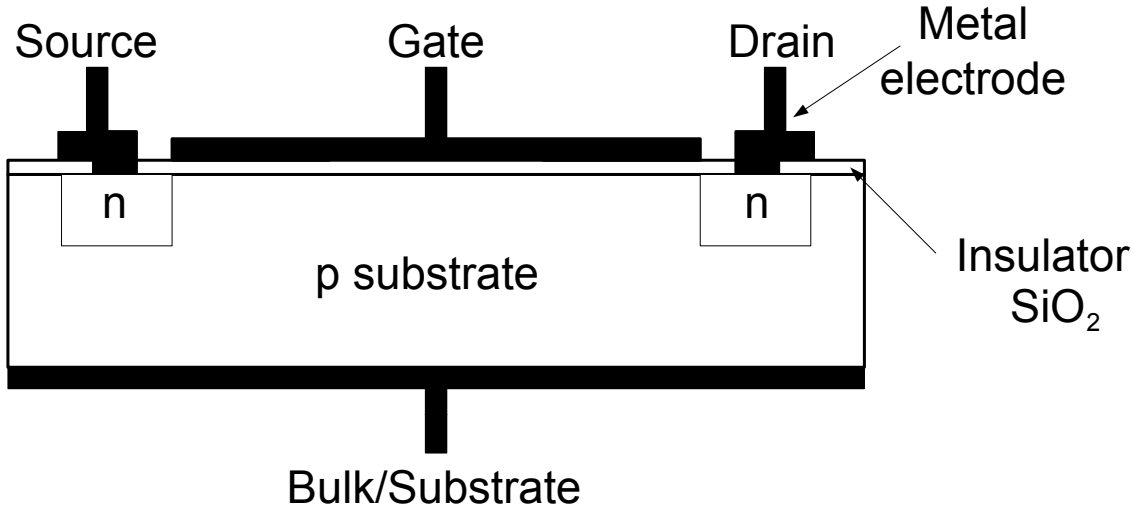


Enhancement MOSFET (E-MOSFET)

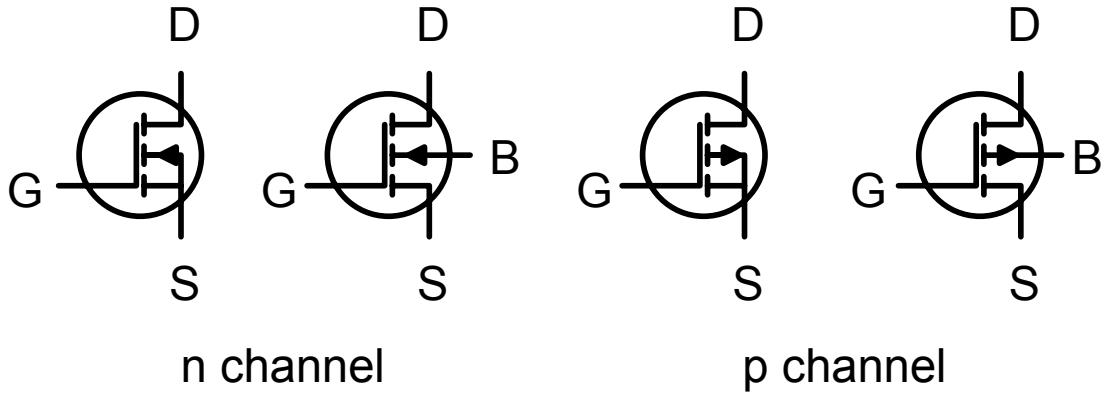
- **The E-MOSFET only operates in the enhancement mode and has no depletion mode. It differs in construction from the D-MOSFET in that it does not have a structural/physical channel.**
- **In an E-MOSFET, the substrate extends completely to the SiO_2 layer. Notice that there is no physical channel between S and D, like the one available in D-MOSFET.**



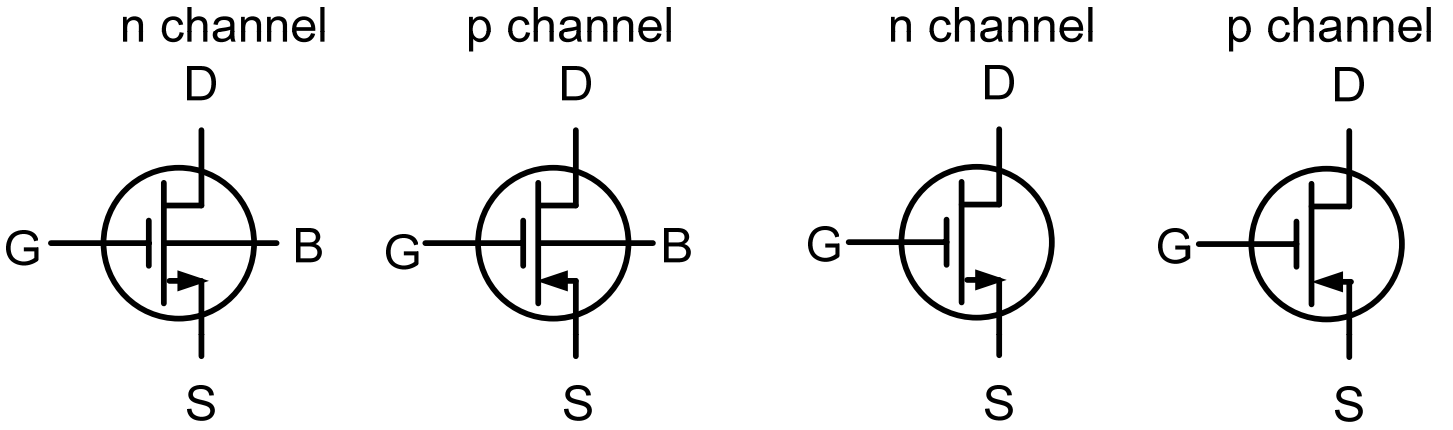
Cross section of conventional E-MOSFET structure is shown below:



Schematic symbols for the E-MOSFET are shown below. The broken lines symbolize the absence of a physical channel.

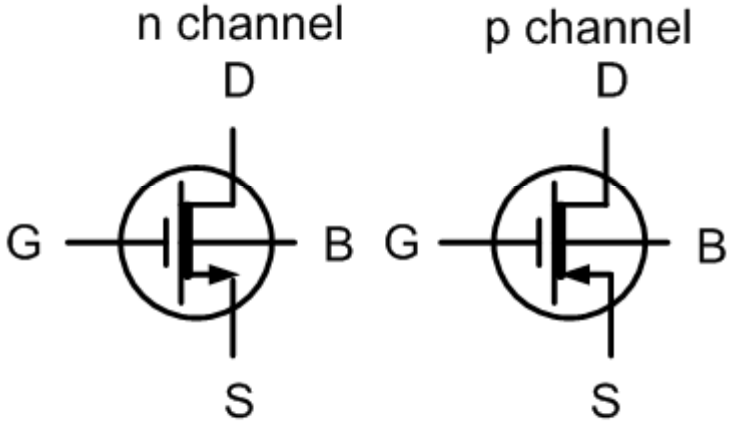


The symbols of the E-MOSFET in the circuit schematics are also normally obtained in the following forms:



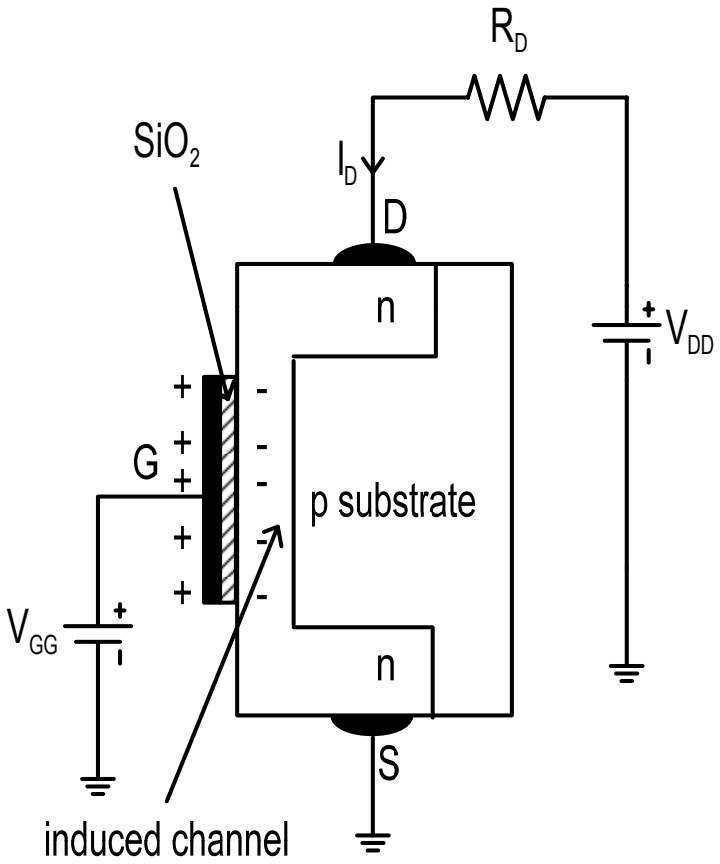
Typically implemented in analog application

Symbols used in CMOS circuits



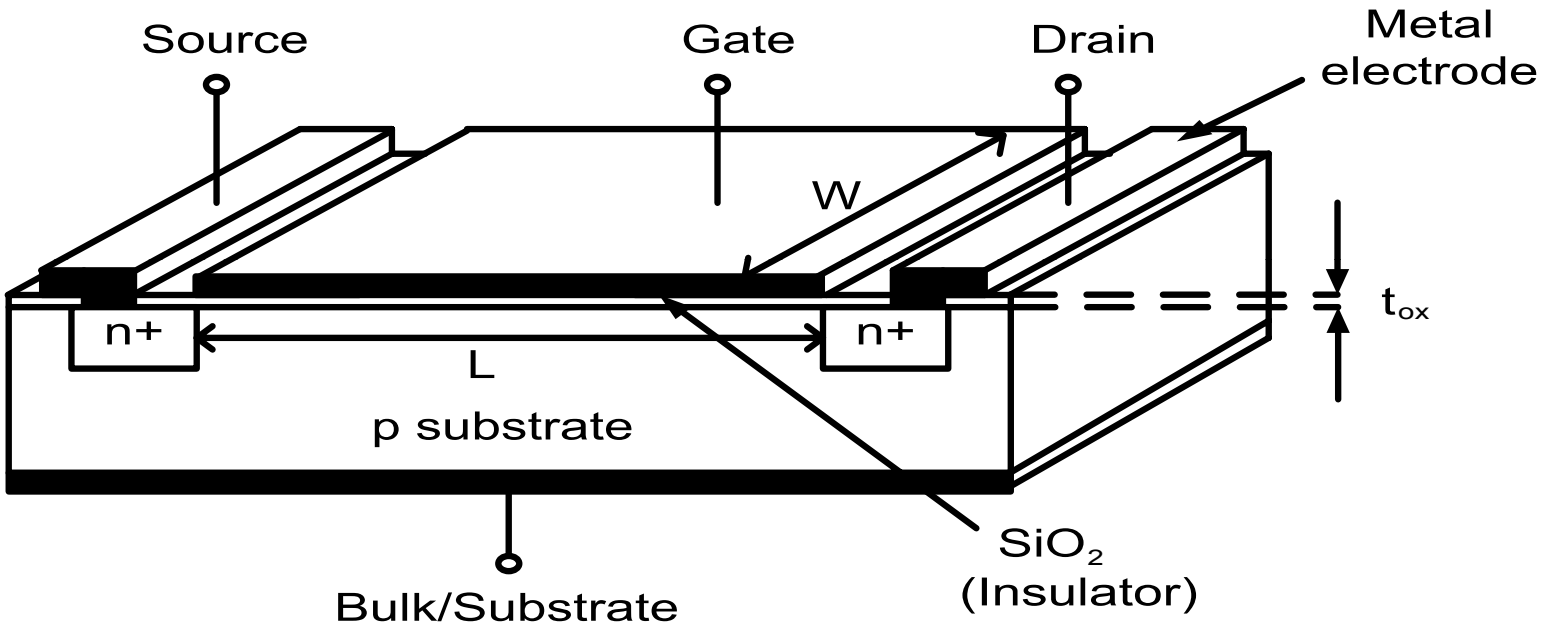
D-MOSFET

For the n-channel E-MOSFET, a positive gate above a threshold voltage induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer. The conductivity of the channel is enhanced by increasing the V_{GS} which can attract more electrons into the channel area. For any G voltage below the threshold value, there is no channel.



E-MOSFET Operation

Cross-section diagram of an E-MOSFET:

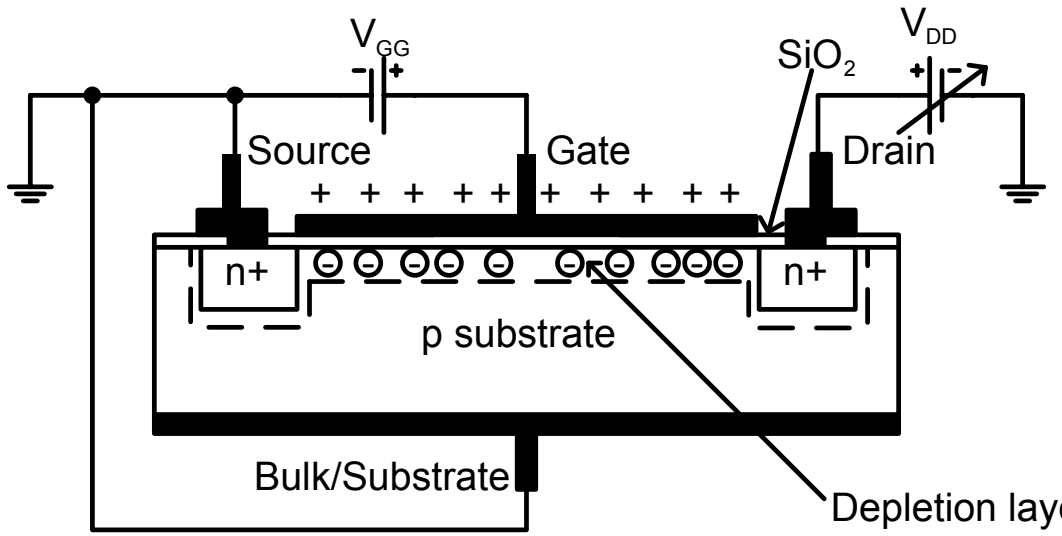


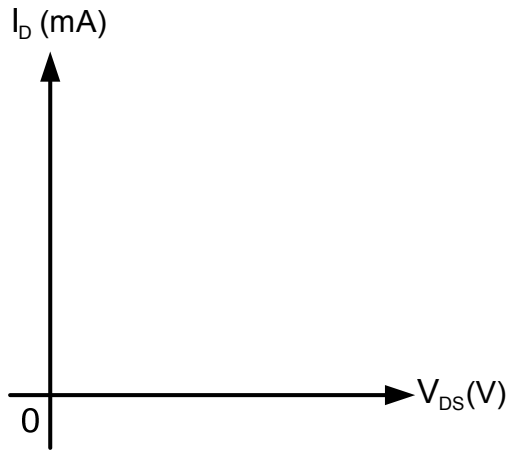
1. **<u>When $V_{DS} = 0$ and $V_{GS} = 0$</u>**

   If $V_{GS} = 0$, there will be no channel induced. Besides this, $V_{DS} = 0$ and therefore no electrons are flowing from S to D. Hence, $I_D = 0$.

2. When $V_{GS} < V_{GS(th)}$

The p substrate underneath the G forms a depletion layer as holes move further into the bulk, away from this area. Fixed negative ions will be left in this depletion layer. As S and D are separated by the depletion layer and the lowly doped p, no current will flow even though V_{DS} is available and positive. In this circuit, $V_{GG} = V_{GS}$ and $V_{DD} = V_{DS}$.

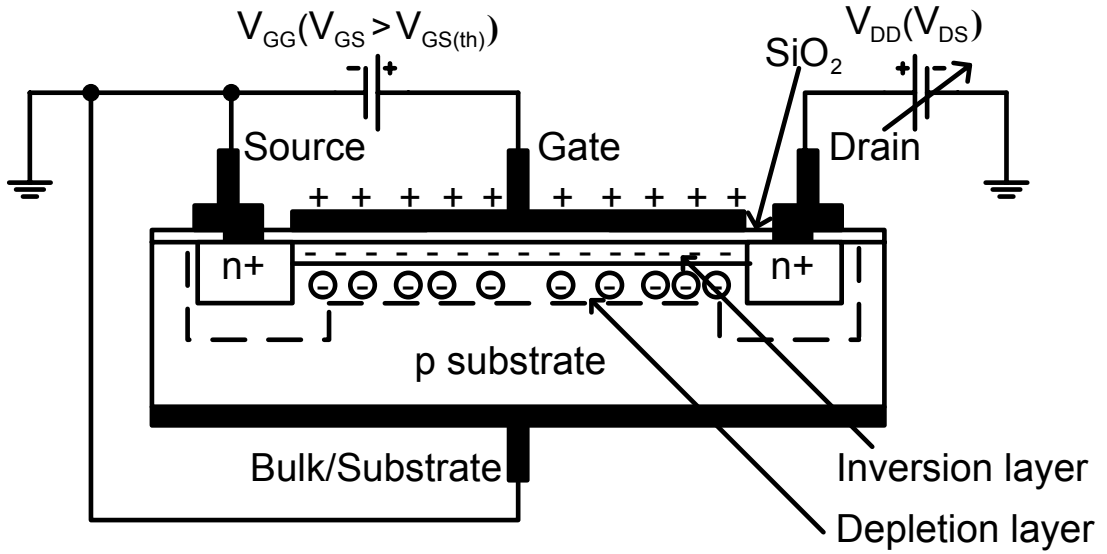




3. When $V_{GS} > V_{GS(th)}$

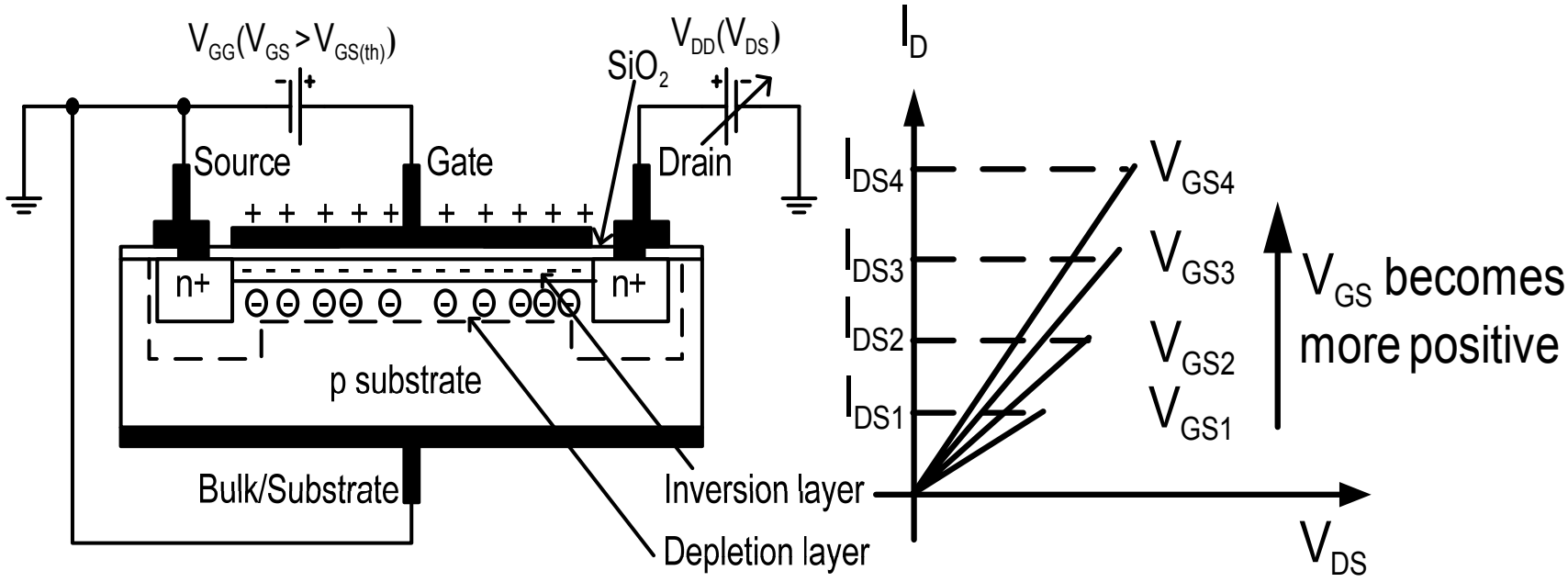
The electrons, which are the minority carriers from the substrate, and the electrons from S and D will be attracted to the region beneath the G and SiO_2. These electrons will form one layer and since they are having charges opposite to the holes of the substrate, this layer is known as the inversion layer. The inversion layer forms the channel that connects the S to D. If $V_{DS} = 0$, I_D will still be 0 as there is no movement of electrons from S to D. If $V_{DS} > 0$, electrons from S will move along the channel toward D and generate current.

- **"Enhancement" for the E-MOSFET is referring to the $V_{GS} > V_{GS(th)}$ that is required to increase or enhance the channel conductivity between D and S.**



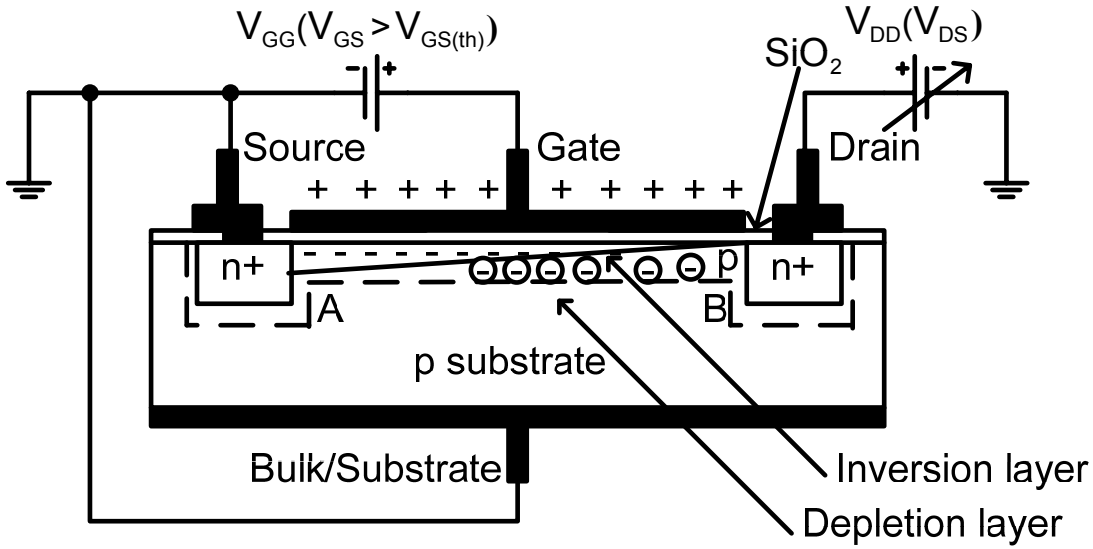
- **If V_{DS} is small, the E-MOSFET is operating as a linear resistor whose resistance is determined by the V_{GS}. When V_{GS} is large, the number of electrons in the channel is increased, conductivity of channel increases, resistance will decrease and current becomes larger.**

- **When $V_{GS} > V_{GS(th)}$ and V_{DS} is small, the device is said to be in its triode region of operation. Under this condition, $I_D \propto (V_{GS} - V_{GS(th)})V_{DS}$. So, if $V_{GS} > V_{GS(th)}$ and $V_{DS} > 0$, I_D will exists. If V_{DS} is increased, I_D will also increase as more electrons will be able to flow from S to D.**

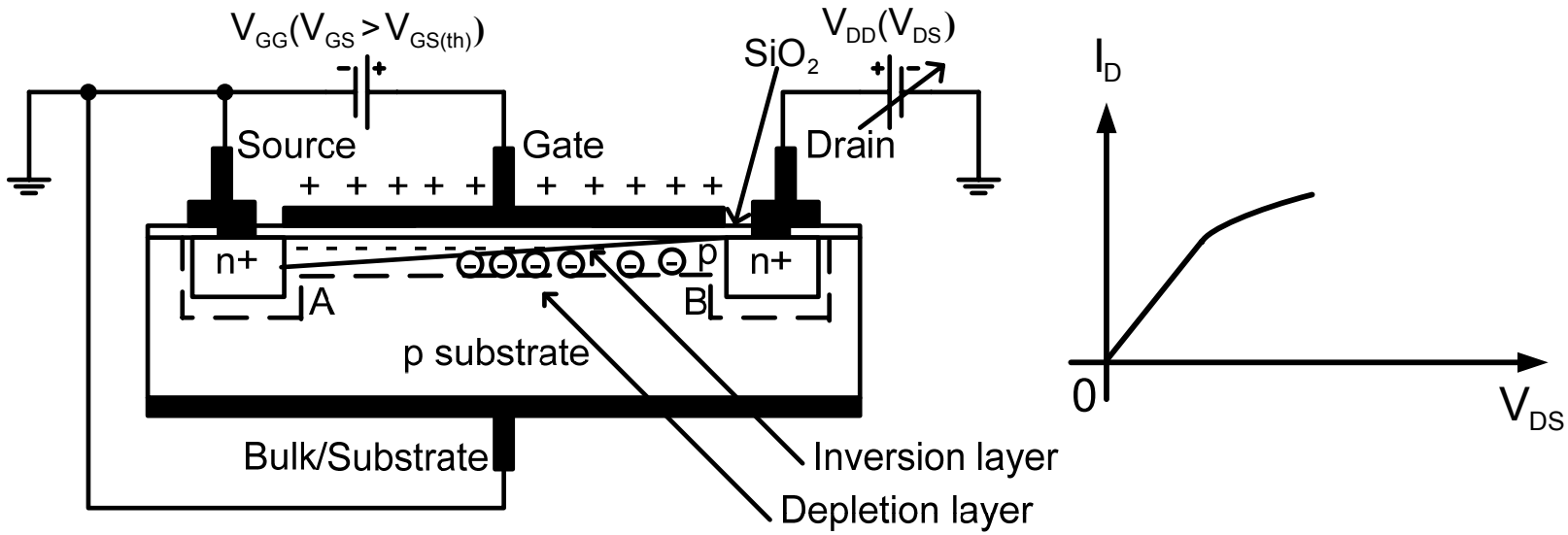


4. When $V_{GS} > V_{GS(th)}$ and V_{DS} is increased (still $V_{DD} < V_{GG}$ i.e. $V_{DS} < V_{GS}$)

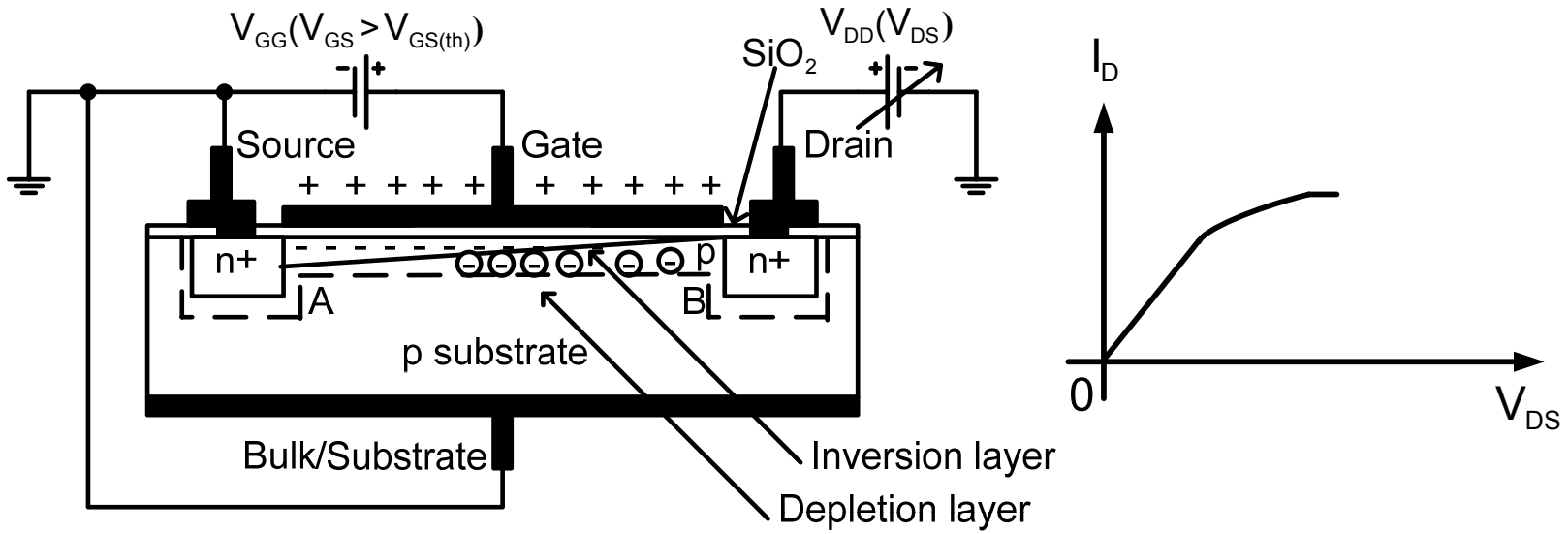
- **Voltage varies along the channel, with 0 V at A (near S) and V_{DD} (or V_{DS}) at B (near D).**
- **The gate-to-channel voltage is V_{GS} at A and V_{GD} at B. The potential at A is dependent on V_{GS} and not on V_{DS}.**
- **$V_{GD} = V_G - V_D = V_{GG} - V_{DD}$**



- $V_{GD} = V_G - V_D = V_{GG} - V_{DD}$
- **If V_{GG} is fixed and V_{DD} is increased, V_{GD} will decrease. The width of the inversion layer is dependent on the voltage across G and the channel. Hence, the channel becomes narrower in approaching B. The channel is widest at A and narrowest at B. The conductivity at B becomes low. The I_D vs V_{DS} slope becomes lower. The current and voltage relationship is no longer linear.**

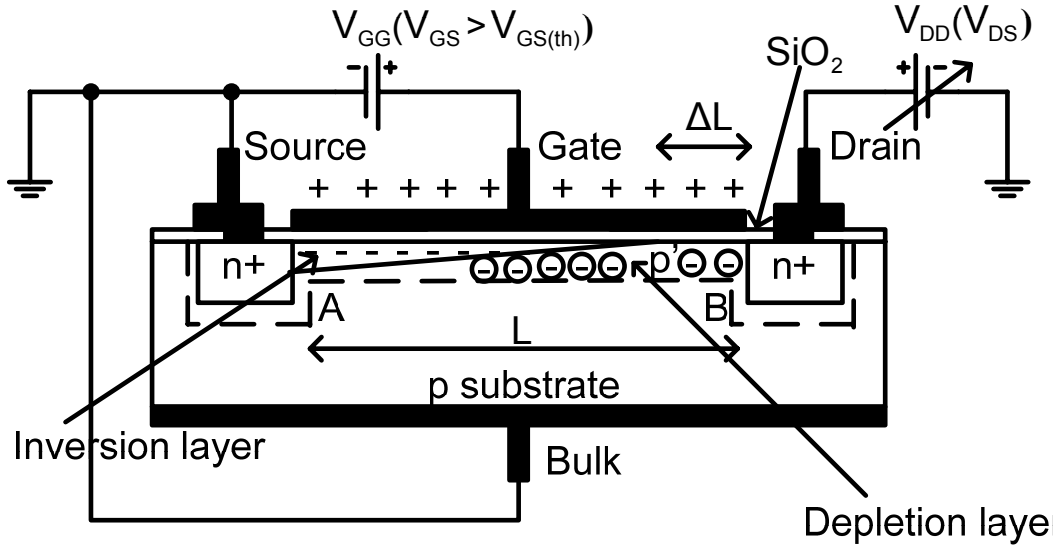


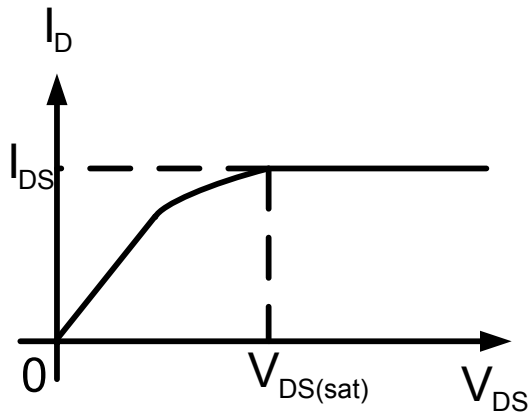
- **If V_{GD} approaches $V_{GS(th)}$, the inversion layer at B will disappear, leaving only the depletion layer. Channel is pinched-off at p. This condition occurs when $V_{DS} = V_{DS(sat)}$.**
- **$V_{GD} = V_G - V_D = V_{GS} - V_{DS} = V_{GS} - V_{DS(sat)} = V_{GS(th)}$**
- **At pinched-off, $V_{DS(sat)} = V_{GS} - V_{GS(th)}$**
- **The charge concentration of the inversion layer near D is 0. As slope = $\Delta I_D / \Delta V_{DS}$ and $\Delta I_D = 0$, the I_D vs V_{DS} slope at this point is also 0.**



5. $V_{DS} > V_{DS(sat)}$

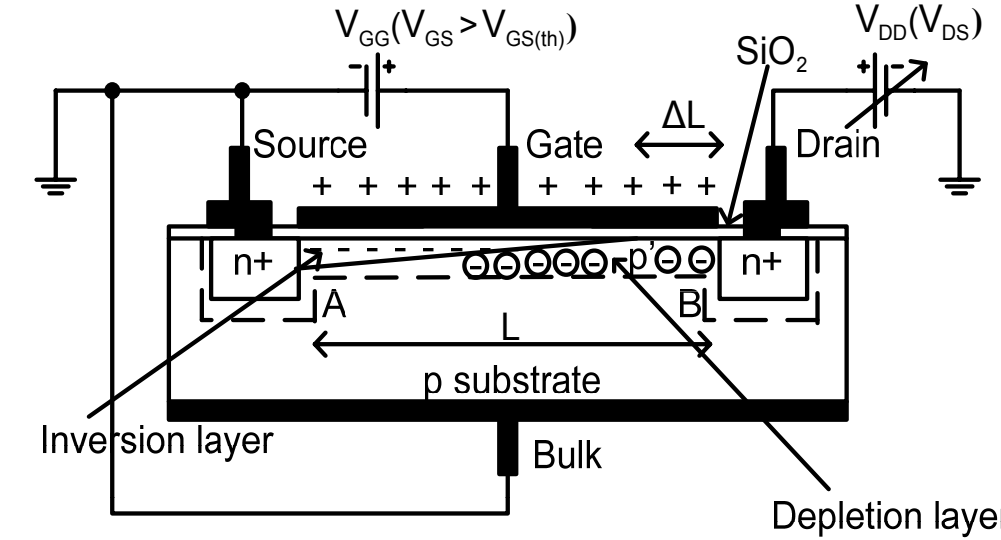
- **The point in the channel where the inversion charge is 0 moves towards S (at point p'). Under this condition, the electrons from S move along the channel toward D, reach p' and will be injected into the space charge region where they will be swept to the D contact by the electric field, E.**
- **If $\Delta L << L$ is to be assumed, I_D will be maintained for $V_{DS} > V_{DS(sat)}$.**

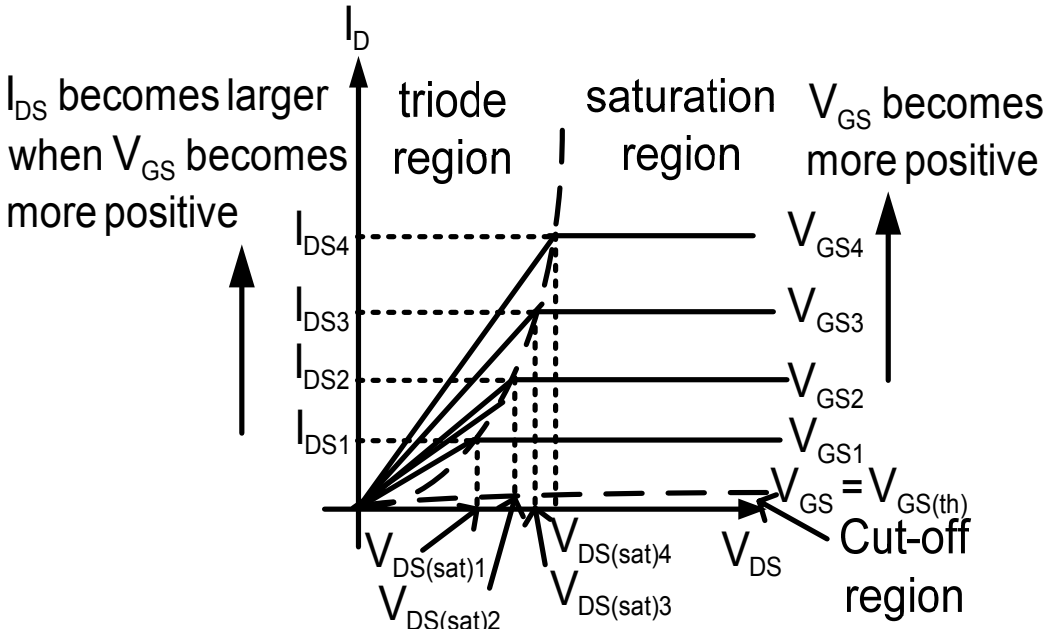




Drain characteristic of the n-channel E-MOSFET

If V_{GS} increases, there will be more electrons in the channel and the conductivity of the channel will increase. Hence, I_D will also increase. The saturation region is where the E-MOSFET will be operating as an amplifier.

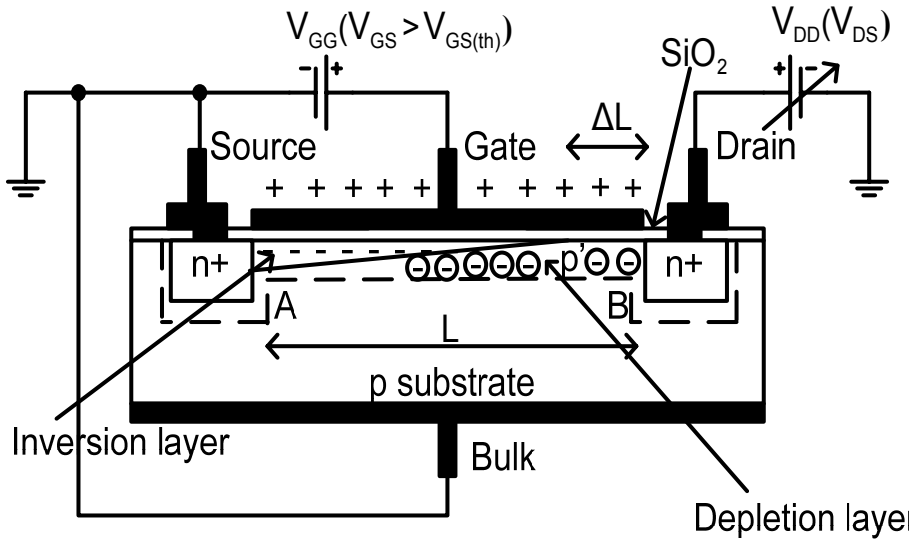


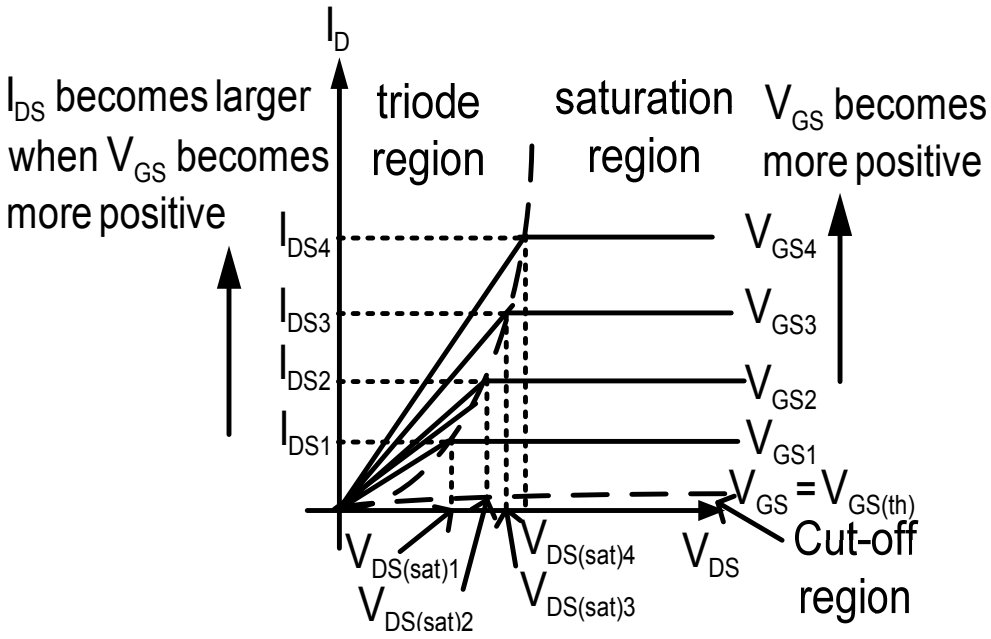


Requirements for current to flow:

1. **To obtain enough carriers in the channel to generate current, $V_{GS} > V_{GS(th)}$.**

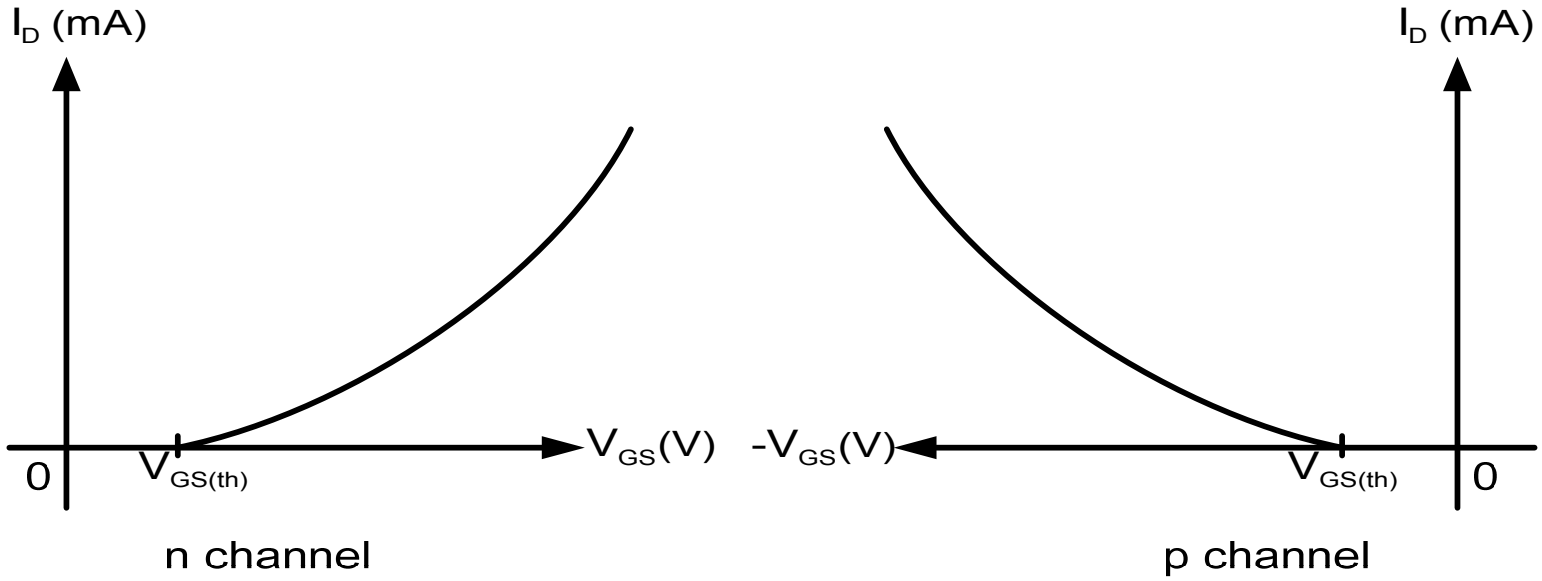
2. **If $V_{GS} > V_{GS(th)}$, $V_{DS} > 0$ to enable electrons to flow from S to D and generate current. If $V_{DS} < V_{DS(sat)}$, the E-MOSFET is in the triode region of operation. Once $V_{DS} > V_{DS(sat)}$, the device will be in the saturation mode of operation.**





E-MOSFET transfer characteristic

- **The E-MOSFET uses only channel enhancement. n-channel device requires a positive V_{GS} to induce a channel and a p-channel device requires a negative V_{GS} for the same purpose.**
- **From the transfer characteristic, it is seen that when $V_{GS} = 0$, $I_D = 0$. There is no I_{DSS} parameter in a E-MOSFET, unlike JFET and D-MOSFET. Notice that there is no drain current until V_{GS} reaches a certain value called the threshold voltage, $V_{GS(th)}$.**

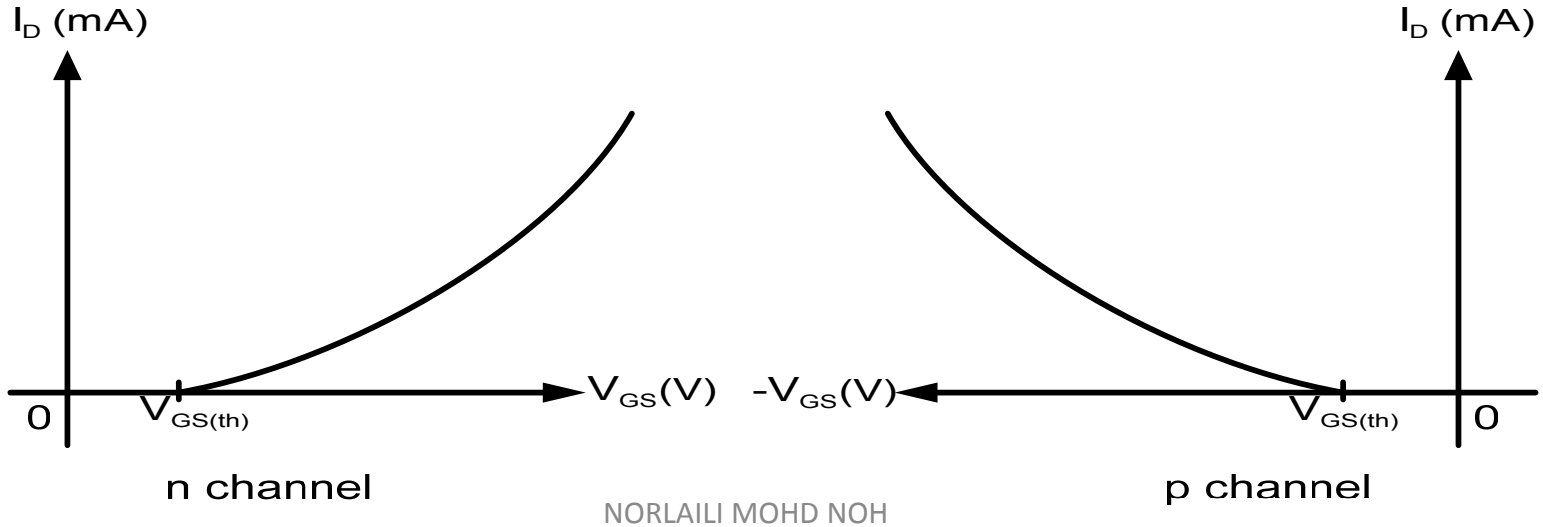


The equation for the parabolic transfer characteristic curve of the E-MOSFET differs from that of the JFET and the D-MOSFET because the curve starts at $V_{GS(th)}$ rather than $V_{GS(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the E-MOSFET transfer characteristic curve is:

$I_D = K(V_{GS} - V_{GS(th)})^2$ where $K = (\mu C_{ox}/2)(W/L)$.

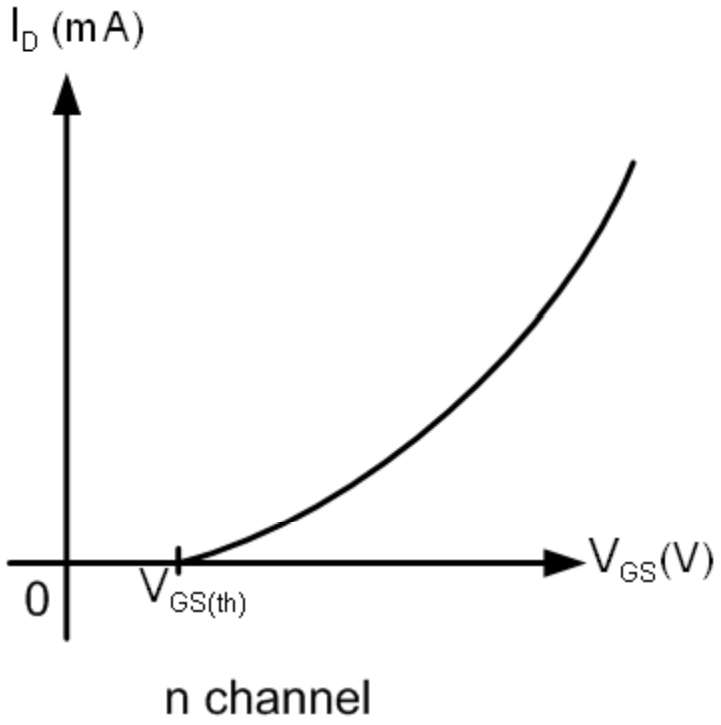
μ is carrier mobility, $C_{ox}=\varepsilon_{ox}/t_{ox}$ is SiO_2 capacitance, W is width and L is length of the channel, respectively. $\varepsilon_{ox}=3.9x\varepsilon_o$ for SiO_2 . $\varepsilon_o=8.84x10^{-12}$ F/m and is the permittivity of free space. t_{ox} is thickness of SiO_2.

K depends on the particular MOSFET and can be determined from the data sheet by taking the specified value of I_D, called $I_{D(on)}$ at the given value of V_{GS} and substitute the values into the equation shown.



Example

The data sheet for a 2N7008 E-MOSFET gives $I_{D(on)}$ = 500 mA at V_{GS} = 10 V and $V_{GS(th)}$ = 1 V. Determine the drain current for V_{GS} = 5 V.

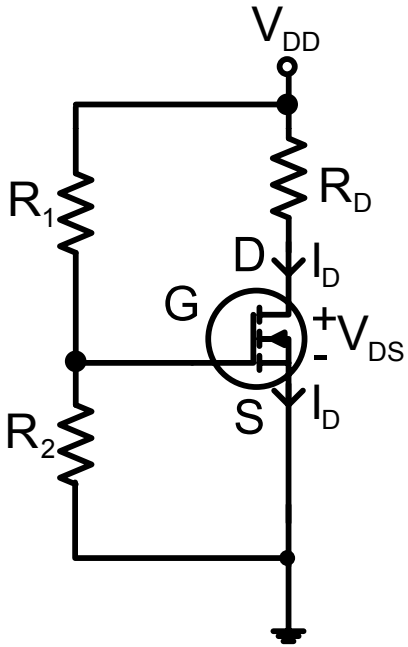


Solution

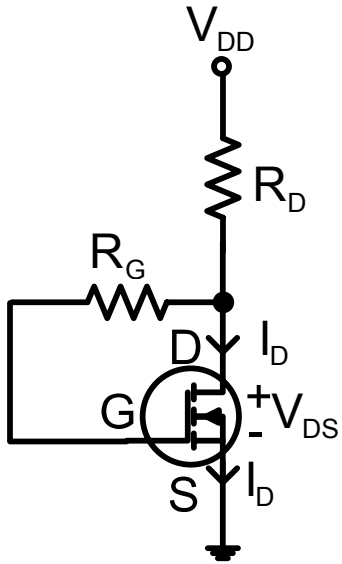
- $I_D = K(V_{GS} - V_{GS(th)})^2$
- $500\ m = K(10 - 1)^2$
- $K = 6.17\ mA/V^2$
- $I_D = 6.17\ m(5 - 1)^2 = 98.7\ mA$

E-MOSFET Biasing

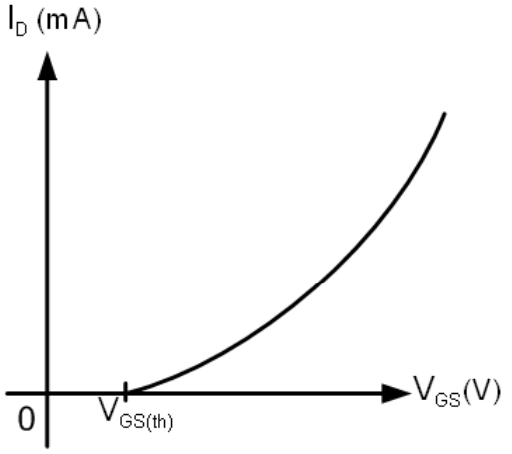
E-MOSFET must have a $V_{GS} > V_{GS(th)}$. Hence, zero bias cannot be used for this type of transistor. Voltage-divider bias and drain-feedback bias can be implemented for this device. These bias circuits can also be used for the D-MOSFET.



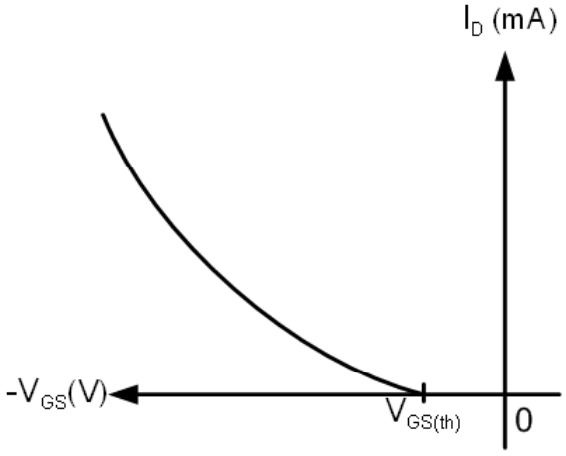
Voltage-divider bias



Drain-feedback bias



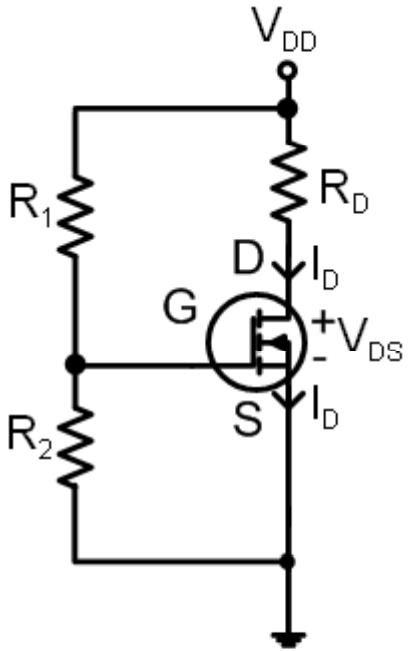
n channel



p channel

Voltage-divider bias

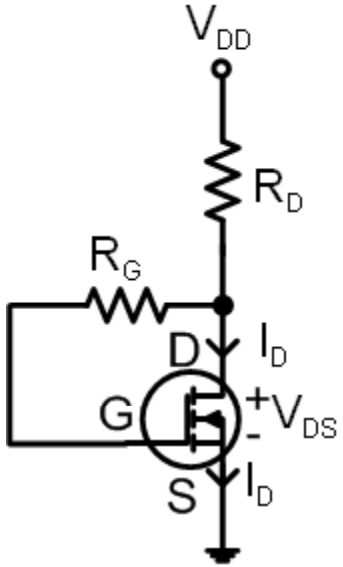
- $V_{GS} = V_G - V_S$
- Since $V_S = 0$, $V_{GS} = V_G$
- $V_{GS} = (R_2 V_{DD}) / (R_1 + R_2)$
- $V_{DS} = V_{DD} - I_D R_D$



Voltage-divider bias

Drain-feedback bias

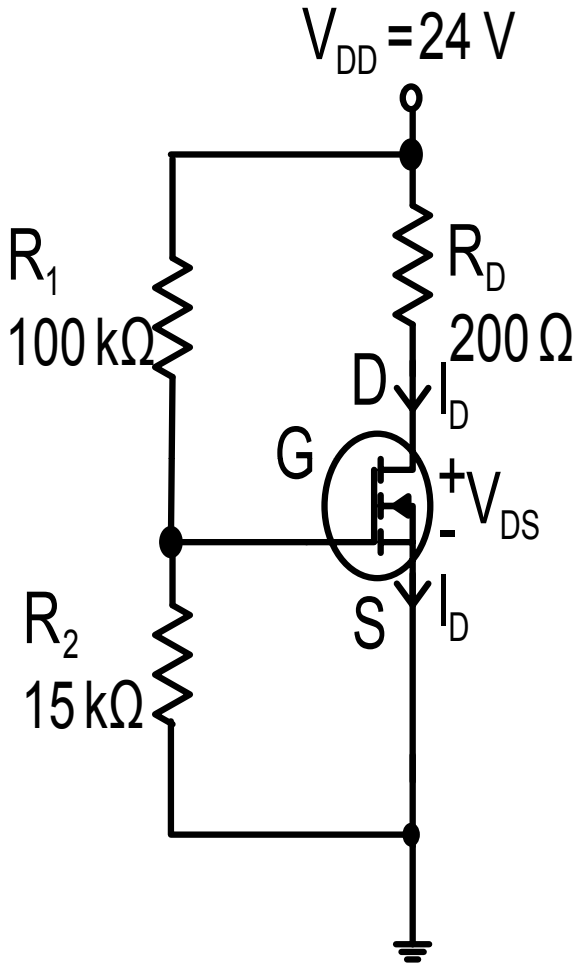
- Since $I_G = 0$, there is no voltage drop across R_G. Therefore, $V_D = V_G$.
- Since $V_S = 0$, $V_{DS} = V_{GS}$.



Drain-feedback bias

Example

Determine V_{GS} and V_{DS} for the following E-MOSFET circuit. Assume that the device in this circuit has $I_{D(on)} = 200$ mA at $V_{GS} = 4$ V and $V_{GS(th)} = 2$ V.

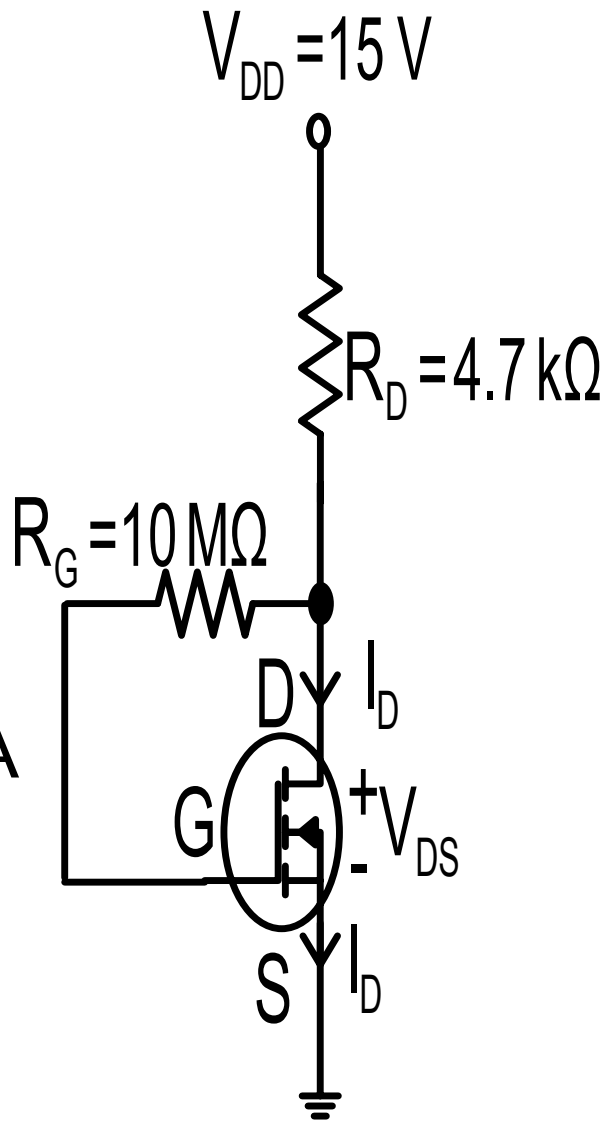


Solution

- $V_{GS} = (R_2\ V_{DD}) / (R_1 + R_2) = 15\ k(24)/115\ k = 3.13$ V
- $I_D = K(V_{GS} - V_{GS(th)})^2$
- $200\ m = K(4 - 2)^2$
- $K = 50\ mA/V^2$
- $I_D = 50\ m(3.13 - 2)^2 = 63.8$ mA
- $V_{DS} = V_{DD} – I_D R_D$
- Hence, $V_{DS} = 24 – 63.8\ m(200) = 11.2$ V.

Example

Determine the amount of drain current in the following circuit. The MOSFET has a $V_{GS(th)}$ = 3 V. Given V_{GS} = 8.5 V.



Solution

- V_{GS} = 8.5 V.
- Therefore, $V_{DS} = V_D$ = 8.5 V.

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{15 - 8.5}{4.7\ k} = 1.38\ mA$$

General expression to relate current, I_D, with V_{GS} and V_{DS}:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2\left(V_{GS} - V_{GS(th)}\right)V_{DS} - V_{DS}^2\right]$$

W = channel width

μ_n = electron mobility (for n-channel E-MOSFET)

C_{ox} = oxide capacitance per unit area

L = channel length

For small V_{DS} (triode region), V_{DS}^2 becomes small and can be assumed insignificant.

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2\left(V_{GS} - V_{GS(th)}\right)V_{DS}\right]$$

$$= \frac{\mu_n C_{ox} W}{L}\left[\left(V_{GS} - V_{GS(th)}\right)V_{DS}\right]$$

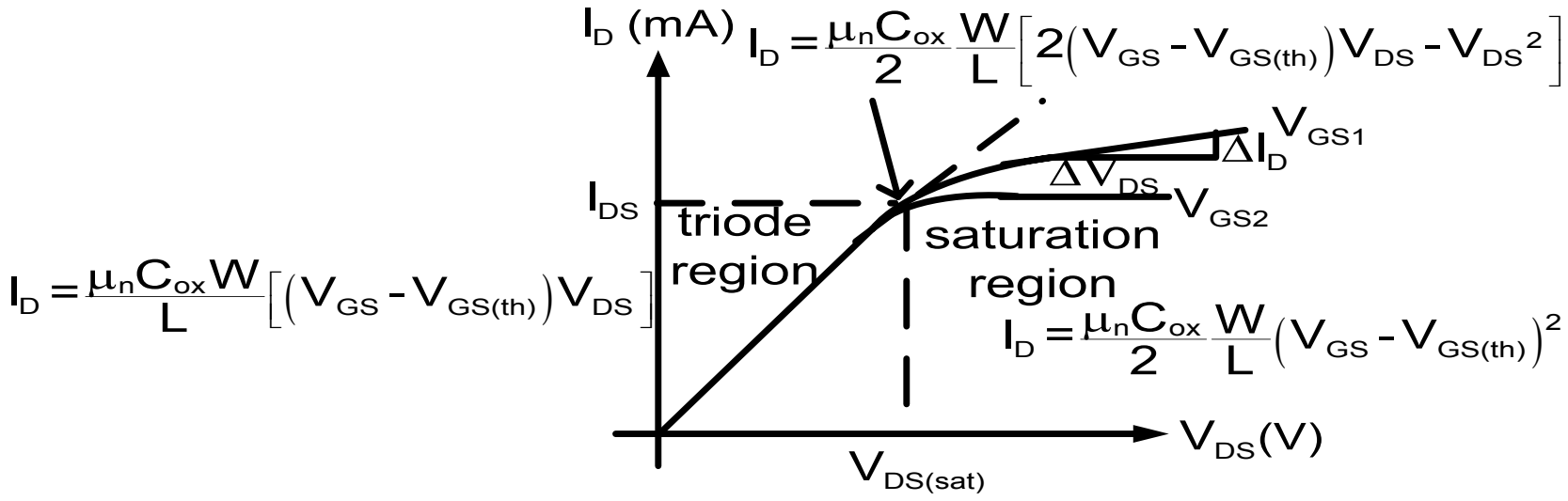
For the $V_{DS} \geq V_{DS(sat)}$ ($V_{DS(sat)} = V_{GS} - V_{GS(th)}$)

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2\left(V_{GS} - V_{GS(th)}\right)\left(V_{GS} - V_{GS(th)}\right) - \left(V_{GS} - V_{GS(th)}\right)^2\right]$$

$$= \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2\left(V_{GS} - V_{GS(th)}\right)^2 - \left(V_{GS} - V_{GS(th)}\right)^2\right]$$

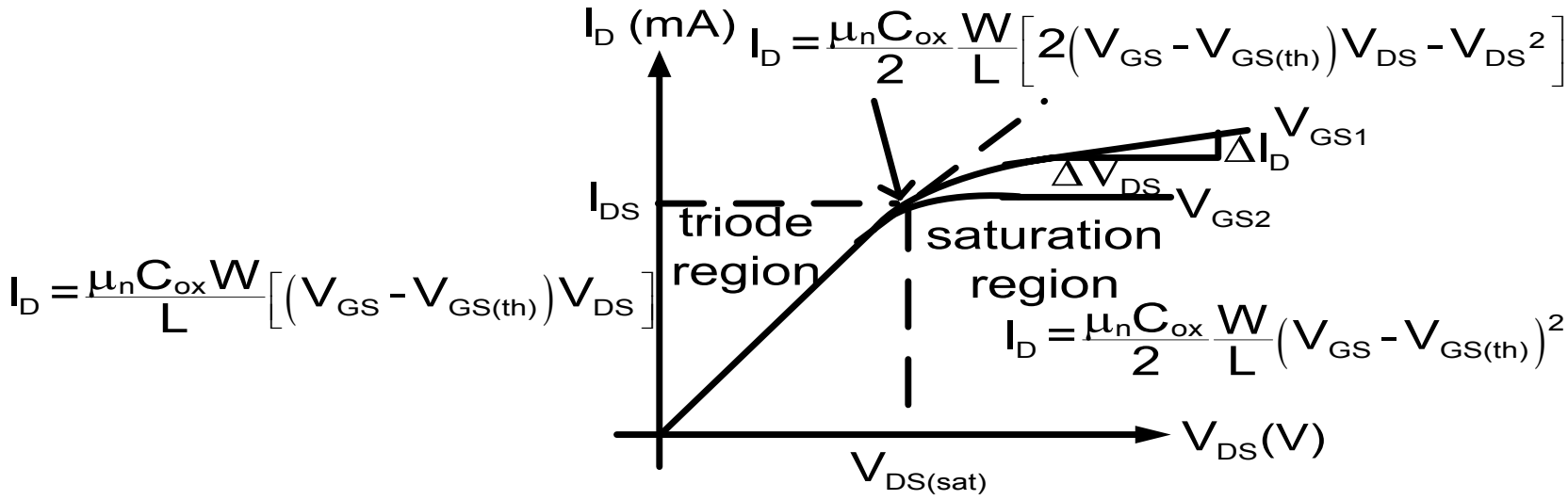
$$= \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{GS(th)}\right)^2$$

$I_D = K(V_{GS} - V_{GS(th)})^2$ where $K = \frac{\mu_n C_{ox}}{2}\frac{W}{L}$.



- **Notice that in the saturation region, I_D is independent of V_{DS} (such as shown by the plot of V_{GS2}).**
- **In reality, I_D does increase a little bit when V_{DS} increases (such as shown by the plot of V_{GS2}).**
- **In the saturation region:**

  Slope = $\Delta I_D/\Delta V_{DS} = 1/r_o$
- **ΔI_D is so small. $1/r_o$ is so small. r_o is very large. To simplify analysis, r_o can be assumed ∞ (open).**

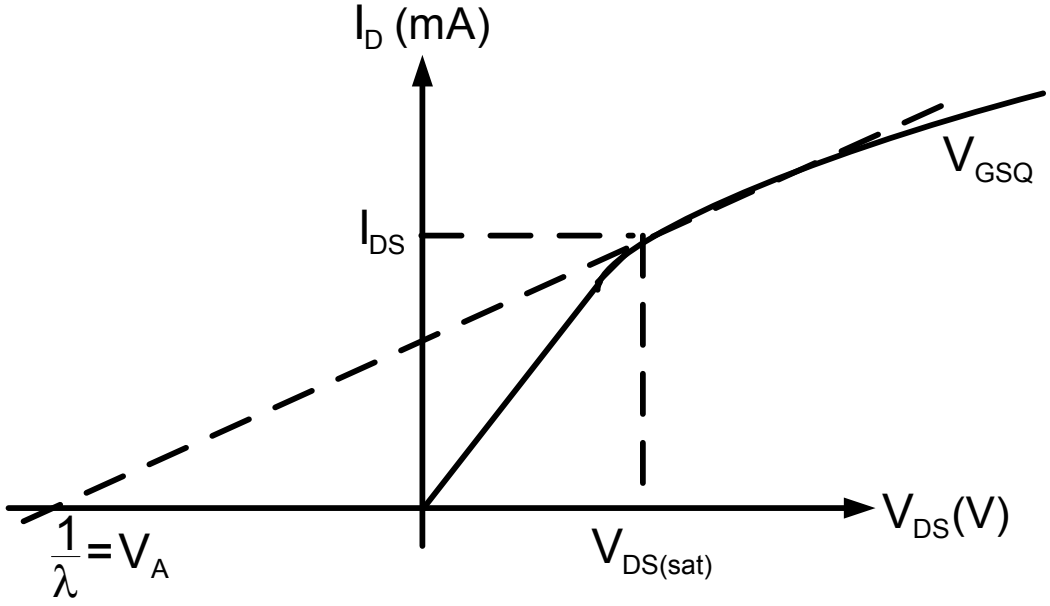


- **If the slope is not ignored,**

$$I_D = K\left(V_{GS} - V_{GS(th)}\right)^2\left(1 + \lambda V_{DS}\right)$$

- **where λ = channel length modulation parameter (typical value is 0.01 V^{-1}).**
- **If extend the slope to the $-V_{DS}$ axis, the line will intersect the $-V_{DS}$ axis at $1/\lambda$.**

- **$1/\lambda = V_A$ = Early voltage**



p-channel E-MOSFET

I-V relationship in PMOS

1. **for $V_{SD} \le V_{SD(sat)}$:** $I_D = \frac{\mu_p C_{ox}}{2}\frac{W}{L}\left[2\left(V_{SG} + V_{GS(th)}\right)V_{SD} - V_{SD}^2\right]$

2. **for $V_{SD} \ge V_{SD(sat)}$ (channel length modulation is ignored and $V_{SD(sat)} = V_{SG} + V_{GS(th)}$:** $I_{DS} = \frac{\mu_p C_{ox}}{2}\frac{W}{L}\left(V_{SG} + V_{GS(th)}\right)^2$

3. **for small V_{SD} :** $I_D = \frac{\mu_p C_{ox} W}{L}\left[\left(V_{SG} + V_{GS(th)}\right)V_{SD}\right]$

   For an n-channel E-MOSFET (NMOS), the $V_{GS(th)}$ is positive whereas for a p-channel E-MOSFET (PMOS), the $V_{GS(th)}$ is negative.