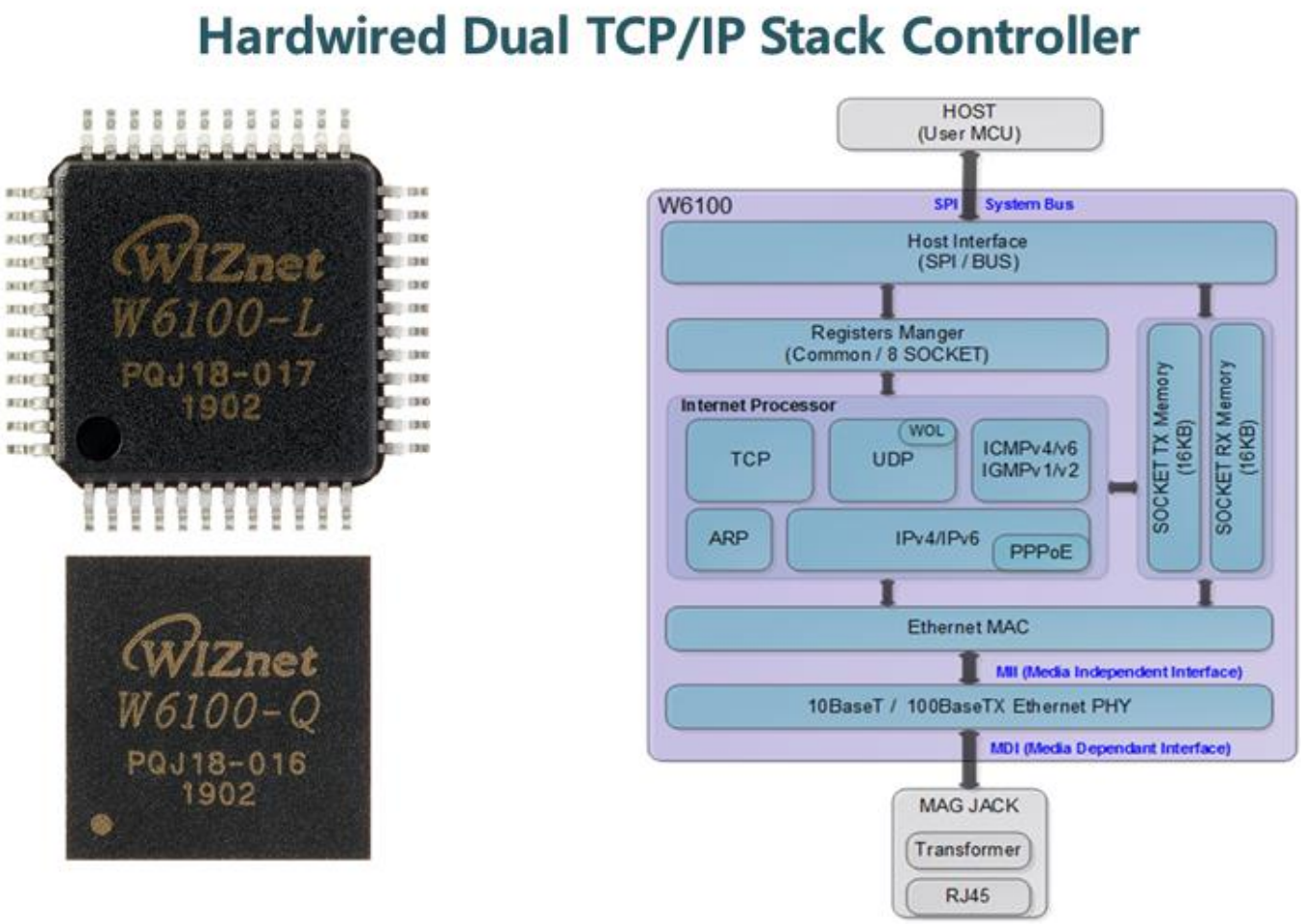
WoW!!! Hardwired Dual TCP/IP Stack Controller - W6100 [PART II]

by MC



Overview

Part I briefly reviewed the overall IPv6 features.

In this Part II, Let's review these IPv6 functions How to implement and apply on Hardwired Dual TCP / IP Stack Controller - W6100.

The belows are features of W6100.

Features

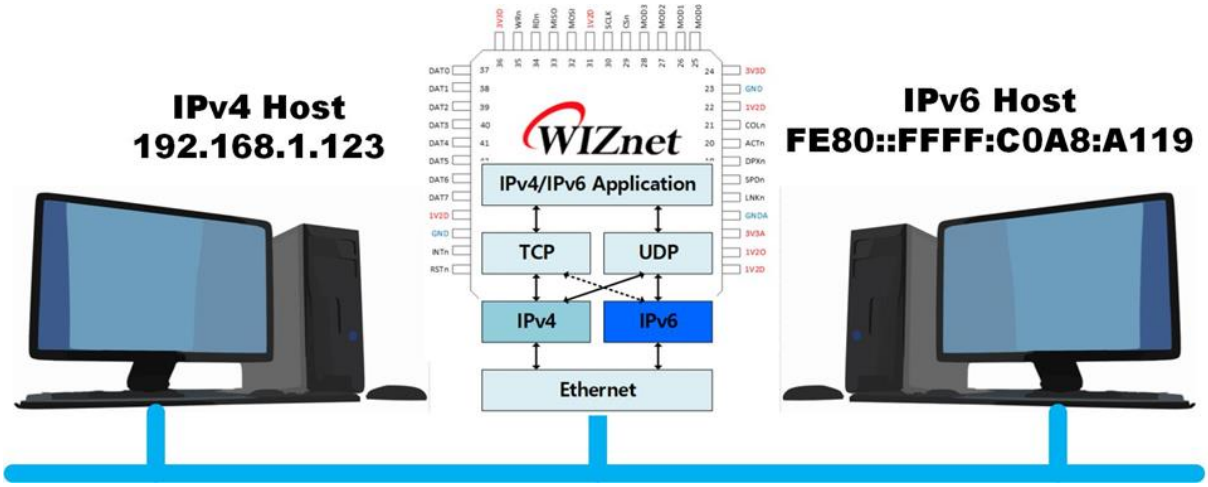
- Support Hardwired TCP/IP Protocols : TCP, UDP, **IPv6**, IPv4, **ICMPv6**, ICMPv4, IGMP, **MLDv1**, ARP, PPPoE
- Support IPv4/IPv6 **Dual** Stack

- Support 8 independent SOCKETs simultaneously
- Support Ethernet Power Down Mode & Clock switching for power save
- Support Wake on LAN over UDP
- Support **SOCKET-less Command**
- Support Serial & Parallel Host Interface
- Internal 32KBytes Memory for TX/ RX Buffers
- 10BaseT / **10BaseTe** / 100BaseTX Ethernet PHY Integrated
- 48 Pin LQFP & QFN Lead Free Package (7x7mm, 0.5mm pitch)
- W5100S **PIN-2-PIN Compatible**

Dual TCP/IP Stack

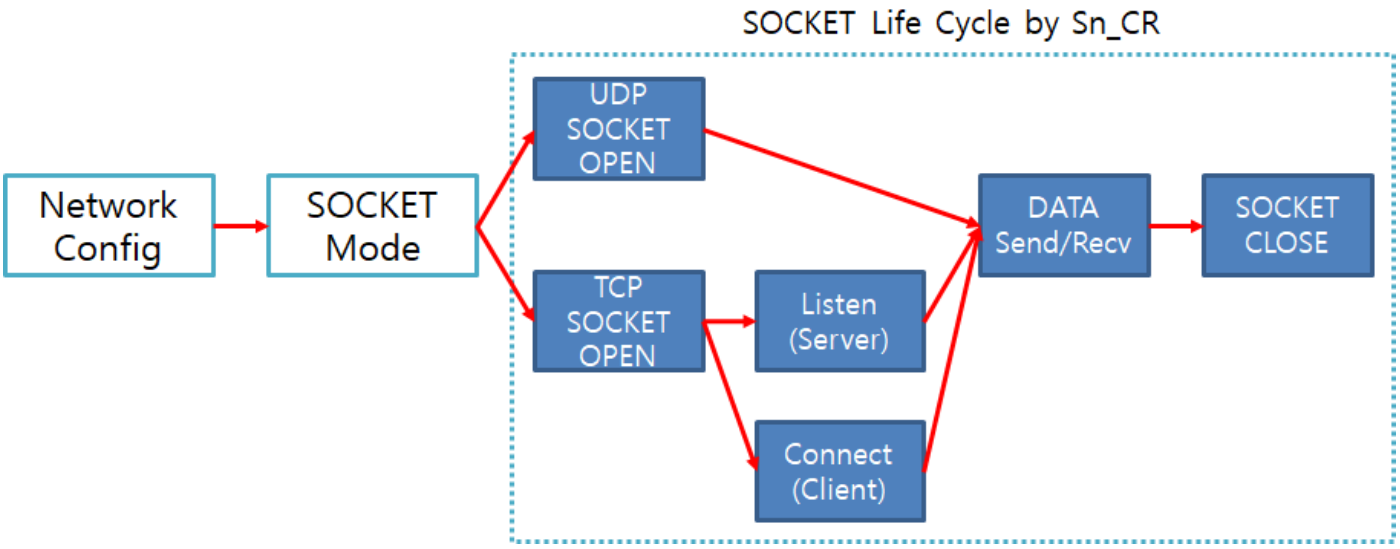
The W6100 supports Dual Stack, one of three IPv6 translation methods. Because Dual Stack has both IPv4 and IPv6 stack, It is capable of supporting IPv6 communication as well as IPv4 communication.

As shown in the following figure, **W6100** can communicate with a packet of upper application layer such as TCP and UDP based on IPv4 address, and also with a packet based on IPv6 address at that same time.



How to use W6100?

After initializing W6100, You can communicate by using the **SOCKETs** of W6100. The **SOCKETs** operates the life-cycle such as following figure.



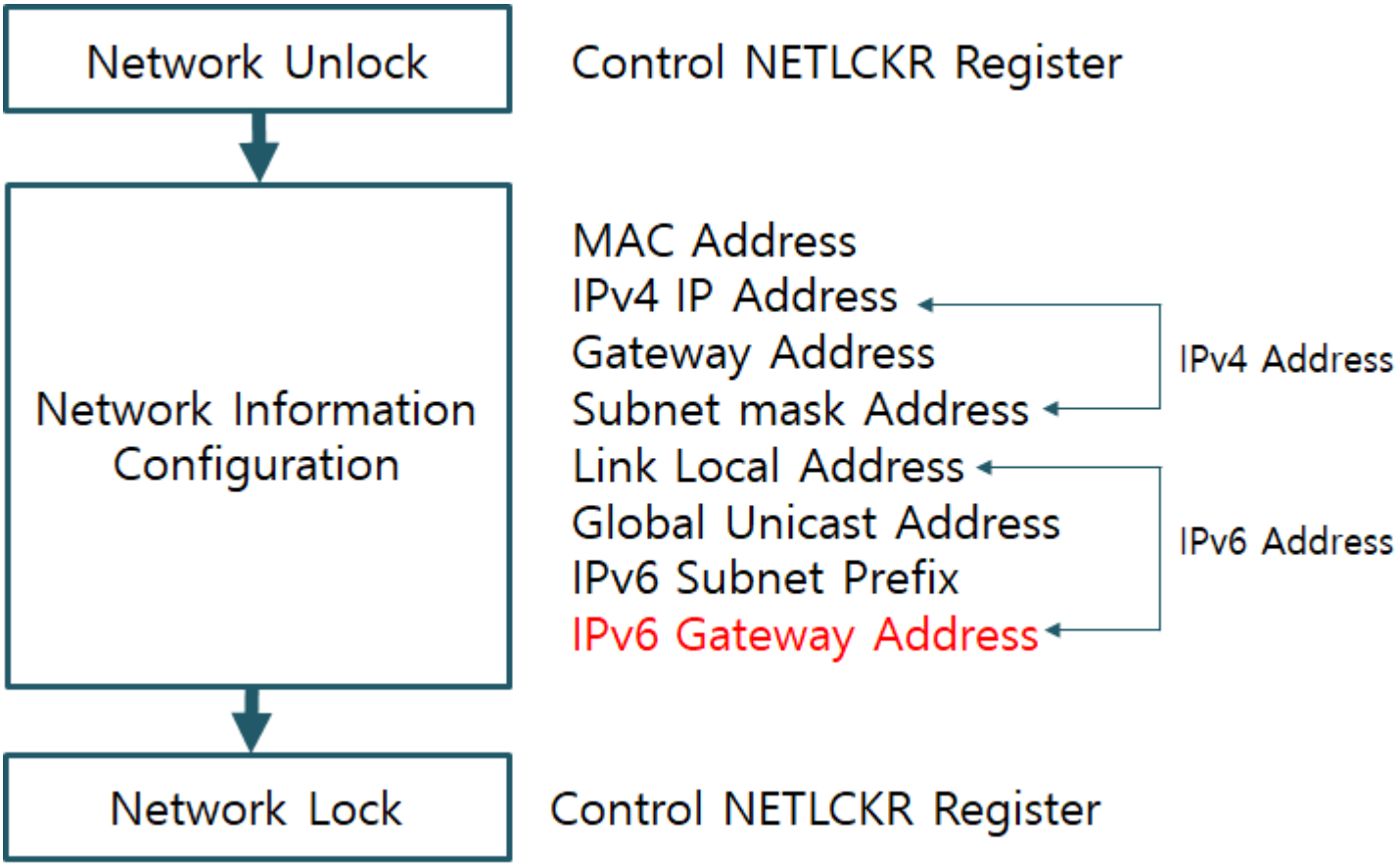
Let's look at the SOCKET life cycle at each stage.

Network Configuration

This processes to configure network information such as MAC address, IP address, and etc. W6100 basically uses Network information for communication. The following lists are the W6100's registers releated with IPv4 and IPv6 network information.

- IPv4 Network Information Registers
  - SHAR : Source MAC Address
  - SIPR : Source IPv4 Address
  - SUBR : Subnet Mask Address
  - GAR : Gateway IPv4 Address
- IPv6 Network Information Registers
  - LLR : Link-Local Address (IPv6 Address used on the same network is generated by itself)
  - GUA : Global Unicast Address (IPv6 Address for external communication assigned from Router or DHCPv6 Server)
  - SUB6R : IPv6 Subnet Prefix Mask
  - GA6R : Gateway IPv6 Address

These registers can be configured after **NETLCKR** is unlocked. This lock function can prevent the network information from being changed due to unexpected errors. After network information configuration, you can also lock these registers with **NETLCKR**.



SOCKET Mode Configuration

8 SOCKETs of **W6100** can be set to one of the following modes and can be opened. The **W6100** has the following new modes for IPv6 addition.

Sn_MR[3:0]	Protocol Mode
0000	Socket Closed
0001	TCP4
0010	UDP4
0011	IPRAW4
0111	MACRAW
1001	TCP6
1010	UDP6
1011	IPRAW6
1101	TCP Dual (TCPD)
1110	UDP Dual (UDPD)

New SOCKET Mode

Dual mode SOCKET is very useful SOCKET mode that can be used when you need to communicate by using both IPv4 and IPv6,or when you need to select one of IPv4 and IPv6 According to circumstances

Note that the **IPRAW SOCKET** mode should be used separately in **IPRAW4** and **IPRAW6** because Dual mode can not be supported in IPRAW SOCKET.

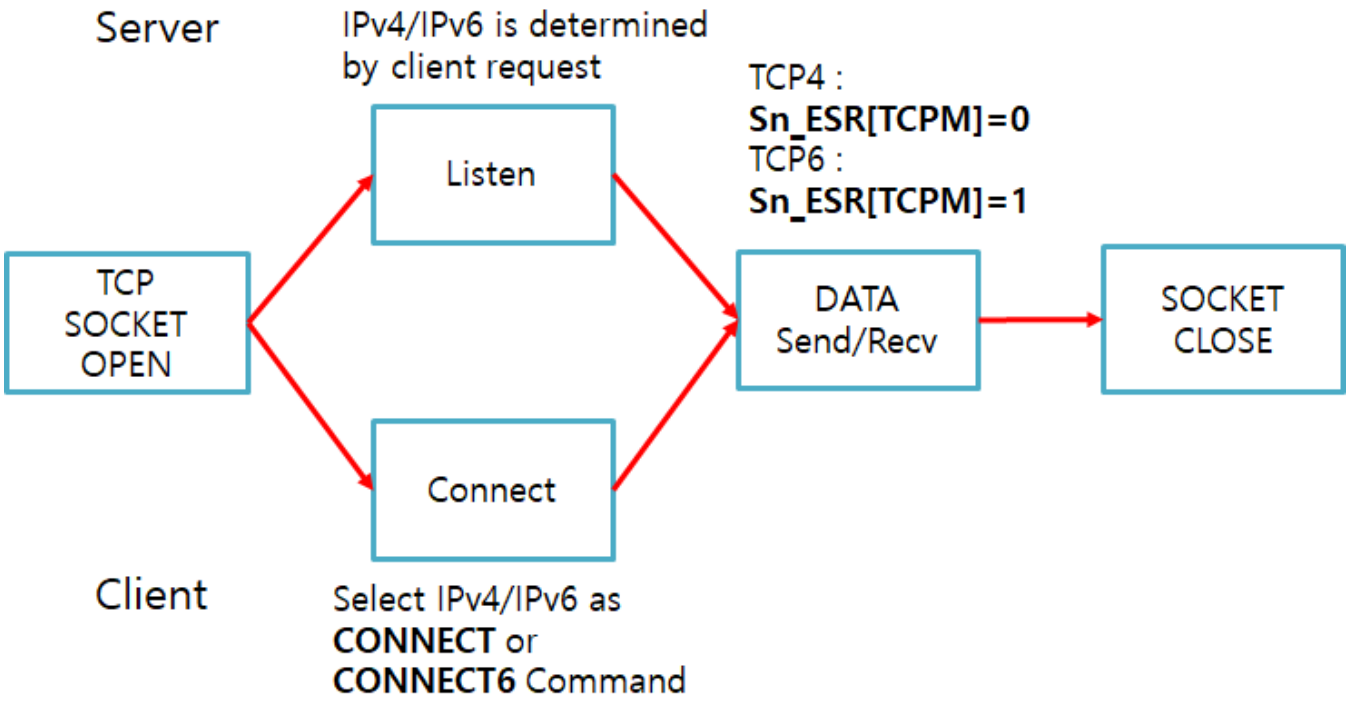
Dual Mode SOCKET is slightly different for TCP and UDP. Let's look at the different SOCKET life cycles of TCP and UDP dual mode.

How to use Dual Mode SOCKET?

- How to use W6100 in TCPD mode?

  The IP version of **TCPD** SOCKET is determined by the IP version of peer when it connects or is connected to the peer, and the determined IP version is kept until the SOCKET is closed.

  - TCP Sever : It is determined by the IP version of peer tried to connect. You can get the verion of the connected TCPD SOCKET through **Sn_ESR[TCPM]** bit.
  - TCP Client : It is determined by SOCKET connect command wwich is used accoding to IP version of peer to connect. SOCKET command(**Sn_CR**) uses **CONNECT** for IPv4 and **CONNECT6** for I



- How to use W6100 in UDPD mode?

  Unlike TCPD Mode SOCKET, **UDPD** mode SOCKET can selectively use both IPv4 and IPv6 every packet. That is, Just only using one UDPD SOCKET, You can receive from a peer which have whether IPv4 or IPv6 address, and it can be also transmitted to the peer.

You can get the IP version of the received packet from the peer through **PACKET INFO** which is included in the front of the packet.

Such like as TCPD, you can send a packet to a peer which has IPv4 or IPv6 address by using SOCKET commands (**Sn_CR**) such as **SEND**for IPv4 and **SEND6** for IPv6.

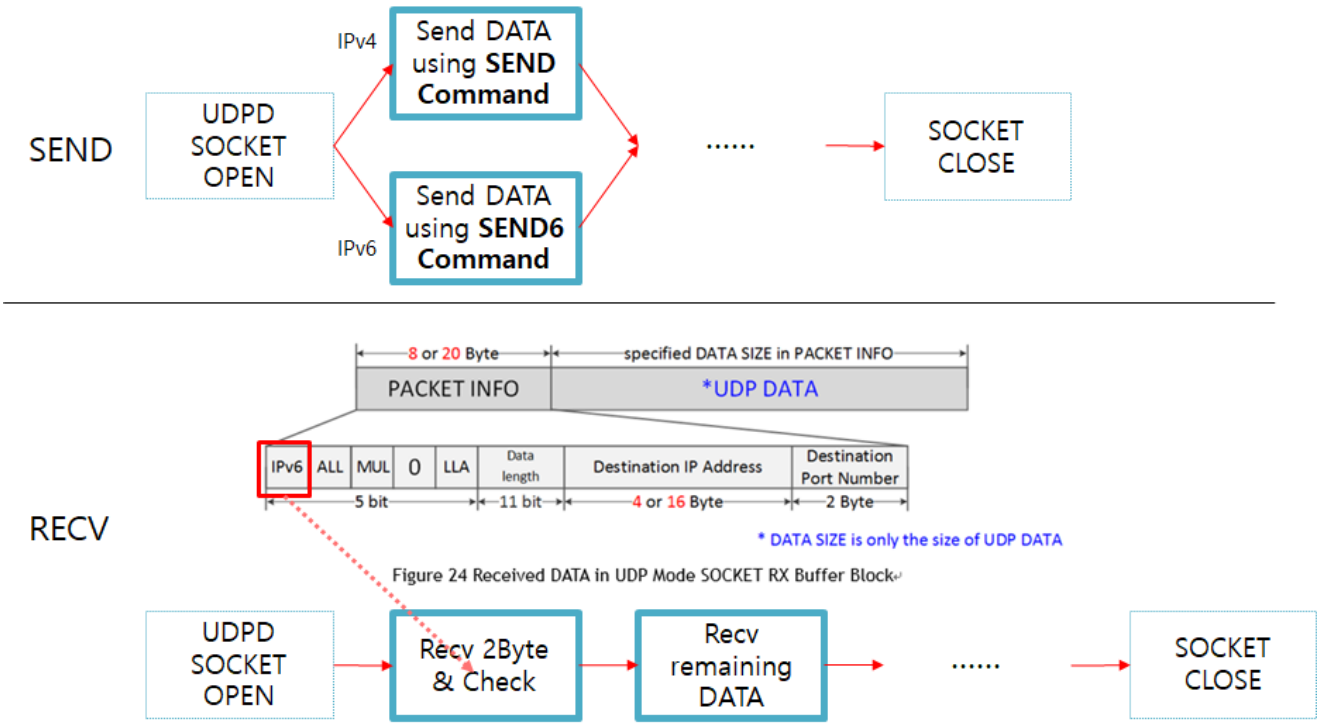
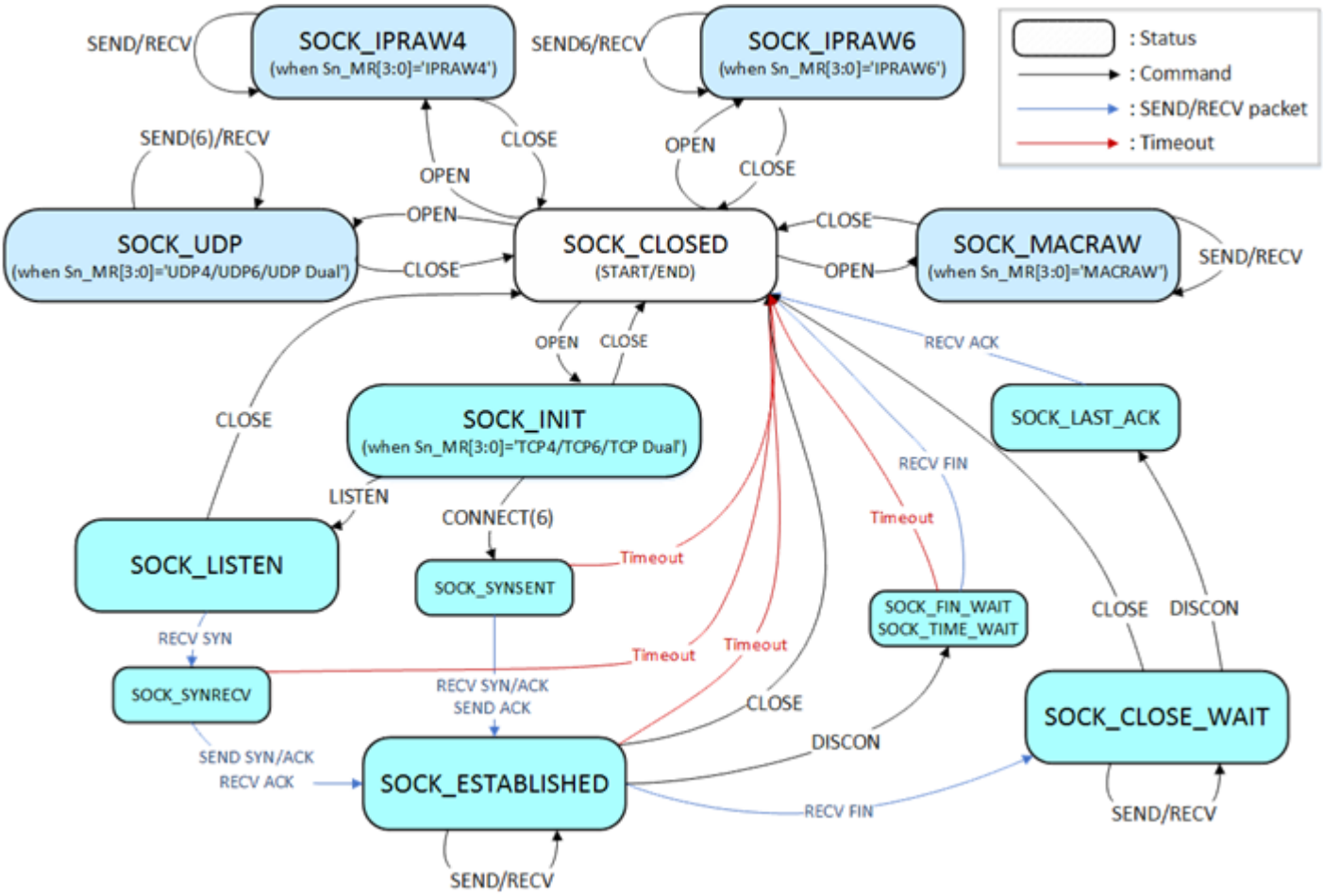


Figure 24 Received DATA in UDP Mode SOCKET RX Buffer Block

SOCKET Status (Sn_CR) transited by SOCKET Command (Sn_CR)

The following figure shows the trnasition of SOCKET status according to SOCKET commnand.

MACRAW, IPRAW4, IPRAW6, UDP mode SOCKET keeps each state after OPEN until CLOSE. Unlikely these SOCEKT mode, TCP mode SOCKET can transit from one status to another according to connection process. That is, TCP mode have different status transition according to TCP operation mode such as SERVER and CLIENT.

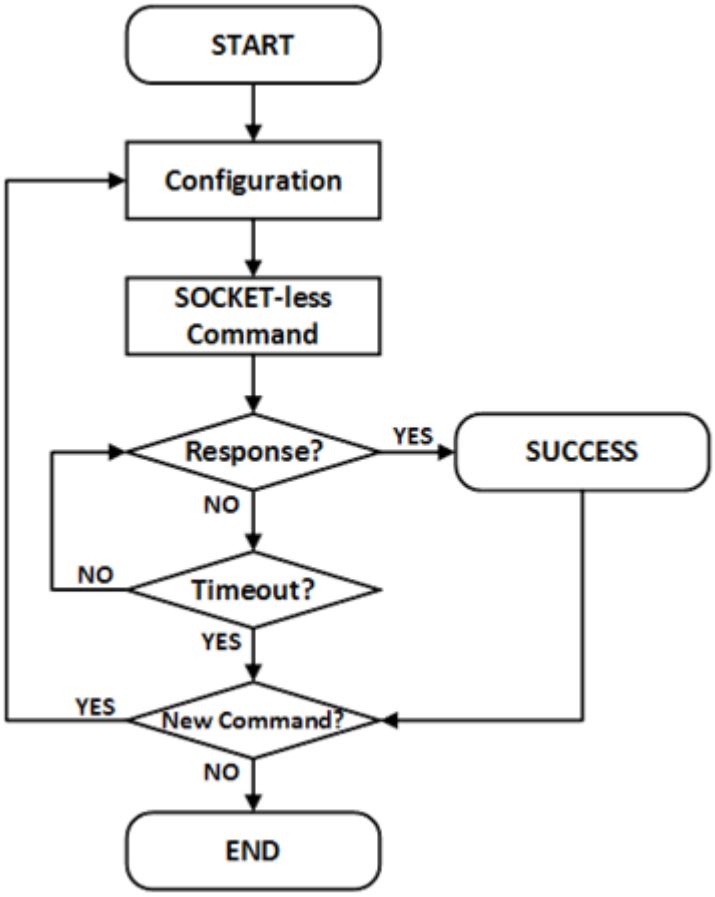


SOCKET-less Command

W6100 can support as following commands without SOCKET.

- ARP : Get the hardware address (MAC) of destination with IPv4
- PING : Request a PING to destination with IPv4
- ARP6 : Get the hardware address (MAC) of destination with IPv6
- PING6 : Request a PING to destination with IPv6
- ICMPv6 for AUTO-Configuration
    - DAD NS : Duplicated Address Detection
    - RS : Request IPv6 network information such as prefix to router
    - Unsolicited NA : Notify the updated network information to neighbor nodes.

The SOCKET-less command (**SLCR**) is processed such as following figure, and the result can be checked by the SOCKET-less Interrupt Register (**SLIR**).



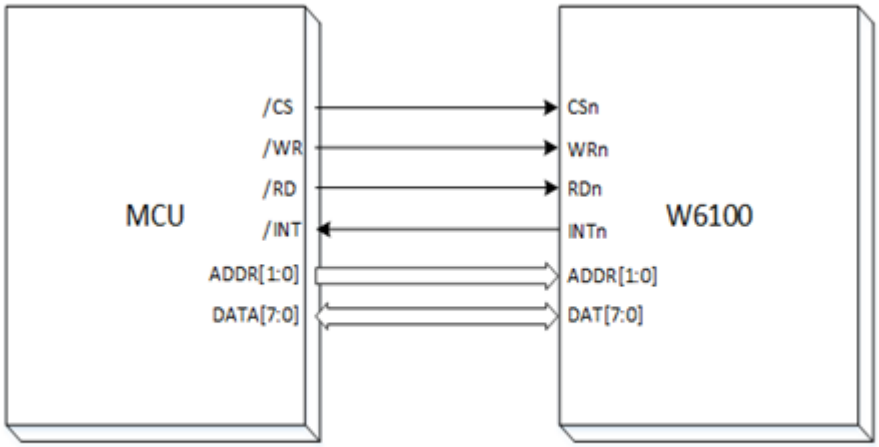
HOST Interface

W6100 can support two access modes for HOST interface.

- Parallel Bus Address Mode: Access the W6100's Register or SOCKET TX/RX memory indirectly using the 8Bit Data bus.
- Serial Bus Access Mode: Access the W6100's Register or SOCKET TX / RX Memory indirectly using SPI signal such as SCS, SCLK, MISO, and MOSI.

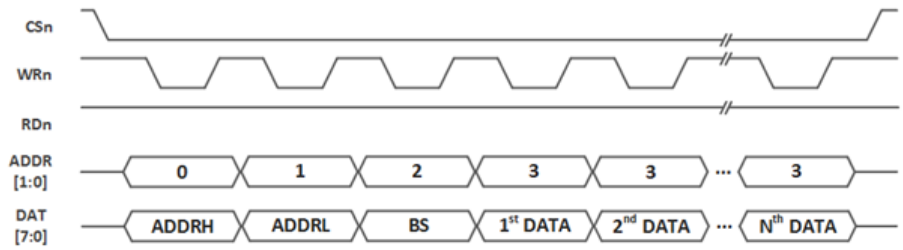
Parallel Bus Access Mode & Timing

To use parallel mode, Set PIN **MOD[3:0]** of W6100 to **"010X"** and connect the related signals such like following circuit.

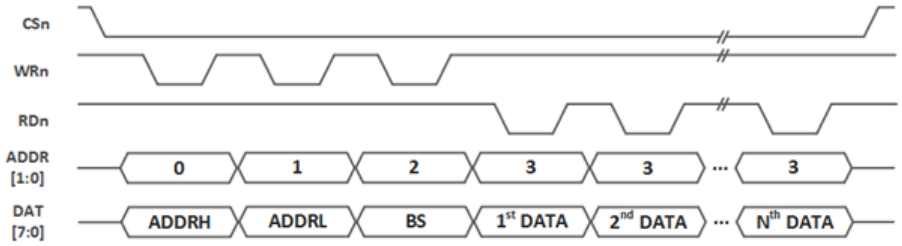


Host Interface in Parallel BUS Mode

In parallel bus mode, You can access W6100 indirectly with **IDM_AR0** (Indirect Mode Address Register 0), **IDM_AR1** (Indirect Mode Address Register 0), **IDM_BSR** (Indirect Mode Block Select Register), and **IDM_DR** (Indirect Mode Data Register) specified with **ADDR0 & ADDR1**.



Parallel Bus N-Bytes Data Write Access



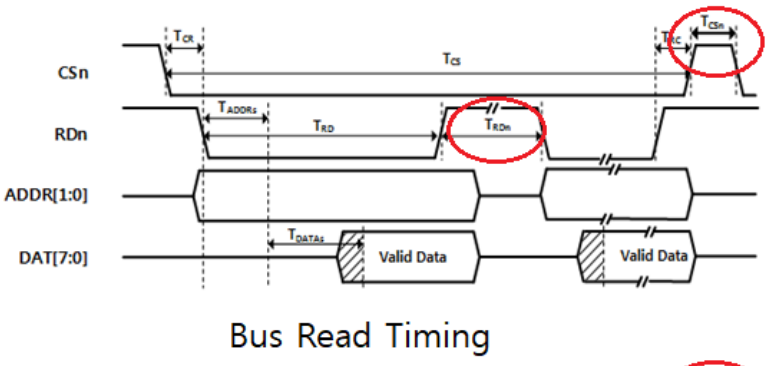
Parallel Bus Mode Continuous Read Access

[7:5]	[4:3]	[2:0]	Description
000	00	Reserved	Common Register
	01		Socket 0 Register
	10		Socket 0 TX Buffer
	11		Socket 0 RX Buffer
001	00		Reserved
	01		Socket 1 Register
	10		Socket 1 TX Buffer
	11		Socket 1 RX Buffer
010	00		Reserved
	01		Socket 2 Register
	10		Socket 2 TX Buffer
	11		Socket 2 RX Buffer
. . .			
111	00	Reserved	Reserved
	01		Socket 7 Register
	10		Socket 7 TX Buffer
	11		Socket 7 RX Buffer

As following table shown, IDM_BSR is used to select COMMON register block, 8 SOCKET register blocks and 8 SOCKET TX/RX buffer blocks.

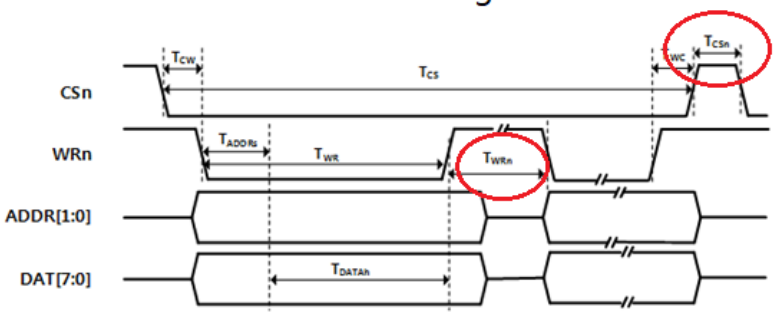
As following figure shows the HOST timing that must keep to use parallel bus mode. Specially, It is remarked that You must do the timing of **T_{CSn}**, **T_{RDn}**, and **T_{WRn}**.

(T~CSn~, T~RDn~, and **T~WRn~)**



Bus Read Timing

Symbol	Description	Min
T_{ADDRs}	Address Setup Time	SYS_CLK
T_{CR}	CSn Low to RDn Low Time	0 ns
T_{cs}	CSn Low Time	4 SYS_CLK
T_{RC}	RDn High to CSn High Time	0 ns
T_{csn}	CSn Next Assert Time	3 SYS_CLK
T_{RD}	RDn Low Time	4 SYS_CLK
T_{RDn}	RDn Next Assert Time	3 SYS_CLK
T_{DATAs}	Data Setup Time	3 SYS_CLK +5ns

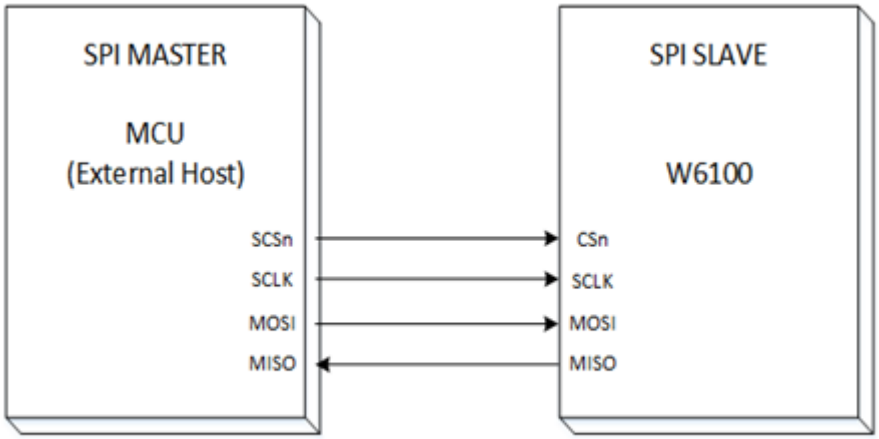


Bus Write Timing

Symbol	Description	Min
T_{ADDRs}	Address Setup Time	SYS_CLK
T_{CW}	CSn Low to WRn Low Time	0 ns
T_{cs}	CSn Low Time	4 SYS_CLK
T_{WC}	WRn High to CSn High Time	0 ns
T_{csn}	CSn Next Assert Time	3 SYS_CLK
T_{WR}	WRn Low Time	4 SYS_CLK
T_{WRn}	WRn Next Assert Time	3 SYS_CLK
T_{DATAs}	Data Setup Time	2 SYS_CLK

Serial Bus (SPI) Access Mode & Timing

To use serial bus mode, Set PIN **MOD[3:0]** of W6100 to **"000X"** and connect the related signals such like following circuit.



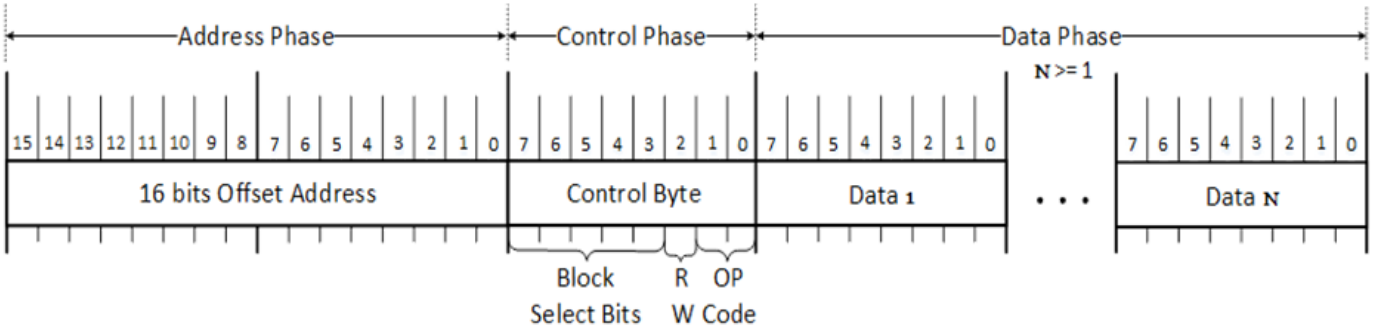
Host Interface in SPI Mode

In serial bus mode, You should transmit and receive synchronously to SCLK the SPI signals such as MOSI and MISO from MSB to LSB of Register Offset Address bits, Block Select bits (**BSB**), R/W bit (**RWB**), **OP** Code bits and Read/Write 8bit Data.

In the following table, Block Select Bits (**BSB**) perform the same function as Parallel BUS Mode, but Read/Write should be distinguished by **RW** bit and data length should be specified by **OP** Code. Data Length has two types: Variable Data Length Mode (**VDM**) and Variable Data Length Mode (**FDM**).

- VDM: Data can be read or written continuously while the CSn signal is low.

- FDM: Be sure to keep the CSn signal low at all times, and set the data length to be read or written through the OP code.

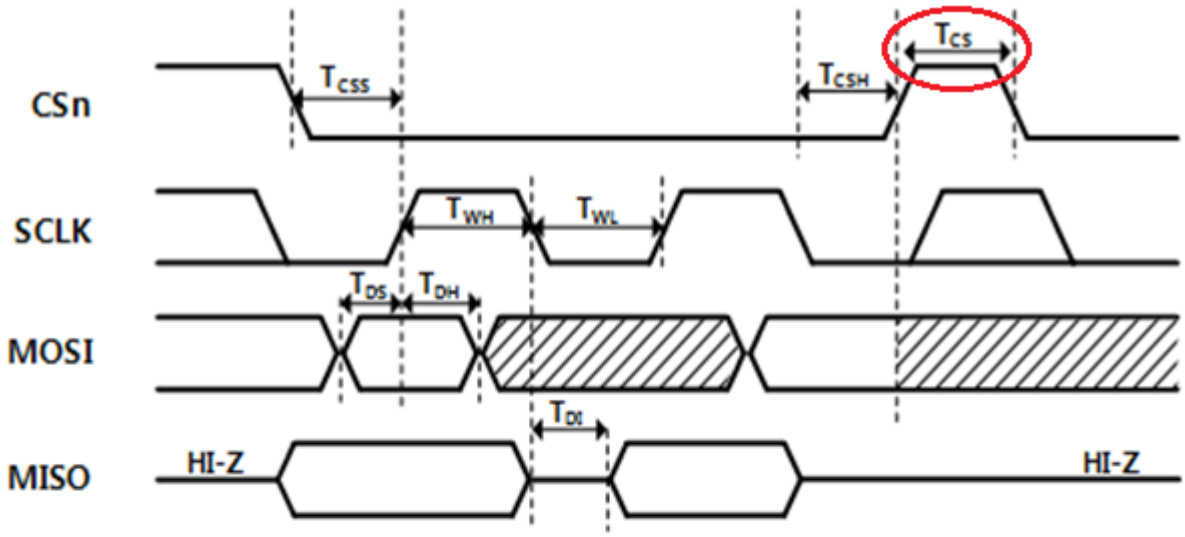


BSB[4:2]	BSB[1:0]	Block
000	00	Common Register
	01	Socket 0 Register
	10	Socket 0 TX Buffer
	11	Socket 0 RX Buffer
001	00	Reserved
	01	Socket 1 Register
	10	Socket 1 TX Buffer
	11	Socket 1 RX Buffer
. . .		
111	00	Reserved
	01	Socket 7 Register
	10	Socket 7 TX Buffer
	11	Socket 7 RX Buffer

RWB	Mode
0	Read
1	Write

OM[1:0]	Mode
00	VDM, N bytes Data Phase (1 ≤ N)
01	FDM, 1 byte Data Phase
10	FDM, 2 bytes Data Phase
11	FDM, 4 bytes Data Phase

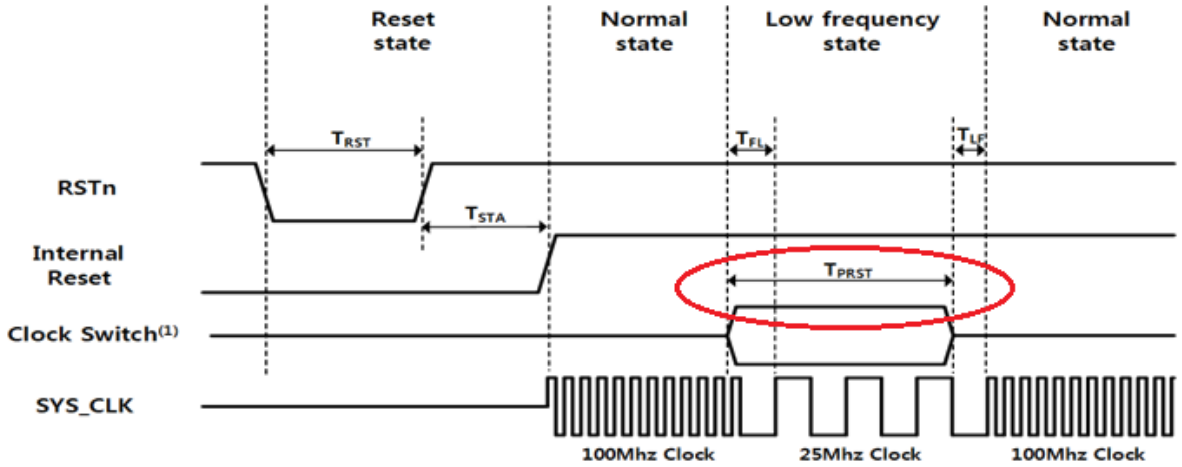
The following figure shows the HOST timing for the Serial BUS Mode signal. Note that if you use VDM Mode, you must obey T_{CSn}.



Symbol	Description	Min	Max	Units
F_{SCLK}	SCLK Clock Frequency		70	MHz
T_{CSS}	CSn Setup Time	3 SYS_CLK		ns
T_{CSH}	CSn Hold Ti me	2 SYS_CLK		ns
T_{CS}	CSn High Ti me	2 SYS_CLK		ns
T_{WH}	SCLK High t ime	6		ns
T_{WL}	SCLK Low T ime	6		ns
T_{DS}	Data Setup Time	3		ns
T_{DH}	Data In Hol d Time	3		ns
T_{DI}	Data Invalid Time	7		ns

Reset & System Clock Switching

The following figure shows the timing of W6100 H/W Reset Timing and System Clock Switching.



Symbol	Description	Min	Typ	Max
T_{RST}	Reset Time	350 ns	580 ns	1.0 us
T_{STA}	Stable Time	-		60.3 ms
T_{FL}	Fast to Low Time by SYCR1[CLKSEL]	100 ns		-
	Fast to Low Time by PHYCR1[RST] or PHYCR1[PWDN]	300 ns		
T_{PRST}	PHY Auto Reset Time	0.6 ms		-
	PHY Power Down Time	200 us		
	Clock Switch Time	200 ns		
T_{LF}	Low to Fast Time by SYCR1[CLKSEL]	100 ns		-
	Low to Fast Time by PHYCR1[RST] or PHYCR1[PWDN]	100 ns		

- Reset Timing (T~RST~)

  Controlled by RSTn PIN, W6100 Reset takes from minimum 350ns to 1.0us depending on temperature and humidity. Therefore, it is advisable to keep the reset signal stable for a period of Max value of 1.0us or more and wait for 60.3ms until the internal clock is stabilize W6100 after reset, then access W6100.

- System Clock Switching

  The W6100 allows the System Clock to change from 100MHz to 25MHz for Power Save. There are 3 cases that the system clock can be changed. In this case you should keep (**T~PRST~**) timing in the above table.

  - PHY Auto Reset Time: The required time during PHY reset set by **PHYCR1[RST]** register bit. System clock is automatically switched to 25MHz during PHY reset.
  - PHY Power Down Time: The required time during PHY power-down mode set by **PHYCR1[PWDN]** register bit. In P PHY-power mode, System clock is switched to 25MHz.
  - Clock Switch: The required time during system clock switches from 100MHz to 25MHz or from 25MHz to 100MHz. by setting **SYCR[CLKSEL]** register bit manually.

ICMPv6 Offload

The following table shows that W6100 is able to offload ICMPv6 with hardwired logics. Unsupported ICMPv6 packets can be handled by software through IPRAW6 Mode SOCKET.

Message	Type	Type value	Send	Recv
Error	Destination Unreachable	1	O	O
Informational	Echo Request	128	O	O
	Echo Reply	129	O	O
Neighbor Discovery	RS (Router Solicitation)	133	O	X
	RA (Router Advertisement)	134	X	Partially
	NS (Neighbor Solicitation)	135	O	O
	NA (Neighbor Advertisement)	136	O	O
	Redirect	137	X	X
Multicast Listener Discovery	MLQ (Multicast Listener Query)	130	X	O
	MLR (Multicast Listener Report)	131	O	X
	MLD (Multicast Listener Done)	132	O	X
Path MTU Discovery	Don't Fragment	3	X	X
	Packet Too big	2	X	X
Others			X	X

Here, W6100 can receive a RA message only when certain conditions are satisfied. That is, if the first option of the received RA message is the source link-layer address (0x01) and the second option is the Prefix information option (0x03), the following registers have correct value. Otherwise, You should receive the RA message using the IPRAW6 Mode SOCKET and process the following information.

- PLR (Prefix Length Register)
- PFR (Prefix Flag Register)
- VLTR (RA Valid Life Time Register)
- PLTR (RA Preferred Life Time Register)
- PAR (Prefix Address Register)

What is different from other WIZnet TCP/IP Stack Controller

The following table show different or enhanced functions between W6100 and other WIZnet chips for users who have an experience used other chips.

		W5500	W5100S	W6100
Host I/F	SPI (18MHz)	15Mbps	12Mbps	15 Mbps
	BUS	-	Max 25 Mbps	Max 25 Mbps
TX/RX Memory(KB)		16/16	8/8	16/16
Socket #		8	4	8
Package		48LQFP	48LQFP/QFN(Pin to Pin)	
Protocol		TCP, UDP, ICMP, IGMP, IPv4, ARP, PPPoE		
		-		IPv6, ICMPv6
PHY	10 BaseT	O	O	O
	100 Base TX	O	O	O
	10 Base Te	X	X	O
Internal Clock Rate		150MHz	100MHz	100MHz
Packet Block		PING	RST, Port Unreachable, PING	
				All IPv4, All IPv6
PSH Flag		Auto	Auto or All	
Socket less command		-	ARP, PING	ARP, PING, DAD, RS, UNA
Port numbers reused connection		X		O
Configuration Lock		X	O	O

Conclusion

In Part I, We reviewed t the brief features of IPv6. And So far, We have reviewed how IPv6 is applied and implemented on W6100.

I did not explain everything about the W6100 in Part II. For first user of W6100, I briefly looked at a few basic features. For more detail information, you can refer to W6100 Datasheet.

I hope this article will help W6100 users. Enjoy your W6100!!!