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A low-glitch binary-weighted DAC with delay compensation scheme

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Abstract This paper presents a high-speed, low-glitch, and low-power design for a 10-bit binary-weighted current-steering digital-to-analog converter (DAC). Instead of using large input buffers to drive a lot of current switches and re-timing latches, the proposed design uses variable-delay buffers with a compact layout to compensate for the delay difference among different bits, and to reduce glitch energy from 132 to 1.36 pV s during major code transitions. The measured spurious free dynamic range (SFDR) has been improved over 10 dB, as compared to DACs without variable-delay buffers. At 250 MS/s update rate, the proposed DAC achieves 56 dB SFDR for 0.67 MHz output frequency and 49 dB SFDR for 94 MHz output frequency with 50 Ω termination. For static performance, the measured integral nonlinearity (INL) and differential nonlinearity (DNL) is less than 1.6 and 1.8 LSB, respectively. The proposed DAC can be used in various applications in industry, including digital video, digital TV, wireless communication system, etc. This chip was implemented in TSMC 1P6M 0.18 μm CMOS technology and dissipates 19 mW from a single 1.8 V power supply.

Keywords Digital-to-analog converter (DAC) · Glitch reduction · Binary-weighted · Current-steering DAC

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1 Introduction

Nowadays, for high-speed digital-to-analog converter (DAC), there are increasing demands in many wireless transmitter, video system and SOC applications. The current-steering DAC is a good candidate for high-speed DAC applications because it can drive low impedance directly with good linearity, and without needing high-speed buffers. Current-steering DACs are based on an array of current sources that are switched to the output which is connected with 50 Ω resistor, and the differential architecture has often been used because even-orders errors could be eliminated. There are three different architectures used to implement the switched current source arrays, they are binary, unary, and segmented. The segmented DAC architectures are widely used in current-steering DACs today [1, 2]. However, unary and segmented DAC architectures need binary-to-thermometer decoders and delay cells, which increase circuit complexity and digital power consumption, so they come at cost (area, power, complexity) for high-speed and high-resolution DACs. Therefore, in this paper we propose the binary-weighted architecture compromising between cost and performance.

The binary-weighted architecture is the simplest design with low digital power and small area, and it also achieves compatible static and dynamic performance compared with other structures [3, 4]. The main drawbacks of the binary-weighted DAC are large differential nonlinearity (DNL) errors and potentially non-monotonic behavior due to device mismatches and timing errors. When the input code was changed, the output will have code dependent glitches, and the glitches often degrade spurious free dynamic range (SFDR) performance. When the input code changes from 2^{n-1} to 2^n (major code transition), for example, from 011….1 to 100….0, the output would have the largest

glitch during the code transition, where the glitch also increases the settling time of the converter. The output glitch comes from three major sources. The first is the clock feed-through and channel charge injection at the current switch. This effect can be improved by shrinking the size of the current switch or series of a buffer between output and switch. The second is rise/fall time asymmetry in the current source [5]. However, if the DAC's output is differential, different rise and fall transitions have even-order distortion only [3], so this effect could be ignored. Finally, the most critical root cause of glitches is the data skew among different current switches corresponding to different bits. As the current switches are also binary-weighted, the capacitive loads of the switch drivers vary, resulting in timing mismatch between bits and high glitches at the output. The timing skew of different bits becomes significant when the DAC operates at high sampling rates because the delay difference degrades SFDR performance and linearity. In this paper, we propose a new binary-weighted DAC with variable-delay buffers to reduce output glitch due to timing mismatches of current switches. The DAC has high-speed and low-glitch characteristics with small silicon area and power consumption for digital circuits.

The rest of this paper is organized as follows. Section 2 describes the architecture of the binary-weighted DAC. In Sect. 3, circuit implementation and analysis of the proposed DAC are presented. Section 4 shows experimental results. The final section addresses the conclusion of this work.

2 Binary-weighted DAC

The most straightforward implementation of current-steering DACs is the binary-weighted DAC. (D_0, D_1,….., D_{N-1}) is a digital input word, where D_0 is the least significant bit (LSB) and D_{N-1} is the most significant bit (MSB), and the output current of the N-bit binary-weighted current-steering DAC can be expressed as

$$\begin{aligned} I_{out} &= (2^0 D_0 + 2^1 D_1 + \cdots + 2^{N-1} D_{N-1}) I_{LSB} \\ &= 2^0 I_0 + 2^1 I_1 + \cdots + 2^{N-1} I_{N-1} \end{aligned} \quad (1)$$

where I_{LSB} represents a unit current or reference current, and I_0, I_1, …. I_{N-1} form the basis of the DAC's output current. The linearity and static performance of the DAC can be estimated early by setting input codes in the order of 2^0, 2^1, …, 2^{N-1} values. By measurement for I_0, I_1, …, I_{N-1} in sequence, the output current could be calculated directly using Eq. (1), and the INL/DNL could be estimated effectively at first without 2^N times of measurement. The binary-weighted architectures are efficient in nature for both design and test.

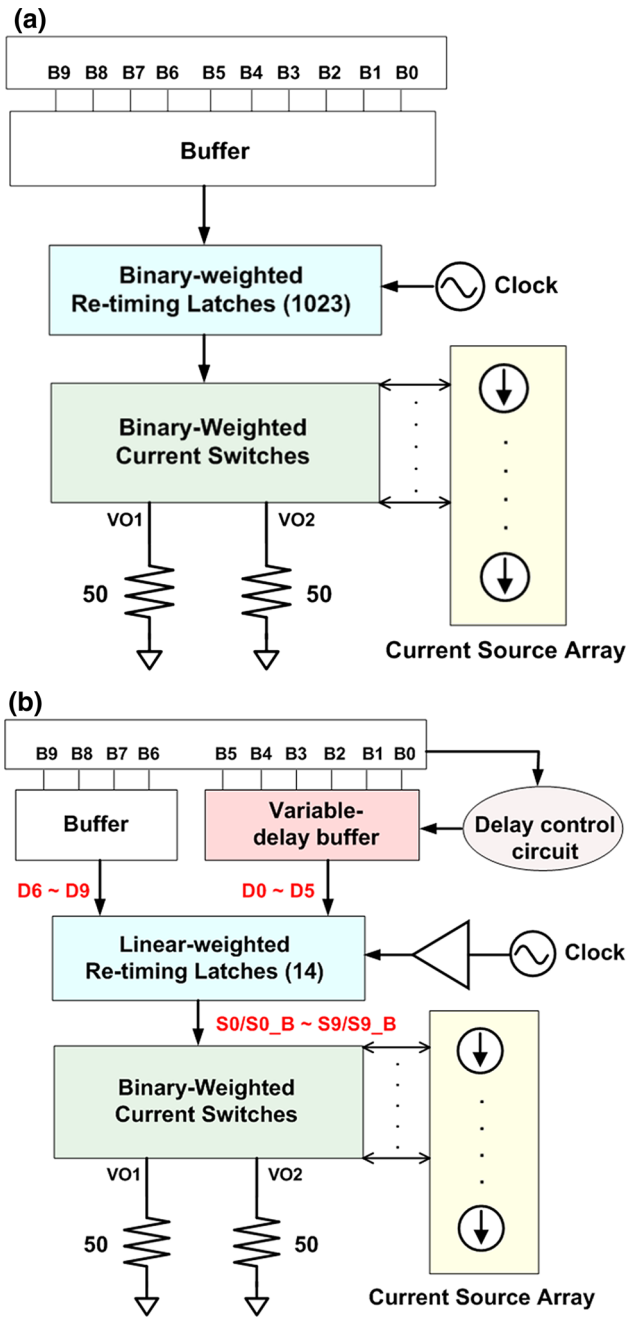


Fig. 1 **a** Architecture of the typical binary-weighted DAC. **b** Architecture of the proposed binary-weighted DAC

The architectures of binary-weighted DACs are illustrated in Fig. 1. The typical topology of a binary-weighted DAC is depicted in Fig. 1(a). As the sizes of the current sources, current switches, and the re-timing latches are all binary-weighted, although the input buffers may not have to be binary-scaled, the sizes of input buffers should be large for driving binary-weighted devices. Thus, the data path delays from different inputs to output are not exactly the same due to the RC parasitic effects of routing wires

Table 1 Number of latches used for different bits

Bit	# of latches
0	1
1	1
2	1
3	1
4	1
5	1
6	1
7	1
8	2
9	4

and process variations of the whole chip. The timing skew between different bits increases as the resolution of DAC increases, and it becomes more serious when the sampling rate is higher. The timing mismatch will produce glitches at the outputs. Moreover, it will degrade the settling time, monotonicity, and overall SFDR performance [6, 7].

Figure 1(b) depicts the block diagram of the proposed 10-bit binary-weighted DAC, where B0–B9 are the digital input signals and D0–D9 are the outputs of input buffers. D0–D9 go through re-timing latches to drive binary-weighted switches, and S0/S0_B–S9/S9_B are the inputs of current switches. With the trade-off concern between operation speed and area, we only use a few latches instead of a set of complete binary-weighted latches, and the number of latches we designed is listed in Table 1. We do not add any compensation circuits at the output of latches. In our design, only one latch is used for Bit 0–Bit 7 individually, two latches are used for Bit 8, and four latches are used for MSB due to the increase of the loading. The total number of latches is 14, which is much less than 1,023, so the area reduction of digital parts is huge, even including variable resistors. Without enlarging driver sizes to drive large loads directly, variable resistors are added between input buffers and re-timing latches to compensate for the loading difference of switch drivers. The number of bits using variable-delay buffers in this chip is six, and the details are discussed in the next section. All transistors we use in this chip are 1.8 V device in standard CMOS 0.18 μm technology.

3 Circuit implementation of proposed DAC

3.1 Variable-delay buffers

As shown in Fig. 2, the variable-delay buffers consist of variable resistors and buffers, where the buffer sizes are fixed for different bits. Because the delay due to an RC network is proportional to R × C, the resistance of variable

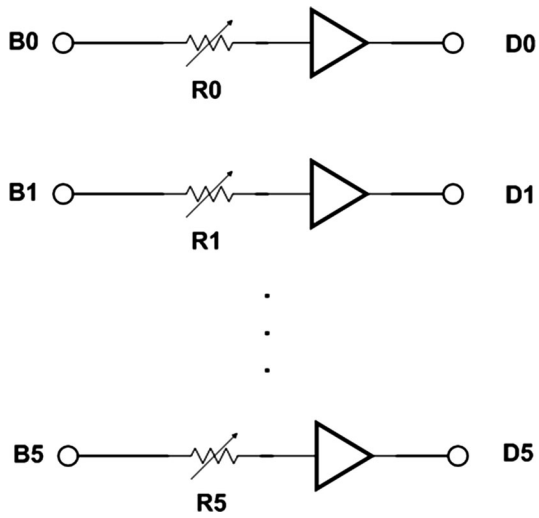


Fig. 2 Schematic of variable-delay buffers

resistors is designed to be binary weighted in the decreasing order from LSB to MSB, where $R_i = R0/2^i$ and i = 0–M–1, M is the number of bits using variable-delay buffers. As MSB's switches have larger sizes and capacitance, variable-delay buffers make the LSB's switches turn on later than MSB's, so the timing skew among different bits will be greatly reduced.

In the chip implementation, according to the parasitic effects of connection wires and transistors, M equals to 6 by glitch simulation at the major code transition. With layout consideration, the resistances of R0–R5 are designed as 4R, 2R, R, R/2, R/4, and R/8, respectively. R is implemented by CMOS transmission gate (TG), so the resistance can be further fine-tuned by control voltage. As shown in Fig. 3(a), the variable resistor is realized by a TG, where PMOS is always ON, and the gate of NMOS is connected to a control voltage VCTR. The variation of this variable resistance is less than that of the traditional CMOS TG with both of the gates of PMOS and NMOS connected to the same control voltage VCTR. Figure 3(b) shows the on-resistance of the variable resistor. As VCTR changes from 0.7 to 1.8 V, the resistance can be varied from 2 to 20 kΩ. If the variable resistance is too large, it will degrade the operation speed of the DAC. On the other hand, if the variable resistance is too small, then the RC delay could not compensate for large capacitance loading. According to Hspice simulation under major code transitions, we found that VCTR ∼1.2 V is the optimum value for 250 MS/s update rate. The waveforms of delayed signals D0–D5 during the major code transition are shown in Fig. 4, where the delay time between D0 and D5 is about 367 ps. As a result, the output glitches due to timing mismatches can be improved significantly. Because the delay is smaller than T/10, where T is 4 ns for 250 MHz clock rate, variable-

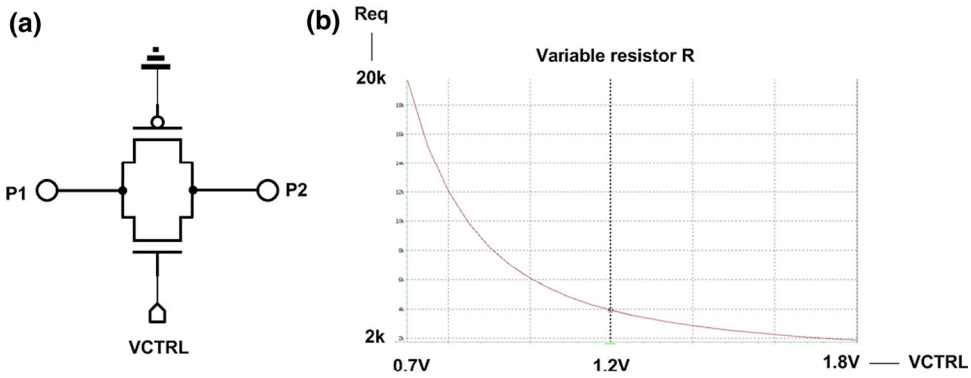


Fig. 3 **a** Variable resistor implementation. **b** Tuning range of variable resistor

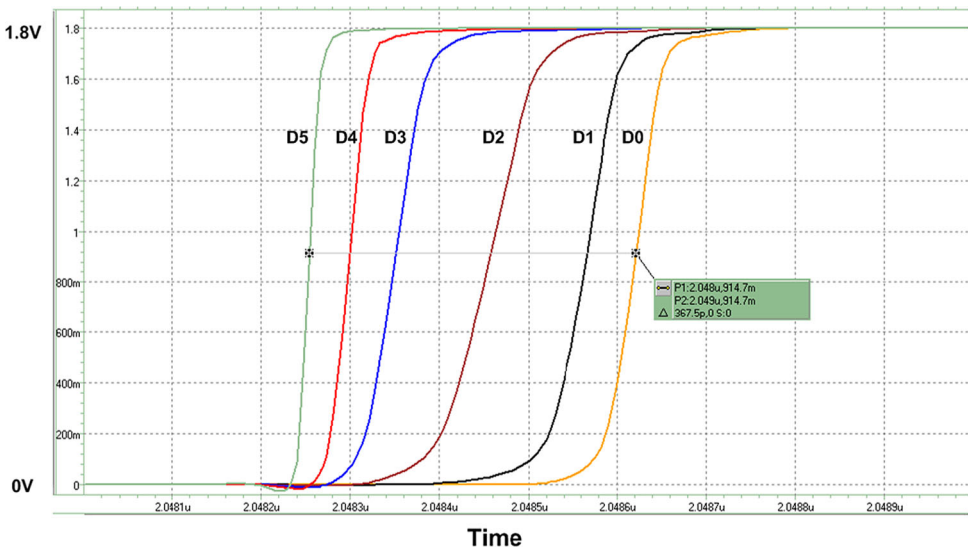


Fig. 4 Time-domain waveforms of signals *D0–D5* during the major code transition

delay buffers would not degrade the operation speed, but only increase little latency.

3.2 Delay control

The output glitch is considered to be data dependent; that is, larger glitches occur when many data bits change at the same time. Usually, the maximum specified glitch energy is observed during the major code transition (switching from 011…11 to 100…00). There are three kinds of output waveforms during the major code transition, as shown in Fig. 5, (a): without compensation, (b): with compensation, (c): over compensation. If the variable-delay buffer technique is applied to every input code transition, then the output will have over-compensation results at some input code transitions, as shown in Fig. 5(c). Because the number of changing bits is usually not so many, the delayed signals will make timing errors bigger, resulting in large glitch at the output. On the other hand, our object is to keep the monotonic behavior of the DAC and to reduce glitch energy within specific transition period when input codes change, so it is not necessary to do 100 % compensation. Therefore, we design a delay control circuit to decide whether to turn the variable-delay buffer on or off. The mechanism of the variable-delay buffers is turned on under the following conditions of input code transitions:

0101111111 → 0110000000

0111111111 → 1000000000

1001111111 → 1010000000

1011111111 → 1100000000

1101111111 → 1110000000

The delay control circuit consists of logic gates and switches to turn on/off variable-delay buffer mechanism. In addition, adding resistors changes the slew rate of input signals, so output glitches can be reduced by slowing slew rates appropriately. As variable resistors in the proposed approach are implemented using CMOS TG, the extra area required is small compared to the other deglitching approaches. Adding variable resistors will not increase DC power, and the total extra digital power for variable-delay buffers is only 50 μW. The technique is effective and has low circuit complexity, making it suitable for the small

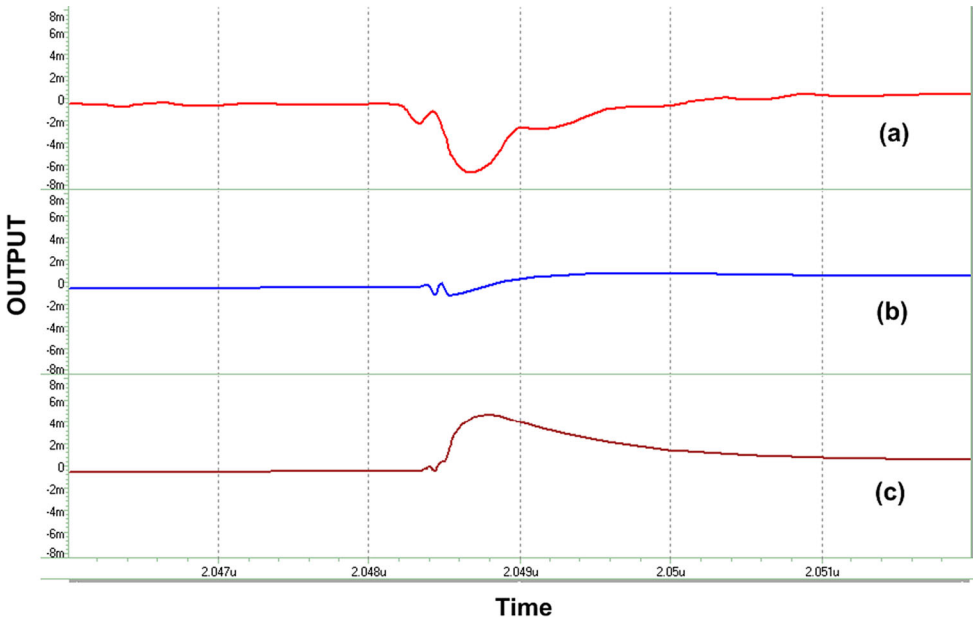


Fig. 5 Output waveforms during the major code transition. (*a*) Without compensation. (*b*) With compensation. (*c*) Over compensation

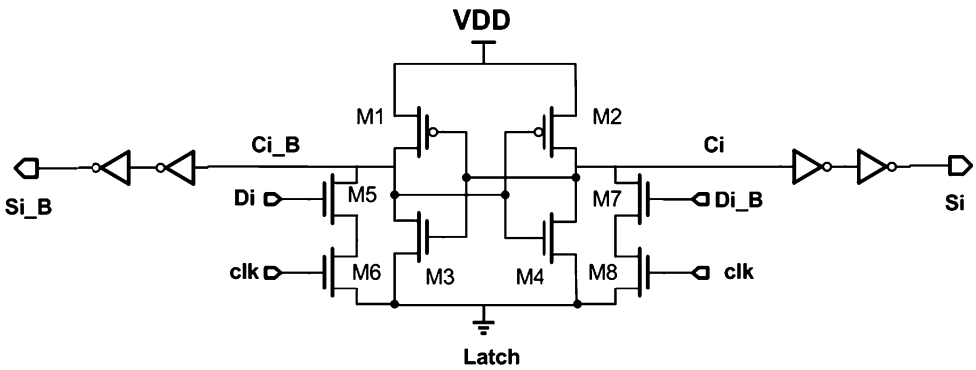


Fig. 6 Circuit diagram of the re-timing latch

area, high speed, and low power requirements of many SOC applications.

3.3 Re-timing latches

Figure 6 shows the schematic of the re-timing latch used in the proposed DAC. Before digital signals control the current switches, it is a must to do synchronization. In order to sample the input data word at the correct timing, a clock delay circuit is inserted in the clock path, that is, the external clock needs to be delayed for a period time before it enters the re-timing latch. The clock delay circuit is a two-bit mux-delay circuit, which can be utilized to compensate for the delay from digital input to latch input. The programmable delay time of the mux-delay circuit can be adjusted from 160 to 340 ps, and it was used to reduce the timing mismatch between data and clock lanes. The re-timing latch is a clock-gated SR positive latch. When clk goes high, the inputs Di and Di_B will change the logic states of outputs Si and Si_B after a propagation delay. While clk is low, Si and Si_B keep the original logic states. Transistors M1–M4 form cross-coupled pairs which regenerate both logic high and logic low. The dynamic latch is designed for high speed operation, so the sizes of transistors M1–M8 are designed small. To drive current switches, there are two inverters inserted between Ci and Si, Ci_B and Si_B, respectively. The intrinsic delay for Si and Si_B is used to lower the cross-point voltage of the switching control signals. Thus, the current switches are never turned off at the same time. Besides, lower VDD also helps to reduce output glitches by minimizing the clock feed-through effect. The re-timing latches cannot synchronize the current switches for different bits because the output capacitance of latches are binary scaled, so both of delay and rise/fall time are different. The LSB switch will be turned on earlier than the MSB switch due to smaller loading. Therefore, the variable-delay buffers are added between input buffers and re-timing latches to compensate for the timing skew, so the input signal of LSB's latch has longer delay than that of the MSB's in the

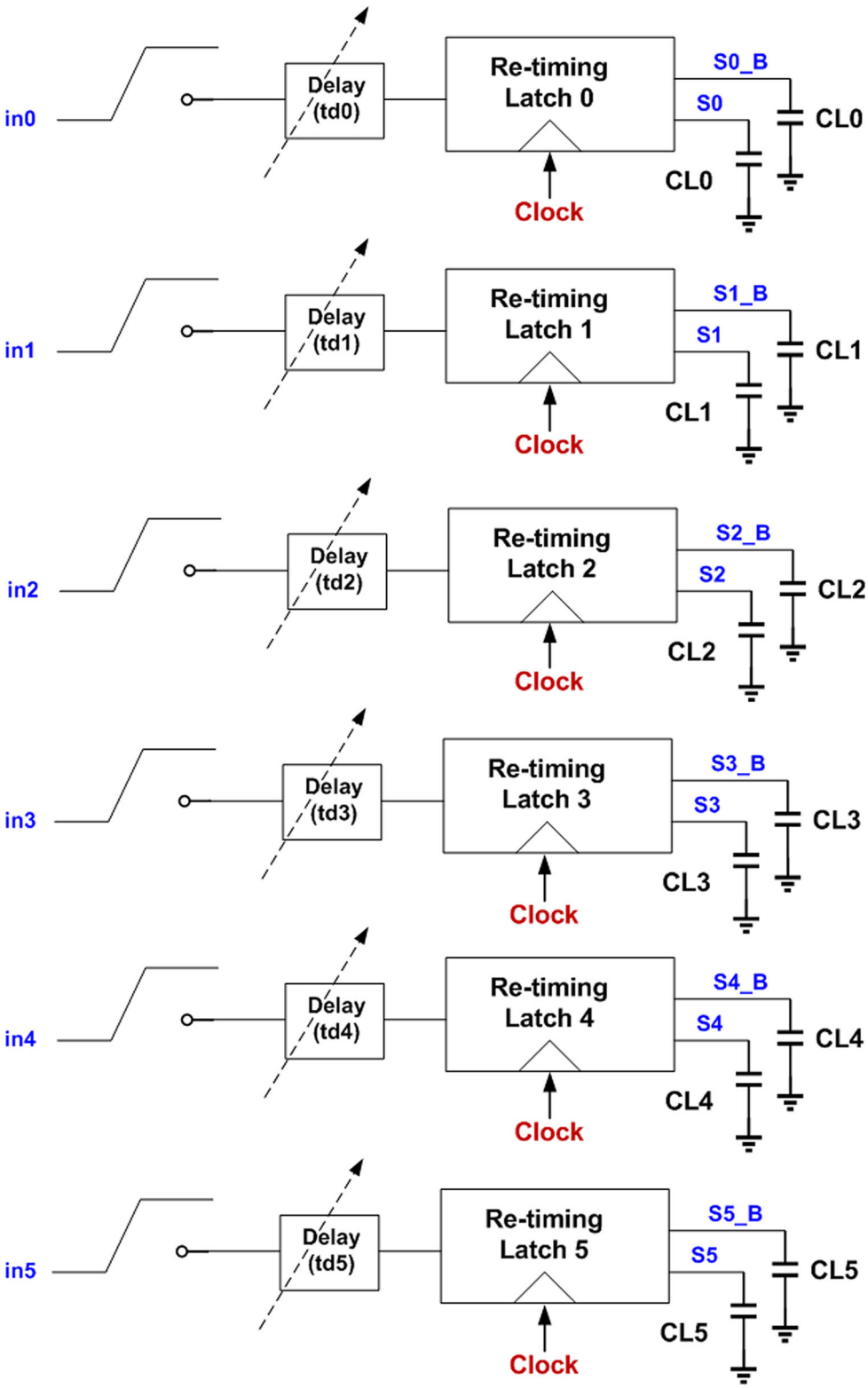


Fig. 7 Simulation configuration of bit 0–bit 5 re-timing latches

variable-delay buffer circuit, and the timing skew can be reduced.

To demonstrate the compensation effect of the variable-delay buffers, the re-timing latches' transient simulation of bit 0–bit 5 for the conventional latching versus variable-delay latching are depicted in Fig. 7. For the conventional latching, tdi = 0, where i = 0–5. S0 will be turned on before S1, S1 will be turned on before S2, and so on. It

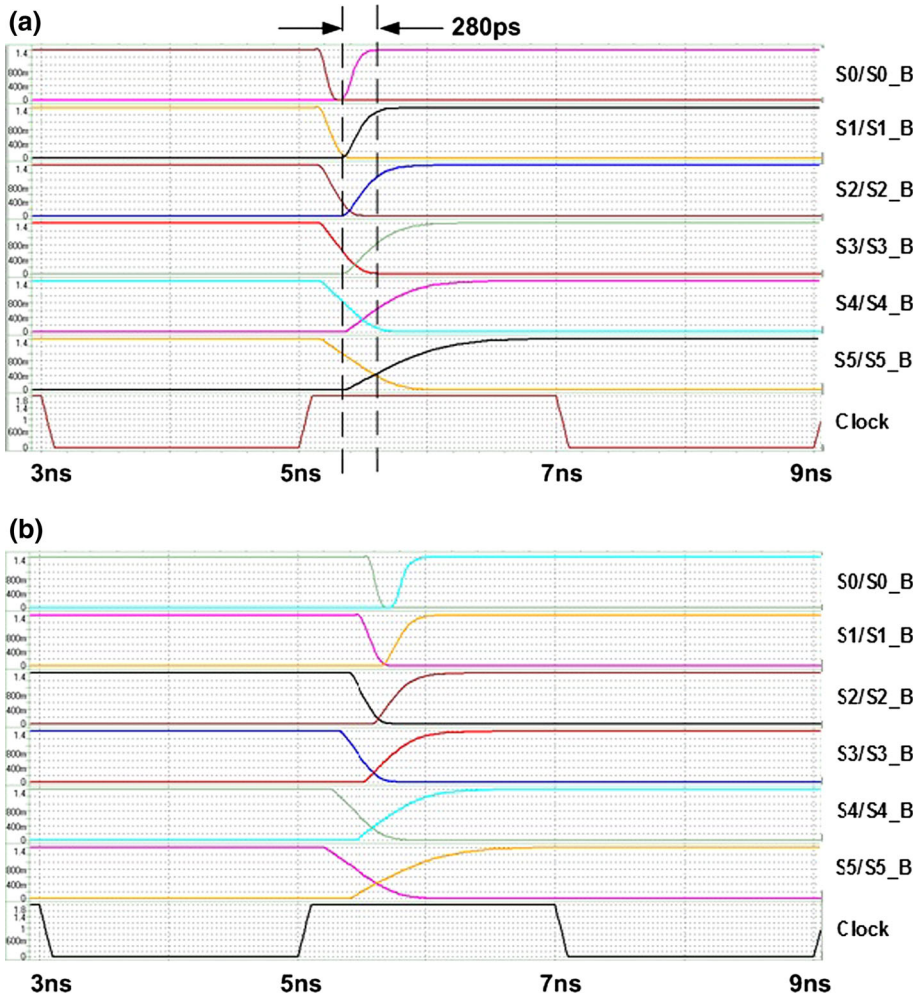


Fig. 8 Simulation waveforms of S0/S0_B–S5/S5_B. **a** Conventional latching. **b** Variable-delay latching

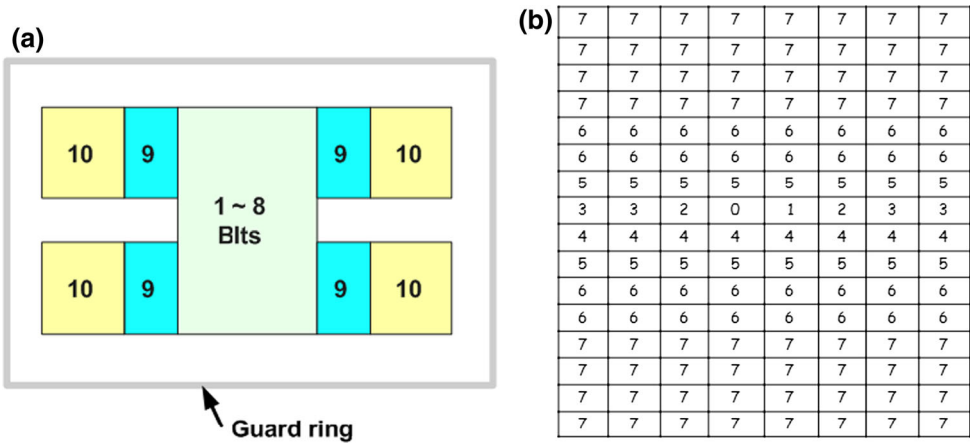


Fig. 9 Floor plan of the CSA

turns out that the cross-point delay between S0/S0_B and S5/S5_B is about 280 ps, as shown in Fig. 8(a). The timing skew is due to different loading of latches, which causes output glitches of the DAC. Figure 8(b) shows the simulation waveforms corresponding to variable-delay latching, where td0–td5 are matched with the RC delay of variable-delay buffers for bit 0–bit 5. CL0–CL5 are the input capacitances of the current switches of the binary-weighted DAC. As a result, the timing skew is greatly reduced. S0 is actually further designed to turn on a little bit later than S1–S5 to cancel out the effect of different slew rates, so the output glitch can be further reduced.

3.4 Current source design

The transistor design of the current source is related to two aspects, static and dynamic performance [8]. The static performance of the DAC is linearity and accuracy, which are characterized by DNL and INL. The static performance is related to the matching of the current sources array (CSA), which is limited by both random and systematic mismatches of current-source transistors. The process gradients introduce systematic device mismatch which is independent of device sizes. The systematic mismatch could be eliminated by structure layout styles, such as common-centroid, symmetry layouts, and dummy devices techniques. The floor plan of CSA layout is illustrated in Fig. 9, where the linear gradient errors, including combination of horizontal gradient and vertical gradient, could be eliminated significantly. The

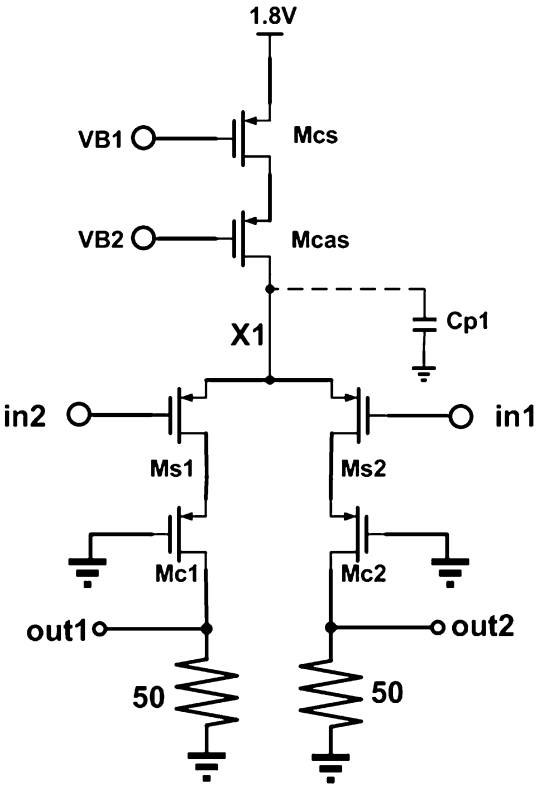


Fig. 10 Current source and switch circuits

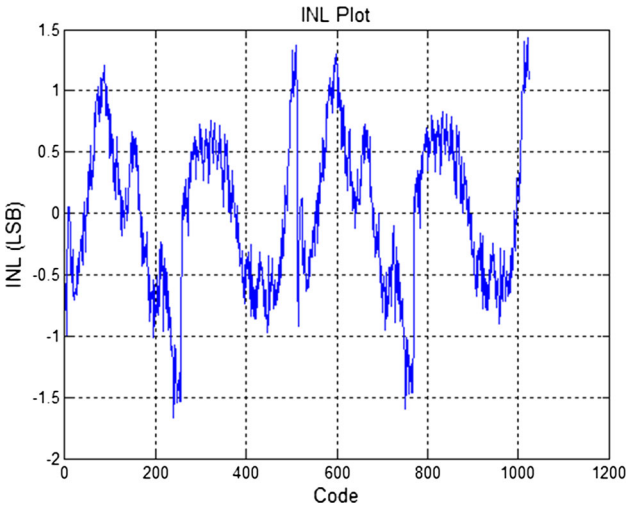
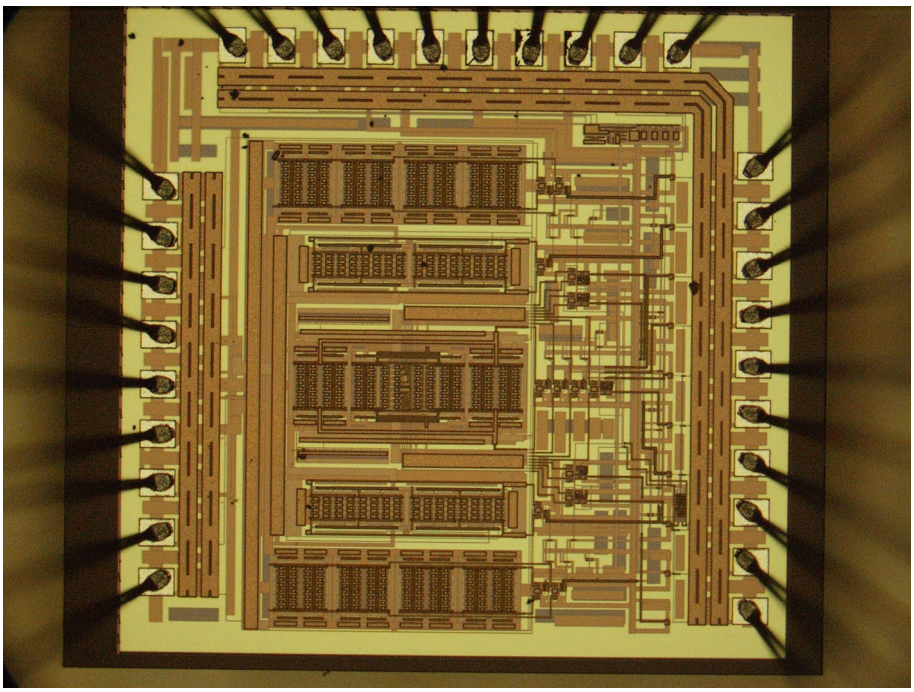


Fig. 12 INL measurement

Fig. 11 Die photo of the proposed DAC



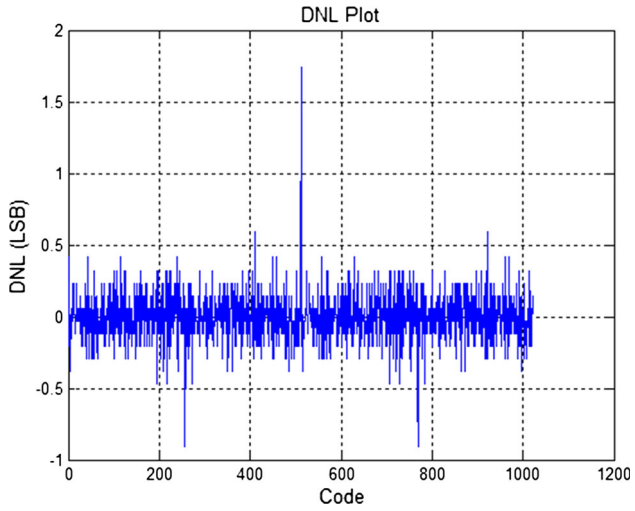


Fig. 13 DNL measurement

IR drop effect is very critical in the post-layout simulation for INL and DNL specs. The width of the metal line should be taken care to achieve minimum resistance and the capacitance effect should not degrade the speed of the DAC. The uniform layout structures are used for clock paths and power paths in this chip to reduce mismatches. In this paper, we do not use layout randomization skill, like the Quad Quadrant switching (Q^2) scheme to suppress higher-order gradient errors [9], because layout randomization often degrades dynamic SFDR at high frequency operation due to large dimension, routing complexity, and timing mismatches.

Random mismatch among the current source transistors cannot be predicted exactly during the design phase. Usually, reducing random mismatch depends on increasing area. The random mismatches are modeled using a Gaussian normal distribution with expected value of zero and a relative standard deviation $\sigma(I)/I$. The statistics among the yield specification of the INL, the resolution, and the standard deviation of the relative unit current for the D/A converter has been proposed before [10]. For the goal of 10-bit accuracy with 99.7 % yield specification at INL $<$ 0.5 LSB, 0.5 % of the standard deviation of a relative unit current is required. The mismatch among MOS transistors in the current source array is dominated by V_{th} and β variations which scale with device sizes [11], where $\beta = \mu CoxW/L$ and V_{th} is threshold voltage. The variance of the difference in drain currents between two equally sized MOS transistors are modeled by the relationship of Eq. 2, where parameters A_{VT} and A_β are technology-dependent constants provided by foundry.

$$\frac{\Delta\beta^2}{\beta} = \frac{A_\beta^2}{WL},\ \Delta V_{th}^2 = \frac{A_{VT}^2}{WL}$$
$$\frac{\Delta I^2}{I^2} = \frac{\Delta\beta^2}{\beta^2} + \frac{4\Delta V_{th}^2}{(V_{gs} - V_t)^2} \quad (2)$$

Using the variation model derived in Eq. (2), combined with the square law of the I–V equation, the design equations of W and L of the current-source transistor can be written as Eq. 3. Since a high yield requires a small value for this standard deviation, this directly implies a large current source area. The over-drive voltage ($V_{gs} - V_t$) of the current-source transistor is chosen to be high to improve the matching further, but it also limits the maximum output swing. In this chip implementation, a single supply of 1.8 V is used for low power concern, and the over-drive voltage is designed as 0.4 V with $I_{LSB} = 10$ µA. From Eq. 3 with TSMC mismatch data, we can derive the transistor size as W = 8 µm and L = 3.5 µm.

$$\frac{W}{L} = 2I \Big/ \left(\mu Cox\left(V_{gs} - V_t\right)^2\right)$$
$$WL = \left(A_\beta^2 + \frac{4A_{VT}^2}{\left(V_{gs} - V_t\right)^2}\right) \Big/ \frac{\Delta I^2}{I^2} \quad (3)$$

Another impact factor which may degrade the accuracy of the DAC is the finite output impedance of the current-source transistor [12]. To meet INL and DNL specifications, the minimum output impedance is required, and the output impedance also impacts dynamic SFDR. As many literatures derived before [13–15], the relationships between INL, SFDR and finite output impedance (Ro) are stated in Eqs. (4) and (5). The required Ro is 26 MΩ with 50 Ω termination to meet 10-bit INL and SFDR specs.

$$INL = \frac{I_{unit} Z_L^2 2^{2N}}{4Ro} \quad (4)$$

$$\text{SFDR} = 20\log\frac{4Ro}{Z_L 2^N} \quad (5)$$

To achieve the minimum output impedance of 26 MΩ, the cascade structure is used for unit current source, as shown in Fig. 10, where transistor Mcas is added between Mcs and the source of current switches Ms1 and Ms2. For reduction of the clock feed-through effect, Mc1 and Mc2 are added between current switches and differential outputs (out1, out2). The sizes of Ms1, Ms2, Mc1 and Mc2 are designed small to avoid the large loading of the switch driver. Besides, the parasitic capacitance Cp1 at node X1 is very critical for dynamic SFDR [16], especially for input frequency greater than Fs/4, where Fs is the clock rate of the converter. Therefore, Cp1 should be minimized in the layout to enhance SFDR, so the connection wires between current switch and Mcas should be as short as possible. The return-to-zero (RZ) technique has been proposed to improve the DAC dynamic performance at high input frequency [17], but RZ data streams are not acceptable for many applications, and it is not suitable for binary-weighted converter due to large output voltage drop at high speed operation.

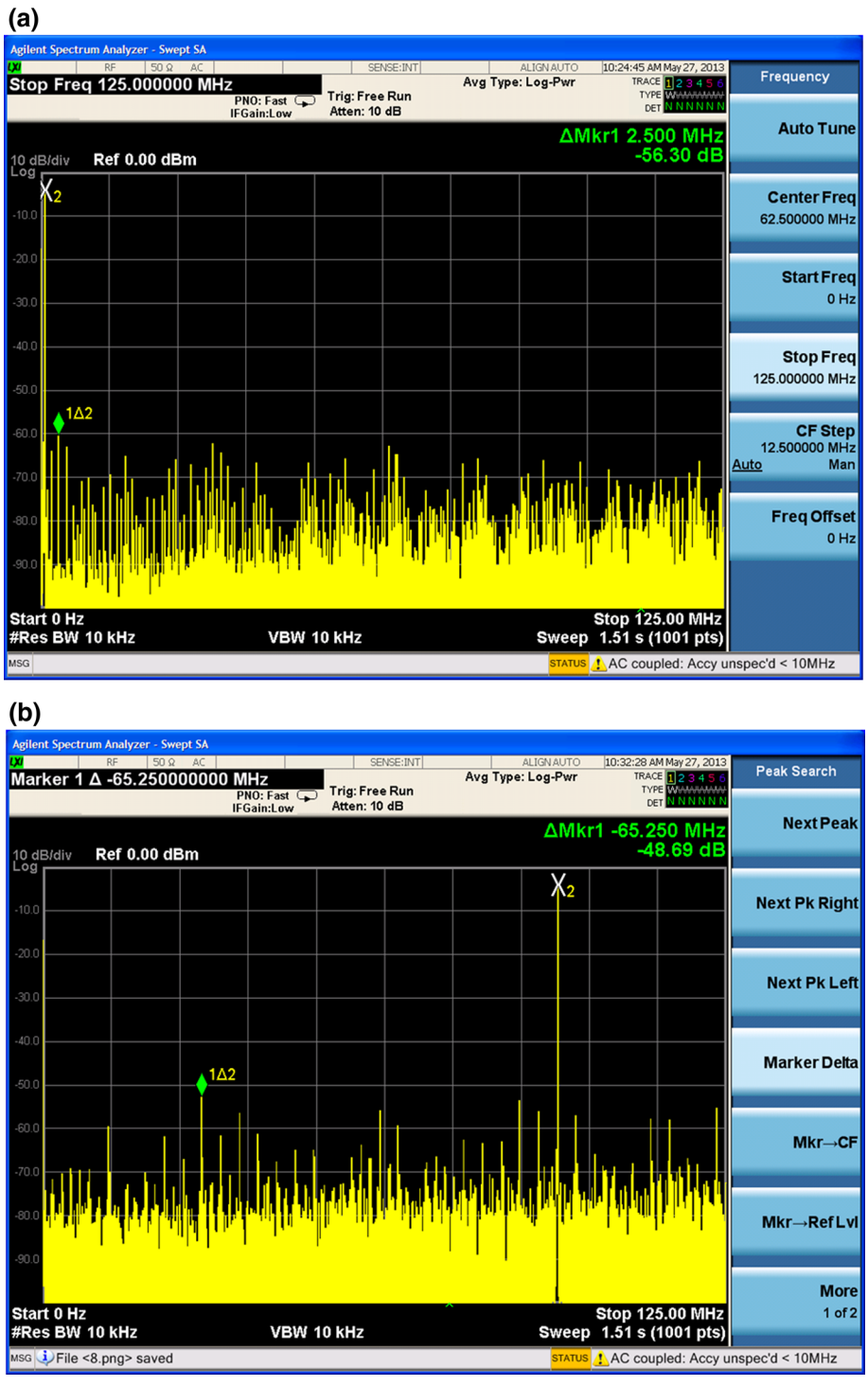


Fig. 14 Output spectrums for **a** 0.67 MHz, **b** 94 MHz at 250 MS/s clock frequency

4 Measurement results

The proposed binary-weighted DAC was implemented in a TSMC 1P6M 0.18-μm CMOS process. The active area of the DAC is 1.1 mm × 1.0 mm. Figure 11 shows the die microphotograph of realized design. All measurements have been performed on differential outputs with 50 Ω loading, respectively. The analog supply voltage and digital supply voltage of the chip are all 1.8 V, and the total current is 10.5 mA.

Figure 12 shows the measured INL profile versus the input code and Fig. 13 shows the measured DNL profile of the 10-bit CMOS DAC. The INL is smaller than 1.6 LSB. The DNL error lies between −1 and +1.8 LSB. In general,

for high resolution DAC, INL is greater 1 LSB without calibration. This major error is due to the mismatch of current source arrays of MSB parts.

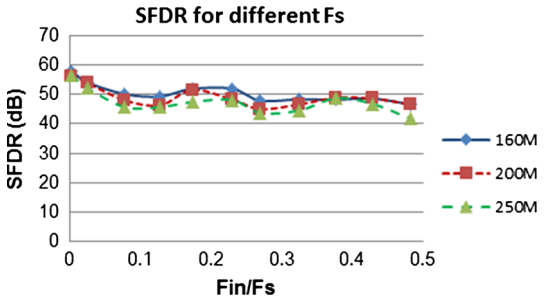


Fig. 15 Measured dynamic SFDR performance

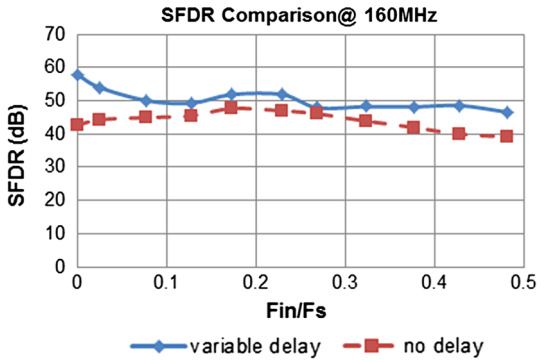


Fig. 16 SFDR comparison between variable delay and no delay

For dynamic test, the DAC has been measured for different conversion rates up to 250 MS/s. The single-tone output spectrum has been measured for several values of the signal frequencies and of conversion rates. At 320 MS/s, the best SFDR is 58 dB with 0.86 MHz output frequency. Figure 14 shows the frequency spectrum for the DAC in which the measured SFDR is 56 dB at output frequency of 0.67 MHz and is 49 dB at output frequency of 94 MHz when the clock rate is 250 MS/s. Figure 15 shows the dynamic SFDR performance for different clock rates of 160, 200, and 250 MHz, respectively. On the horizontal axis, the relative output frequency is plotted, where this relative output frequency is defined as the ratio between the signal frequency and the clock frequency. The measured SFDR results between variable-delay buffer and typical binary-weighted DACs are compared in Fig. 16 for 160-MS/s clock rate. It is clear to see the dynamic SFDR has been improved significantly at most of signal frequencies, and the SFDR improvement is over 10 dB at low signal frequencies and is over 5 dB at most of signal frequencies. The glitch energy measurements for variable-delay buffer and typical binary-weighted DACs during major code transitions are shown in Figs. 17 and 18, respectively. This measurement validates the variable-delay buffer technique, and the glitch energy was reduced from 132 to 1.36 pV s. Table 2 summarizes the performance of the DAC. The Figure-Of-Merit (FOM) is calculated by resolution (N), clock frequency (Fs), and power consumption as follows.

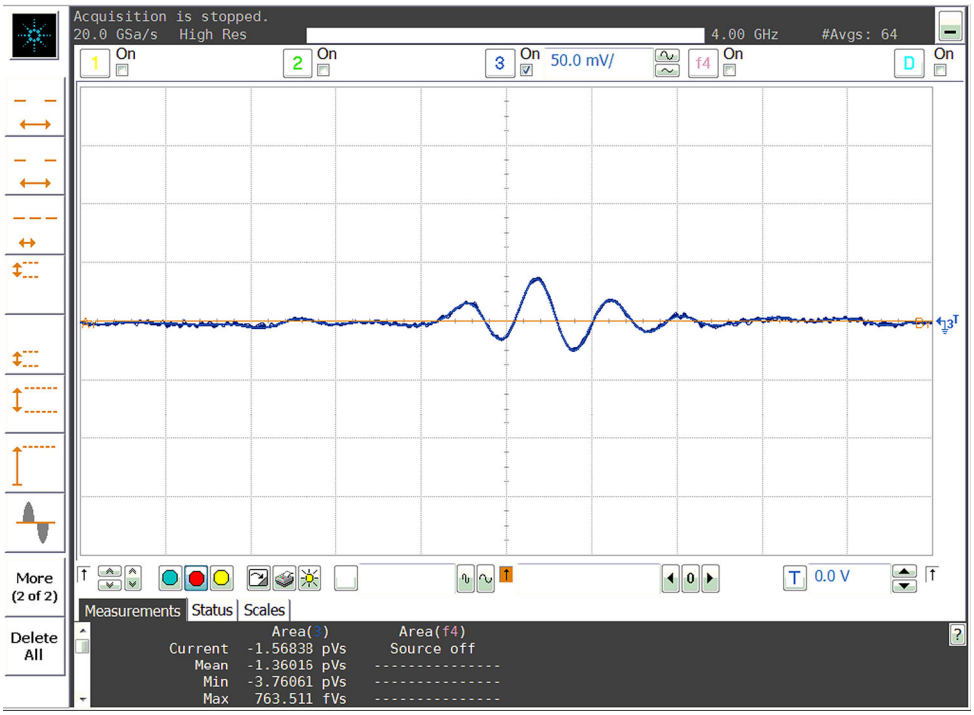


Fig. 17 Glitch waveform of the DAC with variable-delay buffers

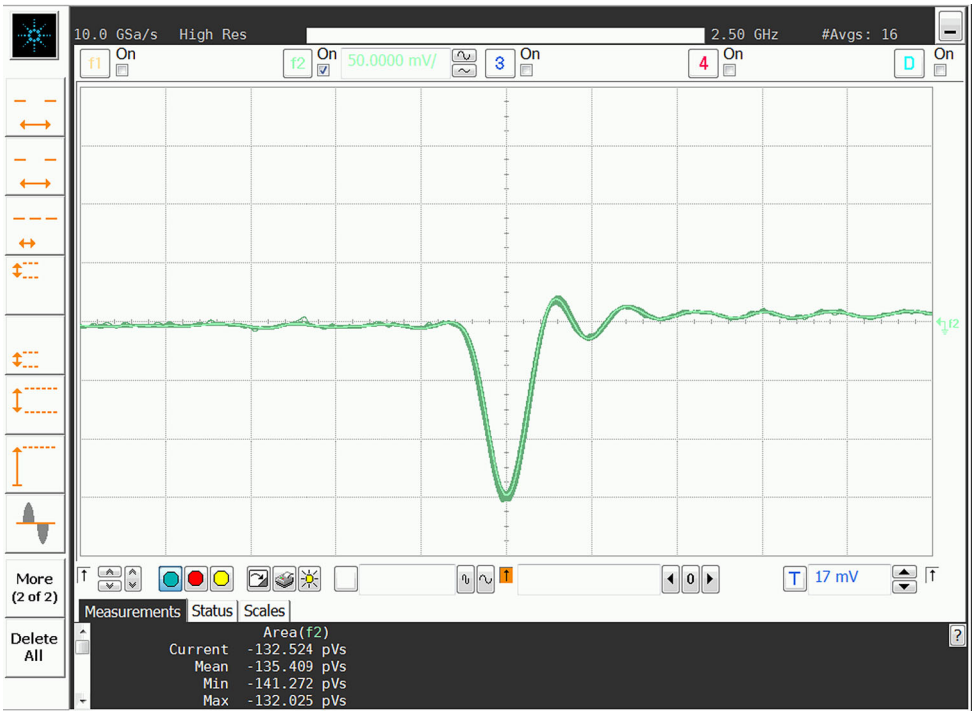


Fig. 18 Glitch waveform of the typical DAC without delay

Table 2 Performance summary

Technology	CMOS 0.18 μm
Resolution	10 bits
Clock rate	250 MS/s
SFDR	58 dB
Glitch energy	1.36 pV s
DNL	1.8 LSB
INL	1.6 LSB
Supply voltage	1.8 V
Power consumption	19 mW
active area	1.1 mm^2

Table 3 Comparison with previously published literatures

	This work	[3]	[17]	[18]	[19]
Technology	0.18 μm	0.18 μm	90 nm	0.35 μm	0.25 μm
Resolution	10	10	8	12	10
Sample rate (MS/s)	250	250	1600	120	200
SFDR (dB)	58	60	57	71	55
Glitch energy (pV s)	1.36	2.64	N/A	31	1.5
Supply voltage (V)	1.8	1.8	2.5/1.2	3	3.3
Power consumption (mW)	19	22	90	52.5	82
FOM ($\times 10^9$)	13,473	11,636	4,551	9362	2,497

$$FOM = \frac{2^N Fs}{Power} \tag{6}$$

Table 3 gives an overview of the comparison of this work with recently presented DACs, with respect to FOM. Finally, the full scale settling time of the DAC was measured, and the rise time (10–90 %) of the DAC is 0.8 ns.

5 Conclusion

A novel deglitching method with low power for a pure binary-weighted DAC is proposed. Experiment results validate the glitch reduction from using variable-delay buffers in the input data path. The glitch energy during major code transition is reduced to 1.36 pV s. The improvement in the SFDR of the DAC is over 10 dB by using variable-delay buffers. The measured SFDR is 56 dB for 0.67 MHz input and 49 dB for 94 MHz input at 250 MS/s update rate, and the INL and DNL are less than 1.6 and 1.8 LSB, respectively. The converter, implemented in TSMC 1P6M 0.18 μm CMOS technology, has an active area of 1.1 mm^2 and dissipates 19 mW from a single 1.8 V power supply.

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