

Tellico Power9 System: Unleashing High Performance Computing at UTK

Presenter: Nigel Tan



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Denver, CO | **hpc**
is now.

IBM Shared University Research Award

- Taufer, Dongarra, Peterson, and Dean lead an IBM Shared University Research (SUR) Award at UTK
- The SUR supported the acquisition of a high-performance computing cluster based on IBM Power9



Greg Peterson, Michela Taufer, and Jack Dongarra (UTK)



Jamie Thomas (IBM), Michela Taufer (UTK) and Mark Dean (UTK)

Hardware Specifications



The UTK cluster includes:

- 4 x 32-core **Power9** nodes (128 GB RAM)
 - 2 x GPU compute nodes, each with 2 Nvidia **V100s**

The cluster is supported by:

- 1 elastic storage server (IBM Spectrum Scale)
- 2 TB raw disk space per compute node
- 1 Infiniband 36 port EDR TOR switch (non-blocking)
- 1 IBM Ethernet switch (48x1Gb+4x10Gb) with 1 GB connectivity for the cluster

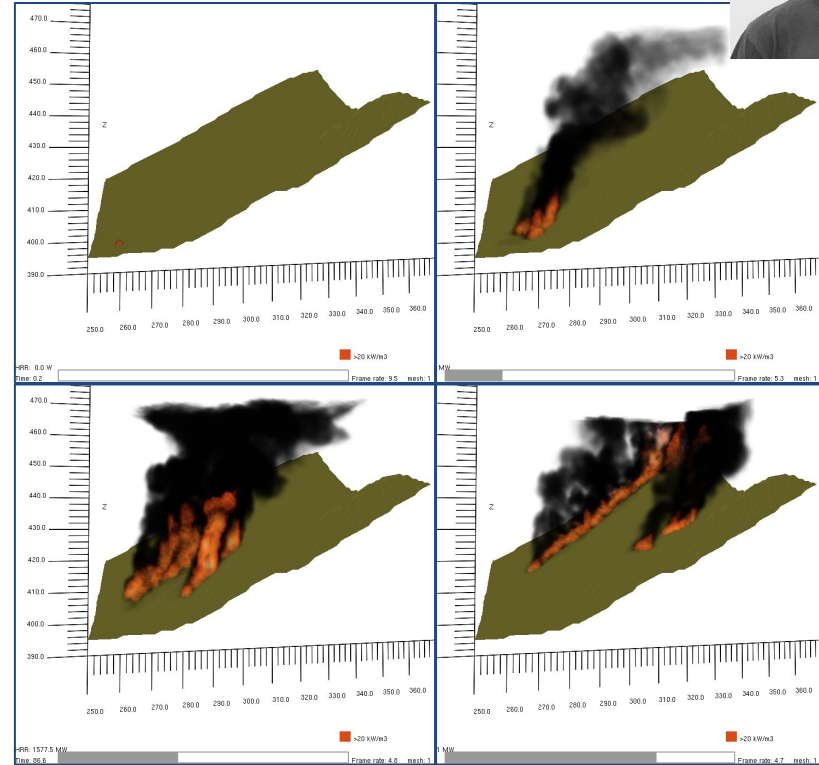
Use Cases

- **Fire simulation:** Simulation of real-world wildfires using NIST's Fire Dynamics Simulator
- Performance Portable Plasma Simulations for the Exascale Era: Quantifying the Costs and Benefits of Portability in **VPIC**
- **A4MD:** Characterizing In Situ Workflows for Molecular Dynamic Simulations
- Computing Properties from X-Ray **Diffraction Patterns of Proteins**

Fire Dynamics Simulator (Gatlinburg)



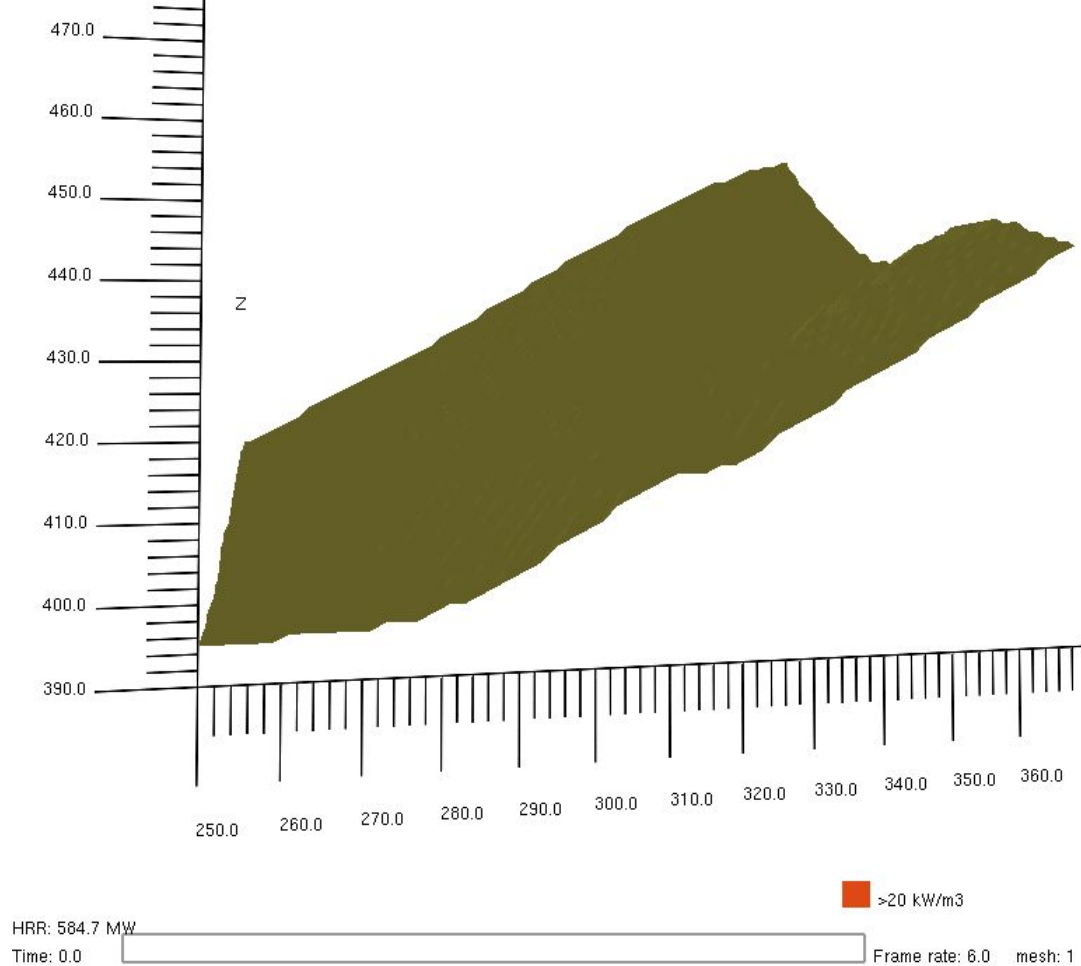
- Tellico lead researcher:
Danny Rorabaugh
- Collaboration between GCLab and Dr. David Icové
- We use NIST's Fire Dynamics Simulator (FDS) to simulate real-world wildfires
- The pictured simulation incorporates topography and vegetation of Gatlinburg, TN as parameters
- The 2016 Gatlinburg wildfire caused 14 casualties and over \$500 million in damages



Simulated Wildfire

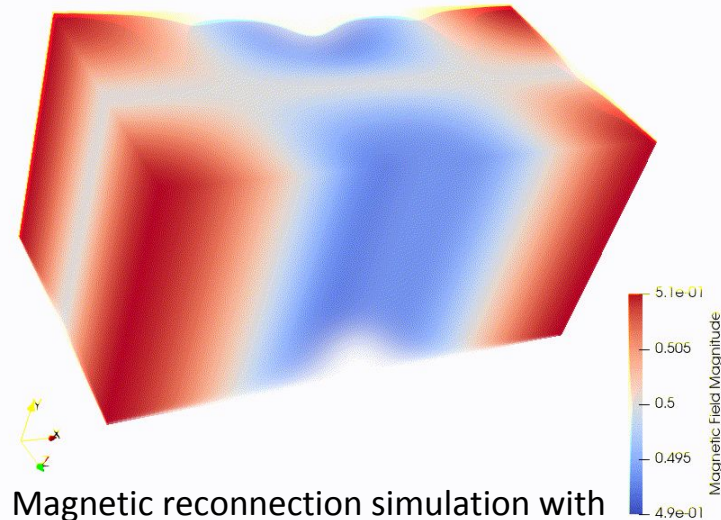
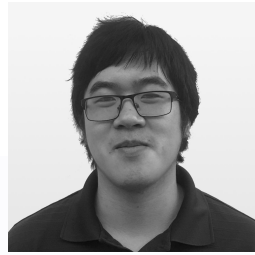
Simulation specs:

- 2016 Gatlinburg wildfire simulation
- 1 node, 16 threads with OpenMP
- 120m × 120m × 100m spatial domain
- 5 frames per second temporal resolution



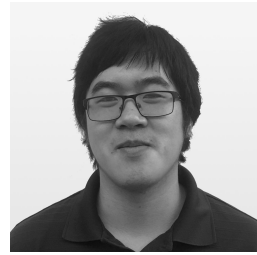
Vector Particle-In-Cell

- Tellico lead researcher: **Nigel Tan**
- Collaboration with Los Alamos National Lab
- VPIC is a high performance PIC code for kinetic plasma simulations
- We are investigating the tradeoffs introduced by the Kokkos portability framework

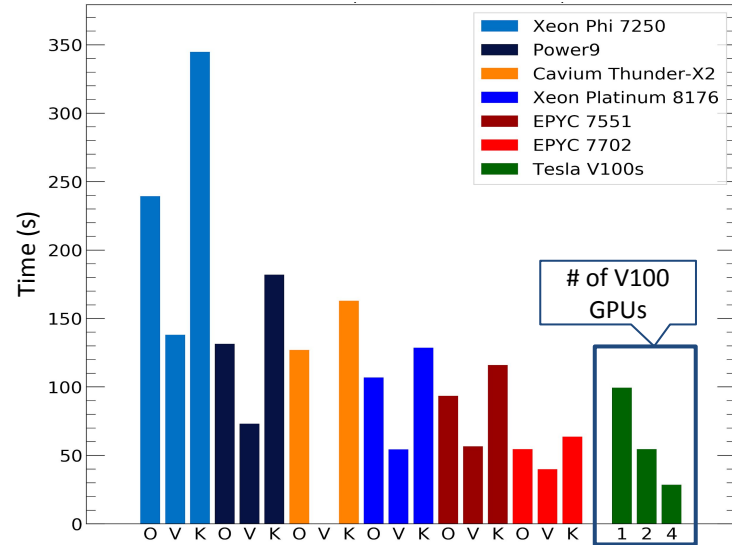
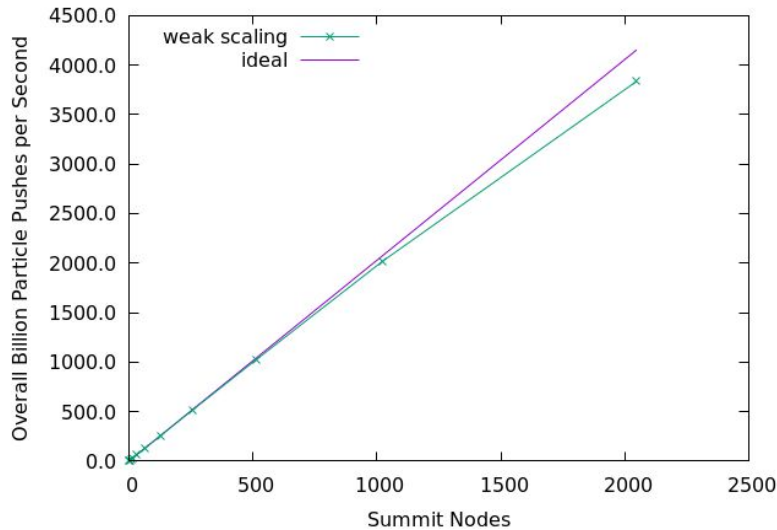


Magnetic reconnection simulation with 4,194,304,000 particles, a single force free current sheet, and conductive boundaries. The simulation ran on Tellico with 64 cores.

Vector Particle-In-Cell



- Initial port achieves near ideal weak scaling on 2048 Summit nodes but needs optimization to reach the match the original

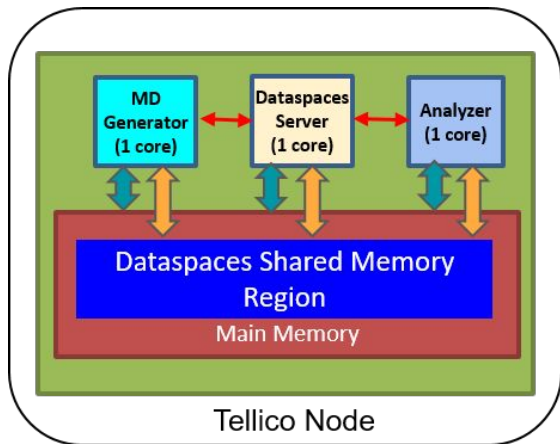


O: Original
V: Vectorized
K: Kokkos

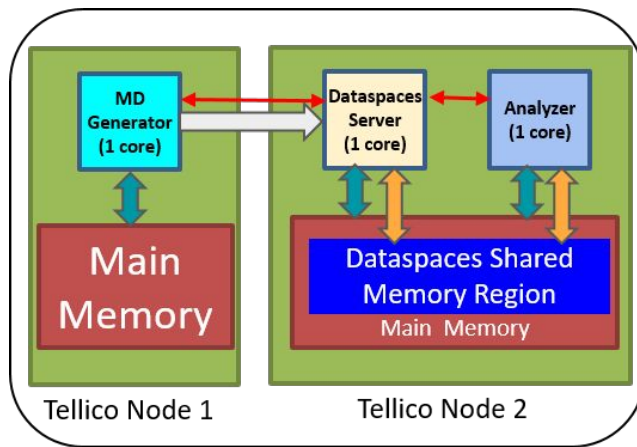


- Tellico lead researchers: **Michael Wyatt** and **Ian Lumsden**
- Collaboration with *USC*, *UNM*, *UD*, and *Cornell*
- We study the execution patterns of molecular dynamic (MD) simulations and analytics for *in situ* and *in transit* dataflows

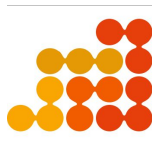
(In Situ)



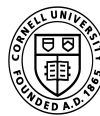
(In Transit)



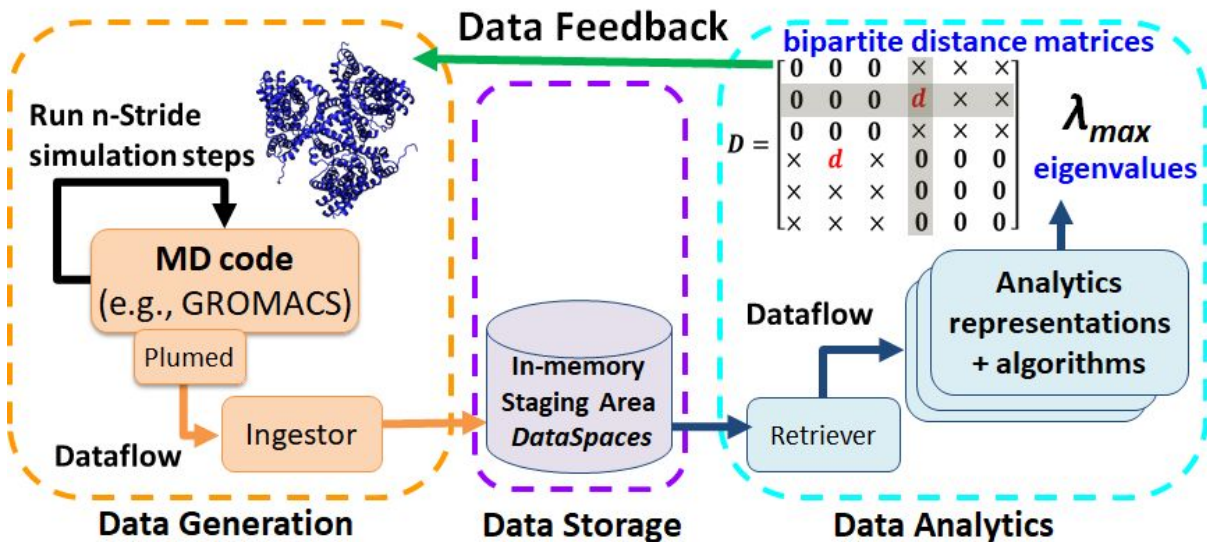
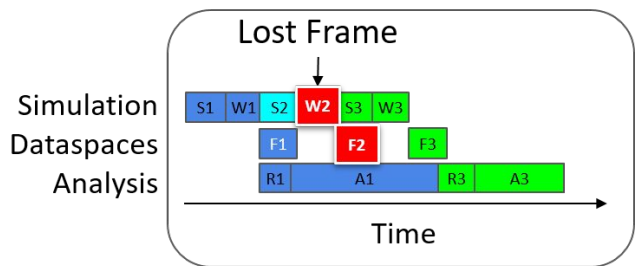
A4MD



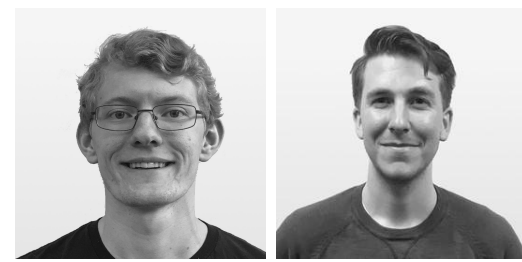
analytics
for molecular
dynamics



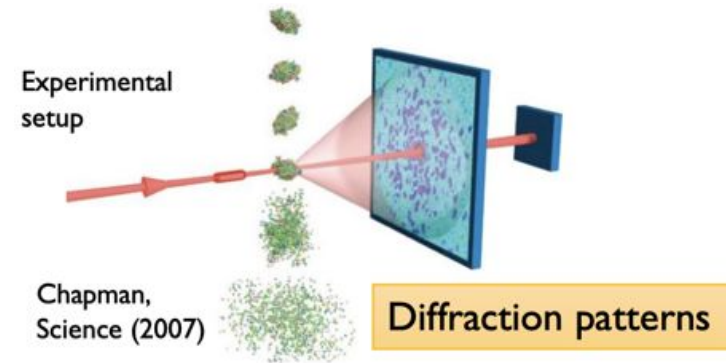
- The rate of frame production/consumption affects when a frame is analyzed or dropped
- We model the MD dataflow to understand the impact of dropped frames on capturing rare MD events



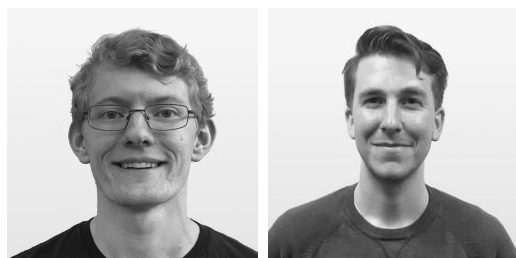
Protein Diffraction Patterns



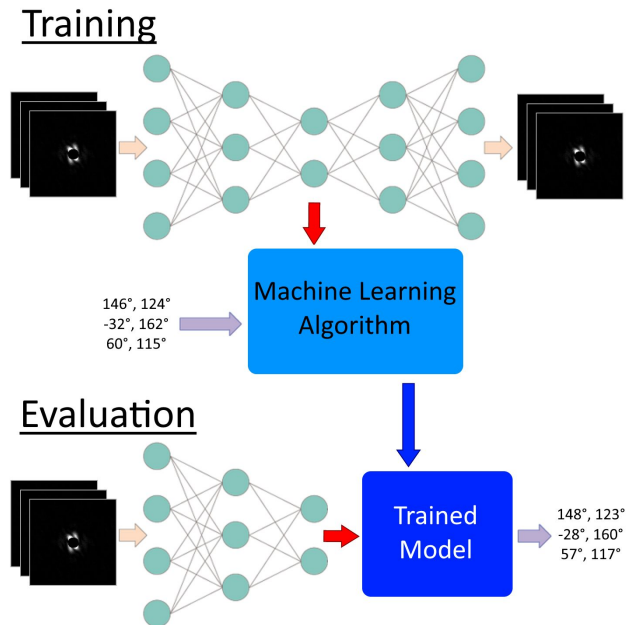
- Tellico lead researchers: **Neil Lindquist** and **Mike Wyatt**
- Collaboration between *GCLab*, *ICL*, and *RIKEN*
- X-ray Free Electron Laser beams create diffraction patterns after hitting proteins that may reveal structural information
- We are interested in differentiating between orientations of a single protein, different structures of a single protein, and different proteins



Protein Diffraction Patterns



- An hourglass-shaped neural network is trained to map the patterns to themselves, which creates low rank representations
- This is used to train a machine learning model to compute the desired properties
- We are using simulated patterns and the protein's orientation to test our workflow, but plan to expand to other properties and real diffraction patterns



Tellico's HPC Impact

- HPL: 1.0046 TFlops
- HPCG: 52.5254 GFlops
- Graph500:
 - 1.023 GTeps, 28 scale (BFS)
 - 0.337 GTeps, 28 scale (SSSP)
- All tests are CPU only using reference implementations on 64 cores
- GPU enabled HPL: ~2 TFlops

Historical Perspective

- Compared to the Cray-1 (1975)
 - Over 6,278 times the computational performance
 - Less than 1/50th the power consumption
- Would place 12th (SSSP) on the Graph500 as of the most recent list

