ESSDERC 2013

Emerging Memories

Livio Baldi, Gurtej Sandhu

Micron Technology

©2013 Micron Technology, Inc. All rights reserved. Products are warranted only to meet Micron's production data sheet specifications. Information, products, and/or specifications are subject to change without notice. All information is provided on an "AS IS" basis without warranties of any kind. Dates are estimates only. Drawings are not to scale. Micron and the Micron logo are trademarks of Micron Technology, Inc. All other trademarks are the property of their respective owners.

Outline

- Solid State Memories: a success story
- A lot of alternatives:
  - Prototypal memories
  - New concepts
- From cell to memory
- Is there a winner?

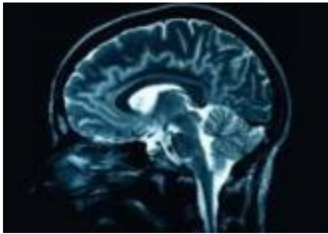
©2013 Micron Technology, Inc.

Outline

- Solid State Memories: a success story
- A lot of alternatives:
  - Prototypal memories
  - New concepts
- From cell to memory
- Is there a winner?

©2013 Micron Technology, Inc.

There is more than one memory



In our head

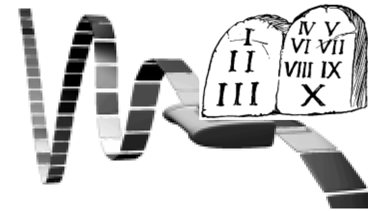
Retention time:

- **Short term memory**: what was in previous slide? (if you still remember it)
- **Long term memory**: what did you learn at school?

But also functions:

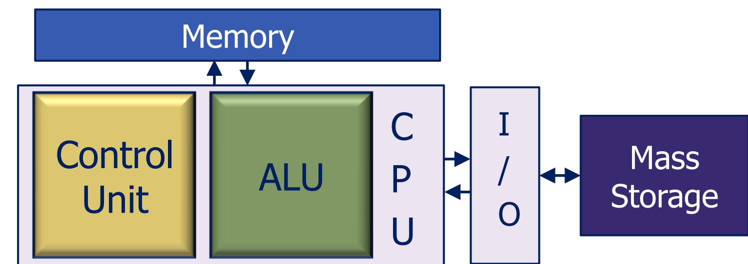
- **Procedural memory**: how to ride a bike, make a knot in your tie,..
- **Semantic memory**: remembering well defined data, e.g. a phone number
- **Episodic memory**: past events, e.g. your trip here, your holidays, the plot of a movie.

and in computers



In Turing machine:

- A memory for **data** (endless tape)
- A memory for the **instructions**



Von Neumann architecture:

- One main memory for data and program
- One mass storage unit

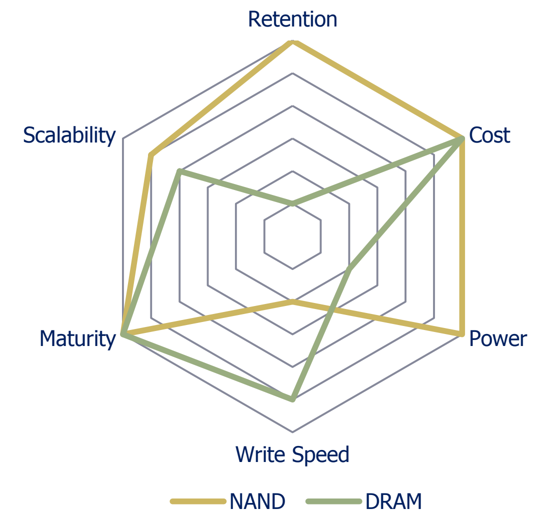
©2013 Micron Technology, Inc.

Memory performances

There is no single parameter to characterize memories:

- Size: how many bits in a single device?
- Retention: how long is information conserved without power supply?
- Endurance: how many times can I change the content before degradation?
- Programming speed: how fast can I change the content?
- Access speed
  - Latency: how long before the first data out?
  - Throughput: which is maximum reading data flow?
- Power
  - Programming
  - Reading
  - Stand-by
- COST: how many bucks per bit (or Byte, or Gigabyte)?

And others (BER, T range, ……)



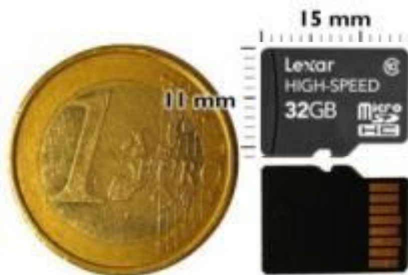
©2013 Micron Technology, Inc.

The evolution of memory systems

- Early Computing
- Early Storage

IBM Hard Disk Drive 1965
Weight > 1ton
Capacity: 5Mbyte

Today:
- 32Gbyte microSD

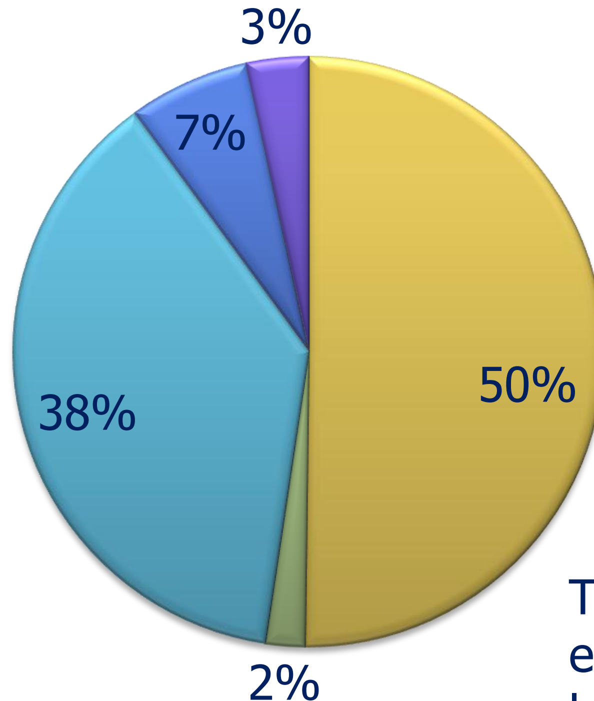


©2013 Micron Technology, Inc.

Memory market

Sales 2012

Total market: 52 B US$



Volatile memory: 52%
Non-volatile: 48%

The market is dominated by two extreme types of memory, with the lowest costs.

Source: IHS iSupply

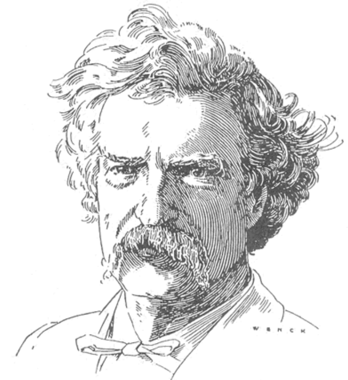
©2013 Micron Technology, Inc.

Scaling Issues

NAND

- Active dielectric thickness
- Isolation aspect-ratio and parasitic coupling
- Statistical effects increase due to few electrons storage
- Increasing weight of Error Correction Algorithms

- DRAM
  - Cell transistor architecture in a 4F2 size (refresh time)
  - Cell capacitor material with high-k dielectric
  - Cell capacitor aspect ratio



BUT:

"The reports of my death are greatly exaggerated".

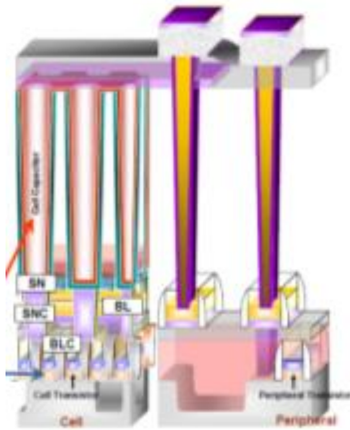
©2013 Micron Technology, Inc.

3-D memories

Manhattan approach:
- more efficient use of real estate by stacking memory cells.

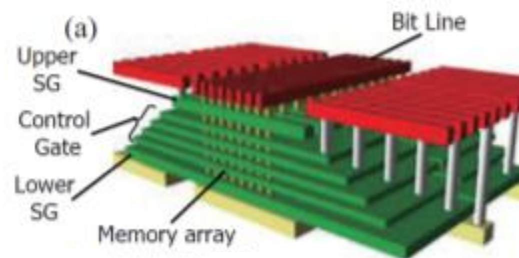
East block approach
- More efficient use of space by putting more bits in the same cell.

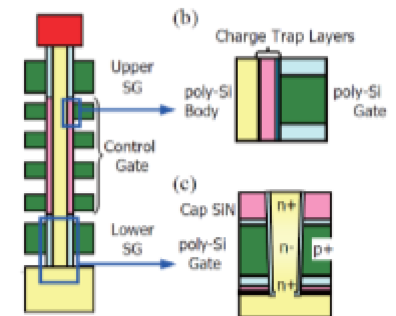
DRAM memory
- From planar capacitor to
- vertically stacked capacitor
- vertical transistor as next step



NAND memory
- Vertically stacked memory cells
- Polysilicon channel
- Better use of area, but
- Cell footprint cannot be scaled
- Density = number of layers
- Cost = number of layers
- Multibit/cell

BiCS





*VLSI 2007

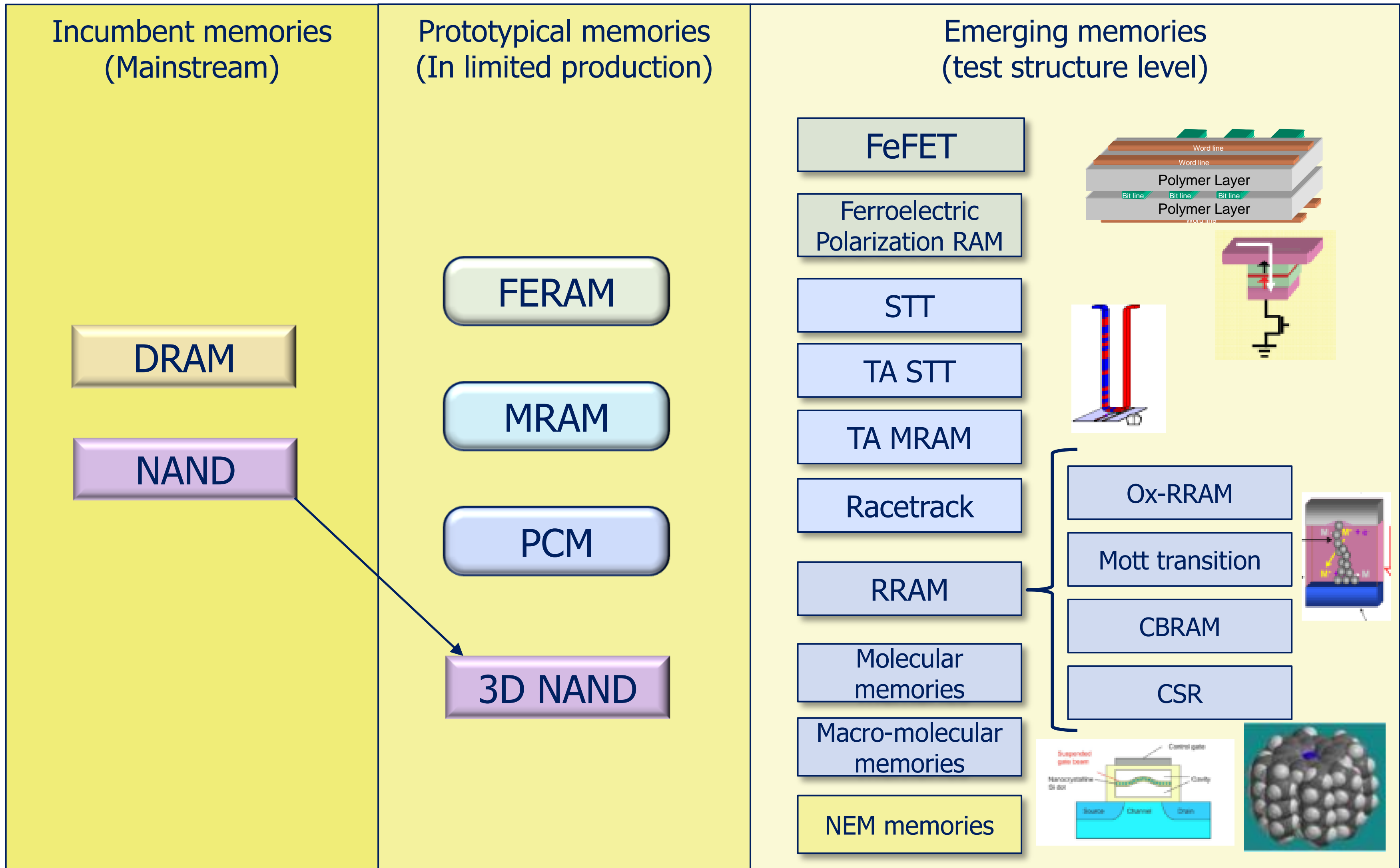
©2013 Micron Technology, Inc.

Outline

- Solid State Memories: a success story
- A lot of alternatives:
  - Prototypal memories
  - New concepts
- From cell to memory
- Is there a winner?

©2013 Micron Technology, Inc.

Memory cell landscape



©2013 Micron Technology, Inc.

Outline

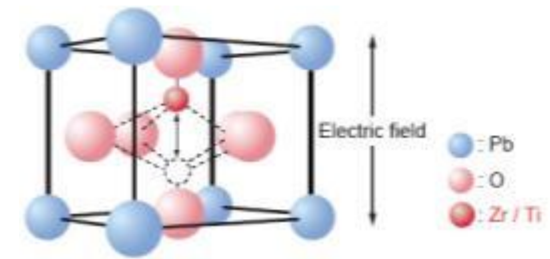
- Solid State Memories: a success story
- A lot of alternatives:
  - Prototypal memories
  - New concepts
- From cell to memory
- Is there a winner?

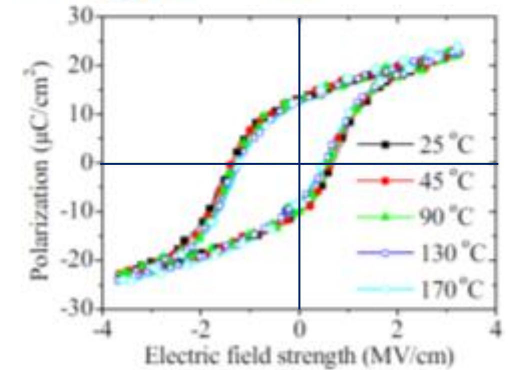
©2013 Micron Technology, Inc.

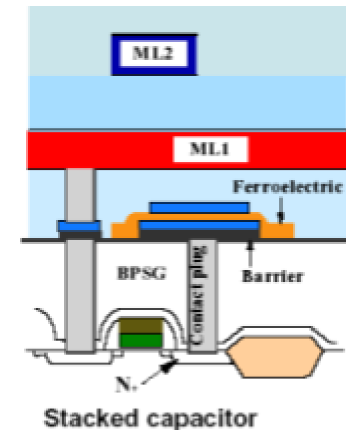
Ferroelectric Memories

- Storing mechanism
  - Permanent polarization of a ferroelectric material induced by external electric field, related to ion displacement in the crystal cell.
  - Most common ferroelectric device is the FeRam
  - DRAM-like cell: 1 transistor, 1 capacitor (1T/1C)
  - Sensing through the displacement current associated to the polarization switch (destructive reading)

  - Two base materials used
    - PZT (PbxZr1-xTiO_3), known since long time
    - SBT ($SrBi_2Ta_2O_9$), more recent material (easier thickness and voltage scalability)







©2013 Micron Technology, Inc.

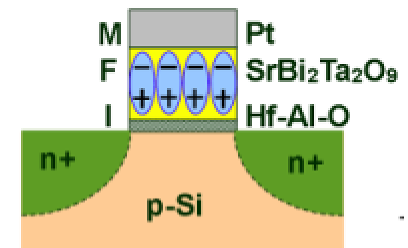
FERAM: Advantages and Issues

- Advantages:
  - Fast (<100ns) and low energy write.
  - High write endurance.
  - Medium/low voltage write.
- Issues:
  - Difficult process integration.
  - Large cell size (25 F^2) and limited scaling potential with respect to Flash and DRAM.
  - Limited read endurance, destructive read-out.
  - Technology gap vs. established technologies.
- Commercially available up to 8Mb (Ramtron, Fujitsu)
- Interest revamped by two emerging concepts

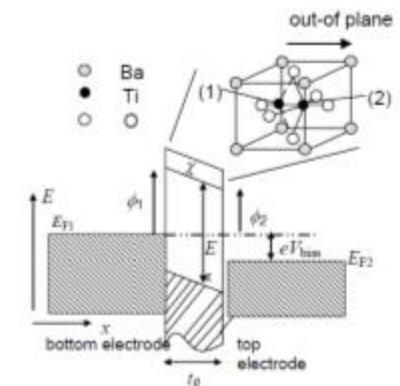
©2013 Micron Technology, Inc.

FeRAM emerging Memories

- Different sensing mechanism
  - Ferroelectric FET: integration of ferroelectric material in transistor gate; Flash-like cell: 1 transistor.
  - Direct sensing of cell threshold, non destructive reading.
  - Issues: large k of ferroelectric material ➔ thick ferroelectric layer ➔ max. aspect ratio limits cell size
  - Read disturbs
  - One paper at this conference



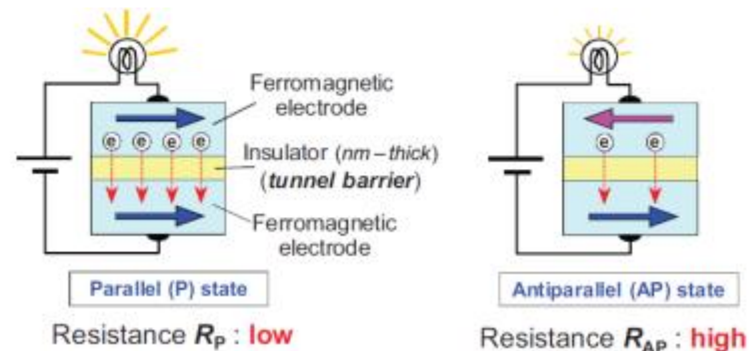
  - Ferroelectric Polarization RRAM: M-I-M tunnel diode where the dielectric is a ferroelectric material
  - Changing ferroelectric polarization can modify the charge injection/transport properties of FE
  - Different mechanisms claimed: Schottky barrier, lattice strain,…
  - Low reading current due to tunnel effect.



©2013 Micron Technology, Inc.

Magnetic Memories

- Storing mechanism
  - Permanent magnetization of a ferromagnetic material
- Sensing mechanism
  - Tunnelling current between two ferromagnetic layers
  - One ‘free’ magnetic layer (easily switchable) and one pinned reference layer
  - Tunnel current depending on mutual orientation of magnetic layers



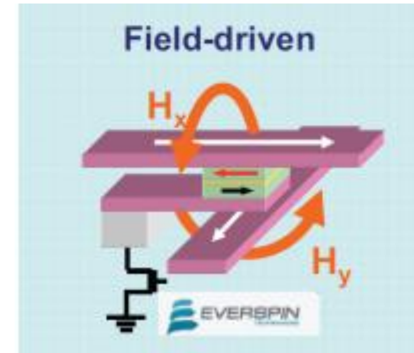
- Main advantages
  - Fast write (<100ns)
  - Low voltage write
  - High write endurance

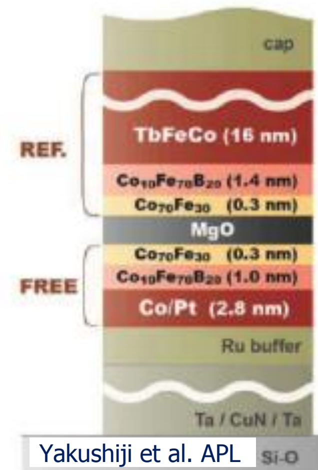
- Freescale first product: 4Mb in 2006

©2013 Micron Technology, Inc.

First Generation

- Tunnel MagnetoResistance (TMR)
  - Programming by current induced magnetic field
- Main issues
  - Difficult process integration (10-12 layers required due to layer matching requirements)
  - Large cell size vs Flash and DRAM (40-80 F^2: IBM, Toshiba), difficult scaling
  - Large write current (>10mA/byte), small read signal
  - Programming disturbs by stray magnetic field
- Heating can assist the switching of the 'free' layer in programming and keep retention and disturb immunity low (Thermally assisted MRAM)
- However heat propagation can become an issue to scaling



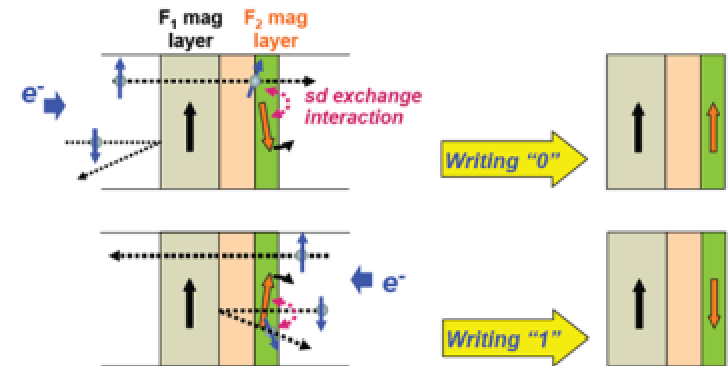


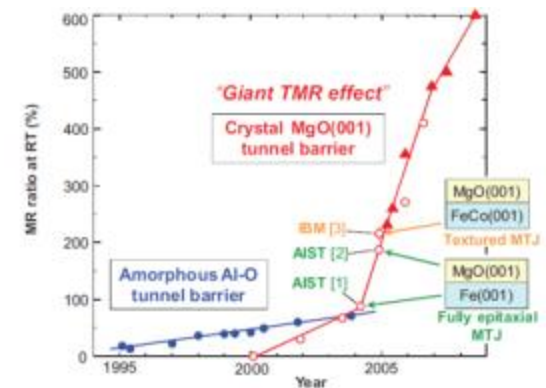
Yakushiji et al. APL

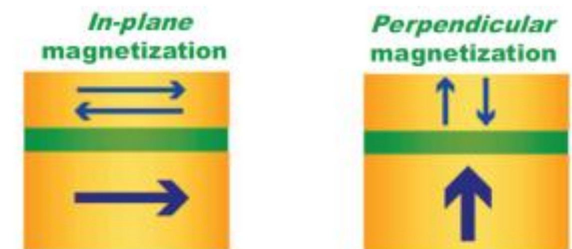
©2013 Micron Technology, Inc.

Second Generation

- Spin-Transfer Torque programming
  - Memory switching by injection of spin-polarized electrons
  - All current directly used for switching
  - Current scales with area.
  - Less disturbs
- MgO dielectric replacing AlO2 -> much better signal
- Perpendicular magnetization instead of parallel -> better scaling, better thermal immunity.
- Cell size down to 14 F2 reported in literature, but average is more than 20.



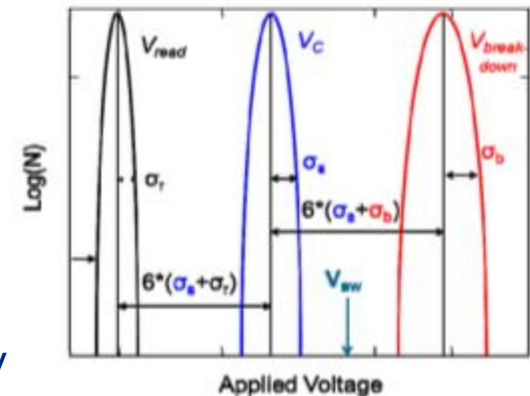




©2013 Micron Technology, Inc.

Some concerns….

- Reading margins
  - 200% is considered high for MRAM, but very low for other NVM types
- Operating margins:
  - Writing voltages in the 0.5-0.6V range;
  - TDDB of dielectric is around 1-1.5V;
  - Read voltage in the 0.15-.2V range
  - Very low margins for safe operation and disturb immunity



J.M.Slaughter, et al. IEDM 2012

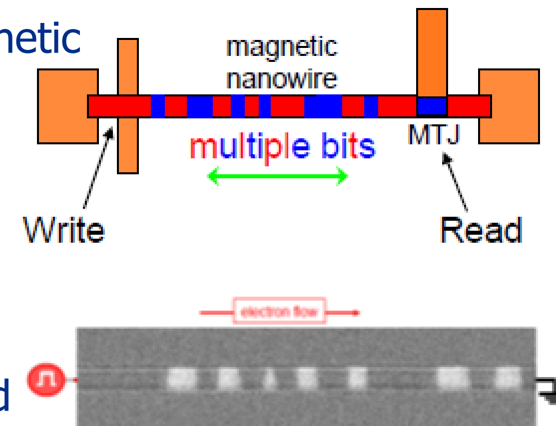
- Tight process control needed due to multilayer structure.
- Possibility of multi-bit operation proposed, but low reading margins.
- Complex read schemes:
  - Conventional with dummy cell, but heavy stress on technology control
  - Self-reference but requires write back

TDDB: Time Dependent Dielectric Breakdown

©2013 Micron Technology, Inc.

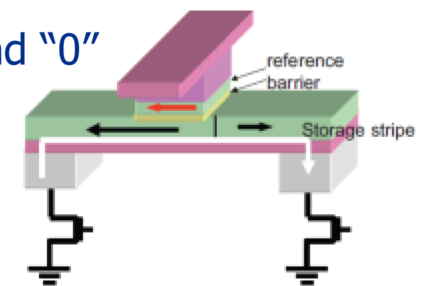
MRAM emerging memories

- Race track memories
  - Proposed by IBM (S.Parkin et al., Science 320, 190, 2008)
  - Shift register organization: bit as domain orientation in magnetic nanowire.
  - One write head and one read head at the ends of the strip.
  - Main issues:
    - Control of domain motion.
    - Current values for domain shift
    - Power consumption: reading requires domain shift and rewriting



S.Parkin et al. IEDM 2011

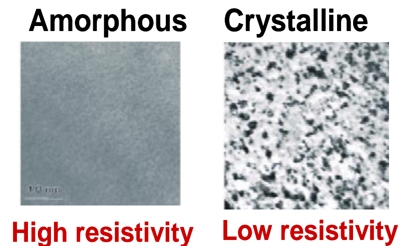
- Alternative Domain Wall
  - Originally proposed by NEC (H.Numata et al. VLSI 2007)
  - Domain wall is shifted left and right by a current, to give “1” and “0”
  - Reading by tunneling current in spin diode.
  - Less reliability problems, but large cell.

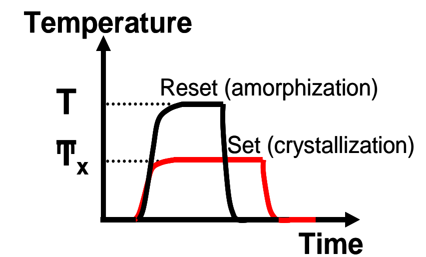


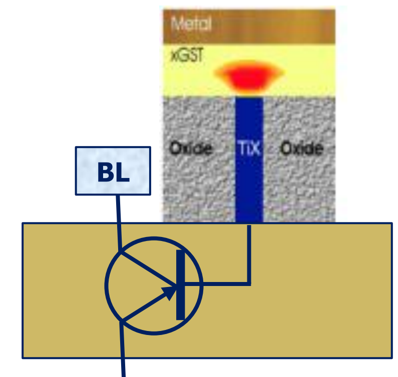
©2013 Micron Technology, Inc.

Phase Change Memories

- Storing mechanism
  - Polycrystalline to amorphous transition in chalcogenide.
- Writing mechanism
  - Current pulse to melt material followed by fast or slow cooling.
- Sensing mechanism
  - Resistivity measurement at low currents
- Cell structure
  - 1 transistor, 1 resistor (1T/1R)
  - Two options: MOS transistor for embedded; bipolar for high density
- Basic material:
  - GST ($Ge_2Sb_2Te_5$ is the most usual, but other compositions also possible)

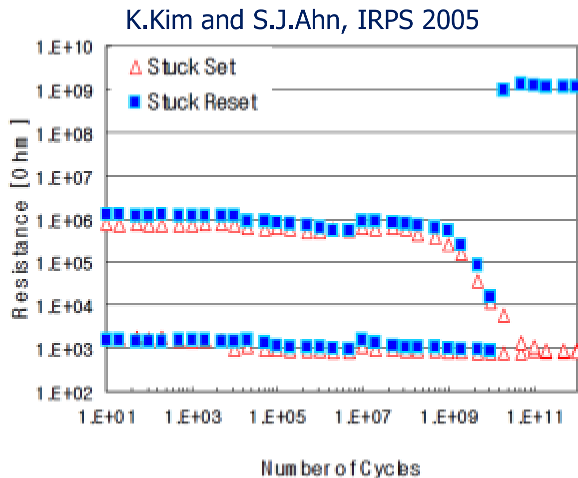


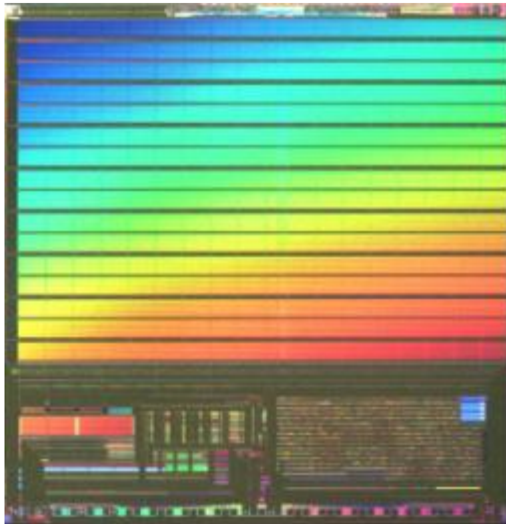




©2013 Micron Technology, Inc.

PCM: Advantages and Issues



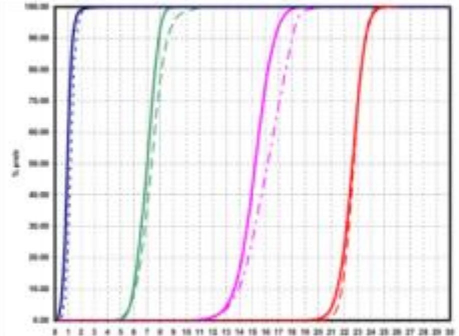


- Main advantages
  - Fast write (<100 ns)
  - Good read signal window (factor ten in resistance)
  - Medium/low voltage write
  - Bit granularity
  - High endurance
  - Cell size comparable to Flash and DRAM
  - Good scalability
- Main issues
  - Process integration for GST
  - Heater-GST interface optimization
  - Writing current (~1 mA), scalable with cell size
  - Retention at high temperature (150° C). Common issue to all emerging memories
- 1Gbit memory available in 45nm technology
  - DDR2 interface
  - NOR Flash legacy spec + bit alterability
  - Chip area: 37.5mm2
  - Power supply range: 1.7V÷2.0V
  - Temperature Range: -40C÷+85C

©2013 Micron Technology, Inc.

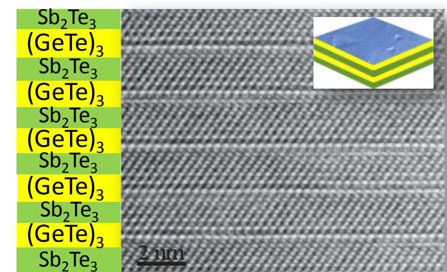
PCM emerging memories

- Multi-level storage
  - Proposed by IBM (Papandreou N. et al., IMW 2011)
  - Using the large Ion/Ioff ratio of PCM cell it seems possible to store 2-3 bit/cell.
  - Densities comparable with NAND appear possible.
  - Main issues: disturbs, threshold drifts



Courtesy of CAMELS project, partially funded under FP6 Programme

- Super-Lattice Memory
  - Originally proposed by NEC (Chong et al. Appl. Phys. Lett. 88 (2006)
  - A super-lattice of chalcogenide layers with thickness within the phase-transition limits.
  - Phase transition assumed to be by motion of Ge atoms without melting.
  - Faster switching, much lower current.
  - Exact mechanism and limits not yet clarified.



Courtesy of PSTRY project, partially funded under FP7 Programme

©2013 Micron Technology, Inc.

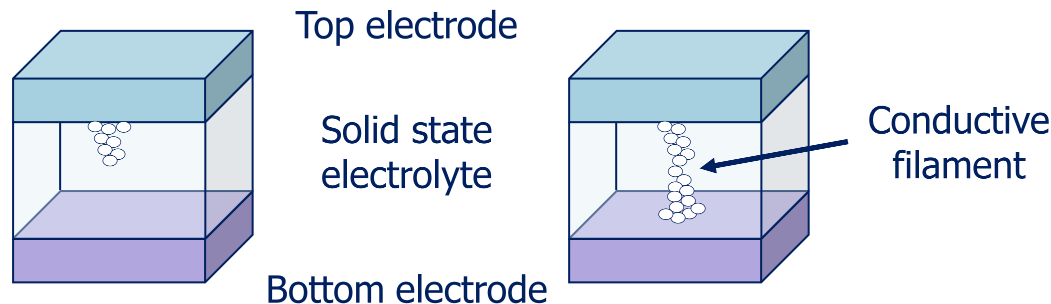
Outline

- Solid State Memories: a success story
- A lot of alternatives:
  - Prototypal memories
  - New concepts
- From cell to memory
- Is there a winner?

©2013 Micron Technology, Inc.

Resistive memories

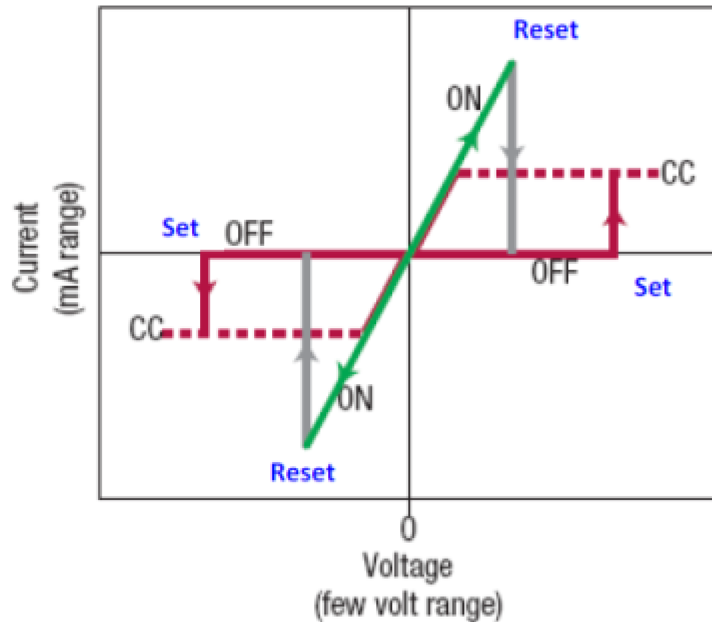
- Formation (and dissolution) of a conductive path between two electrodes:
  - Induced by a voltage pulse
  - Reversible
  - Persistent in time (non volatility)
  - Such as to induce large changes in resistance

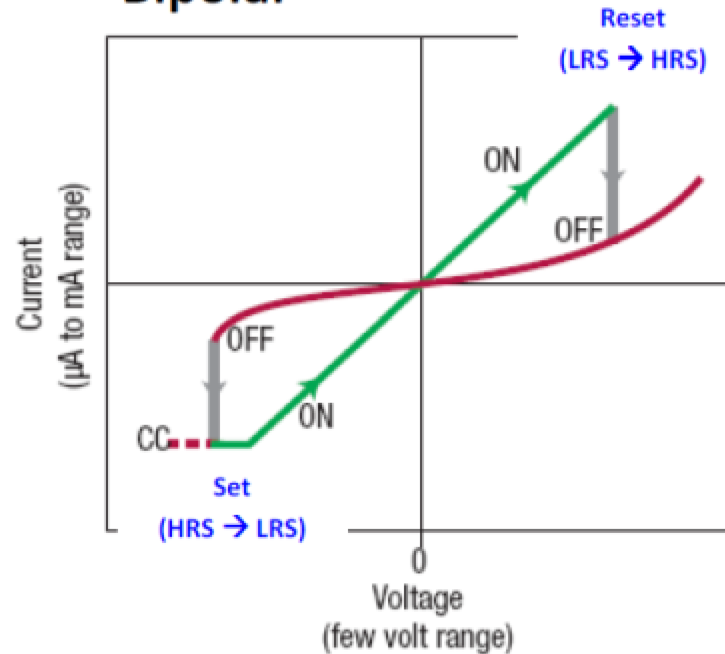


- Conductive filament can have different natures:
  - Metal ions (conductive bridge RRAM or CBRAM)
  - Formation of traps (Oxygen vacancies) OxRRAM
- Generally requires an initialization process ('forming')
- Exact mechanism not yet defined, but phenomenological models available.
- Electrode material plays a critical role.
- 6 out of 8 papers on memories at this conference

©2013 Micron Technology, Inc.

Switching polarity





Type a – Unipolar switching device:

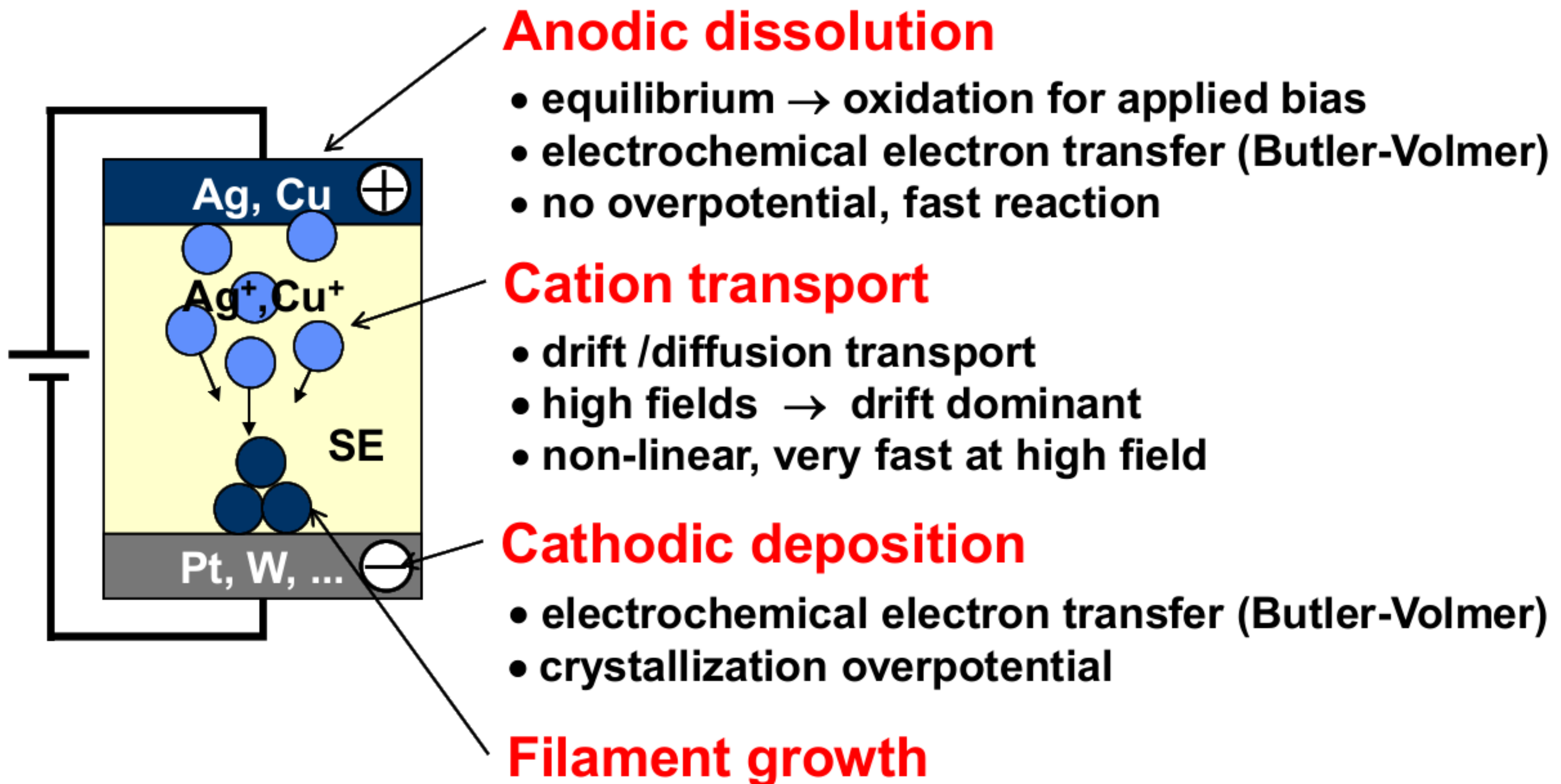
- Switching between ON&OFF depends only upon E amplitude
- Breakdown-type mechanism for Off to On transition (SET)

Type b – Bipolar switching device:

- Switching between ON&OFF depends upon E polarity
- Less stress on material

 ©2013 Micron Technology, Inc.

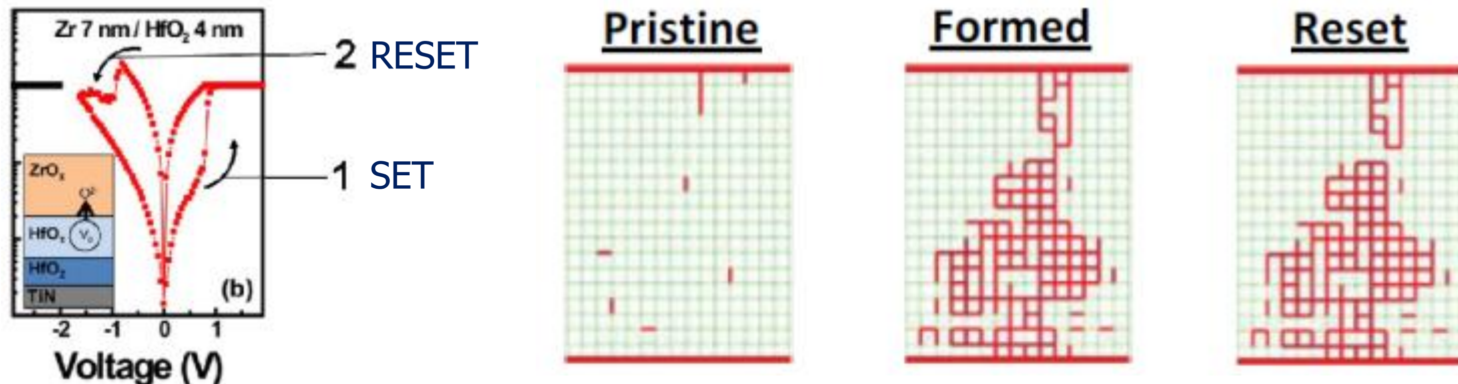
Conductive Bridge RAM



 ©2013 Micron Technology, Inc.

Oxide bridge RAM

- Trap-assisted conduction in metal oxide
  - Formation of a vacancy filament through a forming process (soft breakdown)
  - Conduction through electron tunneling via Oxygen vacancies
  - RESET by dissolution of the filament by oxygen migration and recombination.
  - SET by regeneration of filament through opposite voltage.



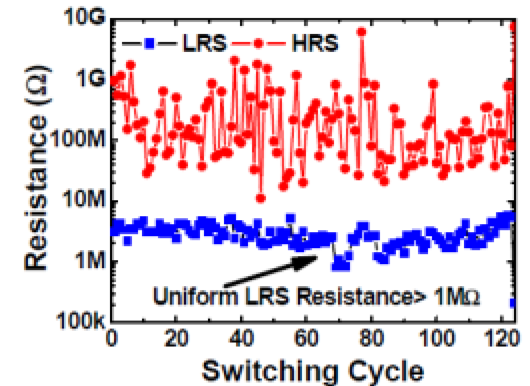
- "Soft breakdown' not very reproducible:
  - Dissolution of filament not always complete. High Ioff currents in RESET.
  - Large variability in On and especially Off states
  - Heating can play an important role

©2013 Micron Technology, Inc.

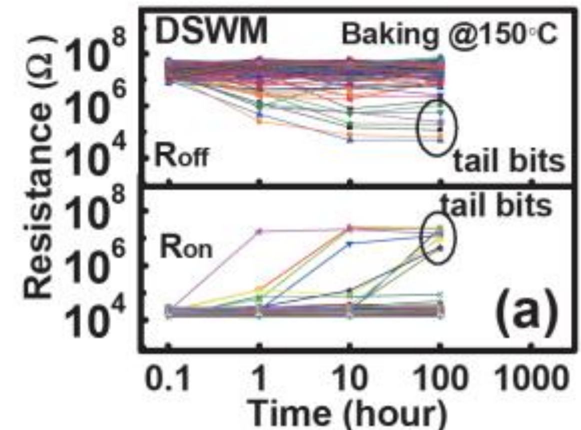
Main concerns of RRAM

- Filament formation not very reproducible
  - Strong dependence on forming process conditions
  - Strong variation in Ioff current, both cell to cell and with cycling
  - RTN noise in high resistance status
  - Sensitive to temperature and voltage stress.
- But:
  - Forming seems avoidable for scaled cells
  - More sophisticated cell architecture and programming algorithms emerging
  - Window seems to improve with cycling

- Not clear understanding of mechanism:
- Complex interplay of cell and electrode materials
- Large variety in materials investigated; materials with an history of integration in CMOS technology (TiO, WO, HfO, TaO) are preferred



Hong-Yu Chen et al., IEDM 2012

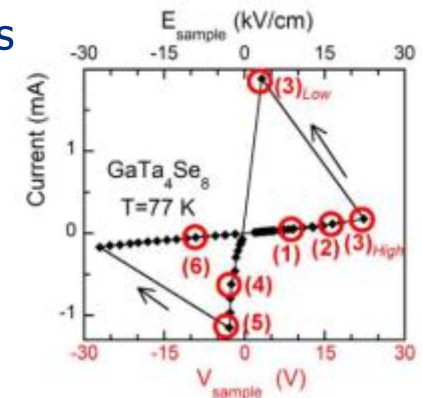


Y.L.Song et al., VLSI 2013

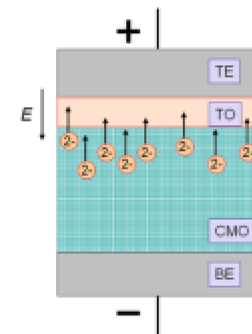
©2013 Micron Technology, Inc.

Other possible RRAM mechanisms

- Mott transition RAM (CeRAM)
  - Charge injection induces a transition from strongly correlated to weakly correlated electrons, resulting in an insulator-metal transition.
  - Explored in VO2, SmNiO3, NiO or more complex combinations (L.Cario et al., Advanced Materials 2010)
  - Exact mechanism still not clear (crystal deformation?)
  - Non volatile?
  - Needs high voltages; 25% Ron/Roff margin at room Tº



- Mixed Valence Oxide RAM
  - Change of tunnel barrier height due to Oxygen ions exchange with conductive metal oxide (R.Meyer et al. NVMTS 2008)
  - Bipolar switching. One order of magnitude between Ron/Roff.
  - A 64Mbit memory presented at ISSCC 2010.

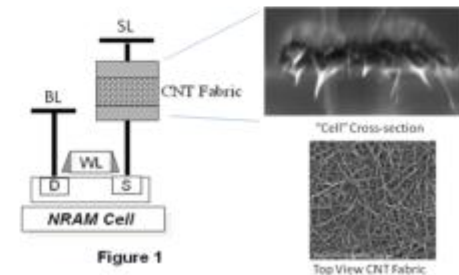


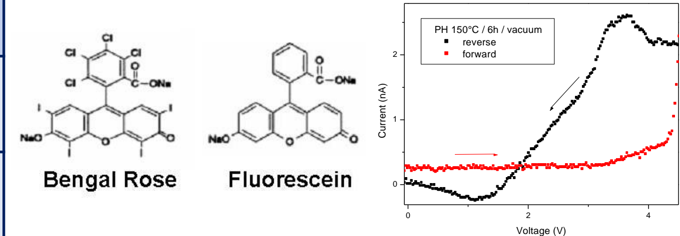
©2013 Micron Technology, Inc.

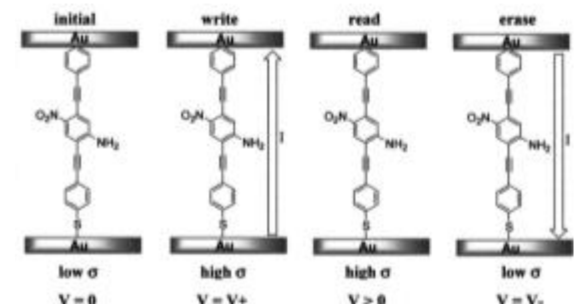
More NVM Concepts: Longer Term

A not exhaustive list…..

Nano-electromechanical memory (NEMM)	
Bi-stable nano-electromechanical switch	Electrostatic Attraction + Van der Waals Adhesion e.g. Nantero CNT memory, cantilever devices
Issues: scalability, endurance, sticking.	
Macromolecular (polymeric) memory	
Polymers with two resistivity states (bengal rose, fluoreiscine)	Switching between different redox states, charge trapping
Issues: material stability, mechanism not yet clear	
Molecular memories	
Single molecules in a cross-point array	Voltage Driven Change in electronic states in Redox
Issues: difficulty in handling single molecules, sensitivity to several parameters, addressing problems.	







©2013 Micron Technology, Inc.

Outline

- Solid State Memories: a success story
- A lot of alternatives:
  - Prototypal memories
  - New concepts
- From cell to memory
- Is there a winner?

©2013 Micron Technology, Inc.

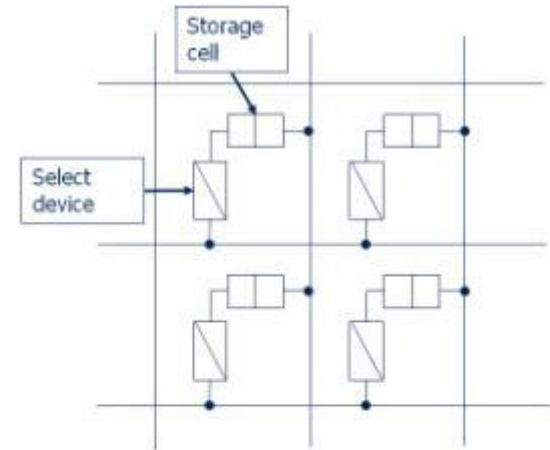
Memory as a system

- Two main functions to an electronic memory:
  - Data storage
  - Data retrieval
- Memories are organized in arrays
  - Storing and retrieval requires selecting the cell
  - Cell selection can be the major issue for different types of storage and is the main contributor to size of memory array.
- Cell selection is often the most critical issue for emerging memories.

©2013 Micron Technology, Inc.

Cell selector and array organization

- Cell selection within the array, and array characteristics can play a major role in the selection of memory technology.
- The selector allows a given memory cell in an array to be addressed for read or write.



- Key requirements for select device:
  - Strong non linear characteristic (switch).
  - In the On state: capability to handle the current required by the memory cell
  - In the Off state: very low leakage current (it limits max. size of array)
  - Compatibility with the process of the memory cell.
  - Small size.
  - Scalability.
- The requirements are especially critical for memories that require bipolar switching.

©2013 Micron Technology, Inc.

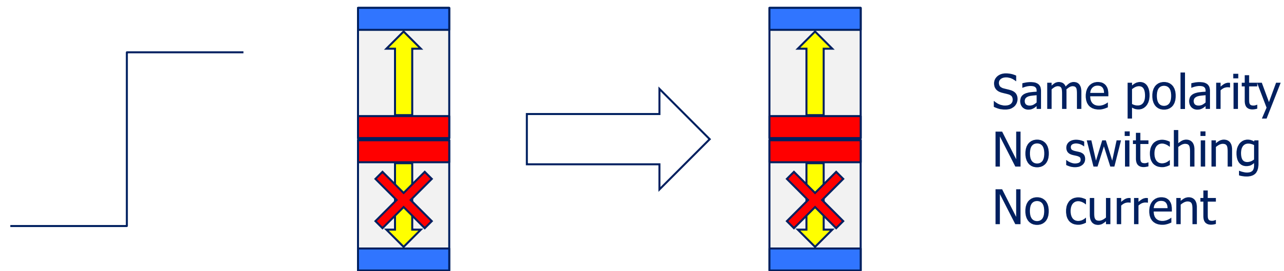
Selector types

- Transistor
  - MOS: easy to integrate, good performances, large size (DRAM, MRAM, FERAM)
  - Bipolar: more complex process, good performances, smaller size (PCM)
- Diodes (unipolar)
  - p-n in substrate: good performances, not for cross-point arrays
  - p-n in poly: can be integrated in back-end, poor Ion/Ioff
  - Schottky: low Ion density, poor Ion/Ioff
- Bipolar devices
  - Devices with strongly non-linear symmetrical I_V characteristics, e.g.
    - Metal-Insulator Transition switch (MIT), e.g. Mott transition switch:
    - Threshold Switch, e.g. Ovonic Threshold Switch
    - Mixed electronic and ionic conduction (MIEC)
  - Very little data available

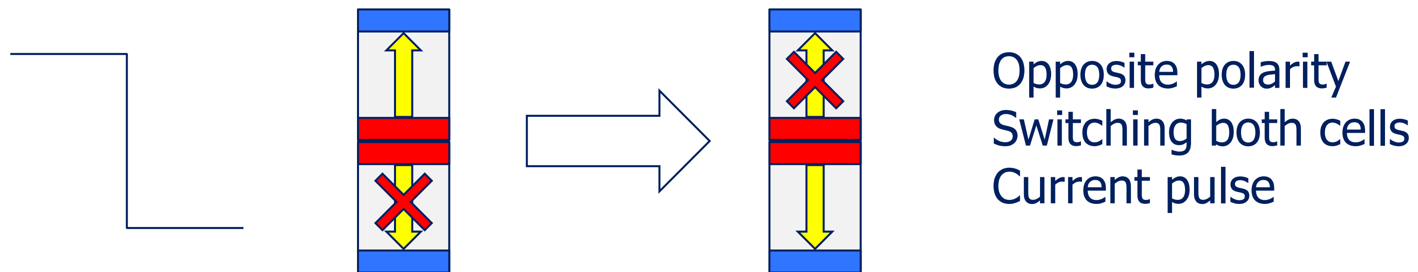
©2013 Micron Technology, Inc.

Complementary Resistive Switch

- An architectural solution
  - Two bipolar RRAM disposed back-to-back.
  - A voltage pulse generate s a current pulse only if polarity is such as to switch both devices.



Same polarity
No switching
No current



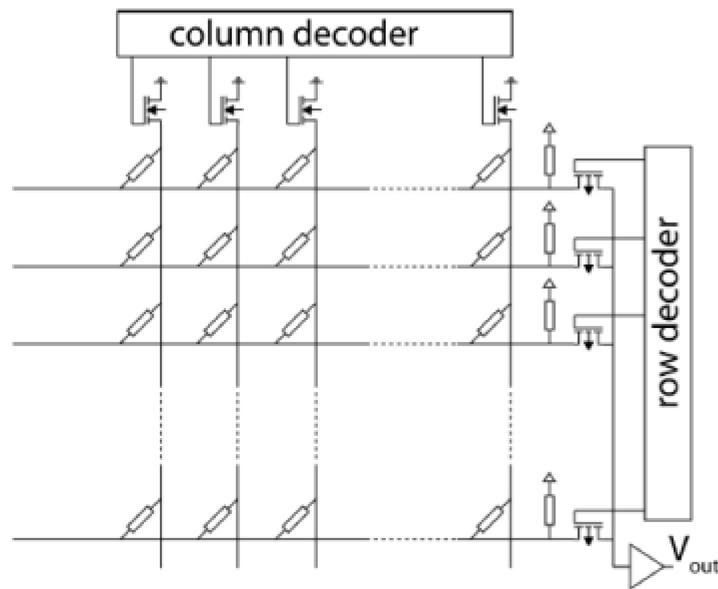
Opposite polarity
Switching both cells
Current pulse

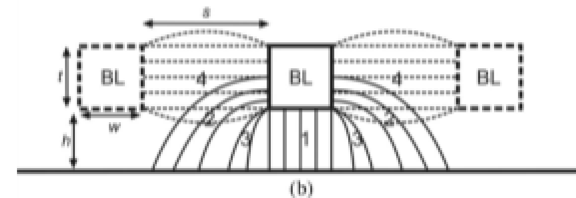
  - Destructive reading as in FeRAM

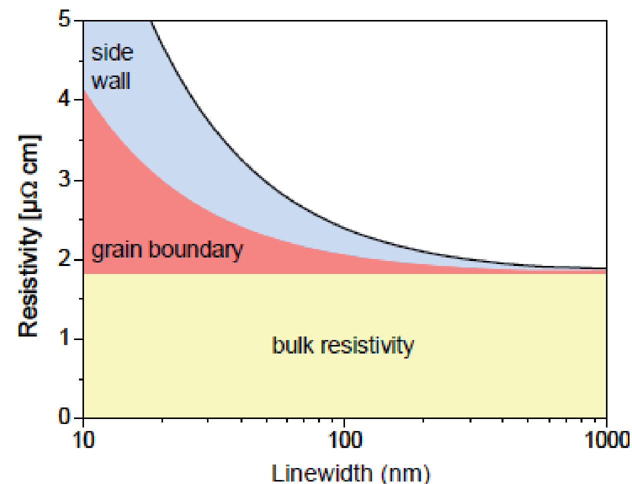
©2013 Micron Technology, Inc.

Real Arrays

- In real arrays, parasitic capacitance and resistance of interconnects cannot be neglected.
- Uniform scaling keeps capacitance constant but increases resistance.







- Also resistivity increases because of sidewall scattering.
- Interconnection delay and capacitance charging time can limit size of memory arrays.

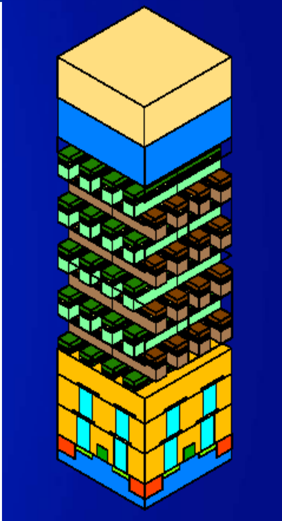
©2013 Micron Technology, Inc.

Outline

- Solid State Memories: a success story
- A lot of alternatives:
  - Prototypal memories
  - New concepts
- From cell to memory
- Is there a winner?

©2013 Micron Technology, Inc.

In summary


Source S.Lai

The ideal memory:

- High density
- Low power consumption
- Non-volatility
- Fast read/write/erase
- Random read/write access
- Endurance against write/erase cycles
- Scalability with low cost

and what is available (from ITRS ERD 2011)

	Prototypical (Table ERD3)			*Emerging (Table ERD5)*					
Parameter	**FeRAM**	**STT-MRAM**	**PCRAM**	**Emerging ferroelectric**	**Nanomechanical memory**	**Redox memory**	**Mott Memory**	**Macromolecular memory**	**Molecular Memory**
Scalability	red	yellow	green	yellow	red	green	?	?	green
MLC	red	red	green	red	red	green	?	yellow	red
3D integration	red	yellow	green	red	red	yellow	?	green	red
Fabrication cost	yellow	yellow	green	yellow	red	yellow	?	green	?
Endurance	green	green	yellow	green	red	green	yellow	red	?

Probably we have to settle for less: no 'universal memory', but several new concepts with interesting performances.

 ©2013 Micron Technology, Inc.

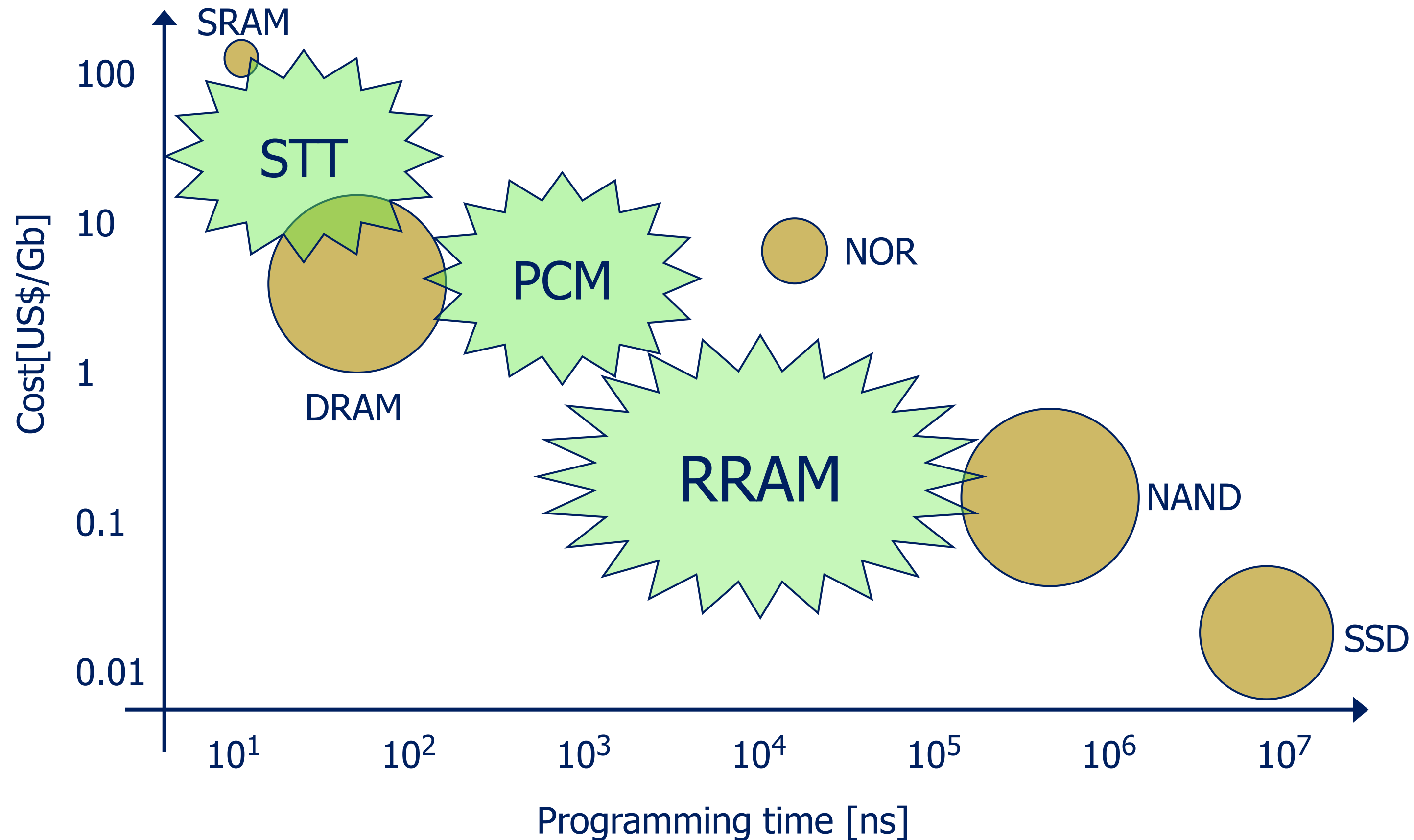
Emerging Memories

A few warnings

- Most of the emerging memories have low programming voltages/energy:
  - Low power dissipation, high programming speed, but
  - Low temperature stability
  - Low reading voltage ➡ low On/Off margin
  - Difficulty to have multilevel storage
  - High sensitivity to read disturbs
- Some concepts are not easily scalable (STT, FeRAM)
- Cross-point cell looks attractive, but:
  - Scaling depends on the availability of next generation lithography

Micron Confidential | ©2013 Micron Technology, Inc.

The competition arena



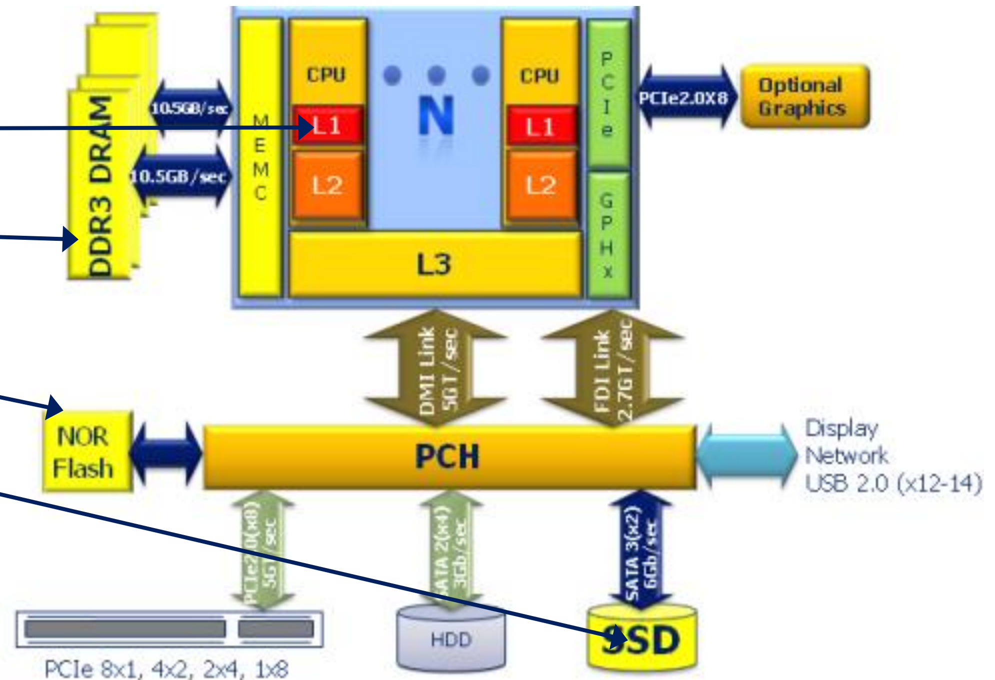
- New memories can fill the gaps between consolidated technologies
- Gain at system level.

©2013 Micron Technology, Inc.

Can we live with one memory?

Present PC architecture

- SRAM
- DRAM
- NOR Flash
- MLC NAND



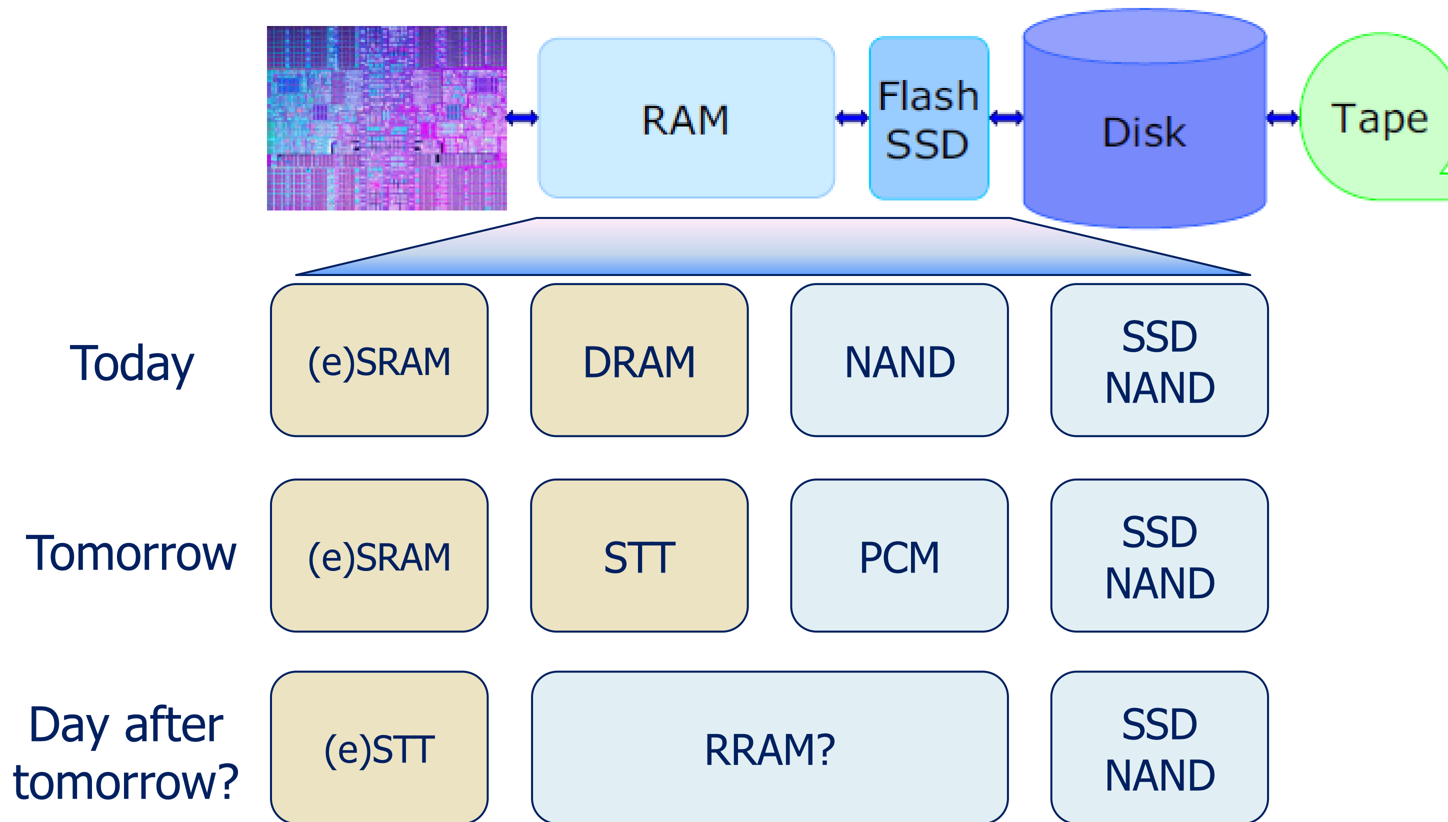
All types of available solid state memories are used.

Three strategy options for new memories:

- Compete with mainstream memory for cost (DRAM and NAND are hard to beat)
- Higher cost but replace more memory types (saving at system level)
- Find a niche in an intermediate position.

©2013 Micron Technology, Inc.

Computer architectures



©2013 Micron Technology, Inc.

A mixed future

- In the longer term the competition is still open between different alternative memories:
  - Choices on materials and architectures are needed to achieve critical mass.
  - Array and selector technology will be as important as the memory cell.
- Probably no "universal solution" but a differentiated landscape
- Memory systems combining different memory types in the same package will probably be the winning solution.

©2013 Micron Technology, Inc.