Fully Depleted Ge CMOS Devices and Logic Circuits on Si

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***Abstract*— We systematically studied Ge CMOS devices and logic circuits fabricated on a GeOI substrate, with the novel recessed channel and source/drain structures. Various channel lengths (L_{ch}) from 500 to 30 nm and channel thicknesses (T_{ch}) from 90 to 10 nm are implemented into the Ge CMOS devices and comprehensive geometry dependence analysis is carried out in terms of both L_{ch} and T_{ch}. With shrinking T_{ch}, the gate electrostatics are enhanced significantly but the on-state performance is found to be deteriorated simultaneously. It is also confirmed that Ge nMOSFETs are more sensitive to T_{ch} than pMOSFETs due to the phosphorus diffusion inside Ge. CMOS circuits, such as inverters, NANDs, NORs, and ring oscillators, are further investigated.**

***Index Terms*— CMOS, Ge, GeOI, logic circuits, MOSFET, recessed channel, recessed source/drain (S/D), scalability, SOI.**

I. Introduction

WHILE the semiconductor industry is struggling to extend the life of Moore's Law in nowadays, non-Si CMOS [1]–[3] is considered as one of the most important approaches to keep boosting the drive current and circuit speed with reduced supply voltage. High mobility channel materials, such as Ge [3] and III–V compounds [1], [4]–[6], are intensively studied for pMOSFETs and nMOSFETs, respectively. Whereas, the poor hole mobility greatly limits the applicability of III–V for manufacturable CMOS technology [1], [5]. Compared with III–V compounds, Ge is quite promising for post-Si CMOS technology [5], [7]–[11], due to its higher and near symmetrical carrier mobilities, large density of state, and relatively matured process. Meanwhile, Ge, as a material, has been widely employed in current Si CMOS manufacturing.

For the last decades, while great achievements have been realized in Ge pMOSFETs, the research of Ge nMOSFETs is significantly lagged behind due to the Fermi level pining [12], [13] in Ge interface. Recently, encouraging progresses have been obtained in Ge nMOSFETs research, in terms of electron mobility [14]–[16], contacts [13], [17]–[21], interface passivation [14], [22], [23], and device scaling [16], [17], [24], [25], making all Ge CMOS possible [17], [22], [26]–[29].

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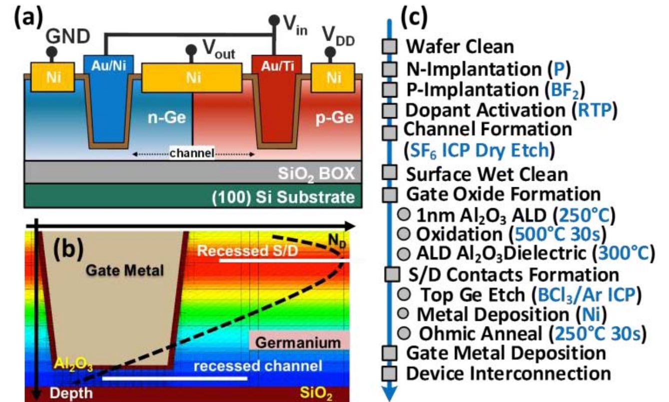

Fig. 1. (a) 2-D device schematic of a Ge CMOS inverter, showing the recessed channel and S/D. (b) Working principle of the MOSFETs in this paper. (c) Simplified fabrication process flow of the Ge CMOS.

As an extension of the previous conference reports [22], [27], [28], this paper thoroughly studies the Ge CMOS devices and circuits on Si by recessed channel and source/drain (S/D). Taking advantage of the dopant distribution profile inside Ge, the recess dry etching process can realize not only a heavily doped S/D for reduced contact resistance but also a lightly doped channel for enhanced gate electrostatics and better V_{TH} tuning. Benefited from the balanced carrier mobilities of Ge and well-engineered gate-stacks, the Ge nMOSFETs and pMOSFETs show near-symmetrical performance. Ge fully depleted CMOS devices and circuits with various L_{ch} from 500 to 30 nm and T_{ch} from 90 to 10 nm are comprehensively studied in terms of device characteristics in ON- and OFF-states for MOSFETs and switching characteristics for logic gates.

This paper is organized as follows. Section II explains the device structures and fabrication processes. Section III talks about the electrical characteristics of Ge pMOSFETs and nMOSFETs, in terms of the device performance and their dependences on device geometry. Section IV presents the Ge CMOS circuit's results, including inverters, NANDs, NORs, and ring oscillators. The scaling metrics of CMOS inverters and ring oscillators are also detailedly explored. A summary is concluded in Section V.

II. Experiment

Fig. 1(a) shows the 2-D cross-sectional cartoon of a Ge CMOS inverter, with recessed channel and recessed S/D depicted. As detailedly described in our previous report [30], the working principle of recessed channel and S/D is shown in Fig. 1(b). Higher doping in recessed S/D enables better contacts and lower doping in recessed channel delivers

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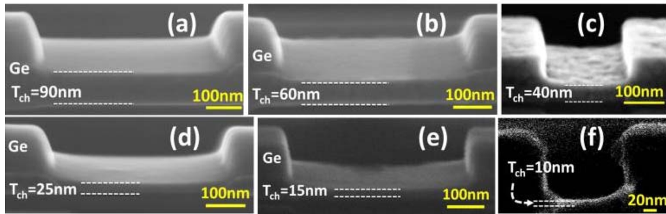

Fig. 2. Cross-sectional images of Ge recessed channels with channel thicknesses of (a) 90 nm, (b) 60 nm, (c) 40 nm, (d) 25 nm, (e) 15 nm, and (f) 10 nm.

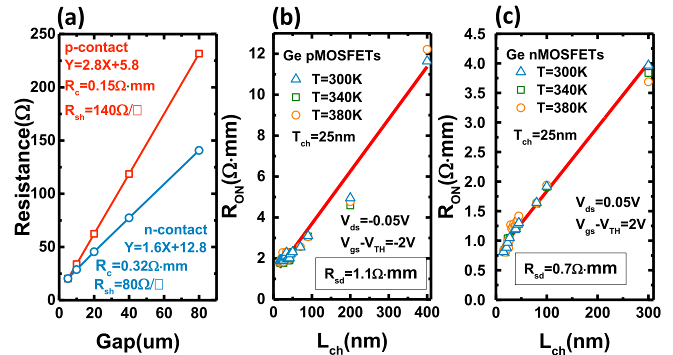

Fig. 3. (a) Typical TLM results of n and p contacts. ON-resistance dependence on L_{ch} of Ge (b) pMOSFETs and (c) nMOSFETs with T_{ch} of 25 nm at different temperatures of 300, 340, and 400 K. R_{sd} is extracted.

enhanced gate control. Fig. 1(c) briefly shows the fabrication process flow.

The device fabrication was carried out on a GeOI substrate. The GeOI substrate is fabricated by Smartcut technology and is composed of 180-nm lightly Sb doped n-type (100) Ge layer, 400-nm SiO_2 buried oxide (BOX) and a (100) Si handling wafer. At first, native oxide stripping was conducted by soaking in diluted 2% HF solution, followed by an organic clean by sequentially soaking in acetone, methanol, and isopropanol for 5/5/5 min. After the mesa isolation based on an SF_6 dry etching, ion implantation was carried out by using P ions for nMOSFET (5×10^{15}/cm^2 at 30 keV) and BF_2 ions for pMOSFET (4×10^{15}/cm^2 at 30 keV), respectively. Note that, both the S/D and gate region of MOSFETs were implanted. The P and BF_2 doping ions were then activated by a common ion activation in rapid thermal anneal at 500 °C for 1 min in N_2 ambient. Compared with our previous report, the simplified common ion activation here was carried out at lower temperature to reduce the thermal budget and the diffusion of P ions.

Next, in an inductive-coupled plasma dry etcher, SF_6 plasma was employed to partially etch away the Ge layer in the channel area, leaving a thin lightly doped recessed channel. The channel dry etching is calibrated to have a good aspect ratio and the etch rate is about 3 nm/s. By precisely controlling the dry etching time, different channel thicknesses of 90, 60, 40, 25, 15, and 10 nm were realized. The recessed channels with different T_{ch} values are shown in Fig. 2. To remove the surface damages caused by dry etching, a surface wet clean was then conducted by three times cyclically soaking in 2% HF solution and DI water, ending at third soaking in HF to maintain a hydrophobic surface. The rough edges on the Ge surface could be smoothened by the cyclic oxidation in DI water and etching in HF solution. Then, 1-nm atomic layer deposition (ALD) Al_2O_3 was deposited as the capping layer at 250 °C and the low temperature was adopted to reduce the formation of low-quality native oxide during the ALD process. GeO_x passivation layer was then formed by thermal annealing in pure O_2 ambient at 500 °C for 30 s. Next, the common ALD gate dielectric of 8- or 5-nm Al_2O_3 was deposited at 300 °C. After finishing the gate-stack, common recessed S/D dry etching was conducted by first striping the oxide covering the S/D region and then removing the top less doped Ge layer. The BCl_3/Ar-based recessed S/D dry etching is carefully calibrated to precisely control the etching rate to be around 15 nm/min. 100-nm Ni was then deposited as the contact metal, followed by a common ohmic anneal at 250 °C for 30 s in N_2 ambient. The metal gate was formed by 40/60-nm Ti/Au for pMOSFETs and 40/60-nm Ni/Au for nMOSFETs. Finally, devices were connected for CMOS logic gates.

In total, seven steps of electron beam lithography were employed in the layer patterning. Note that the MOSFETs in this experiment are majority carrier devices working in accumulation mode and their threshold voltages (V_{TH}) are relatively lower compared with the inversion mode devices, since extra gate bias is needed to deplete the channel. Resulted from this, high work-function metal of Ni/Au and low work-function metal of Ti/Au were employed in nMOSFETs and pMOSFETs, respectively, to tune V_{TH} for CMOS circuits. The equivalent-oxide-thicknesses (EOTs) are calculated using the physical thickness and dielectric constant of the gate dielectric, considering both GeO_x and the Al_2O_3 capping layer. The phyical thickness of GeO_x has been comfirmed to be 0.6 nm by TEM and that of Al_2O_3 is 6 or 9 nm, resulting in an esitmated EOT of 4.5 or 3 nm. More detailed C–V characterization is needed for accurate EOT calculation.

III. Ge CMOS Transistors

A. Device Characteristics

Fig. 3(a) shows the typical TLM results on n- and p-Ge. Low R_c of 0.32 and 0.15 $\Omega \cdot$mm and sheet resistance (R_{sh}) of 80 and 140 Ω/□ are achieved on n- and p-type Ge contacts, respectively. Fig. 3(b) and (c) shows the ON-resistance (R_{ON}) versus L_{ch} of pMOSFETs and nMOSFETs with T_{ch} of 25 nm at different temperatures. The S/D series resistance (R_{sd}) is extracted to be 0.7 and 1.1 $\Omega \cdot$ mm for nMOSFETs and pMOSFETs. Although R_c of p-type Ge contact is smaller than that of n-type Ge contact, R_{sd} of pMOSFETs is larger than that of nMOSFETs because of a factor of two larger R_{sh}. R_{sd} shows negligible dependence on temperature, indicating the dominance of the tunneling current in the ohmic contacts.

Fig. 4 shows the transfer characteristics of ultrathin body (UTB) Ge pMOSFETs and nMOSFETs, fabricated on the common substrate with 10-nm T_{ch} [shown in Fig. 2(f)] and different channel lengths from 100 to 50 nm at V_{ds} of ∓0.05, 0.5 and 1 V. Both of the two sets of devices show good I_{ON}/I_{OFF} ratio of around 10^5. For bulk Ge MOSFETs, high

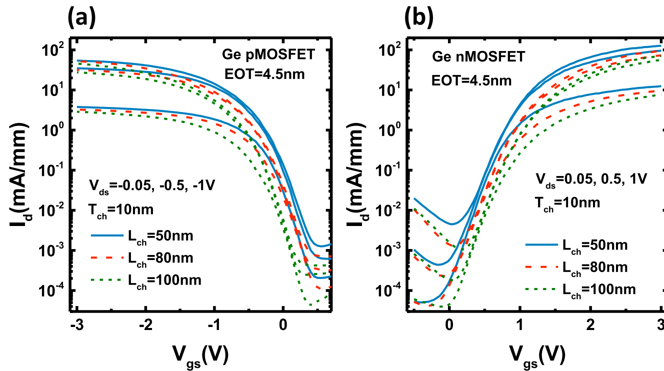

Fig. 4. Transfer curves of 10-nm T_{ch} Ge MOSFETs with 4.5-nm EOT and different L_{ch} values of 100, 80, and 50 nm, at various $|V_{ds}|$ of 0.05, 0.5, and 1 V. (a) pMOSFETs. (b) nMOSFETs.

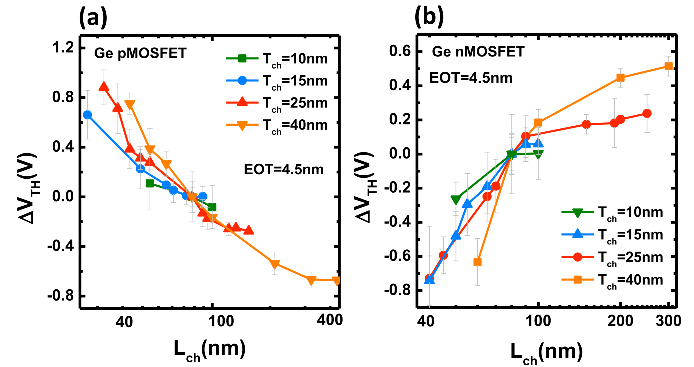

Fig. 5. ΔV_{TH} [$V_{TH} - V_{TH}(L_{ch} = 80$ nm)] relationships with L_{ch} of Ge planar MOSFETs with T_{ch} of 10, 15, 25, and 40 nm and same EOT of 4.5 nm. (a) pMOSFETs. (b) nMOSFETs.

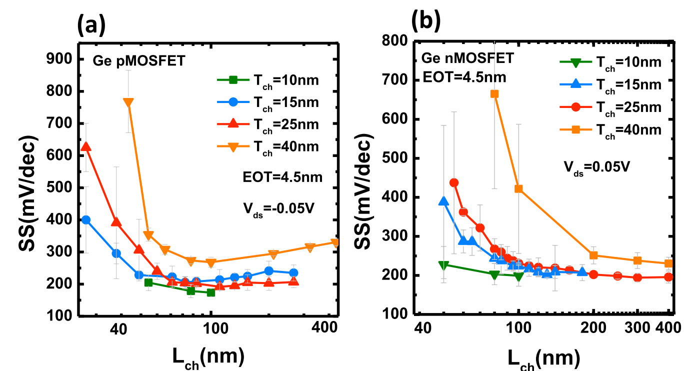

Fig. 6. SS relationships with L_{ch} of Ge planar MOSFETs with T_{ch} of 10, 15, 25, and 40 nm and the same EOT of 4.5 nm at low V_{ds} of $\mp$0.05 V. (a) pMOSFETs. (b) nMOSFETs.

device I_{ON}/I_{OFF} ratio is very challenging due to the junction leakage current to body caused by the defects in nonoptimized S/D implantation and the punch through effect in short channel case, especially for Ge nMOSFETs, due to the high diffusivity of P ions [18], [20], [31], [32]. The good device I_{ON}/I_{OFF} ratio can be mainly attributed to the excellent gate control from the UTB channel and the BOX layer in the GeOI substrate, which blocks the leakage path from drain to body. Because of the UTB channel structure, the MOSFETs still maintain good OFF-state current of below 10 nA/μm at high V_{ds} bias of 1 V for scaled channel lengths of 50 nm.

Meanwhile, with smaller channel length, the OFF-state current increases slightly and the transfer curves shifts positively and negatively for nMOSFETs and pMOSFETs, respectively, which is commonly known as the V_{TH} roll off due to short channel effects (SCEs). With shrinking L_{ch}, both subthreshold swing (SS) and drain induced barrier lowering (DIBL) also increase but the DIBL still remains below 100 mV/V, further confirming the excellent SCE immunity in the UTB channel. Note that the SS of these devices is acceptably large, due to thick gate oxide with an EOT of 4.5 nm used.

Comparing the two types of devices, nMOSFETs show about two times higher drain current than pMOSFETs, which can be attributed to mobility difference between electrons and holes inside Ge and the different series resistances in nMOSFETs and pMOSFETs. The carrier mobilities are extracted to be 35 and 10 cm^2/Vs for electrons and holes at N_{inv} of 5×10^{12} cm^{-2}, respectively, through split-C–V measurement over long channel devices with 10-μm L_{ch}. Meanwhile, in our previous report [28], the R_{SD} values of nMOSFETs and pMOSFETs are extracted to be 0.7 and 1.1 $\Omega \cdot$ mm.

B. L_{ch} Dependence of Device Characteristics

To further study MOSFET's behavior related to the device geometry, channel length scaling study is carried out first.

Fig. 5 shows the V_{TH} dependence on L_{ch} of Ge planar pMOSFETs and nMOSFETs with different T_{ch} values of 40, 25, 15, and 10 nm. Since these devices were not fabricated in parallel, to exclude the influence from process variations and different gate metals used, ΔV_{TH} in relative to V_{TH} of 80-nm L_{ch} devices with the same T_{ch} is used in the comparison. The scale bars reflect the standard deviations of results obtained in around 20 measured devices at each point. With decreasing L_{ch}, both pMOSFET and nMOSFET show clear trend of V_{TH} roll-off. It is found that shrinking T_{ch} in planar devices could effectively reduce the V_{TH} roll-off from 1 to 0.2 V, proving better gate electrostatics in thinner channel devices. For fully depleted MOSFETs, reducing channel thickness could physically decrease the thickness of depletion region [33], thus, relieving the requirement of minimum channel length for an acceptable V_{TH} shift and providing better device scalability. By scaling gate dielectric and employing 3-D channel structure, smaller V_{TH} shift would be expected [34].

SS scaling metrics of the same sets of devices in Fig. 5 are shown in Fig. 6. The SS first remains the same and then increases exponentially with reduced L_{ch}. In shorter channel device at fixed V_{ds} bias, the S/D transverse electrical field increases, resulting in loss of the controllability over the carriers of the vertical electrical field induced by gate bias. Thus, SS degrades with smaller channel lengths. Enhancing the vertical electrical field by using thinner channels could sufficiently improve the gate control, as proved by reduced SS in smaller T_{ch} devices.

Fig. 7 shows the DIBL scaling metrics for pMOSFETs and nMOSFETs. Similar to that of SS, DIBL first keeps as a constant but then increases exponentially with decreasing L_{ch},

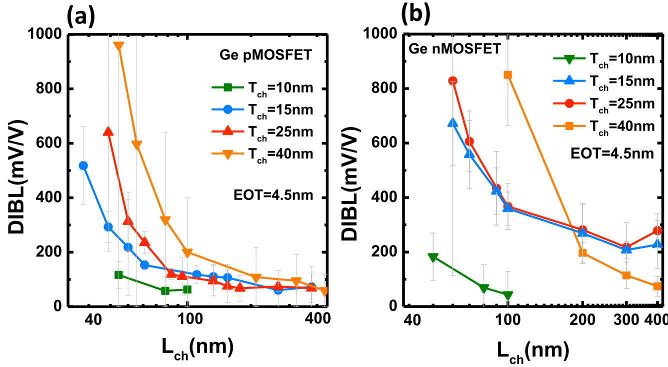

Fig. 7. DIBL relationships with L_{ch} of Ge planar MOSFETs with T_{ch} of 10, 15, 25, and 40 nm and the same EOT of 4.5 nm. (a) pMOSFETs. (b) nMOSFETs.

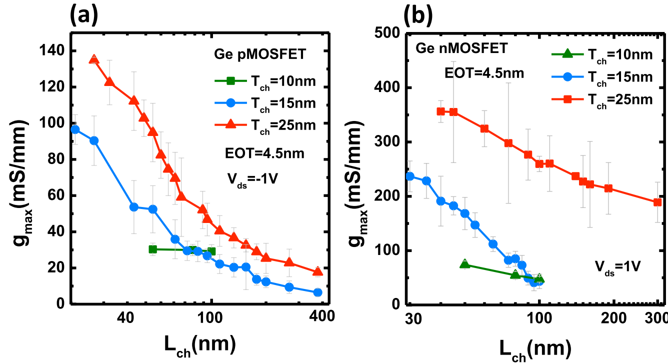

Fig. 8. Maximum transconductance relationships with L_{ch} of Ge planar MOSFETs with T_{ch} of 10, 15, and 25 nm and the same EOT of 4.5 nm at low V_{ds} of ∓ 1 V. (a) pMOSFETs. (b) nMOSFETs.

which is also related with SCEs. By thinning down the channel, DIBL could be effectively suppressed. It is also worth noting that L_{ch} at which DIBL starts to rise rapidly is reduced with smaller T_{ch}, pointing out better channel length scalability in thinner channels.

For the ON-state performance of the devices, Fig. 8 shows the maximum trans-conductance (g_{max}) scaling metrics of planar MOSFETs with 10-, 15-, and 25-nm T_{ch} at high V_{ds} of ∓ 1 V. g_{max} increases almost linearly with reduced L_{ch}, due to reduced channel resistance. Meanwhile, it is quite interesting that g_{max} degrades a lot with thinner channel. This can be mainly attributed to mobility degradation and reduced cross-sectional area for the accumulation channel. It is widely reported [35], [36] that the carrier mobility is deteriorated in thinner channel or smaller channel sizes due to severer surface roughness scattering and phonon scattering. What is more, especially for Silicon-on-Insulator (SOI)-based devices, stronger self-heating effect in thinner channel could also reduce the mobility [37], [38], since the heat dissipation from channel to substrate is more limited. Meanwhile, the g_{max} difference between pMOSFETs and nMOSFETs is mainly caused by the mobility difference, and different series resistances resulted from the nonoptimized common ion activation process during CMOS fabrication.

C. T_{ch} Dependence of Device Characteristics

Besides the channel length dependence study, the influences of channel thickness on device behaviors are also investigated.

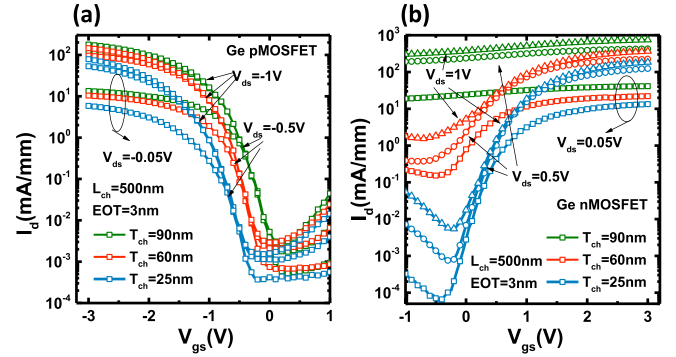

Fig. 9. Transfer curves of 500-nm L_{ch} Ge MOSFETs with 3-nm EOT and different T_{ch} values of 90, 60, and 25 nm, at various $|V_{ds}|$ of 0.05, 0.5, and 1 V. (a) pMOSFETs. (b) nMOSFETs.

Fig. 9 shows the transfer curves of 500-nm L_{ch} Ge MOSFETs with an EOT of 3 nm and different T_{ch} values of 90, 60, and 25 nm at various V_{ds} bias. Similar to the channel length dependence, in thinner channels, the curves shift negatively and positively for pMOSFETs and nMOSFETs, respectively. However, it is found that the nMOSFETs are much more sensitive to T_{ch} than the pMOSFETs. The I_d–V_{gs} curves of pMOSFETs just shift with almost no I_{ON}/I_{OFF} ratio and SS degradation and the DIBL is also negligible due to the long channel length of 500 nm. While, with thicker channels, the curves of nMOSFETs show much larger V_{TH} shifts with rapid I_{ON}/I_{OFF} ratio, SS and DIBL degradations. Especially, the 90-nm T_{ch} nMOSFET has almost no gate modulation to the drain current, indicating very weak gate control. This prominent distinction existing between pMOSFET and nMOSFET could be due to that the doping profile is different for n- and p-type ion implantation in Ge. As mentioned earlier, the n-type P ions inside Ge is much more diffusive than the p-type BF_2 ions [13], [31], which is one of the key challenges in realizing well behaved Ge nMOSFETs. As a result, large amount of p ions would diffuse deep into the channel area in the thermal process during device fabrication, leading to higher channel doping density in nMOSFETs than pMOSFETs. It will further reduce the maximum depletion width (W_{dm}) of the channel, making the gate harder to deplete the whole conducting Ge channel layer.

In other words, W_{dm} would be much larger in pMOSFETs than nMOSFETs at the same T_{ch}. For fully depleted MOSFETs with $T_{ch} < W_{dm}$, both p- and n-type devices' gate control should be similar, as proved by the 25-nm T_{ch} ones. Whereas, with increasing T_{ch} from 25 to 90 nm, W_{dm} of pMOSFETs would increase slightly with almost no change to the gate control but W_{dm} would decrease rapidly in nMOSFETs due to the fast rising P concentration, leading to W_{dm} reaching down to T_{ch} or even smaller and deteriorating gate electrostatics, as confirmed by the 60- and 90-nm T_{ch} ones.

Figs. 10 and 11 show g_m–V_{gs} and output curves of the same set of devices in Fig. 9. On the condition of same T_{ch} and L_{ch}, nMOSFETs show better ON-state performance because of the higher electron mobility. For pMOSFETs, the 90-nm T_{ch} device has the largest g_{max} due to higher majority carrier concentration induced by higher doping.

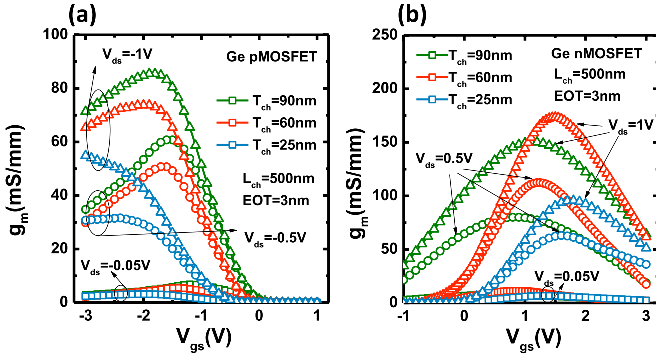

Fig. 10. g_m versus V_{gs} curves of 500-nm L_{ch} Ge MOSFETs with 3-nm EOT and different T_{ch} values of 90, 60, and 25 nm, at various $|V_{ds}|$ of 0.05, 0.5, and 1 V. (a) pMOSFETs. (b) nMOSFETs.

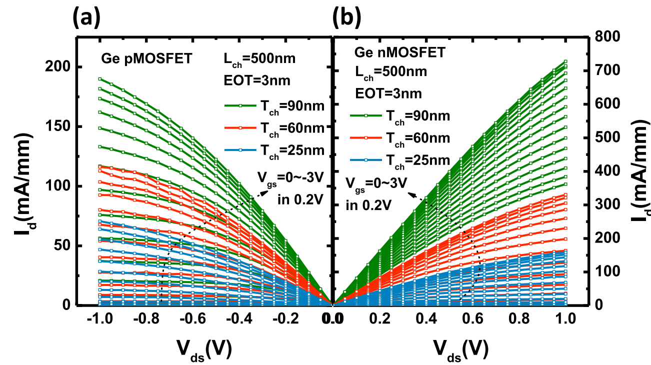

Fig. 11. Outptut curves of 500-nm L_{ch} Ge MOSFETs with 3-nm EOT and different T_{ch} values of 90, 60, and 25 nm with $|V_{gs}|$ from 0 to 3 V in 0.2 V step. (a) pMOSFETs. (b) nMOSFETs.

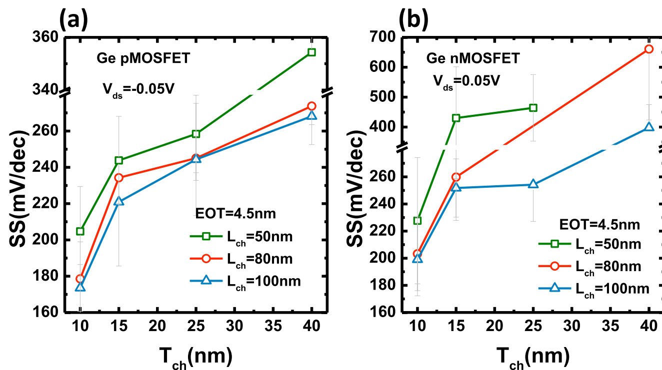

Fig. 12. SS relationships with T_{ch} of Ge planar MOSFETs with L_{ch} of 50, 80, and 100 nm and the same EOT of 4.5 nm. (a) pMOSFETs. (b) nMOSFETs.

However, for nMOSFETs, g_{max} of the 90-nm T_{ch} is smaller than that of the 60-nm T_{ch} device. This can be partly explained by: 1) larger OFF-state leakage and loss of gate control in thicker channels and 2) the fact that the P ion concentration in the 90-nm T_{ch} channel is much higher than that of the 60-nm T_{ch} channel, leading to lower electron mobility caused by impurity scattering.

To further clarify the explanation above, channel thickness dependence is investigated. Fig. 12 shows the SS relationships with T_{ch} of Ge MOSFETs with an EOT of 4.5 nm and different L_{ch} values of 50, 80, and 100 nm at V_{ds} of $\mp$0.05 V. The SS is reduced by shrinking T_{ch}, in a near linear

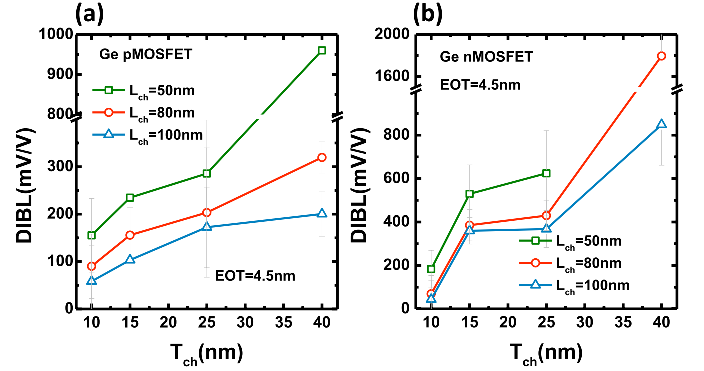

Fig. 13. DIBL relationships with T_{ch} of Ge planar MOSFETs with L_{ch} of 50, 80, and 100 nm and the same EOT of 4.5 nm. (a) pMOSFETs. (b) nMOSFETs.

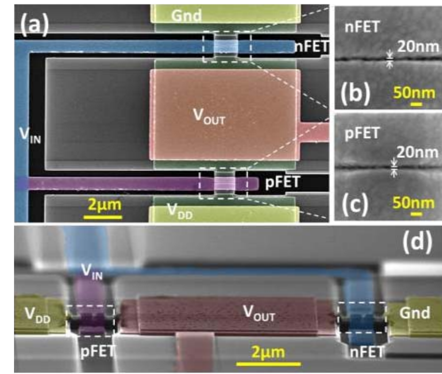

Fig. 14. (a) Top–down view of a fabricated Ge CMOS inverter with the smallest channel length under the SEM. (b) and (c) Zoom-in images of the gate areas in the CMOS inverter in (a), the channel length is 20 nm. (d) Bird's eye view of a CMOS inverter under SEM.

relationship, due to better gate control explained previously. For T_{ch} below 25 nm, the SS of two types of devices keeps at a low range and pMOSFETs have slightly better SS, but not very significantly. Nevertheless, for T_{ch} higher than 25 nm, nMOSFETs show much more prominent SS degradation, which is almost twice higher than that of pMOSFETs, in great consistence with the results shown in Fig. 9. Furthermore, in Fig. 13, the DIBL relationships with T_{ch} for the same sets of devices also confirm the explanation on doping concentration difference. Similar to that of SS, DIBL remains at low ranges in both nMOSFETs and pMOSFETs for T_{ch} < 25 nm but much more rapidly rises in nMOSFETs when T_{ch} increases to 40 nm.

IV. Ge CMOS Circuits

Since both nMOSFETs and pMOSFETs have been realized on the same GeOI substrate, they are further interconnected for functional CMOS circuits.

A. Ge CMOS Logic Gates

Fig. 14(a) shows the false-colored SEM image of a Ge CMOS inverter with the smallest 20-nm L_{ch} in top–down view. For the circuit structure, the gates of the pMOSFET and nMOSFET setting on SiO_2 isolation region (the dark area)

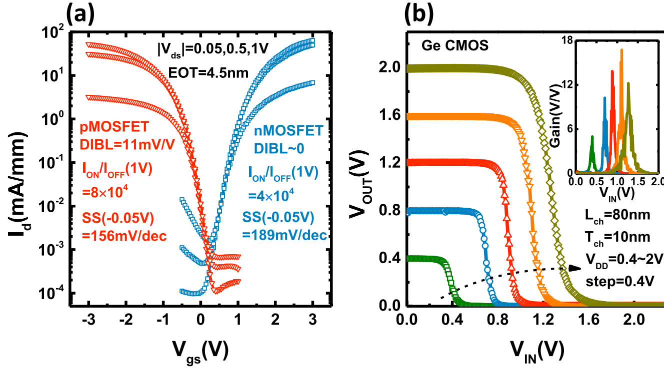

Fig. 15. (a) I_d–V_{gs} curves of the pMOSFET and nMOSFET in a CMOS inverter with T_{ch} of 10 nm and L_{ch} of 80 nm at $|V_{ds}| = 0.05$, 0.5, and 1 V. (b) Voltage transition curves of the same CMOS inverter in (a) at various V_{DD} from 0.4 to 2 V. Inset: extracted voltage gain relationship with V_{IN}.

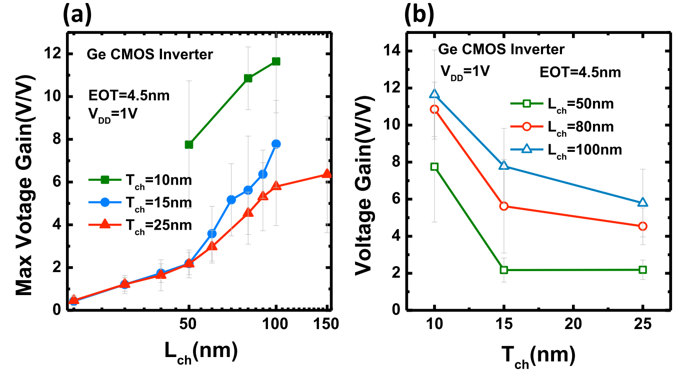

Fig. 16. (a) I_d–V_{gs} curves of the pMOSFET and nMOSFET in a CMOS inverter with T_{ch} of 10 nm and L_{ch} of 80 nm at $|V_{ds}| = 0.05$, 0.5, and 1 V. (b) Voltage transition curves of the same CMOS inverter in (a) at various V_{DD} from 0.4 to 2 V. Inset: extracted voltage gain relationship with V_{IN}.

are connected as the input electrode and drains of the two are connected as the output electrode with the sources of pMOSFET and nMOSFET are used as the supply and ground electrode, respectively. The enlarged gate areas with L_{ch} of 20 nm are shown in Fig. 14(b) and (c). Fig. 14(d) shows the tilted SEM image of a Ge CMOS inverter, clearly showing the small notch on the gate metal caused by channel recessing.

Benefited from the most balanced carrier mobility in Ge and carefully engineered gate-stacks, Fig. 15(a) shows the transfer curves of the pMOSFET and nMOSFET in a typical 80-nm L_{ch} and 10-nm T_{ch} CMOS inverter, showing near-symmetrical performance. Thanks to the ultrathin channel, low DIBLs are obtained on both of the devices with 11 mV/V for the pMOSFET and a near-zero value for the nMOSFET and the SSs are 156 and 189 mV/decade at $|V_{ds}|$ of 50 mV. It is further confirmed by the large I_{ON}/I_{OFF} ratio of around 10^5 at high V_{ds} bias of 1 V. Fig. 15(b) shows the output voltage (V_{OUT}) versus input voltage (V_{IN}) curves of the same CMOS inverter in Fig. 15(a), showing a steep voltage transition. The voltage gains $[\Delta(V_{OUT})/\Delta(V_{IN})]$ are further extracted and given in Fig. 15(b) (inset). The maximum voltage gain is 17 V/V at V_{DD} of 1.6 V, delivering a 70% increase over previously reported results [5] with the same L_{ch} but a larger T_{ch} of 25 nm.

The device geometry dependences of Ge CMOS inverters are also investigated. Fig. 16(a) shows the maximum voltage gain scaling metrics of Ge CMOS inverters with T_{ch} of 25, 15, and 10 nm at $V_{DD} = 1$ V. With shrinking L_{ch}, the maximum voltage gain is reduced, which is also related with the SCEs. As determined by inverter's working mechanism, the voltage gain strongly depends on the output conductance (g_d) of pMOSFET and nMOSFET as inverter's components. Smaller g_d gives higher voltage gains. Due to the DIBL induced by SCE, higher g_d would be expected in shorter channel MOSFETs, resulting in reduced voltage gains in CMOS inverters. By enhancing the gate electrostatics through employing thinner channels, the DIBL would be suppressed, thus reducing g_d and improving the voltage gains. Fig. 16(b) shows the maximum voltage gain relationships with channel thickness of inverters with various L_{ch} at V_{DD} of 1 V.

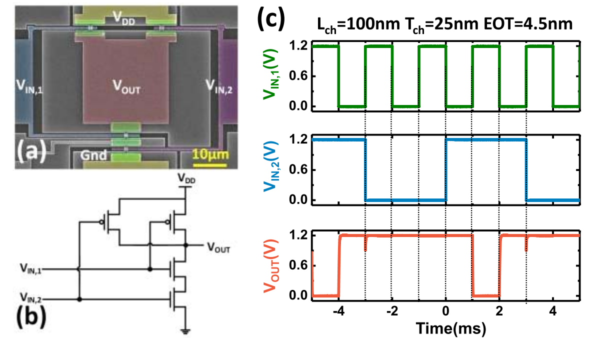

Fig. 17. (a) Top–down false-colored SEM image of a NAND logic gate. (b) Circuit diagram of the NAND logic gate. (c) Response signals of a 100-nm L_{ch} NAND logic gate with 25-nm T_{ch} and 4.5-nm EOT to two square-wave input signals in the time domain.

The 10-nm T_{ch} channel delivers more than 200% improvement over the 25-nm T_{ch} one and this improvement is even more prominent in the shortest channel devices with 50-nm L_{ch}.

Other logic gates, such as NAND and NOR, are also realized and analyzed. Fig. 17(a) and (b) shows the top–down view of a fabricated NAND logic gate under SEM and its circuit diagram. The output signal of a 100-nm L_{ch} NAND gate with 25-nm T_{ch} and 4.5-nm EOT responding to two input signals at a supply voltage of 1.2 V is shown in Fig. 17(c). Four combinations of input states 1 1, 0 1, 1 0, and 0 0 are used and the output signal shows sharp transitions. Fig. 18(a) and (b) shows the top-down view of a fabricated NOR logic gate under SEM and its circuit diagram. The output signal of a 100-nm L_{ch} NOR gate is provided in Fig. 18(c), with same testing conditions applied in the NAND gate.

B. Ge CMOS Ring Oscillators

Because of the well calibrated and stabilized fabrication processes, the MOSFETs in this paper have a decent performance and high yield, enabling the operation of CMOS ring oscillators, which requires good consistency of working CMOS inverters with high voltage gain. A fabricated nine-stage ring oscillator is shown in Fig. 19(a) and (b) shows the output signal of a Ge ring oscillator with L_{ch} of 50 nm at V_{DD}

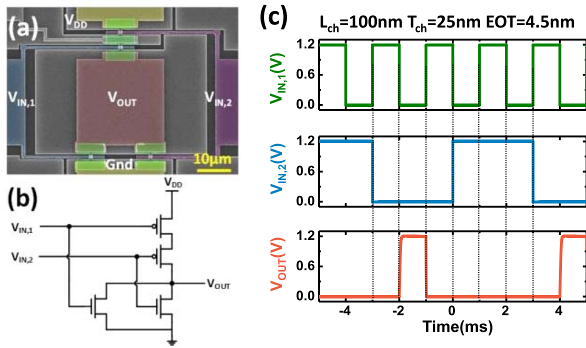

Fig. 18. (a) Top–down false-colored SEM image of a NOR logic gate. (b) Circuit diagram of the NOR logic gate. (c) Response signals of a 100-nm L_{ch} NOR logic gate with 25-nm T_{ch} and 4.5-nm EOT to two square-wave input signals in the time domain.

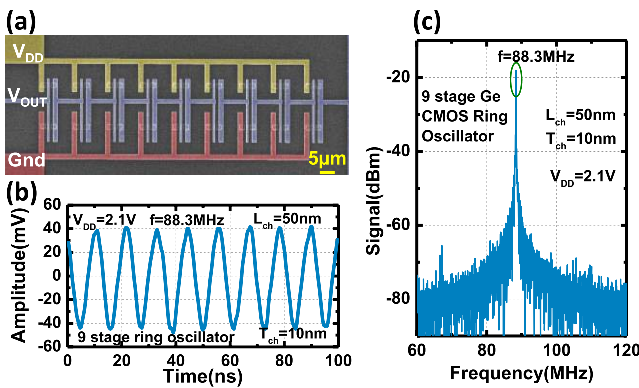

Fig. 19. (a) Top–down false-colored SEM image of a fabricated nine-stage ring oscillator. (b) Output signal of a nine-stage ring oscillator with 50-nm L_{ch} at V_{DD} of 2.1 V. (c) Oscillator power spectrum of the same ring oscillator in (b), indicating a oscillation frequency of 88.3 MHz.

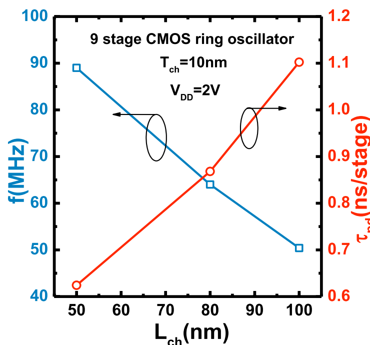

Fig. 20. Oscillation frequency and propagation delay per stage relationships with L_{ch} of the nine-stage ring oscillators in this paper at V_{DD} of 2 V.

of 2.1 V in the time domain. The power spectrum of the same device is shown in Fig. 19(c), showing an oscillation frequency of 88.3 MHz. The propagation delay (τ_{pd}) is calculated to be 629 ps by $\tau_{pd} = 1/2\ nf_0$, where n is the number of stages and f_0 is the oscillation frequency. The maximum oscillation frequency obtained is 102 MHz (not shown). Note that the demonstrated oscillation frequency is still far below the state-of-the-art Si CMOS technology, due to the large series resistance and fringing capacitance resulted from the non-self-aligned process at the device level, and large parasitic capacitance from the test pads for measurement. Basically, it is a physical demonstration, which cannot reflect the potential performance of Ge ring oscillators. The oscillation frequency could be further improved by reducing the gate to S/D overlaps to decrease parasitic capacitance and reducing the S/D resistance to increase the drive current.

To further examine the scalability of the circuits, nine-stage ring oscillators with different channel lengths are shown in Fig. 20. The oscillation frequency increases and τ_{pd} decreases with smaller L_{ch} at the same V_{DD}. It could be easily understood: with shrinking L_{ch}, the drive current of inverters increases but the gate capacitance decreases. Thus, the gate delay resulted from the charging and discharging of the fan-out capacitor is reduced. Hence, the speed of the circuit gets improved.

V. Conclusion

We experimentally study the Ge CMOS devices and logic circuits with the recessed channel and S/D structures. Various channel lengths and channel thicknesses are implemented into the device fabrication. Detailed investigation on L_{ch} and T_{ch} dependences of device behaviors are conducted in terms of MOSFET OFF-state performance, such as V_{TH} roll off, SS, and DIBL, g_{max} as the ON-state performance, maximum voltage gain for CMOS inverters and oscillation frequency for CMOS ring oscillators. This paper provides valuable evidences of Ge as a promising candidate to replace Si in future's low-power and high-speed CMOS logic applications.

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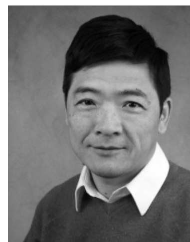

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