Fast14™ Technology Overview

Synopsis

Developed for use with standard CMOS processes, Fast14™ Technology provides breakthrough, multi-GHz performance with the productivity associated with industry-standard, semi-custom, static design tools. Three years of development have resulted in completion of Intrinsity's Fast14 Technology. This technology solves the productivity and manufacturing problems of dynamic circuits. Fast14 Technology consists of a combination of four patented elements:

Unique clocking style — Addresses race conditions associated with dynamic logic.
1-of-N Dynamic Logic (NDL™ family) — A new dynamic logic family that dramatically reduces the number of gate delays required for a given function.
Wire Twizzling™ process — Reduces noise in routed signals.
EDA tools suite — Fully automates the implementation of dynamic circuits.

Fast14 Technology has been used to design and produce a test chip, which demonstrates high yields at 2.2 GHz. The chip contains a pair of mini-CPUs each containing a 64-bit register file, two 32-bit ALUs, a sequencer, scan control, a 2 KB instruction RAM and a 2 KB data RAM. Analysis of the test silicon indicates a process margin and voltage margin similar to static circuits, proving the suitability for robust volume production of products incorporating Fast14 Technology.

Fast14 Technology derives its name from the atomic number of silicon, which directly translates to "Fast Silicon".

Introduction

Ultra-high-speed circuits are normally created through the use of dynamic logic. Historically, dynamic logic is accompanied by a host of undesired side effects in terms of noise sensitivity, clocking control, signal race conditions, and semiconductor process sensitivity. Additionally, the requirement of synchronizing latches or flip-flops reduces the amount of time in a cycle that is available for performing computations. The difficulties in designing processors with dynamic logic (both productivity and manufacturing yields) have relegated dynamic circuits to highly-specialized, hand-tuned circuits in desktop and server processors.

Fast14 Technology removes these impediments. At the same time, it requires a small fraction of the design resources or development time needed for best-in-class dynamic circuits. The technology uses standard wafer fabrication processing, yielding up to a three-fold improvement in speed with comparable wafer fabrication processes.

There are two essential phases in the generic digital design process. In the first phase, EDA tools are used to create the design. The second phase uses a different set of EDA tools to check the design for correctness and design goal compliance. In today's digital designs, both phases use tools from EDA industry leaders to develop "static" circuits. Intrinsity replaced the majority of the tools necessary to create static circuits with its own proprietary tools that create NDL™ circuits. Industry-standard tools are then used to check the resulting design.

Dynamic Logic History

Dynamic logic was the main method for designing early microprocessors and calculator chips in the 1970s. The style was principally used to eliminate DC power in NMOS and PMOS circuits. The processors were relatively simple by today's standards, but required careful handcrafting or very slow clocking styles to successfully design for data versus clock race conditions. Small teams of engineers handcrafted every transistor, wire, and clock to maximize yield for an acceptable, but narrow, process window and voltage range.

With the advent of CMOS fabrication processes in 1980, fundamental events changed the landscape for dynamic circuits:

- CMOS static circuits inherently eliminated the DC power issues of NMOS and PMOS circuits.
- Static circuits did not have the dynamic data versus clock race conditions, eliminating the need for careful, handcrafted design.
- Static circuits operated over a much wider process window and voltage range than dynamic circuits.

These factors resulted in improved manufacturing costs, more predictable design cycles and most importantly the advent of Electronic Design Automation (EDA) tools. EDA tools brought tremendous productivity improvements and time-to-market predictability to new products. These improvements far outweighed the one major disadvantage...the speed loss associated with abandoning the use of dynamic circuits.

With the impact of CMOS processes, the challenge of using dynamic circuits has plagued every processor design team. DEC's Alpha was one example of processor performance that took the world by surprise in 1992, but over time the lack of productivity and marginal manufacturing windows proved the design style to be unsustainable.

Today, only very small sections of the highest performance desktop and server processors use dynamic circuits, requiring tremendous efforts to achieve robust, high-yielding products.

The Challenge

To enable EDA tools to automate and unleash the performance potential of dynamic circuits required finding solutions to challenging technical barriers:

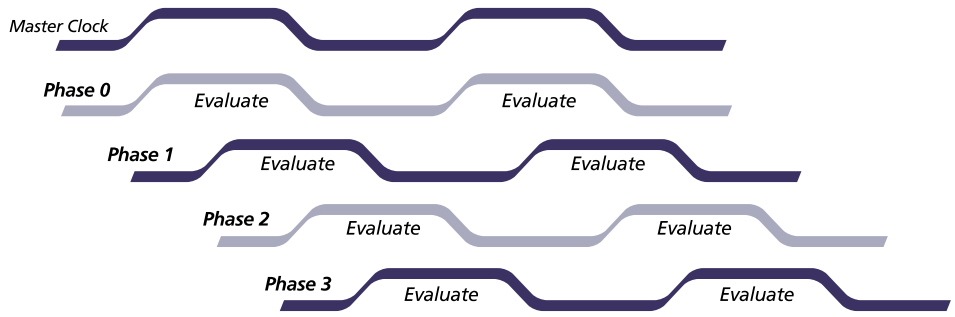
- Address data versus clock race conditions through EDA tools.
- Removal of noise-induced functional failures by minimizing signal coupling to quiet neighbors.
- Support of manufacturing and debug SCAN techniques used widely with static CMOS.
- Automation of circuit design and transistor and wiring layout, with no manual intervention.
- Manufacturing tolerances and yields competitive with static designs.

Intrinsity's $Fast_{14}$ Technology has been developed over the past three years to solve these dynamic circuit problems and consists of a combination of four patented elements:

- Unique clocking style - Addresses race conditions associated with dynamic logic.
- 1-of-N Dynamic Logic (NDL™ family) - A new dynamic logic family that dramatically reduces the number of gate delays required for a given function.
- Wire Twizzling™ process - Reduces noise in routed signals.
- EDA tools suite - Fully automates the implementation of dynamic circuits.

Clocking: Solving Race Conditions

Intrinsity's Fast14 Technology effectively addresses the data versus clock race conditions of classic dynamic circuits through a patented clocking technique and new EDA tools. With a four phase, uniform overlapping clock circuit and straightforward logic rules, the clocking scheme removes the need for latches from the logic. This improves overall speed and facilitates the development of EDA tools that can safely, predictably, and quickly generate a multi-GHz circuit.



NDL™ Family

1 of N Dynamic Logic, or NDL family, is a brand new logic family that reduces the number of gate delays needed to accomplish the same logic function. Fewer gate delays enable higher speed circuits.

NDL gates are a dynamic logic family where data path and control logic use radix encoded signals.

For example, to represent the values 0 through 3:

- Static logic traditionally encodes the values into two bits (wires). In a clock cycle, zero, one, or two of the wires may switch.
- Classic (dual-rail) dynamic logic uses four wires, as it requires the complement of each bit. In a clock cycle, two wires will switch.
- NDL gates also use four wires, but in a clock cycle at most only one wire will switch.

The use of NDL gates results in fewer gate delays to perform the same function versus static or classic dynamic logic. Another benefit is that fewer transistors and wires are switching, saving nearly half of the power versus classic dynamic logic.

STATIC LOGIC
2 bits
2 wires
0.1 or 2 switching

A1	A0	Result
0	0	0
0	1	1
1	0	2
1	1	3

DUAL RAIL DYNAMIC LOGIC
2 bits
4 wires
2 switching

A1	$\overline{A1}$	A0	$\overline{A0}$	Result
0	0	0	0	Pre-Charge
0	1	0	1	0
0	1	1	0	1
1	0	0	1	2
1	0	1	0	3

1 of 4 NDL™ LOGIC
2 bits
4 wires
1 switching

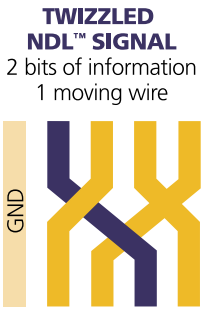
A3	A2	A1	A0	Result
0	0	0	0	Pre-Charge
0	0	0	1	0
0	0	1	0	1
0	1	0	0	2
1	0	0	0	3

While the gates are dynamic, they can operate at slow clock speeds and maintain state when the clock is stopped. NDL gates used for scan chains do not add any gate delays to the logic speed path.

A large portion of Intrinsity Inc.'s patent portfolio covers this new logic family.

Wire Twizzling™ Process

The Wire Twizzling process is a patented method for routing NDL signals, reducing coupling noise and improving signal speed with no area penalty. Intrinsity can automatically determine wire length, predict noise, and route signals to meet a noise specification. The NDL family uses primarily a 1-of-4 signal convention, which means that in a bundle of four wires, only one wire will transition in a clock period, while the other three wires act as a virtual ground. Using the Twizzling process, the wires half way through a long route effectively share noise to different neighbors, reducing destructive signal noise by a factor of four compared to random routing.



EDA Tools For Dynamic Logic

Intrinsity has written a suite of tools that automate the creation phase for dynamic logic. The tools integrate well into standard EDA tools used by the industry in the check phase for compliance to design targets (timing, power, noise, reliability).

While inventing the concepts behind Fast14 Technology took only a few months, the EDA tools creation was a monumental effort. A substantial effort spanning three years was required to develop tools that could effectively be used to deliver predictable and repeatable results.

The technology is applicable to a wide range of products, ranging from desktop/server products to embedded processors and ASICs. Fast14 Technology is proven in a standard CMOS fabrication processes, requiring no special processing technologies.

Additionally, the EDA flow allows the inclusion of non-performance-critical, traditional RTL/synthesis-based logic to be integrated on the same die.

Intrinsity Dynamic Circuit EDA Tools

Creation	Check and Analyze
• NDL™ logic entry • Floor planner • Noise avoidance wire estimator • At-speed, intelligent dynamic circuit design • NDL™ cell generation • NDL™ bundle routing • Block & global routing (3rd party and Intrinsity)	• Layout Extraction • Logic verification check • Layout check • Speed analysis • Noise analysis • Electromigration analysis • IR Drop analysis
Intrinsity EDA Tools	**Third Party Standard EDA Tools**

Fast14 Technology Test Chip

On August 13, 2001, Intrinsity announced the results of a technology test chip utilizing Fast14 Technology. The test chip project proved all aspects of Fast14 Technology:

- Productivity and predictability of dynamic logic EDA tools suite.
- Patented technology claims and applicability to products.
- Robustness of technology in terms of yield and manufacturability

The test chip included a pair of mini-CPUs each containing a 64-bit register file, dual 32-bit ALUs, a sequencer, scan control, a 2KB instruction RAM and a 2KB data RAM. Fabricated in a standard 0.18 µm CMOS process, the device exhibited high yields at 2.2 GHz and 1.75 volts. A white paper discussing the details of the test chip results are available.

Products Using Fast14 Technology

Intrinsity is disclosing initial details of the first two commercial products utilizing Fast14 Technology. The products are based on the industry standard MIPS® Instruction Set Architecture and will deliver the highest performance processors for embedded systems. Both products are scalable from 1.5 GHz to 4 GHz, nearly 4 times the clock speed of embedded processors on the market today. Products based on Fast14 Technology will meet the power expectations of high performance embedded systems by delivering products tuned for 5 W-15 W of power.

FastMATH™ is the world's first Adaptive Signal Processor™ architected to meet the demands of today's real-time, adaptive algorithm designs. FastMATH consists of a native matrix and vector math unit coupled with a MIPS architecture-based RISC processor. FastMATH provides the performance of ASICs with the advantages of software programmability.

FastMIPS™ is the highest performance general-purpose processor for embedded markets. For high-performance embedded systems, FastMIPS will deliver an ideal system solution where performance is demanded and power is important.

For more information on Intrinsity, visit our Web site at **www.intrinsity.com** or contact us at (512) 421-2100.