TIA TELECOMMUNICATIONS SYSTEMS BULLETIN

Application Guidelines for TIA/EIA-485-A

TSB-89-A
(Revision of TSB-89)

January 2006

TELECOMMUNICATIONS INDUSTRY ASSOCIATION

The Telecommunications Industry Association
represents the communications sector of

Electronic Industries Alliance

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(From Standards Proposal No. 3-3615-RV1, formulated under the cognizance of the TIA TR-30.2 Subcommittee on DTE-DCE Interfaces).

Published by

Printed in U.S.A.

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Application Guidelines for TIA/EIA-485-A

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FOREWORD

This document was prepared as part of the A revision to TIA/EIA-485 to separate applications information that was interspersed in the standard and to embellish it. As the working group proceeded, it became clear the effort would have grown into a book in an attempt to cover all of the application aspects. The results are necessarily a compromise between thoroughness and time spent. It is the hope of this group that this bulletin provides sufficient guidance to apply TIA/EIA-485-A and to add to this document in the future.

1 Introduction

This engineering publication provides guidelines for applying circuits complying with TIA/EIA-485-A, referred to as 485 hereafter, to form a balanced multipoint data bus. The versatility of the 485 electrical standard covers a wide variety of data interchange applications all of which this publication cannot cover. The intent is to provide basic design guidelines of the physical layer.

In applying the drivers and receivers defined in 485, the reader should keep several important considerations in mind. The first consideration is the actual configuration of the system with regard to the number of drivers and receivers, the operating speed of the system, the method of interconnecting the equipment, and the system margin. The implementer should consider performance capabilities of the equipment in establishing the margin allotments. The referencing standard should specify these requirements.

2 Glossary of terms and definitions

Balanced is a description of two circuits that have identical electrical properties such that when driven with signals of equal magnitude but in opposite directions there is no ac common-mode energy in the two circuits (see **Differential mode**).

Common-mode Voltage is one-half of the vector sum of the voltages between each conductor of a balanced interchange circuit and ground. The common-mode voltage is the sum of ground potential difference, driver common-mode output voltage (*generator offset voltage*), and longitudinally coupled noise.

Common-Mode is the shared signal component of two or more signals to a common reference point. Mathematically, the common-mode signal is the arithmetic mean of the signal amplitudes.

Data Signaling Frequency is $\frac{1}{2T}$, where T is the minimum unit interval and uses the units Hz (Hertz). (It is generally the largest magnitude frequency component of the signal's Fourier series representation.)

Data-Signaling Rate is $\frac{1}{T}$ where T is the minimum unit interval and uses in the unit bit/s (bits per second). Its value is also the same as the clock frequency in a single-edge sampled synchronous transmission.

Data Transfer Rate is the number of desired bits of data received per unit time. It may be different from the data-signaling rate, which uses the same units.

Differential Mode is a signaling mode that uses one of a driven signal pair as the zero potential reference.

Distributed-Parameter circuit is a model of an electrical circuit with large physical dimensions with respect to the wavelength of the input signal.

Electromagnetic Compatibility (EMC) is the modern term describing the absence of conducted and radiated emissions or susceptibility that exceed specified limits or cause system performance degradation.

Electromagnetic Interference (EMI) replaced RFI in the 1950's and presently describes conducted and radiated emissions that are above specified limits or cause system performance degradation.

Eye Pattern is a measure of the data signal transmission path quality using an overlay pattern of random data signal transitions.

Generator (See **Line Driver**)

Ground Potential Difference is the difference between the signal ground potential between the active generator and a receiver of an interchange circuit.

Longitudinally Coupled Noise Voltage is an unwanted voltage coupled inductively or capacitively between any two points along the balanced interconnecting cable.

Hysteresis is the difference between the positive- and negative-going receiver input voltage thresholds.

Input Sensitivity is the minimum input signal voltage that a receiver detects.

Input Threshold Voltage is the input voltage that causes a receiver to change state.

Inter-Symbol Interference is the time displacement of a state transition due to a new wave (subsequent signal) arriving at the receiver site before the previous wave has reached its final value.

Jitter is the time variation of a significant time instance of a signal.

Line Driver is the component of an interchange circuit that is a source of the transmitted signal (used interchangeably with *generator*).

Line Receiver is the component of an interchange circuit that provides for the detection of interchange circuit signals and indicates the logical state of the bus to the receiving equipment.

Line Transceiver is a line driver and receiver with driver outputs and receiver inputs connected together at the bus interface.

Lumped-Parameter Circuit is a model for an electrical circuit with small physical dimensions with respect to the wavelength of the input signal.

Multidrop is a data bus structure that has one transmitting and two or more receiving connections.

Multipoint is a data bus structure that has two or more transmitting and any number of receiving connections.

Node is a point at which conductors from two or more circuit elements join.

Off-state Output is an output of a line driver that does not actively drive the normal operating load to a minimum level for either logical state. (Commonly referred to as a *high-impedance state*)

Party line (See **Multipoint**)

Point-to-Point is a data bus structure that has one line driver and one receiver on it.

Propagation Delay is the time it takes for the output of a circuit to respond to an input signal.

Radiated Emissions (RE) are emissions that originate within equipment or its associated cabling and transmit unguided to the external environment via electromagnetic waves.

Radiated Susceptibility (RS) is an undesirable equipment response that appears on the equipment output because of electromagnetic waves being impressed upon the equipment.

Radio Frequency Interference (RFI) (See **EMI**)

Significant Time Instance is the time when a time-varying signal achieves a level or range of levels that signifies a logic state change.

Single-ended Mode is a signaling mode that uses a single driven line.

Skew is a time difference between significant instances of different signals or the time difference between significant time instances on the same signal (sometimes referred to as *pulse skew*).

Transmission Line is an electrical model for a distributed parameter interchange circuit.

Unbalanced is a signaling method that is not balanced. (Also known as **Single-ended Mode**)

Unit Interval is T, where T is the minimum time interval that can occur between any desired logic state changes in a binary signal (the signal pulse width).

3 System definition

3.1 General description

A 485 bus will normally consist of multiple communication controllers in separate chassis and power domains connected via shielded twisted-pair cabling. There may be one or more signal pairs in the cable each having multiple drivers, receivers, or transceivers depending upon the application requirements. The signal return path is through the earth ground connection at each chassis or through a wired ground in the cable. It is generally undesirable to have both return paths.

Cable routing is generally a daisy chain (direct run from chassis to chassis) although some systems may allow stub cabling from a main backbone cable. Each signal pair will normally have a resistor, equal to the characteristic impedance between the pair, at the extreme ends of the backbone.

3.2 Applications

Applications requiring an economical rugged interconnection between two or more computing devices employ 485 drivers, receivers, or transceivers in data transmission circuits. The low-noise coupling of balanced signaling with twisted-pair cabling and the wide common-mode voltage range of 485 allows data exchange at data-signaling rates up to 50 Mbit/s or to distances of several kilometers at lower rates.

Note- The data-signaling rate of 50 Mbit/s is attainable with the semiconductor technology currently available. The upper bound for the data-signaling rate is constrained only by the switching speeds of the drivers and receivers and the characteristics of interconnecting media.

Numerous higher-level industry standards reference 485 including:

ANSI X3.129-1986, Intelligent Peripheral Interface (IPI)
ANSI X3.131-1993, Small Computer Systems Interface-2 (SCSI-2)
ANSI X3.277:1996, SCSI-3 Fast-20 Parallel Interface (Fast-20)
ANSI X3.253:1995, SCSI-3 Parallel Interface (SPI)
BSR/ASHRAE 135P (BACnet)
DIN 19245: Profibus, Process Field Bus
DIN/ISO 8482: German version of ISO/IEC 8482
DIN66348/2: Interface and control for serial transmission of measurement data, start-stop-operation, 4-wire bus (Often called DIN-Bus)
IEEE 1118 1990, Microcontroller System serial Control Bus (aka BitBus)
ISO 11519: Road vehicle - Low-speed serial data communication Part 1: Low-speed controller area network (CAN) (Comment: Modified RS485 interface), Part 6: Vehicle area network (VAN) (Comment: Modified RS485 interface)
ISO 9316: Information processing systems - Small Computer System Interface (SCSI)
SAE J1587 Nov. 1990, Joint SAE/TMC Electronic Data Interchange Between Microcomputer Systems in Heavy Duty Vehicle Applications
SAE J1708 Oct. 1990, Serial Data Communications Between Microcomputer Systems in Heavy Duty Vehicle Applications
SAE J1922 Dec 1989, Powertrain Control Interface for Electronic Controls used in Medium and Heavy Duty Diesel On-Highway Applications

These standards cover data interface applications as divergent as high-end computer systems to the drive trains of bulldozers.

3.3 Environment

As with any system design, designers should consider the natural and induced environmental conditions the system could encounter during operation. While conditions of wind, rain, temperature, motion, shock, etc. need consideration, the designer should give particular attention to the electromagnetic environment. The most common failure of 485 circuits is due to electrical overstress to the line circuit bus pins. This is more likely as the transmission distance and coupling with the environment is increased. The drivers and receivers conforming to 485 can operate with a common-mode voltage between -7 V and 12 V.

3.4 System diagrams

Figure 1 through Figure 7 schematically shows example signal paths that connect up to five nodes with 485 transceivers. Any number or combination of drivers, receivers, or transceivers are allowed as long as the electrical load presented to a driver does not exceed its drive capability as described in the following sections.
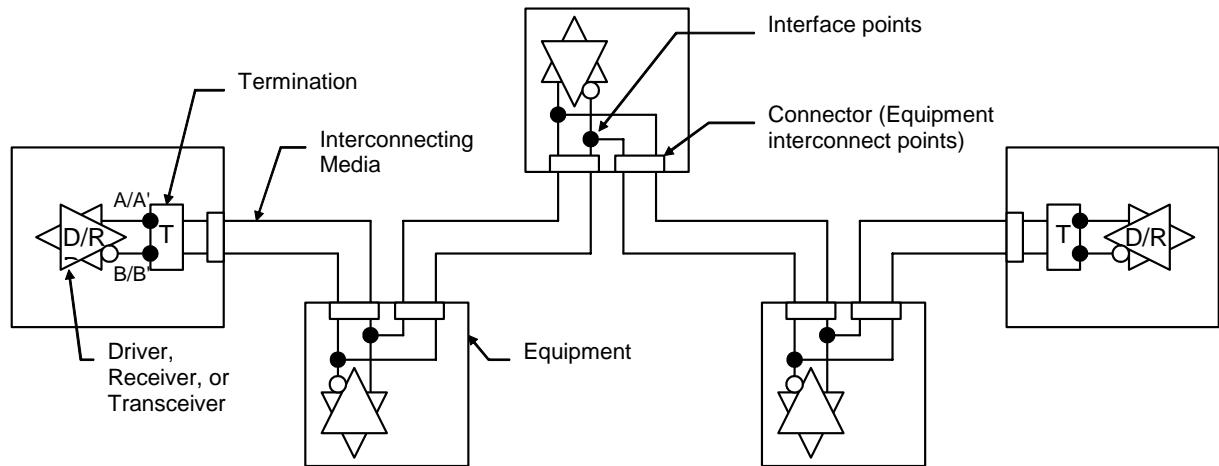
Figure 1 - General 485 system configuration.
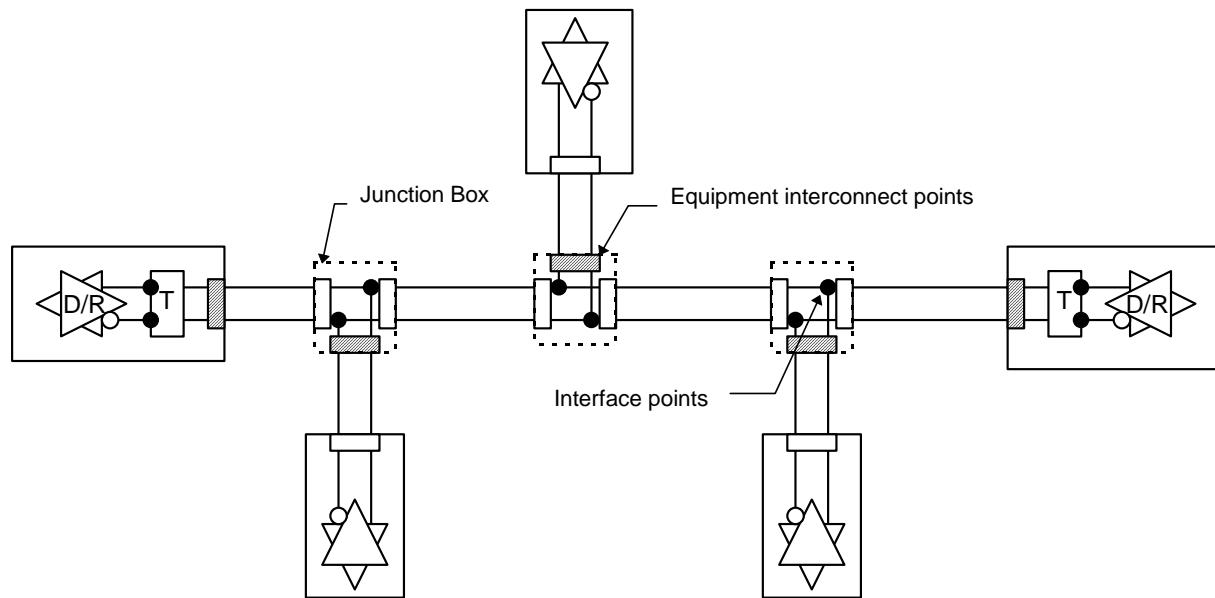
**Figure 2 - 485 bus with stub cables off a main backbone cable.**
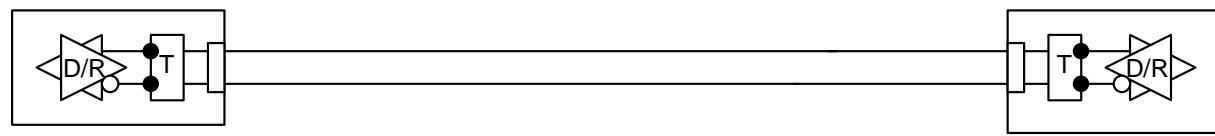
Figure 3 - Point-to-point connection.
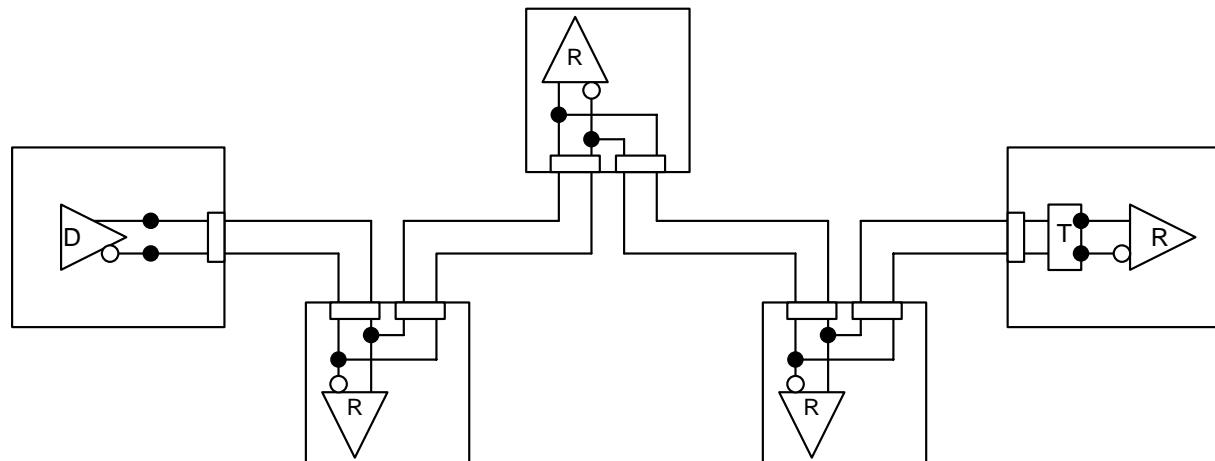
Figure 4 - One driver and multiple receivers (multidrop).
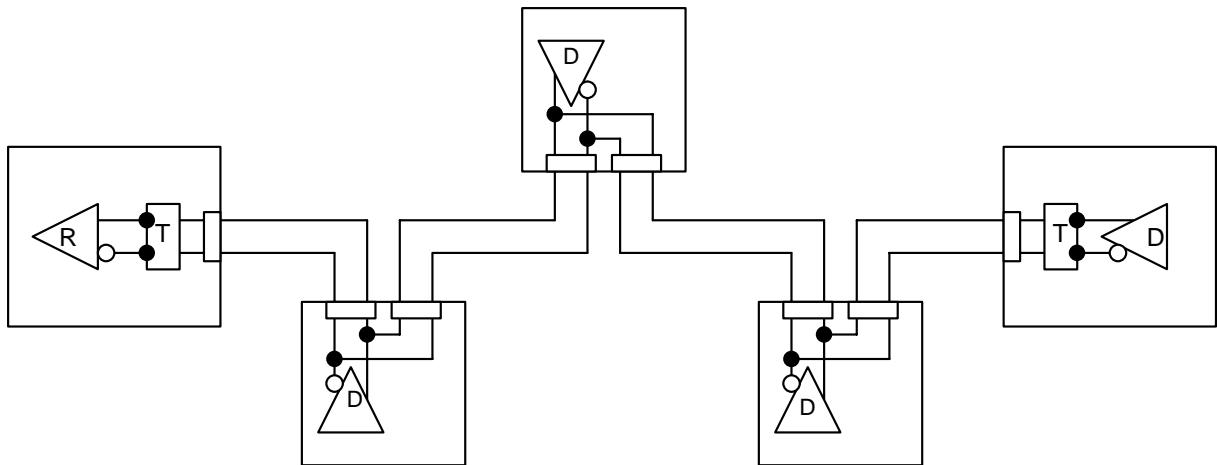
Figure 5 - One receiver and multiple drivers.

Equipment
interconnect point
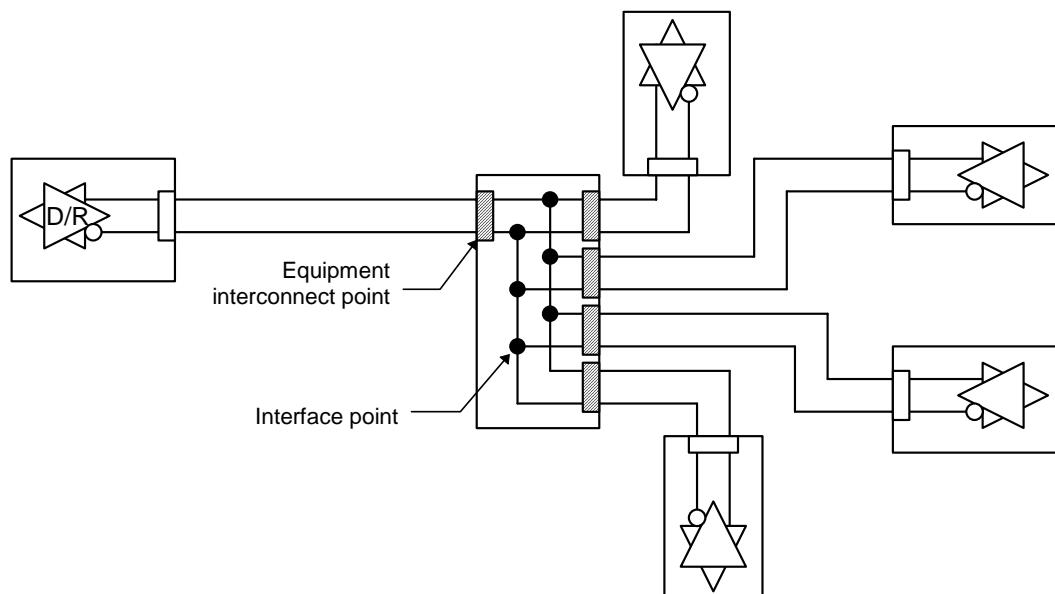
Interface point

Figure 6 - Star configuration (not recommended).

Unpopulated
card slot
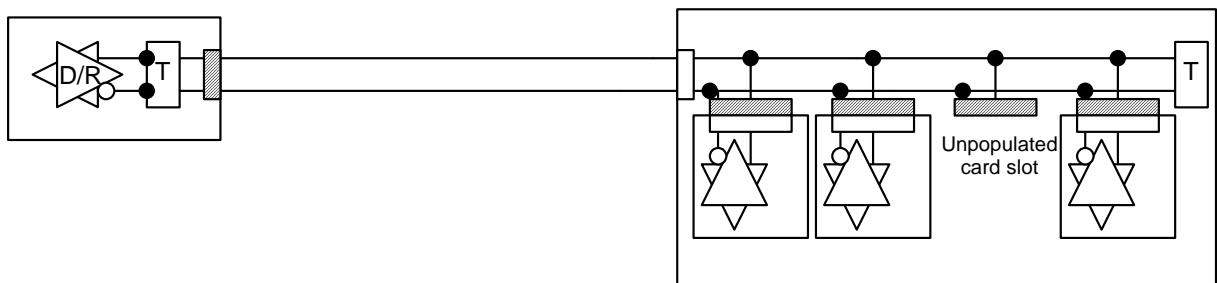
Figure 7 - 485 backplane example.

3.5 Interface definition

There are two interfaces of concern to the system designer, the physical and the electrical interface. The physical interface is the *equipment interconnect* and usually a connector. In some systems, there will be a number of connectors in the signal path and the location of the interconnect point becomes indistinct. In this case, any connector can be designated as the equipment interconnect point as long as the electrical characteristics to either side of that point meets the requirements for a driver, receiver, transceiver, or the interconnect media.

The electrical interface is at the *interface points* and is the point at which the distributed-circuit-parameter effects on the 485 signals are no longer negligible. In other words, the media side of the interface point appears electrically more as a transmission line and the equipment side more as lumped circuit elements. The interface point is any point along the conducting path to or from the bus where the signal propagation delay is less than 1/2 of the 10%-to-90% transition time of the input signal. The interface point may not coincide with or beyond (from the equipment's perspective) the equipment interconnection. The challenge to the designer, in most cases, is to make it do so.

4 Electrical Characteristics

4.1 Interconnecting media

The interconnecting media is that part of the system that connects the interface points and includes the cables, connectors, and termination. Practically any interconnecting media can form a 485 bus. The quality of the media used for the data channel primarily determines the usefulness of the bus. As such, when designing a 485 bus, the designer should give sufficient effort in selecting the proper media for the speed, distance, and noise environment of the application. While the actual configuration of the interconnection is application dependent, the remainder of this section provides some guidelines that may be helpful in the choice of the interconnecting means.

4.1.1 Characteristic impedance

The characteristics of the drivers to be connected and the length of the bus determine the proper electrical signal model for the interconnection. In the most general application of 485, the interconnecting media of a 485 bus is a distributed-parameter circuit and, in its simplest form, as a lossless transmission line. In this case, the interconnecting media electrically appears as a resistance at the interface points. The resistance value is the characteristic impedance (Z_0) of the line and is a function of its physical construction and electrical properties.

The value of Z_0 is important for two reasons; it determines the first-step signal level at the interface point and the nominal impedance value for line termination. A standard 485 bus can accommodate a media Z_0 as low as 120Ω with full common-mode loading and voltage range. A 485 driver is capable of driving lower differential characteristic impedance with compromise to the common-mode loading or common-mode voltage range (see 4.2.1).

Cable manufacturers measure Z_0 for cables intended for data transmission and normally provide this value in the cable specifications. Table 1 provides the characteristic impedance of several example cables. For very high-speed transmission, look for further

characterization of the cable in terms of Z_0 variation with frequency, uniformity along the length, or both.

Table 1 - Characteristic impedance of various twisted-pair cable constructions

Cable	Construction	Differential Z_0	Capacitance unbalance[1]
A	24 Ga. solid conductor, polyethylene insulation, unshielded, 16 pF/ft	$100\Omega \pm 15\%$ from 1 MHz to 100 MHz	2%
B	24 Ga. stranded conductor, foam-polyethylene insulation, shielded, 12 pF/ft	$120\Omega \pm 15\%$ from 1 MHz to 10 MHz	3%
C	24 Ga. stranded conductor, polyethylene insulation, shielded, 16 pF/ft	$100\Omega \pm 15\%$ from 1 MHz to 10 MHz	5%
D	24 Ga. stranded conductors, PVC insulation, unshielded, 30 pF/ft	$60\Omega \pm 20\%$ at 1 MHz	10%
E[2]	28 Ga. stranded conductors, polyethylene insulation, shielded, 12 pF/ft	120 ohms $\pm 10\%$ from 1 MHz to 33 MHz	3%

The interconnecting media may not be cables but, as in backplanes, copper traces on a printed circuit board. Numerous printed circuit board design tools are available that control the characteristic impedance of the traces as one of the basic design criteria.

4.1.2 Data signaling rate and distance (Attenuation)

The voltage drop from the resistance in the conductors fundamentally limits the distance that a 485 can transmit and recover a signal. At some length, the steady-state differential signal drops below the receiver's differential input voltage threshold and not be recovered. Figure 8 shows the equivalent dc circuit of a standard 485 bus. From it, it is obvious that R should be less than 390Ω to maintain the minimum 485 voltage levels.
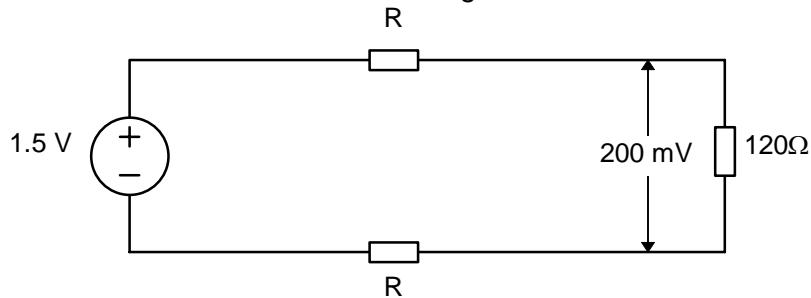
Figure 8. - 485 bus dc circuit model.

Twenty-four Ga. wires have a resistance of about $25\Omega/1000$ ft. This would require over 3 miles of cable to exceed the 390Ω maximum dc resistance limits. Of course, operating a

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[1] Capacitance unbalance refers to how closely the electrical characteristics of each line of the signal pair match. The values provided are typical. See 4.1.3 for further discussion.

[2] Typical cable used for SCSI.

data bus at dc and with no noise margin is not practical and further length limitations are required.

When pushing the extremes of distance or data rates, the designer should not ignore second-order affects of the media. There is no simple electrical model to account for attenuation with frequency, intersymbol interference, phase dispersion, skin effects, proximity effects, common-mode voltage, and others. The designer should empirically determine the performance of the media in these regards.

In the nominal frequency range covered by this application, around 10 MHz, cable attenuation is inversely proportional to conductor diameter and to characteristic impedance. Below 1 MHz, cable attenuation is proportional to conductor cross-sectional area (DCR, Figure 8). Above 100 MHz, second-order effects become very significant.

At lower frequencies, below 1 MHz, DC resistance dominates distance limitations. At higher frequencies, around 10 MHz, line length versus data signaling rate is nearly proportional to cable attenuation.

Example: Referring to Table 1, cable B and cable E are similar except for conductor size. Cable E has 28 Ga. conductor, which is about 1/2 of the diameter of 24 Ga. in cable B. Cable E has the expected attenuation level about 2 times that of cable B, at 10 MHz. Cable E can be expected to have the same data signaling rate over about 1/2 of the distance as cable B.

Example: Cable B has 120Ω characteristic impedance compared to cable A with 100Ω. Cable A would normally exhibit about 20% less attenuation than cable B but cable B has stranded conductor that normally results in about 20% less attenuation over solid conductor. The two effects would offset and cable A and cable B have similar attenuation levels and, therefore, nearly identical data signaling rate performance.

The single most useful measurement on the interconnecting media is the eye pattern. Figure 9 shows the maximum cable length versus data signaling rate for a Belden #9842 cable and a typical 485 line driver with a 10 ns output transition time and 5% and 20% jitter. This set of curves may be used as a guideline for cable selection and subsequent jitter budgeting
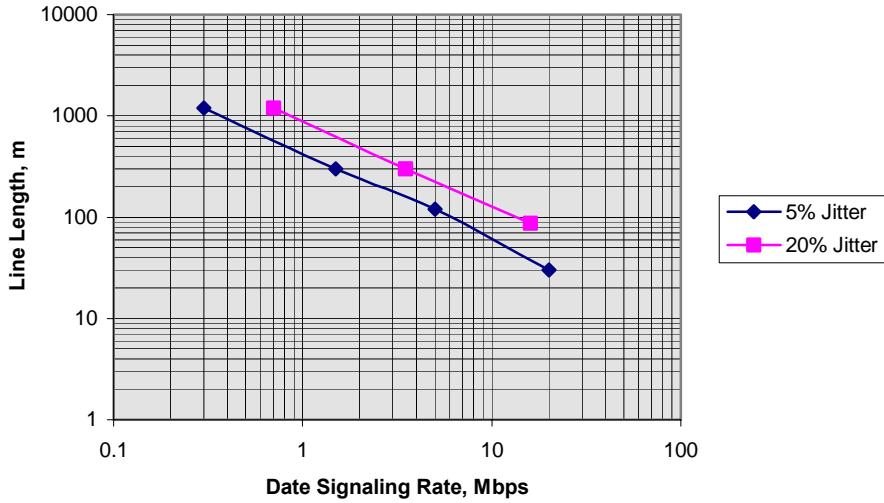
Figure 9 - Maximum line length versus signaling rate.

In lieu of the eye pattern, a simple measurement of the signal rise time out of a length of cable yields an estimation for the maximum length at a specific data-signaling rate using the following rule.

Equation 1 - Data signaling rate versus distance rule

$$t_{10\%-90\%} \leq \frac{T_{min}}{2},$$

where $t_{10\%-90\%}$ is the 10%-to-90% transition (rise or fall) time of the signal at the end of the interconnection and T_{min} is the minimum unit interval.

The guidelines above are for non-encoded non-return-to-zero data. There exists data encoding patterns that reduces the dc component of the data signal. Such encoding has the effect of reducing intersymbol interference and extending the transmission distance or data-signaling rate. (See 6 List of References for further information.)

Receiving equipment exhibit varying tolerance to jitter. A 5% eye-pattern jitter is used here as a conservative guideline however, the designer should take into account the performance of the receiving equipment when defining the system jitter or skew budget.

4.1.3 Noise coupling

Since 485 is a balanced signaling method, we are concerned primarily with the differential characteristics of the media. The matching of the characteristic impedance of each signal line to the signal return (ground) becomes a factor in differential noise coupling. Since this is a secondary effect with a complex model, we will simply recommend that the designer match the single-ended impedance of each signal line. Differential noise coupling is minimized by twisting the wires of the signal pair, shielding, and balancing the interconnect media.

4.1.4 Termination

The termination of a 485 bus can be a simple resistor or more elaborate circuit to provide other functions. The fundamental purpose of the termination is to maximize ac signal power transfer from the interconnect media. Matching the differential impedance of the termination circuit with the characteristic impedance of the interconnection maximizes signal power transfer. A discontinuity in or mismatch of the termination and interconnect impedance causes a reflection of some of the signal back into the interconnection. A reflection of sufficient magnitude and polarity can result in an undesired change in the bus logic state or, in the presence of common-mode noise, possible damage to the interface circuitry.

The termination shown in Figure 10 is the simplest termination for a 485 bus and performs the fundamental task of minimizing reflections. Since this is an ac phenomenon, the designer should select the construction and material of the termination circuit for the application bandwidth.

+ Signal

T

$Z_0 \, \Omega$

$Z_0 \, \Omega^* \pm$
10%,
1/2 W**

- Signal

* or closest standard value
**1/4 W rated resistor may be used
but at less than a 50% derating
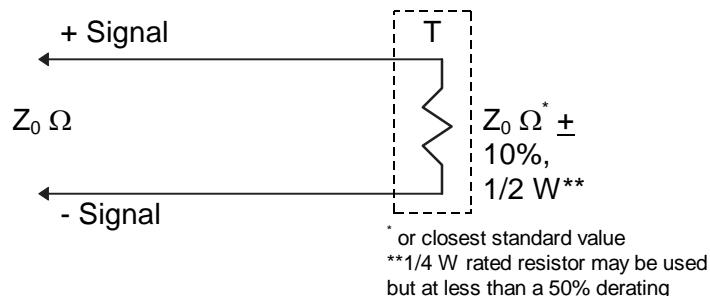
Figure 10 - Simple differential termination.

Although simple, the termination shown in Figure 10 has some disadvantages. In the absence of an active driver on the bus, it will pull the differential voltage to near zero volts, which places the bus in an indeterminate state to an active receiver. Later paragraphs discuss remedies for this condition. Another minor drawback of this termination is that it dissipates power under steady-state conditions.

In applications that allow long periods of steady-state high or low-level conditions to exist on the bus and are power sensitive, capacitive coupling of the termination resistor can lower power consumption. Figure 11 shows such a termination. The values provide a -3 dB frequency of about 7 kHz.

+ Signal

T

$Z_0 \, \Omega$

$Z_0 \, \Omega \pm 10\%$

0.22 μF ± 20%
10 V, ceramic, non-
polar

- Signal
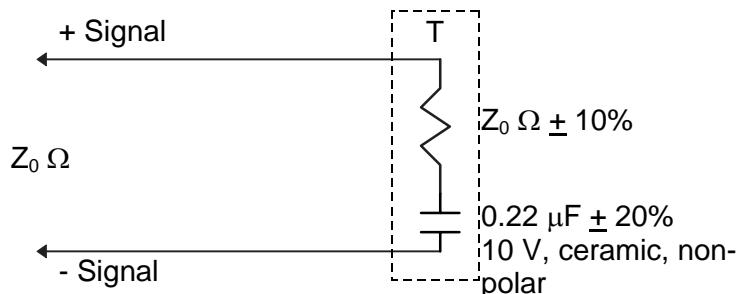
Figure 11 - Capacitive coupling of the termination resistor

In some very electrically noisy environments, it may be advantageous to provide a lower common-mode impedance path to ground than that offered through the inputs of a receiver. The termination circuit of Figure 12 provides tertiary noise rejection, after proper system shielding and grounding, for high-impedance (electric) fields. (Note that the circuit matches single-ended impedance to ground for each line and maintains balance.) Although this termination may help in certain noise environments, the maximum common-mode voltage range would be about -2 V to 7 V with 32 unit loads (see 4.2.1). If properly applied, there would be less common-mode noise coupling anyway. We do not recommend this termination for use where the primary noise source is from low-impedance (magnetic) fields.
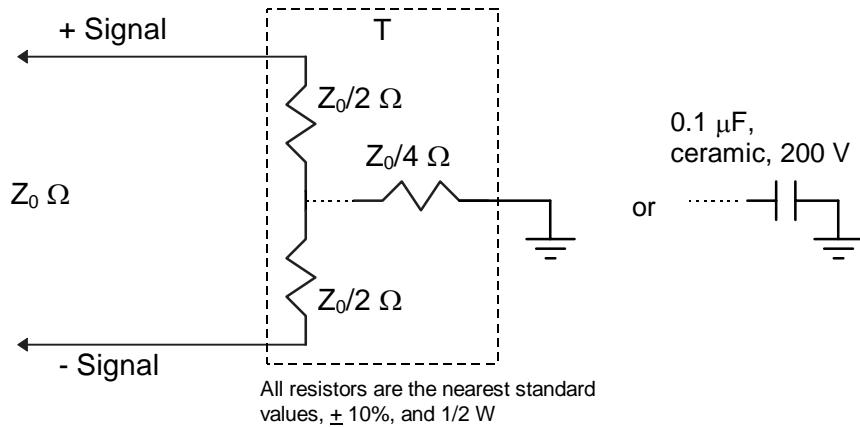
Figure 12 - Low common-mode impedance termination

It is not always necessary to provide termination of the interconnection. If the distributed parameters of the interconnection determine the electrical response, termination is generally required. By definition, this means that the shortest wavelength (highest frequency component) of the input signal is shorter than the overall length of the circuit. Conversely, if the signal wavelength is longer than the length of the circuit, lumped parameters describe the circuit. This is the basis for the guideline given in Equation 2.

Equation 2. Definition for distributed or lumped load circuit model

$$t_{10\% - 90\%} \geq 2t_{pd} \ ,$$

where $t_{10\%\text{-}90\%}$ is the 10% to 90% transition (rise or fall) time of the input signal and t_{pd} is the one-way propagation delay along the greatest length of the interconnection.

Equation 2 basically says that if the fastest transition time of a driver output is greater than two one-way delay times, the interconnect is not a transmission line and there is probably no need to terminate it.

4.2 Bus loading

Drivers complying with 485 assure a minimum drive capability. To assure that the 485 bus stays within this capability, the designer should know and account for the electrical characteristics of the attached interchanges in the system design and specification. Attached equipment should meet steady-state load requirements in terms of the number of unit loads and input offset bias (balance). The input ac characteristics of an interface should also be compatible with the intended data-signaling rate and bus configuration.

4.2.1 Steady-state load

In addition to a 60-Ω differential resistive load, each 485 driver can drive up to 32 unit loads (UL's) steady state over a -7 V to 12 V common-mode voltage range. Compliance testing to the *Differential Output Voltages with Common-mode Loading* requirement of the standard (section 4.2.3 of TIA/EIA-485-A) verifies this performance.

The two 375Ω resistors in the standard test circuit represent the equivalent common-mode resistance of 32 12-kΩ loads and consists of both receivers, drivers in the passive state, and any common-mode loading presented by the termination. Since the output current of the drivers is budgeted between the differential and common-mode loads, there is the possibility of operating with a higher number of unit loads if the common-mode voltage range of the application is smaller than the maximum allowed.

Figure 13 shows a graph of the maximum number of unit loads on a compliant 485 driver versus the bus common-mode voltage and equivalent differential load resistance. It shows that over the full-spec range of -7 V to 12 V, a driver supports up to the 32 unit loads. It also shows that if the common-mode voltage range were -1 V to 5 V, a driver supports more than 50 unit loads, at least in the steady state.

The driving driver may also handle lower differential loads than the 60Ω of the standard test circuit. Again, lower differential loads come with a compromise in the common-mode loading to remain within the assured driver output current.
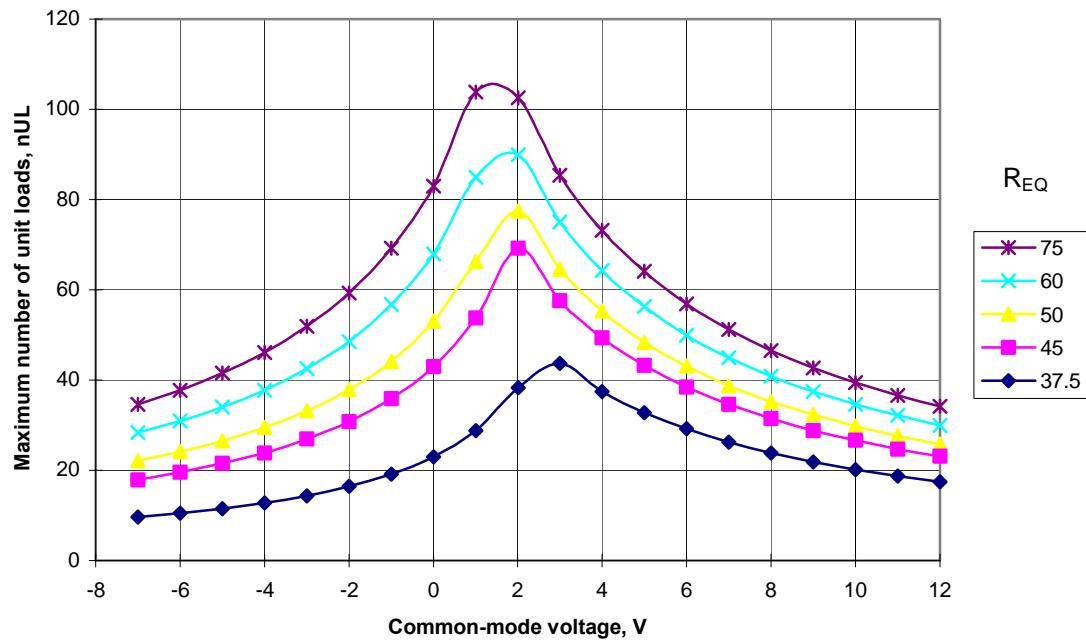

Figure 13 - Maximum number of unit loads versus common-mode voltage and R$_{EQ}$

4.2.2 Time-varying load

Devices connected to the interconnect media at the interface points will contain reactive components which will affect a signal on the bus. The design goal should be to make the ac effects from the loads either negligible or within the allowed noise budget. There are three primary concerns to the system designer: reflection, unbalance, and distortion of the signal.

The goal here is to obtain an incident-wave state transition at all interface points. It is possible to construct a 485 bus that works without incident-wave switching and need only meet the dc loading requirements by assuring that sampling of the bus state occurs at least three round trip delay times after any state change. The round trip delay time is the twice the propagation delay between the longest electrical path of the bus. If the bus meets these criteria, there is generally no need for terminating the interconnection or other ac loading considerations.

4.2.2.1 Reflections

Reflections will occur whenever a signal wave front in one characteristic impedance meets a media of another characteristic impedance. Conservation of energy at such a boundary requires that some of the signal energy reflect to whence it came.

4.2.2.1.1 Stubs

Loads modeled by a simple lumped circuit containing inductance, capacitance, and resistance construct the standard 485 bus. Once distributed effects become non-negligible, the system analysis becomes unwieldy and beyond the scope of this document. To determine if a load connected at the interface point is a lumped circuit, we apply the guideline given in Equation 2 to the circuit between the interface points and the line driver, receiver or transceiver.

Making this determination requires knowledge of the shortest 10%-to-90% rise or fall time of any signal driven to or from the interconnection. If not restricted by specification in the referencing document, the designer should use a minimum transition time of 5 ns based upon a survey of the semiconductor technology currently available. Should faster drivers become available, the reader should modify the following guidelines for the faster edge rates.

From the perspective of transmitting equipment, the input signal would be the output voltage of a driver. Figure 14 shows three channels of an oscilloscope with differential probes connected at various points along the circuit with the signal transition at each point.
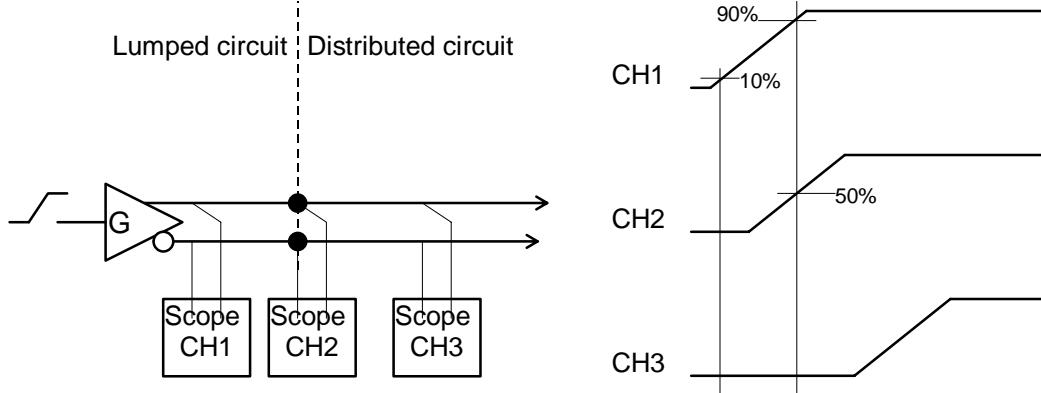
Figure 14 - Determining if load represents a lumped circuit to the 485 bus.

If the line of demarcation between lumped and distributed circuits occurs prior to the interface points, the load does not meet the lumped-circuit requirement and will result in signal reflections.

Conversely, reversing the measurement, placing channel 1 at the interface points, and verifying the line of demarcation does not occur prior to the receiver keeps proper ac loading of the receiving equipment.

4.2.2.1.2 Distributed loads

Even if all of the loads attached to a 485 bus meet the criteria for a lumped circuit, the capacitive loading effects can cause a localized impedance mismatch to the nominal impedance of the media. The characteristic impedance of a length of bus with lumped loads attached, Z', may be approximated by Equation 3.

Equation 3. - Approximate loaded media characteristic impedance.

$$Z' = Z_0 \sqrt{\frac{1}{\left(1 + \dfrac{C_L}{dC}\right)}}$$

Where Z_0 is the nominal characteristic differential impedance and C is the unit-length differential capacitance of the unloaded media, C_L is the lumped differential capacitance of the load, and d is minimum distance between loads.

For a bus designed with no steady-state differential biasing, we recommend that the loaded bus characteristic impedance be more than 60% of its unloaded characteristic impedance. For our example cables in Table 1 and a $C_L = 20$ pF, this equates to the minimum load spacing listed in Table 2. (Note that Table 2 includes a media, F. This represents a typical backplane implementation.)

Table 2. - Minimum spacing between 20-pF differential loads for a loaded impedance of 60% of the unloaded characteristic impedance

Media	C, pF/ft.	d, ft.
B or E	12	0.9
A or C	16	0.7
D	30	0.4
F	50	0.2

4.2.2.2 Balance

The imbalance of impedance to ground of the differential pair determines, in part, the susceptibility of a network to interference, whether the result of inductive or capacitive coupling. Assuming the coupling of interference to each of the two conductors is equal; the imbalance of the impedance to ground will determine the magnitude of the component of the interference that appears between conductors. Consider an active generator at one end of a cable and several Off-state generators and receivers bridged at the other end. Neglecting the generator output signal, the circuit of Figure 15 approximates the configuration. Where,

R_s is, at high frequencies, the characteristic impedance of the media, and a low frequencies, the loop resistance.

Z_a, Z_b, and Z_c are the corresponding impedance of the combination of bridged receivers.

e_i is the magnitude of the interfering signal, as would appear to ground at one end of the media with the other end shorted to ground.

e_n is the conductor-to-conductor or differential component of the interference resulting from impedance imbalance.
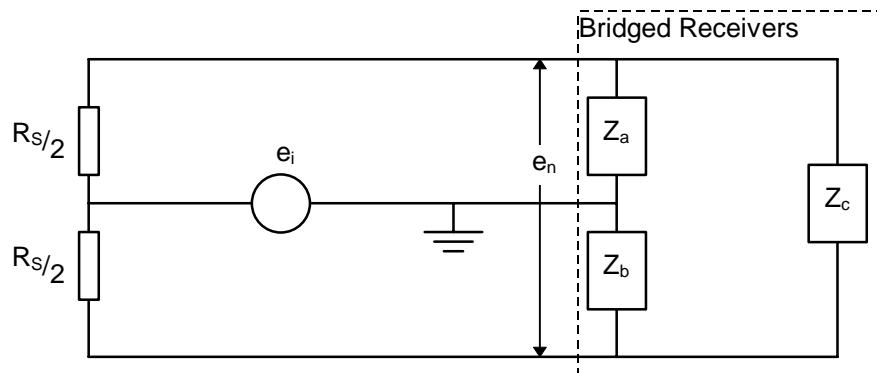

Figure 15. - Noise model for a 485 circuit

Note that an active driver or media provides a low impedance to ground from both conductors of the signal pair, and therefore, a common-mode voltage will appear at the bridged-receiver end of the media as a voltage to ground with a source impedance of $R_s/4$)

For the equivalent circuit shown, the balance of concern is the ratio of the voltage of the common-mode interference to the resultant differential noise voltage, e_n, or

$$Balance = 20\log\left|\frac{e_i}{e_n}\right| \text{ dB}$$

and, for $G_S = {}^1/R_S$ and $Y_X = {}^1/Z_X$,

$$\frac{e_i}{e_n} = \frac{(2G_S + Y_a)(2G_S + Y_b) + Y_c(4G_S + Y_a + Y_b)}{2G_S(Y_b - Y_a)}$$

Let $(Y_a - Y_b) = Y_d$ and assuming $Y_a \ll G_S$, $Y_b \ll G_S$, and $Y_c \ll G_S$, as is typical, the following approximation is obtained.

Equation 4. Approximate ratio of common-mode to differential noise voltage

$$\frac{e_i}{e_n} = \frac{2G_S}{Y_d} \quad .$$

This suggests that the imbalance of the configuration is inversely proportional to the sum of the differences in the admittance to ground for the two input terminals of the bridged receivers and that it is essentially independent of common-mode admittance to ground ($Y_a + Y_b$) of the receivers.

Balance is of concern up to a least the maximum frequency of a signal to which receivers will respond. Differences in the capacitance to ground, from the two receivers' input terminals, of only a few picofarads can cause significant imbalance if the response of receivers extends to many megahertz. For example, 10 receivers, each having a capacitance difference to ground of 10 pF bridged on a 120-Ω cable, would result in a balance at 10 MHz of about 10 dB. ($e_n \approx 2.2$ V with $e_i = 7$ V). At higher frequencies (e.g. 50 MHz), the configuration would appear to have one conductor grounded.
The configuration and associated relationship discussed here are only typical. The relationships would not be valid for many other configurations. It only demonstrates that, in using devices that conform to the requirements of 485, a designer of a network should consider the imbalance in the devices, media, and associated equipment.

4.2.2.3 Distortion
In most applications, the media will determine the ultimate bandwidth of the data channel. In some high-speed short-distance connections, the ac loading from bus connections may become a significant factor. If a 485 load meets the lumped-circuit and spacing criteria, a differential input capacitance of the load of 30 pF or less should keep this effect from being significant up to the 50 Mbit/s data signaling rate included in this document.

Table 3 provides a guideline for the maximum data-signaling rate with load capacitance based upon a lossless transmission line, 120Ω characteristic impedance media, and maximum data-signaling rate of ${}^1/(2t_{10\%-90\%})$. Again, this restriction only applies to lossless media that does not further limit the data-signaling rate.

Table 3. - Load capacitance and theoretical maximum data signaling rate for a 120-Ω cable

Differential input capacitance, C_L	Max Data signaling Rate (Mbit/s)
15 pF	91
30	46
45	30
60	23
100	14
750	2

4.2.2.4 Hot plugging

Hot plugging a 485 device to a bus can take on several levels of complexity. The simplest case is one in which the equipment remains physically connected to an active bus and the operator removes or applies power to the equipment. Maintenance of the interface loading characteristics during such an event usually implies that a driver have power up/down glitch-free performance. This circuitry maintains a high-impedance output below a certain supply voltage threshold regardless of the input conditions. Above this threshold, the inputs conditions determine the state of the driver outputs.

The more complex scenarios involve the physical connection of equipment to an active bus. If equipment meets the ac and dc loading criteria, the time sequence of the mechanical connection usually determines the perturbations of the bus signals. If present in the connector, the first connection should be ground, then power, and then signals. The advantage of 485 signaling over others during hot-plugging operations is its common-mode voltage range and balanced signaling. Although the instantaneous perturbation of the signals present on the active bus are inevitable, as long at they remain common to both signal lines and within the bus common-mode voltage range, they will not cause a bus state change. The critical timing will be the delay between making the connections between the lines of a signal pair.

4.3 Noise budgeting

The minimum signal voltage presented to the receiver should be equal to or larger than the worst allowable receiver threshold. Any receiver input voltage in excess of the value is margin. The amount of margin needed in a system will depend upon noise consideration, allowable error rate, and amount of allowable signal distortion. To determine the cable characteristics, the user should first decide on the amount of receiver voltage desired at the worst-case receiver. The designer uses this information to determine the minimum cable characteristics.

A 485 receiver's worst-case receiver input voltage threshold is $\pm$ 200 mV and a driver's worst-case differential output voltage is $\pm$ 1.5 V. This leaves at least 1.3 V to budget across the various differential noise contributors. Noise is any unwanted signal and, for a 485 bus, includes differential voltages from; signal attenuation from the media (4.1.2), noise coupling

to the media (4.1.3), reflections (4.2.2.1), unbalance (4.2.2.2), and, in some cases, a differential bias voltage (4.4). (Note that an intentional bias voltage is a desired signal for one state of the bus but is unwanted in the other state(s) and, hence, can be considered noise.)

4.4 Fault conditions

The following sections deal with some of the common fault conditions that may occur on a 485 data circuit. A steady-state bias via an external resistor network compensates for all of the conditions. The application of this bias will depend on the fault conditions to be remedied and other system performance constraints. These are typical examples and the reader should analyze the application of any or each with the complete 485 bus circuit in mind. No cases will damage a 485 compliant line circuit.

4.4.1 Idle-line failsafe

The developer of a system using 485 drivers, receivers, or transceivers should consider the situation in which all drivers may be in the passive state. With the termination circuits shown in Figure 10, Figure 11, and Figure 12, an active receiver will assume no specific logical state under this condition. When the data transmission protocol does not handle this situation, the circuit of Figure 16 may be used to provide a dc bias of between 206 mV and 271 mV to the bus using 5% tolerance resistors. There is only need for providing the bias voltage at one termination.
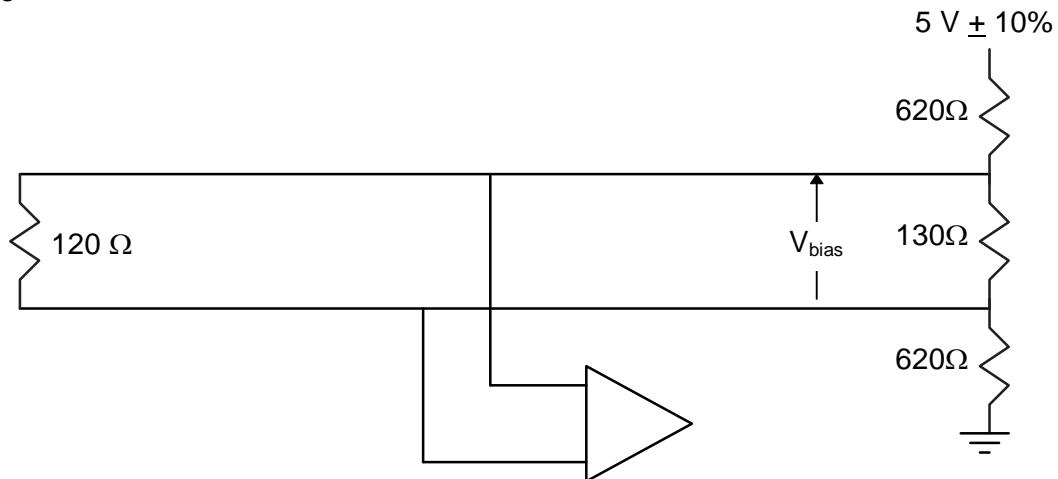

Figure 16. - Idle-line failsafe bias circuit

Use of this circuit does require some system-level tradeoffs and cautions:

− The bias voltage will reduce the differential noise margin.

− There is budget for only an additional 12.5 unit loads on the bus and maintain the full -7 V to 12 V common-mode voltage range capability.

− System power requirements increase.

− Power loss at the location of the bias circuit will remove the failsafe.

4.4.2 Open-line failsafe

An active non-terminated receiver disconnected from the 485 bus causes the open-line condition and is the easiest condition to remedy. In fact, most 485 receivers available today have integrated bias circuits to provide a known output state when the inputs are open circuited. The circuit of Figure 17 provides this feature or defeats the default state provided by the receiver. Determining the pull-up and pull-down resistance values requires knowledge of the number of unit loads (nUL) presented by the receiver circuit. Use of this circuit will increase the nUL by approximately 10% and add less than 3 mV differential bias to a normally terminated bus for each such circuit connected.
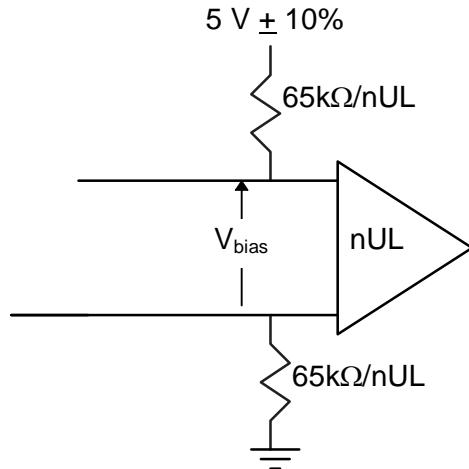

Figure 17. - Open-circuit failsafe bias circuit

4.4.3 Shorted-line failsafe

A short circuit between the lines results in an indeterminate logic state. If a known logic state is required at the receiving equipment, an input circuit such as the one shown in Figure 18 can provide a defined output state under this and the idle-line and open-circuit conditions.
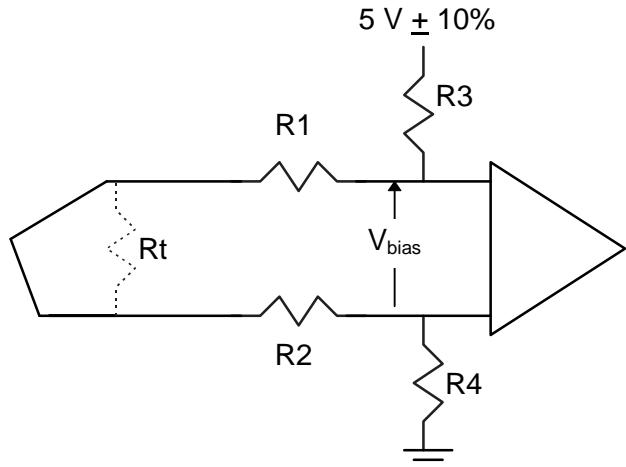

Figure 18. - Shorted-line failsafe bias circuit

The resistors R1 through R4 provide a V_{bias} of 200 mV with the inputs short circuited and meet the nUL and attenuation constraints imposed by the system requirements under normal conditions. Table 4 shows some values for resistor networks along with the number of unit loads added by each. The attenuation value provided in the table would be with a receiver with a 12 kΩ input resistance.

Table 4. Typical resistor values for short-circuit failsafe circuit

R1, R2	R3,R4	nUL	A, dBV
180 Ω	3.9 Ω	2.94	-0.52
470 Ω	10 kΩ	1.15	-0.72
750 Ω	15 kΩ	0.76	-0.93
1100 Ω	22 kΩ	0.52	-1.15
1500 Ω	30 kΩ	0.38	-1.40
2200 Ω	39 kΩ	0.29	-1.87
3300 Ω	56 kΩ	0.20	-2.50

A combined generator and receiver or transceiver prohibits the use of this circuit. Any series resistance in the output of a worst-case 485 driver prevents compliance with the minimum output level requirements.

4.4.4 Contention

Two or more drivers are connected to the same transmission line create the potential condition where both drivers are simultaneously in the active state. If one or more drivers are sourcing current while another is sinking current, excessive power dissipation may occur within either the sourcing or sinking driver. Contention describes this condition since multiple drivers are contending for one transmission line. Since system requirements may dictate that more than one driver is active simultaneously, the Generator Contention Test of the 485 standard provides a practical limitation on the output current and driver power dissipation. Contention may occur during system initialization, under hardware or software faults, or if allowed by the communication protocol.. Protocols may allow stations that are sharing one line to compete for a transmission, resulting in multiple drivers being active simultaneously. However, one station will eventually succeed in acquiring the line, thereby ending the contention.

The output current of a 485 driver is limited to ± 250 mA and, although not required by standard, most modern 485 drivers include a thermal shutdown feature. These features prevent permanent damage to the line circuit. However, there is no reliable method to detect a contention by sensing the differential bus voltage.

5 System Specification Requirements

The referencing standard should provide the following specifications to minimize interoperation problems. This list is not all inclusive but is some of the most critical.

System definition: number of nodes allowed, bus configuration, cable length(s), and data transfer rate

Mechanical interface: connector style, interface dimensions, connector contact assignments

Functional: communication protocol, signal quality, timing budget, noise budget, data signaling rate, data transfer rate, failsafe requirements

Electrical: interconnecting media, power, ground, signal ground/common, other non-485, and shield contact characteristics.

Environmental: ambient temperature, storage temperature, EMC

6 List of References

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