DS90

1121-30

DS90-2x Computer board

B

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SWEDEN

Record of changes:

Revision	Date	Comments
A	880425	First version
B	890427	Changed pages: 32,35,61,62,70

Contents

1 DESCRIPTION

The 1121-30 high performance low cost single board supermicro computer is the main component in the DS90-2x computer system. It is based on the true 32 bit M68020 CPU, intended to support office automation, data communication, industrial control and advanced workstation applications.

1.1 Highlights

The 32 kbytes cache memory allows operation without waitstates at 20 MHz CPU-clock frequency and expected hit rates greater then 90%. Up to 4 processor planes, each containing CPU, PMMU, FPU and cache, can execute system and user tasks concurrently for highest performance. The main memory can be expanded to 28 Mbytes, and up to 64 Mbytes using future 4 Mbit memory chips. Up to 16 serial channels can be used internally by low cost hardware expansion. More serial channels can be added using VME expansion board as terminal concentrators.

The VME expansion facility enables VME bus masters to access the main system memory and allows the system CPU(s) to access all slaves on the VME bus. System memory is protected against unauthorized access from the VME bus.

Full support is provided for expansion with I/O-boards from the proprietary DataBoard 4680 series.

Two high speed SCSI interfaces are supported by DMA and provides very fast data transfer between mass storage devices and main memory. Both interfaces supports multi-master functions on the SCSI bus, allowing the sharing of mass storage devices between several systems as well as high speed direct computer-to-computer communication with data transfer rates higher then 1.5 Mbytes/second.

The diskette interface supports all existing recording standards like FM and MFM, includes various data transfer rates 250/500 kbytes/sec, motor speeds 300/360 rpm and different sector lengths. Up to three diskette drives can be accessed alternately.

1.2 Basic configuration

The basic configuration is one large board (1121-30), which is described in this datasheet. It has the following resources:

- M68020 CPU with 16.67 MHz clock.
- M68851 PMMU paged memory management unit, supporting up to 2 Gbytes logical memory per process with full virtual memory support.
- M68881 FPU floating point unit, for up to 20 times increased execution speed.
- 32 Kbytes cache memory, accessed without waitstates, using 16 bytes block size and immediate write through.
- Prepared for multiprocessor expansion with three more CPU-planes on expansion boards with CPU, PMMU, FPU and cache memory.
- 4 Mbytes memory. Up to 28 Mbytes with mounted expansions and up to 64 Mbytes using future 4 Mbits chips and expansion. Hardware parity check of memory.
- DMA (HD68450) with 3 independant channels, all having separate 16 bytes hardware buffers for high speed performance.
- 4 serial V24-ports. Up to 16 internal ports with mounted expansions, (in the DS90-2x computers limited to 12 internal ports due to space limitations). Expansion is possible with more serial ports using terminal concentration boards.
- Two high performance SCSI interfaces with multi master capabilities. E.g. for Winchester disc and tape streamer or fast computer-to-computer communication.
- Diskette interface for up to three 5 1/4" drives.
- Flexible interface expansion capability for DataBoard I/O, VME-boards, graphics and others, using an expansion backplane mounted on the basic board.
- Real time clock with battery backup, NVRAM for parameter storage and a flexible hardware interrupt system.
- Support for VME includes multi master capability and selective protection for internal memory from bus masters on VME boards.
- Support for DataBoard includes automatic 'card select' generation and selective access protection.

1.3 Expansion boards for the 1121-30.

- 1120-30 CPU expansion plane, CPU, PMMU, FPU, Cache.

- 2020-30 4 MB memory module for direct mounting on the 1121-30. Optionally 16 Mb if 4 Mbit chips are used. Logically three boards are supported.

- 2022-00 8 Mb memory module for direct mounting on the 1121-30, using 1 Mbit chips in two layers. Optionally 32 Mb with 4 Mbit chips. Logically three boards are supported.

- 5172-10 4 serial V24-ports. Two 5172-boards can be mounted on 1121-30 in DS90-2x. Logically three boards can be supported.

- Different expansion backplanes are available for mounting on the 1121-30, with VME and DataBoard slots.

These are described in separate datasheets.

For further I/O-expansion a DataBoard I/O-expansion rack and/or a VME expansion rack are available connected through adapters. Alternatively IQ-IO-systems for direct industrial level signals can be connected.

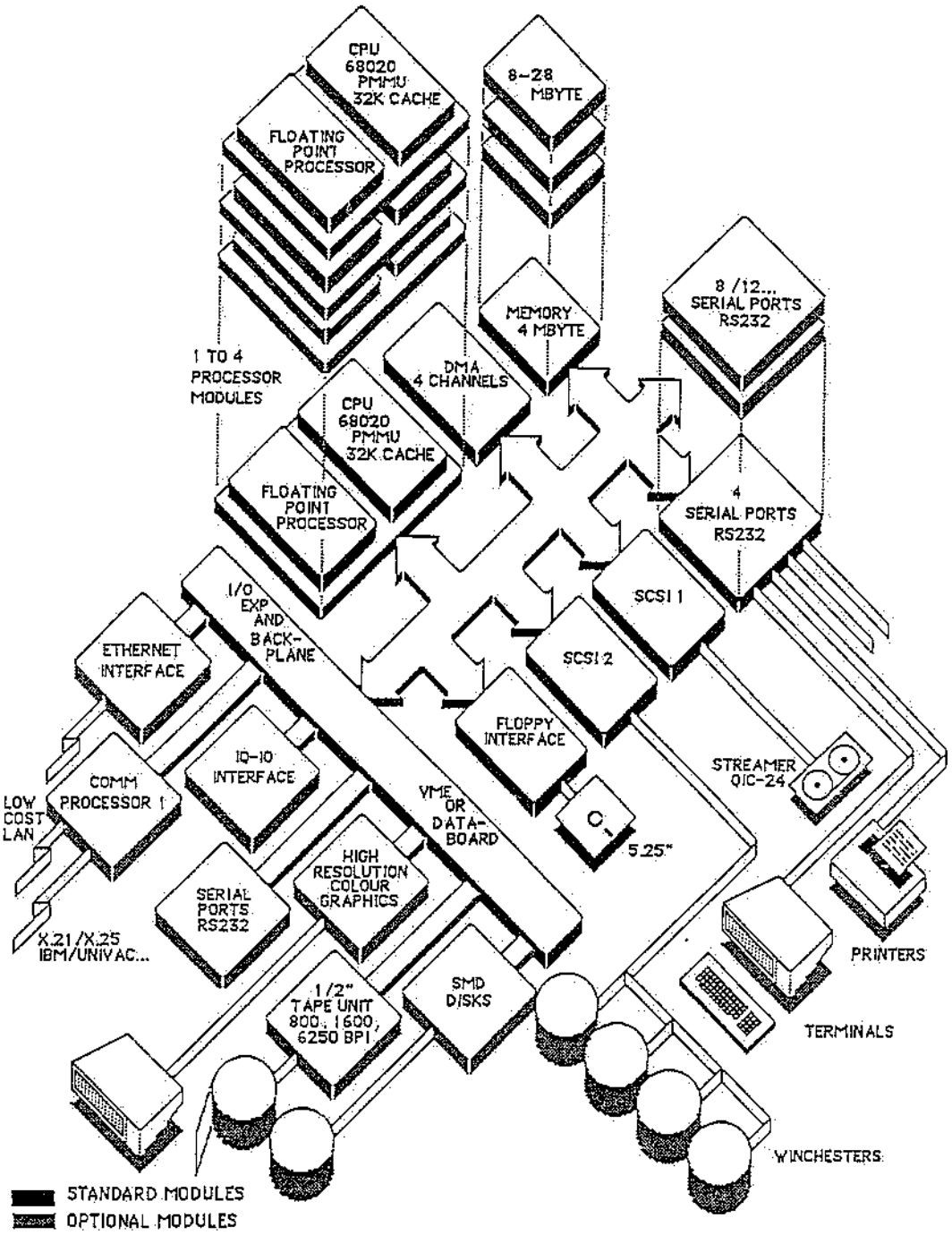
Note! For earlier versions of the 1121 computer board, other memory and CPU expansion boards are used. These can not be used with 1121-30.

For 1121-10 Use only the 2020-20 memory expansions boards.
No CPU expansion board can be used.

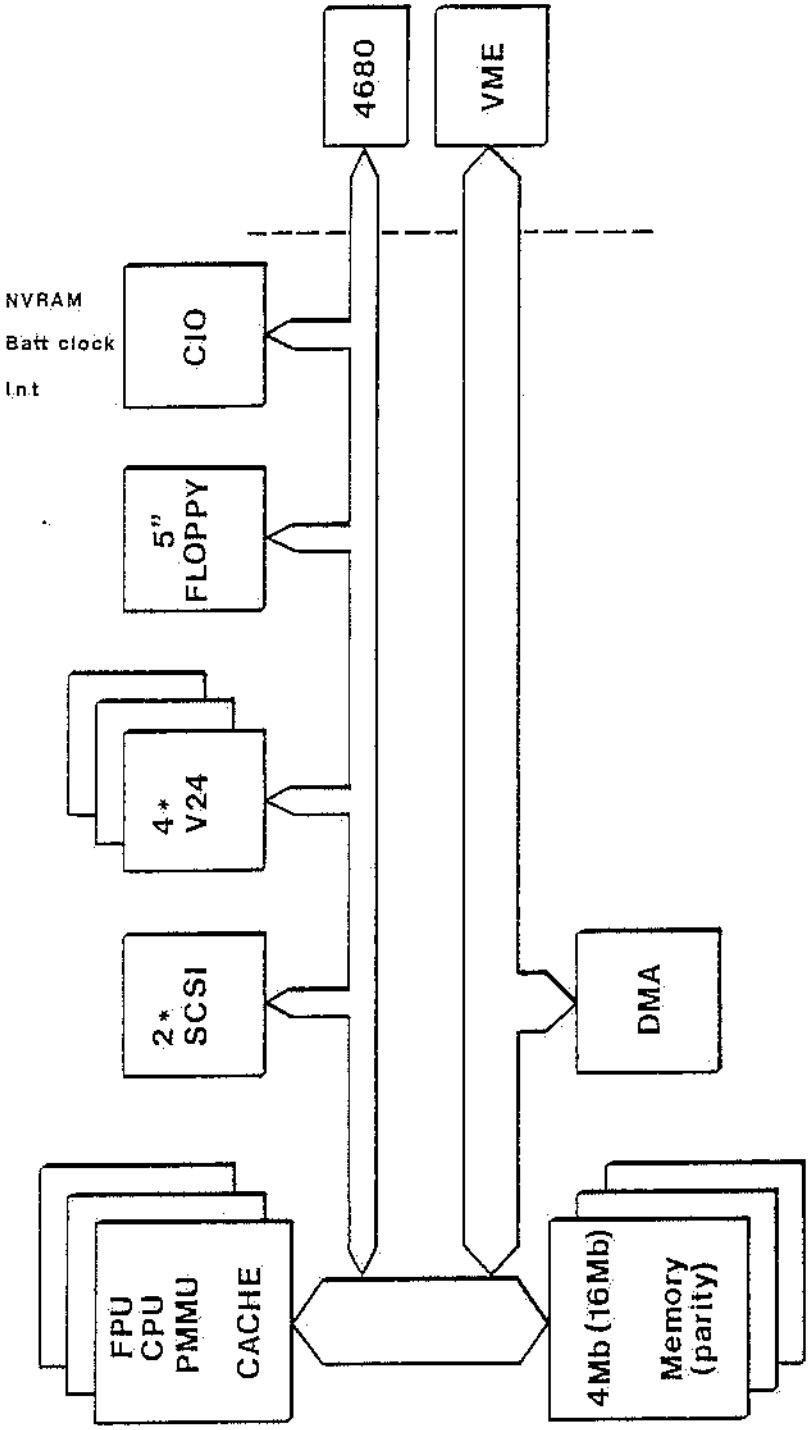
For 1121-20 Use only the 2020-20 memory expansions boards.
Use only the 1120-20 CPU expansion boards.
For the software viewpoint, there is no difference between 1121-30 and 1121-20.

2 HARDWARE BLOCK DIAGRAMS.

System overview DS90-21



Block diagram



3 SOFTWARE ENVIRONMENT

3.1 Logical address spaces.

Any program can use up to 2 Gbytes logical address space, as the system contains full support for virtual memory and memory management for the MC68020 processor.

User accesses beyond this limit result in error traps. The logical address space 2 Gbytes - 4 Gbytes is reserved for testing of the on-board cache memory system.

Logical address space types.

There are several types of address space types defined, depending on the type of instruction executing and if the code is executed in user mode or supervisor mode.

Type	FC2	FC1	FC0 function code
User data space	0	0	1
User program code space	0	1	0
Supervisor data space	1	0	1
Supervisor program code space	1	1	0
CPU space	1	1	1

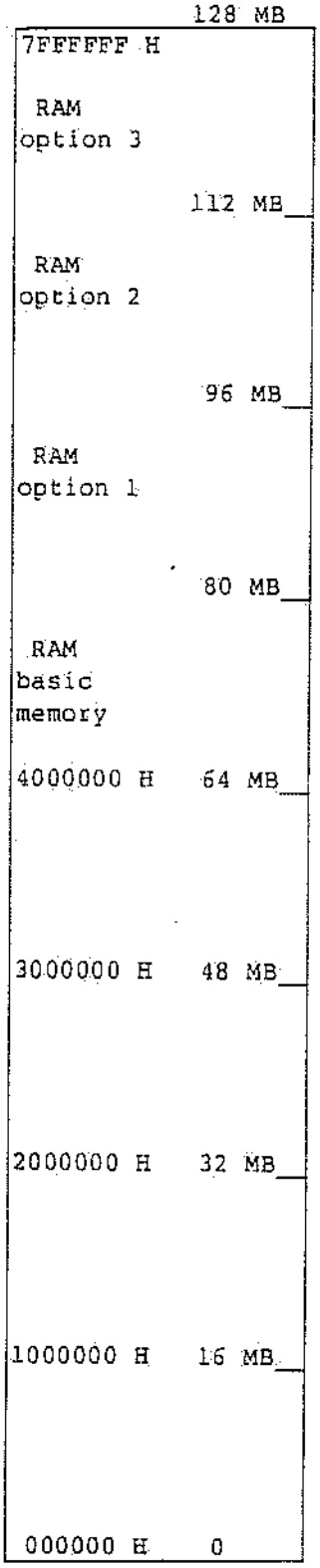
The CPU space is used for coprocessor communication, interrupt acknowledge cycles and for special cache memory control. Accesses to the MC68851 PMMU and MC68881 FPU are handled through the standard coprocessor instructions in MC68020.
All user entries or all supervisor entries in the cache can be selectively erased by accessing one of the logical addresses 002C000 or 002E000 Hex in CPU-space. See the section about the cache memory.

Stack data area (A30=1)

In the cache memory, the logical user and supervisor data spaces with A30=1 are assumed to be used for the stack data area to enable a separate cache segment for the stack. For efficient use of the hardware, the software should make use of this feature.

3.2 Physical address space.

Physical address bits PA0..PA26 access normal system resources.
Physical address bits PA27, PA28, PA29, PA30 are not used.
Physical address bit PA31 is used for cache inhibit.



3.3 Summary of I/O and physical memory space access addresses.

Resource	Base address(hex)	Size(bytes)	Width(Bytes)	Type
PROM	000xxxx(0..FFFF)	64 kb	1	RO
CPU attention	001000n(n=0,4,8,C)	1	1	RW
LED control	0010010	1	1	WO
Watch-dog kick	0010020	1	1	RO
Real time int.reset	0010020	1	1	WO
Parity error syndrome	0010030	1	1	RO
Error syndrome reset	0010030	1	1	WO
Slave CPU reset	0010100	1	1	RW
CIO port C Data	0020000	1	1	RW
CIO port B Data	0020010	1	1	RW
CIO port A Data	0020020	1	1	RW
CIO control	0020030	1	1	WO
CIO int. vector	0030000	1	1	RO
SCC control	010n000(n=0..F)	1	1	RW
SCC data	011n000(n=0..F)	1	1	RW
SCC int. vector	0130000	1	1	RO
SCSI 0 control/status	0200000	1	1	RW
SCSI 0 pointer	0200020	1	1	RW
SCSI 0 data buffer	0200030	16	1	RW
SCSI 1 control/status	0210000	1	1	RW
SCSI 1 pointer	0210020	1	1	RW
SCSI 1 data buffer	0210030	16	1	RW
Diskette control/stat	0220000	1	1	RW
Diskette pointer	0220020	1	1	RW
Diskette data buffer	0220030	16	1	RW
Diskette 1797 cmd/stat	0230000	1	1	RW
Diskette 1797 track	0230010	1	1	RW
Diskette 1797 sector	0230020	1	1	RW
Diskette 1797 data	0230030	1	1	RW
DataBoard I/O	03xxxxx(See below)	1 Mb	1	RW
DMA channel 0	04000xx(x=0..FF)	256	2	RW
DMA channel 1	04001xx(x=0..FF)	256	2	RW
DMA channel 2	04002xx(x=0..FF)	256	2	RW
DMA channel 3 (Not used)				
DMA int. vector	0430000	1	1	RO
VME protection table	1xxxxxx(0..3FF000)	4 Mb	2	RW
VME access	2xxxxxx(0..FFFFFF)	16 Mb	2	RW
VME short I/O	300xxxx(0....FFFF)	64 kb	2	RW
VME int.vector	3FFFFFv(v=2 or 8)	16	2	RO
RAM base	4xxxxxx	4Mb/16 Mb	4	RW
RAM opt.1	5xxxxxx	4Mb/16 Mb	4	RW
RAM opt.2	6xxxxxx	4Mb/16 Mb	4	RW
RAM opt.3	7xxxxxx	4Mb/16 Mb	4	RW

3.4 Details of I/O-addresses.

'int. vector' : Interrupt vector to be read when an interrupt has been detected. An interrupt acknowledge cycle is simulated on the indicated circuit or subsystem.

'Width' : Indicates access mode (byte,word,long word)

'Type' : Indicates if data can be:
RO Read only, RW Read/Write, WO Write only

'SCC-channel' : n (0..F Hex) is a code for the channel number. Each SCC has two channels, where an even 'n' indicates port B and an odd 'n' port A.

Channels 0..3 are on the main board.

'n'	Channel		'n'	Channel
1	lp	(0)	9	tty08
0	console	(1)	8	tty09
3	tty02		11	tty10
2	tty03		10	tty11
5	tty04		13	tty12
4	tty05		12	tty13
7	tty06		15	tty14
6	tty07		14	tty15

'DataBoard' : A17..A12 contains card select code 0..3FH.
A19 contains bit 7 of the card select code.
A4..A2 contains I/O-strobe 0..5 if A18=0.
A18=1 Special commands. A18 is also bit 6 of the card select code.
A18=1, A4=0 Read CSB* map for card detection.
A18=1, A4=1 I/O-commands with EXP* strobe for expansion systems.

4 HARDWARE CONFIGURATION AND INSTALLATION.

4.1 Configuration of the 1121-30 board

* Processor block (CPU-plane) with the CPU, MMU, FPU and 32 kbytes cache memory. Optionally up to three more CPU planes (1120-30) can be mounted on the board, immediately above the standard block.

* Central kernel logic area, with bus access control and support for VME and DataBoard expansion. This block also contains the Boot-PROM.

* DMA block with support for the SCSI and diskette interfaces.

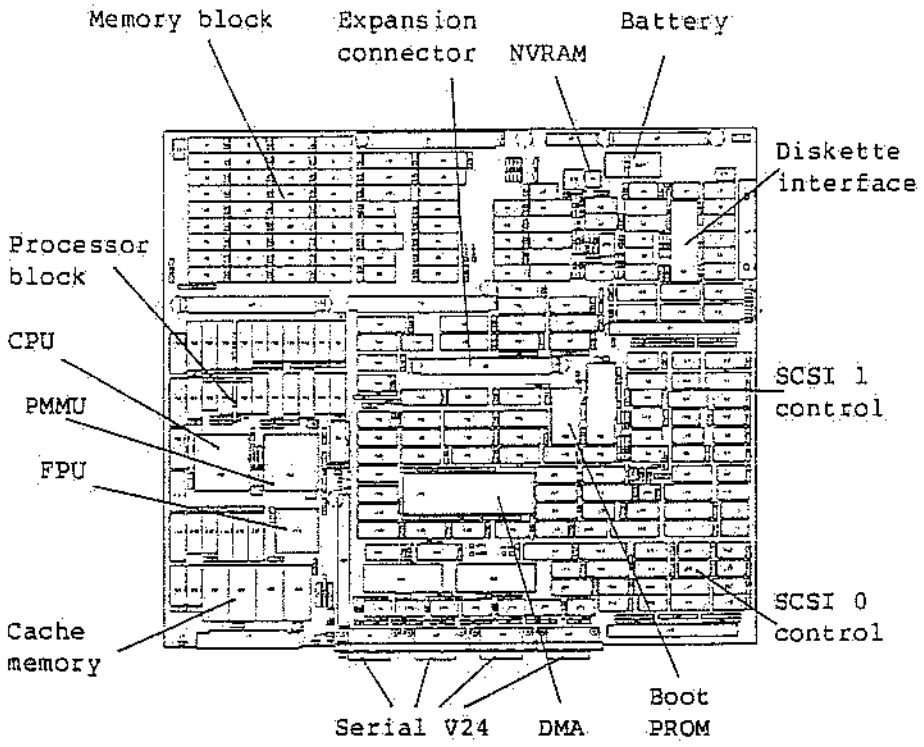
* Memory block (4 MB) and parity check logic. Up to three more memory expansion boards (2020-30 or 2022-00) can be mounted immediately above the standard memory up to a total of 28 Mbytes memory. (Up to a total of 64 Mbytes using 4 Mbit chips).

* Four serial channels. Three expansion boards (5172-10) can be mounted above this area, connected through a ribbon cable. These connectors are easily accessed from the back of the system.

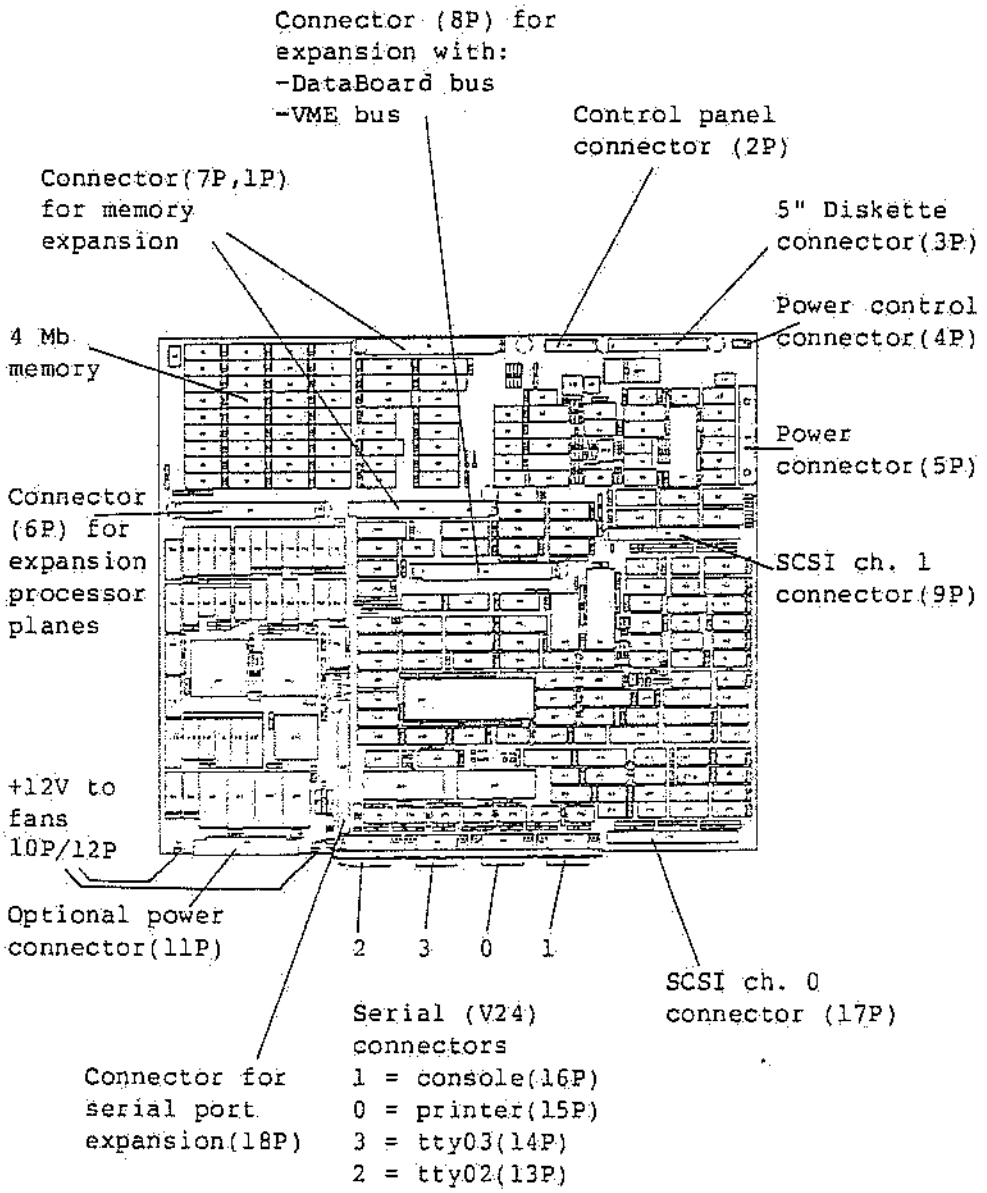
* Two independant SCSI interfaces.

* 5 1/4 inch diskette interface.

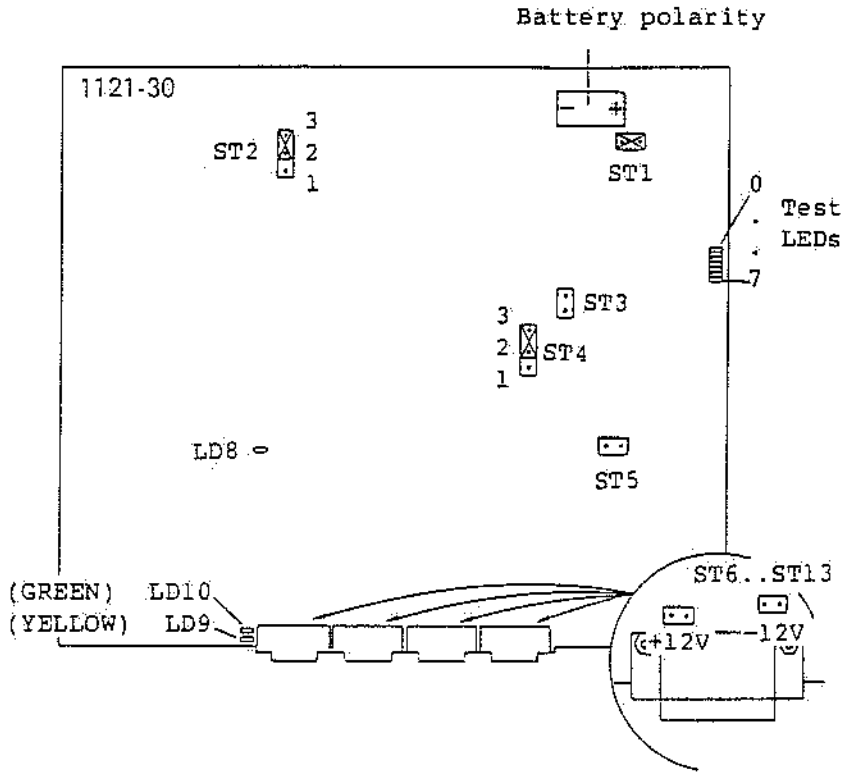
* Expansion connector for different types of expansion systems.



4.2 Connectors on the board



4.3 Jumpers and LED's



Jumpers (standard set-up indicated) ON=Closed, OFF=Open

ST1	ON	Head load on pin 4 to diskette drive.
ST2	2-3	4 Mb memory (1 Mbit chips) Select 1-2 for 16 Mbyte (4 Mbit chips).
ST3	OFF	Used to connect an NMI test switch.
ST4	2-3	32 kb BootPROM(27256), 1-2: 64 kb (27512).
ST5	OFF	Only 'on' for early warning NMI from watchdog.
ST6 -- ST13	OFF	Only 'on' to select +12V or -12V power output through serial connectors. Even jumpers for +12V and odd jumpers for -12V.

LEDs

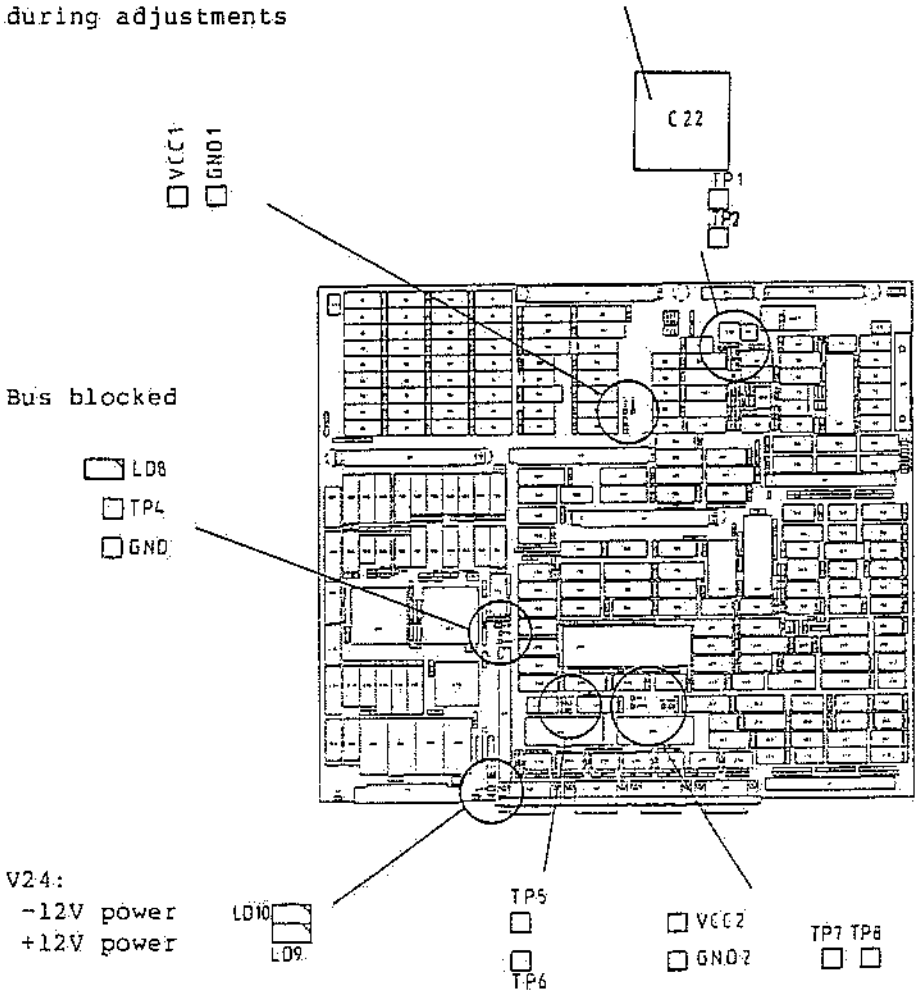
LD0..LD7	Test LEDs, program controlled.
LD8	Blinks normally. Lights up when the system bus is blocked, i.e. when a master has to wait for the bus. (See also TP4).

LD9 (Yellow) +12V to serial V24(RS232C) buffers available.
LD10 (Green) -12V to serial V24(RS232C) buffers available.

Test points on the 1121-30 computer board

Suitable +5V measuring point during adjustments

Real time clock tuning capacitor



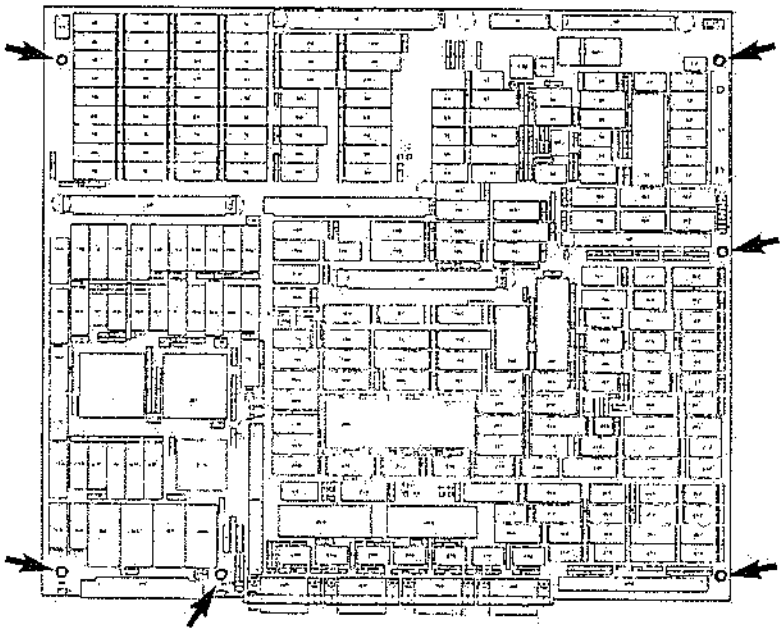
V24: Baud rate frequency * 16

Test points

TP1 Real Time Clock oscillator frequency 32768 Hz.
TP2 0V
TP3 Reserved.
TP4 System bus blocked signal. Low when blocked. See LD8.
TP5 tty03 baud rate frequency * 16
TP6 tty02 baud rate frequency * 16
TP7 printer baud rate frequency * 16
TP8 console baud rate frequency * 16

4.4 Installing the 1121-30 mechanically.

The 1121-30 board is mounted with 6 screws on distances in the computer.



4.5 Power connections.

Connect the power and the power control signals to either of the two available connectors, depending on the mechanical requirements. When an external power supply is used, the 11P connector on the back is used and the 5P connector is used with an internal supply. Power control signals can be connected to the 4P connector but is also available in 5P and 11P.

The power control signals are:

POWER* Active low power-on signal from the computer board. Normally activated by the control panel switch. Alternatively a software command can pull this output low, through an open-collector, TTL-level non-isolated circuit.

ACLOW* Power-low input signal from optional external power fail detection circuitry (UPS-option). Active low means power low. This signal should be read regularly by the operating system. Non-isolated TTL-level input.

General comments on power connection to a computer system

1 - Always use transient filter circuitry on the mains connector.

2 - The following rules apply for equipments, connected directly without galvanic isolation between them:

Always connect all equipments to the same 220V AC phase. If the distance between different equipments are large and isolated communication is not used, a separate power cable should be provided to assure this requirement.

The chassis earth in all equipments should be interconnected and should only be connected to mains earth on one point in the system.

If possible, the 0V logic level should only be connected to the chassis earth on one point in the system. This point should be close to the computer power supply.

3 - Calculate the maximum current in the +5V and +12V/-12V cables and the the total current in the 0V cables to assure that the cables selected support this current without voltage drops.

4.6 Installing peripherals, expansions and options.

Normally turn the power off before connecting any equipments. Only the external cables for the serial channels might be connected / disconnected on-line, with care.

- Control panel.
- Minifloppy (5 1/4") drives.
- Winchester drives and tape streamers.
- Terminals, printers, modems and other serial equipments.
- Floating point option.
- Boot-PROM.
- Battery.
- Memory expansion.
- Processor block expansion.
- Serial port expansion.
- Expansion backplanes.

4.6.1 Control panel

The control panel is connected through a ribbon cable to the board. Max cable length is 1 m.

4.6.2 5 1/4 inch diskette drive

Up to 3 minifloppy drives can be connected in parallel to the diskette connector (3P) through a ribbon cable. Max cable length is 2 m. The drive identity shall be set by jumpers on the drive controller to different values, normally 0, 1 or 2. The ST1 jumper is normally set to give the head load signal (HDLD*) on pin 4 in the 5" connector. For details, see the technical description.

4.6.3 Winchester disc drives and streaming tape drives

These are connected to the SCSI connectors (17P and 9P). For highest performance one drive (with controller) should be connected to each SCSI channel. The drive identities are set to 0 on both drives in this case. The following configuration is standard.

SCSI 0:	Connector 17P:	Tape streamer
SCSI 1:	Connector 9P:	Winchester drive with controller and expansion to external disks with controllers.

Note! On DS90-20, any external winchester disks are connected to SCSI 0 (14P), due to mechanical reasons.

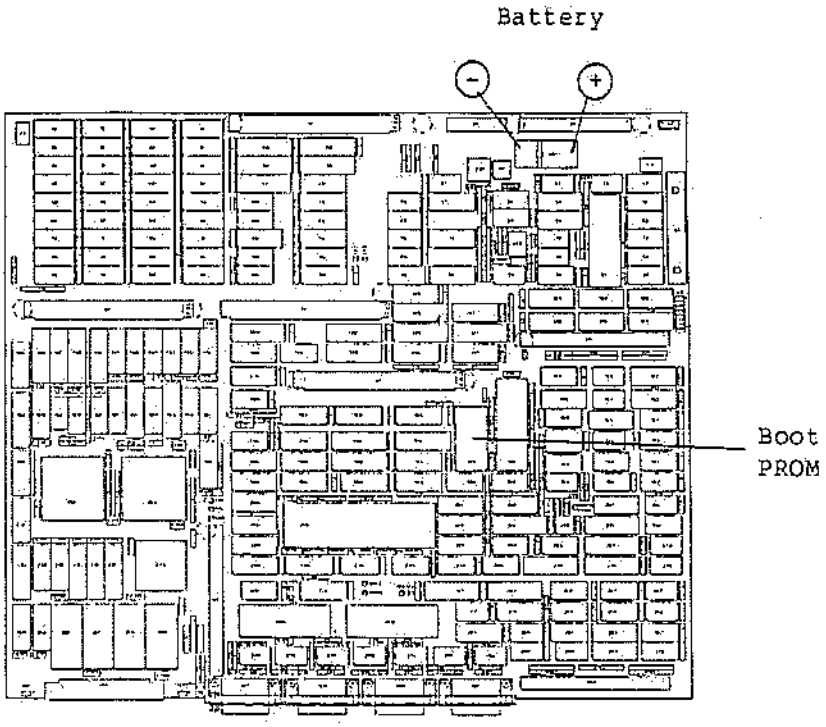
It is possible to interconnect up to 8 units with each SCSI-cable. Each unit shall have a different drive identity. The on-board SCSI-units are as standard set up with the own SCSI-identity 7, leaving the id 0..6 for the external units.

4.6.4 Boot-PROM and Battery

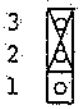
A standard boot-PROM is always delivered mounted in the system. The boot-PROM is of the type EPROM 27256 (32 Kbytes) and is mounted in the 28-pin socket (18T) near the DMA. See the figure below. The jumper ST4 can be changed if an EPROM of the type 27512 shall be used.

Battery

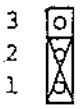
The battery is always delivered mounted in the system. The battery type is GE 013 or equivalent and the position and polarity is shown in the figure below.



ST4



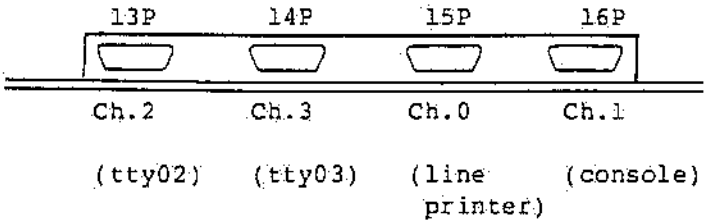
NORMAL: Boot-PROM is of the type 27256 (32 kbytes).



Boot-PROM is of the type 27512 (64 kbytes).

4.6.5 Terminals, printers, modems and other serial equipments.

These are connected at the serial ports with standard connectors. The cables shall have DA15S connectors. See the connector section for the pinning. The channel positions on the board are:



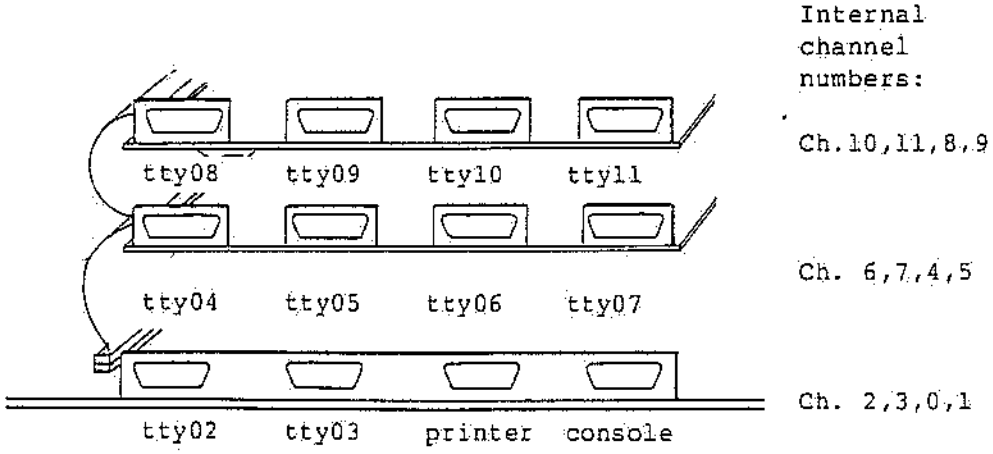
4.6.6 Serial port expansion.

Up to three serial expansion boards (5172-10) can be mounted on the chassis back plate and connected through a ribbon cable to the 18P connector on the computer board. The expansion boards are mounted above the on-board serial channels. In present computer chassies, however, only up to two boards can be mounted due to limited space.

On the expansion chassis, the tty device numbers (tty04, tty05,...tty07 etc.) are in order, from left to right, in spite of the channel number order.

The RTxC clock input is not available on the expansion connectors.

Jumpers on the 5172-10 boards shall be set to select the computer type DS90-2x and the channel number range.

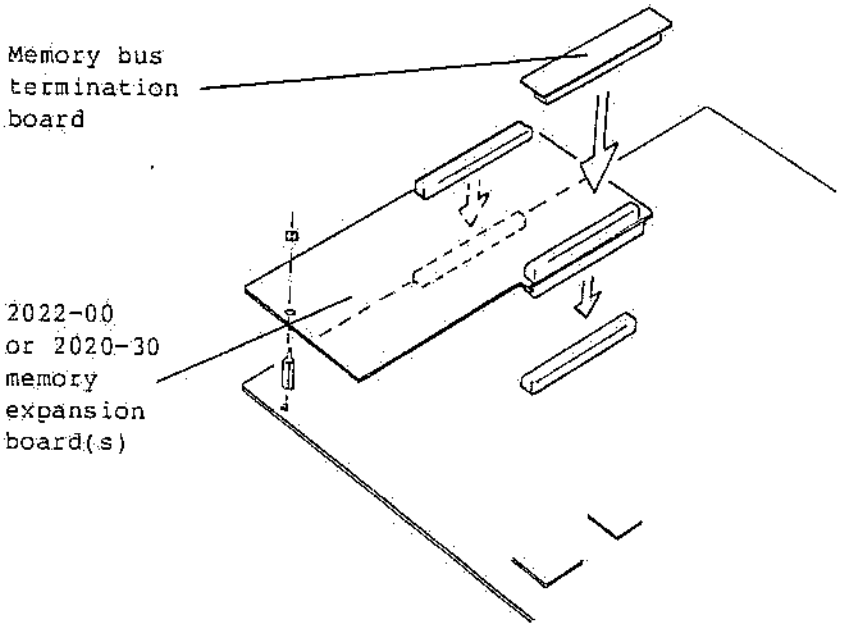


4.6.7 Memory expansion.

The onboard memory is 4 Mbytes with 1 Mbit memory chips. By replacing the memory chips with 4 Mbit RAM chips, the on-board memory will be 16 Mbytes. The parity check logic is on the main board, common to all memory.

NOTE! The 5213-00 memory bus termination board MUST always be mounted on the inner connector on the last expansion board, or on the main computer board if no expansion is used.

Up to three 2020-30 or 2022-00 memory expansion boards are mounted with screws and distances on top of the on-board memory. With three expansion boards a total of 16 - 28 Mbytes memory is achieved, using 1 Mbit memory chips with 2020-30 or 2022-00 boards. With 4 Mbit chips on all boards and on the main board, up to 64 Mbytes memory can be used.



The identity of the memory expansion boards are set by using the proper configuration circuit according to the following table.

2020-30:	Memory board	Circuit 4N	Circuit 7M
4 Mb	3	pat 1083-1	pat 1061-1
	2	pat 1083-1	pat 1061-0
	1	pat 1083-0	pat 1061-1
	main board	pat 1083-0	pat 1061-0

2022-00:	Memory board	Circuit 7S	Circuit 4N
8 Mb	3	pat 1089-1	pat 1061-1
	2	pat 1089-1	pat 1061-0
	1	pat 1089-0	pat 1061-1
	main board	pat 1089-0	pat 1061-0

4.6.8 Processor plane expansion.

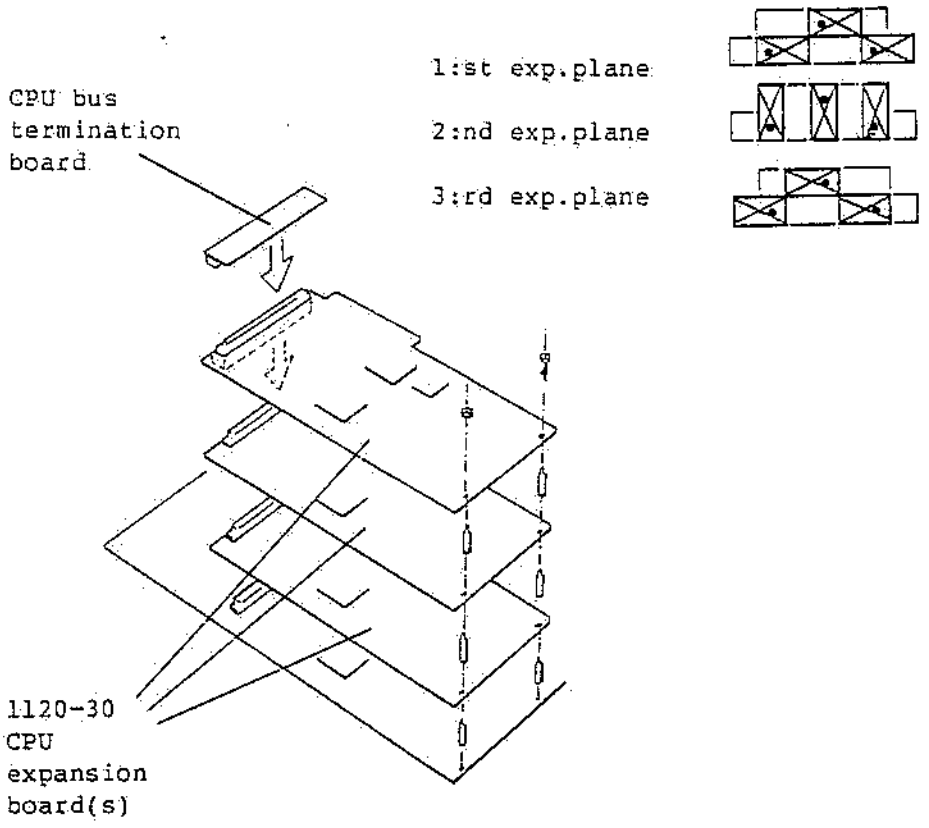
The 1121-30 board contains an expansion connector and logic to handle up to four parallel processor planes, mounted on separate boards directly on top of the standard processor block area.

Each block contains a complete CPU-plane with a MC68020 CPU, a MC68851 PMMU, a MC68881 FPU and 32 kbytes cache memory.

The processor expansion boards are mounted with screws and distances on top of the on-board CPU-plane area.

NOTE! The 5212-00 CPU bus termination board MUST always be mounted on the connector on the last expansion board, or on the main computer board if no expansion is used.

Three jumpers on each processor plane must be set to select the correct control strobes for plane 1, 2 or 3. These jumpers controls the CPU attention interrupts and the bus requests and grants.



4.6.9 Expansion backplanes.

Expansion back planes are inserted in the expansion connector in the center of the computer board, with any expansion slots turned to the back above the serial channels.

Mechanically the backplane with its guides for the expansion slots are mounted on the chassis.

5. TECHNICAL DESCRIPTION

5.1 Processor planes

Each 1120-30 processor plane contains the MC68020 CPU, the MC68851 PMMU (paged memory management unit), the MC68881 FPU (hardware floating point unit) as well as a 32 kbytes cache memory area with supporting circuits.

The CPU-plane 0 on the main board always handles all hardware interrupts as well as hardware reset. Reset of the expansion CPU-planes are handled by the CPU attention register.

Note! It is not allowed to issue a software reset instruction as this signal does not reset all subsystems.

Three jumpers on each expansion plane (1120-30) shall be set differently to identify each CPU-plane. CPU-plane 0 is always on the main board.

The jumpers are shown in the previous installation section.

5.2 CPU Attention registers

The different CPU-planes execute independant of each other, and the communication between the CPU's is handled by the CPU attention registers.

An attention interrupt on level 5 can be issued to any CPU-plane (including plane 0), by writing to the CPU attention register for the selected CPU-plane. Any memory location can be used as common for information, providing the cache is disabled for the used memory.

NOTE! Before a write attempt to the attention register, it should be tested to be passive. An indivisible byte access cycle shall be used when updating the register.

The reset of the slave CPU-planes (planes 1, 2 and 3) are software controlled through the reset attention register.

After a hardware reset or power on, the CPU attention registers are set active (0FFH) by hardware and the slave CPU-planes are held in a reset condition until the main CPU has set up the system and released the reset attention registers.

NOTE!! The software reset instruction may not be issued in this system, as it is not connected to all subsystems.

Assert interrupt to a selected CPU-plane:

```
Address: 001000n Hex physical address, n=0,4,8,0CH
         n indicates the CPU-plane, 0..0CH => Planes 0..3.
Access:  Byte access.
Write:   Assert/deassert IRQ5 on respective CPU-plane.
         Data bit 31: 1=Assert, 0=Deassert.
Read:    Read the value, 0FFH if asserted, 0 if not asserted.
```

After detection of an attention interrupt request, the CPU interrupt attention register should be reset by the receiving CPU to the passive value (0), to indicate its presence. At system start, one slave CPU at a time is activated and detects which plane it is by reading the interrupt attention registers to find out which is active. This is necessary as the same boot PROM program is used for all CPU planes.

Assert reset to all slave CPU-planes (1-3):

```
Address: 0010100 Hex physical address
Access:  Byte access.
Write:   Assert/desassert RST to CPU-planes 1, 2 and 3.
         Data bit 31: 1=Assert, 0=Deassert.
Read:    Read the value, 0FFH if asserted, 0 if not asserted.
```

The slave CPU planes are held at reset until the main CPU releases the reset attention register. Only the main CPU can read the value 0FFH from the reset attention register.

5.3 Bus arbitration and memory protection

Bus arbitration

In a high performance multi-processor system efficient hardware arbitration and protection logic is required to allow sharing of the system resources.

The arbitration logic resolves the bus requests using a "round robin" algorithm. The use of cache memory on all CPU-planes in combination with very fast arbitration logic provides a high throughput on the system bus. System bus requests can be issued from any of the following units:

- from any of 4 CPU-planes
- from DMA for SCSI or diskette I/O
- from memory refresh logic
- from current VME-bus master

For testing purposes the LD8 LED, positioned close to the FPU, is turned on at bus requests which can not be immediately served. The light intensity of this LED will in this way be higher at a high bus load when several bus masters compete for the bus resource. This bus load signal is also available on the TP4 test point.

See the section about VME for bus requests TO the optional VMEbus expansion boards.

Memory protection

The paged memory management units (PMMU) on each CPU-plane provides protection, logical to physical address mapping and virtual memory support towards the system resources as well as for access to expansion units with a page size of 4 kbytes.

The DMA works directly with physical addresses in the main RAM memory towards the SCSI and diskette interfaces.

Note that the different access protection and address translation functions in the system, including the cache memory handling, are independant. It is the responsibility of the operating system to assure that no protection violation occurs.

5.4 System clocks

The present CPU-clock is 16.67 MHz, but the system is designed to allow a system clock frequency up to 20 MHz, still working without wait-states at accesses to the cache memory.

Separate clocks are used for the peripherals to achieve independance of the CPU-clock.

For the baudrate generation on the serial channels (SCC) a 1231 kHz clock is available.

A 16 MHz clock is available on the expansion connector for the VME-bus expansion and is used in the diskette interface.

A separated 32768 Hz crystal is used for the real time clock, having battery backup. From this clock a 64 Hz interrupt signal is derived for the operating system date and time clock.

5.5 Cache memory

5.5.1 Cache memory segmentation

To increase speed (zero wait states) and decrease the system bus load, each CPU-plane is provided with its own cache memory. An efficient solution with a high cache hit rate requires a fairly large cache memory.
Each cache memory is 32 kbytes and works in the physical address space. The cache is divided into 8 logical segments, each with the size of one page, 4 kbytes. One logical segment is used for each of the logical address types and in addition separate segments are used for the data area and stack data area, assuming that the logical address bit A30 separates these two areas in the logical memory.

NOTE! For best performance the software should separate the data and stack area by the logical address bit A30. This subdivision conforms to the used pages size of the memory management unit and enables a high cache hit rate.

Segment name	FC2	FC1	A30
User data	0	0	0
User stack data	0	0	1
User program code low address	0	1	0
User program code high address	0	1	1
Supervisor data	1	0	0
Supervisor stack data	1	0	1
Supervisor program code low address	1	1	0
Supervisor program code high address	1	1	1

5.5.2 Cache memory features

The cache system features a line size of 128 bits, write through and fast invalidate.

When a byte, word or long word not present in the cache memory is needed, it has to be loaded from the main memory. However, to reduce overhead, a total of 16 bytes are always loaded in one memory cycle, a page mode cycle of 4 times 32 bits.

To make sure that the main memory always contains correct data, without extra cache handling overhead, the "write though" approach is used. Every write access goes directly to the main memory and only if there already is an entry in the cache with this address, also the cache is updated.

When new data is loaded into memory by another CPU-plane, DMA or a VME-bus master, it is essential to force cache loading at the next access to this memory area. This is done by an access (read or write with dummy data) to one of two special addresses in "CPU-space". (Compare section 3).

- Invalidate all user entries in the cache: 002C000 Hex
- Invalidate all supervisor entries in the cache: 002E000 Hex

5.5.3 Cache inhibit

Some areas of the physical address space may not be cached, for example I/O-space and memory areas common to two or more CPU-planes, DMA or VME-bus masters. In this implementation only the main RAM memory may be cached. PMMU initiated cycles to fetch map tables from a common RAM area will not be cached.

The operating system software shall define which pages shall be cashable or not cashable. This is done by PMMU commands by defining the PA31 address bit in the page descriptor. Note that the CI bit is not used on the PMMU. See the MC68851 PMMU manual for the commands.

PA31 = 1 This page will be cashable.
PA31 = 0 Not cashable.

5.5.4 Cache memory implementation

The cache system consists of data RAM, tag RAM, valid RAM and tag comparators and is local for each CPU-plane.

The data RAM size is 8k long words, addressed with FC2, FC1, A30 and A11..A2, where A30 is a logical address bit and Ann indicates physical address bits. When the CPU writes to an address, present in the cache, the cache can be updated when writing in byte, word or long word mode, by using separate write strobes for each byte. The maximum allowed RAM access time is 100 ns, using 16 MHz CPU-clock.

The tag RAM is addressed with FC2,FC1,A30 and A11..A4. The data stored in this memory is the high physical address bits PA27..PA12, which is the page tag. Write in tag RAM will only be done during cache load. The maximum allowed RAM access time is 45 ns, using 16 MHz CPU-clock.

The valid RAM is addressed as the tag RAM. It contains the valid bit for each tag address. At cache load a one is written to the valid bit, marking the entry valid. Physically the RAM is split in two circuits, one for user entries (FC2=0) and one for supervisor entries (FC2=1). As the circuits features chip reset, two logical addresses in CPU-space are used to separately clear (invalidate) all user or all supervisor entries in the cache without affecting the other. See 'cache memory features' above. The maximum allowed RAM access time is 45 ns, using 16 MHz CPU-clock.

The tag comparators compare the actual physical address bits PA27..PA12 with the value stored in the tag RAM. If equal and the valid bit is set, the data is taken from the cache data RAM, a cache hit is achieved. If the required address is not found or not valid, the CPU cycle is rerun and a cache load bus cycle is requested.
If on the other hand the address bit PA31 is zero, caching is disabled and data will be directly accessed from the bus.

5.5.5 Cache test and verify

For test purpose, logical addresses 2Gb - 4Gb are reserved for reading the cache tag information (logical A31 high). When reading with the logical address bit A31 high, no bus cycles or re-run will be generated in the system. Instead a 32 bit data value will be read containing the following data.

One cache RAM position is accessed. The tag comparator compares the physical address with the tag address bits and returns the value 0 if they are equal, providing also the corresponding valid bit is 1. The tag address bits PA27..PA12 are always returned together with the valid bit.

Bit	Function
31..20	-- Reserved for future use. Unspecified at read. --
19	Cache comparator output, PA27..PA20. 0 = Equal.
18	Cache comparator output, PA19..PA12. 0 = Equal.
17	-- Reserved for future use. Unspecified at read. --
16	Valid bit. 1 = Valid
15..0	Tag address bits PA27..PA12

Testing of the data RAM can be done in the following order:

a) The memory area with the test program should be non-cachable.
b) Select a physical memory page (4 kbytes) in the main RAM area as test area and define it as cachable.
c) Do the test for each of the 8 cache segments (4 kbytes):
   - Write all zeroes to the test area. The cache is not affected.
   - Verify the test area. In this way data = 0 is loaded to all positions in the cache segment and all entries are made valid.
   - Write and read check patterns, testing cache data RAM.
   - Check tags for correct page information and validity as below, to ensure the data RAM test was correctly performed.

Testing of the tag RAM can be done in the following order:

a) The memory area with the test program should be non-cachable.
b) Select two or more physical memory pages (4 kbytes) in the main RAM area as test area and define it as cachable. The physical addresses shall differ in as many bits as possible.
c) Do the test for each of the 8 cache segments (4 kbytes):
   - Do a dummy read for data in the first word of the first test page to initiate a cache load cycle and a tag RAM write.
   - Verify the tag RAM, by a new read at the same address but with the logical address bit A31 high.
   - Verify the tag RAM by selecting an address in another page and A31 high. This time the tag comparators should signal "not equal".

5.6 Main memory, Memory management (PMMU)

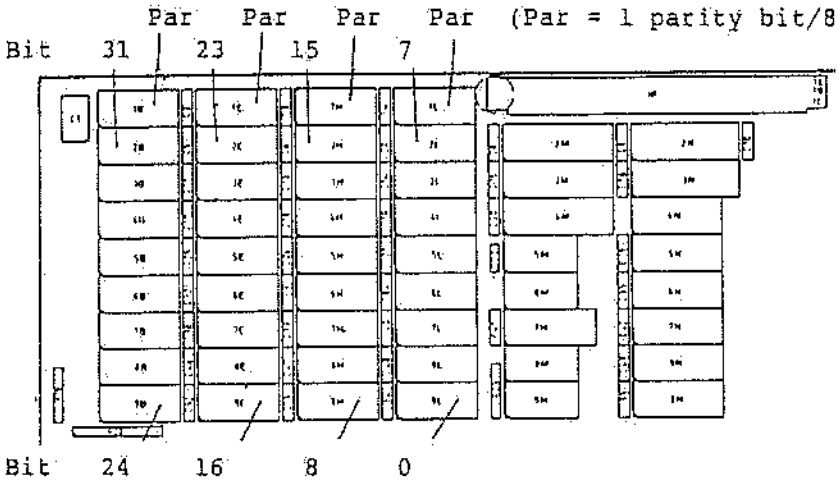
The main board is equipped with 4.0 Mbytes dynamic RAM memory in 36 chips with 1 Mbits each. A 32 bit data bus is supported and the memory is configured to use one bit from each chip to form one long word (32 bits + 4 parity bits).

The onboard logic for parity generation and detection requires 1 extra bit per 8 bit byte.

The RAM circuits shall be 100 ns dynamic RAM when the CPU-clock 16.67 MHz is used. Example: TC511000P-10 or equivalent.

By replacing the memory chips with 4 Mbit chips, the on-board memory will be 16 Mbytes.

The memory layout with 1 Mbit circuits is given in the figure below. The data bits in each 32 bit word is indicated in addition to the four parity bits.



Memory management unit (PMMU)

The paged memory management unit PMMU (MC68851) on each CPU-plane provides address translation from logical to physical addresses, access protection and virtual memory support.

In this system the page size shall be 4 kbytes and up to 2 Gbytes of logical memory per process is mapped to a maximum of 128 Mbytes physical address area (PA0..PA26). In addition, each page in the physical memory area can be defined as cachable or not cachable by specifying the physical address bit PA31 in the PMMU page definition. Note that the CI bit in the PMMU is not used.

NOTE! Each CPU-plane contains one PMMU and all PMMU's should use the same map tables in a common memory area. The cache is automatically disabled at PMMU-initiated cycles to fetch map table data.

For programming details, see the Motorola MC68851 PMMU manual.

5.7 Parity error handling

The parity check logic is on the main board and used for the main RAM memory, including any expansion RAM.

At each write to the RAM memory, the parity logic adds one parity bit for each 8-bit byte. This is done also if the parity is disabled (Se below).

At each read from the RAM memory, the parity logic tests the parity. If a parity error occurs, the parity syndrome register is updated and a bus error is generated, if enabled, to be trapped by the operating system.

The bus error generation at a parity error can be enabled or disabled and the parity can be defined as even or odd through port B on the CIO.

After a parity error has occurred, a parity syndrome byte can be read at the physical address 0010030 Hex. After reading, the parity syndrome register should be cleared by writing any dummy value to this address. Write access will set bits 7 and bits 3..0 to 1.

If a parity error caused by a DMA access is detected, the DMA operation is aborted and the program should read the appropriate DMA register to detect the error.

NOTE!
Always check the parity syndrome register after each completed DMA transfer from the RAM memory, as a parity error at the last long word transferred is never detected by the DMA.

Parity syndrome byte: At physical address 0010030 Hex.

Bit	Function
7	0 = Parity error at DMA access
6..4	-- Reserved. Unspecified at read.
3	0 = Parity error on memory data 0..7
2	0 = Parity error on memory data 8..15
1	0 = Parity error on memory data 16..23
0	0 = Parity error on memory data 24..31

5.8 System control.

General system control is performed through a CIO circuit (Z8536A). The CIO is connected to the system interrupt level 2.

The CIO port A is used to detect interrupt signals from the SCSI and floppy interfaces as well as from the DataBoard extensions. 4 DataBoard interrupt levels are supported. The hardware signals are active low (0) except for the diskette interface. For this reason, the CIO port A should be programmed for inverted input on bits 1..7 and non-inverted on bit 0. With this set-up, active signals correspond to the data bit values below. System interrupt shall be given on any of these signal.

Bit	Function
7	In 1 = SCSI 0 interface interrupt
6	In 1 = SCSI 1 interface interrupt
5	In 1 = IRQ5* DataBoard 4680 interupts (scanner)
4	In 1 = IRQ4* DataBoard 4680 interupts
3	In 1 = IRQ3* DataBoard 4680 interupts
2	In 1 = IRQ2* DataBoard 4680 interupts
1	In 1 = IRQ1* DataBoard 4680 interupts
0	In 1 = Diskette interface interrupt

The CIO port B provides a number of hardware control signals and supports a few input signals. The hardware control signals are active low (0). For this reason bits 7..3 shall be defined as inverted outputs and bits 2..0 as inverted inputs. With this set-up, active signals correspond to the data bit values below.

Bit	Function
7	1 = Enable buss error generation on RAM parity error
6	1 = Even RAM parity / 1 = odd parity.
5	1 = Turn the "IDLE" console lamp ON.
4	1 = Enable VME subsystem (Release SYSFAIL*).
3	1 = Power off sent to the hardware system.
2	In 1 = SYSFAIL* from the VME subsystem.
1	In 1 = Console key in "OFF" position. 1 = "AUTO" pos.
0	In 1 = DMA interrupt request.

The CIO port C is used to access the onboard real-time clock and the NVRAM. Both are accessed serially, with a software generated transfer clock on one bit of the CIO-port.

For details on the CIO ports A and C, see sections about interrupts, NVRAM, Real-time clock, DataBoard expansion as well as the CIO manual (ref 5).
The physical access addresses to the CIO are:

```
CIO Port C data: 0020000 Hex
CIO Port B data: 0020010 Hex
CIO Port A data: 0020020 Hex
CIO Control:     0020030 Hex
CIO int.vector:  0030000 Hex
```

5.9 System boot and Power-up/Power-down sequence.

The system is restarted about 1 second after power-on or after a reset signal from the control panel switch or the watchdog circuits.

The Boot-PROM is one 27256 EPROM (32 kbytes) with a start-up program, executed at power on. Optionally a 27512 EPROM (64 kbytes) may be used.

For details on the power-up and power-down sequencies, see the maintenance manual for the used system.

Power-on.

The default status after power on is with any expansion CPU-planes disabled by RST status in the CPU attention register and any VME master access to the main system disabled by a passive high level on all CIO port B bits. The internal test LEDs are turned off and the PMMU is reset. When reset is released, the main CPU starts executing at the boot-PROM address 0.

Normally the boot-PROM contents are copied to RAM after initial tests and handshaking between the CPU-planes. The main CPU normally loads the operating system.

Power down.

The "power off" control bit in the CIO port B is be used for software controlled power down, as a low level out (0) on this port is required to disactivate the POWER ON output signal in the power connector.

After detection that the control panel key has been turned from "AUTO" to the the "OFF" position (CIO port B, bit 1) the operating system can make a controlled shut-down before turning the power off.

5.10 Hardware interrupt system.

At hardware interrupts, the system is designed to use autovectors. During an interrupt acknowledge cycle from the hardware, the processor fetches one of 7 possible autovectors. Further identification of an interrupt source is possible by reading interrupt vector registers, associated with each interrupt level. Reading these registers simulates interrupt acknowledge cycles, fetching the appropriate vector from the VME, SCC or CIO subsystems. Processors on optional CPU-planes can only respond to hardware interrupts on the levels 7 and 5 (marked *).

Int. level	Source	Vector source
7 *	NMI* (push button or early warning)	None
6	RTC-interrupts (64 Hz)	None
5 *	Attention between processor planes	None
4	VME interrupt high level	From VME
3	Serial communication channels	Resp. SCC
2	I/O-subsystem through CIO	CIO
1	VME interrupt low level	From VME

Level 7 .NMI*

This level is a non-maskable interrupt. On the jumper pins ST3, an external NMI* push button can be connected, initiating interrupt when closed. In addition the ST5 jumper can be closed to enable the early warning signal from the watchdog to generate an NMI* interrupt. See the Watchdog desription.

Level 6 RTC-interrupt

Here a 64 Hz clock signal is detected as clock tics for the system data and time clock. The signal is derived from the Real-Time clock on the board. This interrupt must be reset by a write access to the physical address: 0010020 Hex.

Level 5 CPU attention interrupt

Any CPU-plane can request attension from another specified CPU-plane by writing to the CPU attention register, asserting the level 5 interrupt request line.

Level 4 VME high level interrupt

At an interrupt from a VME source on this level, the 8 bit vector is read from the source at the physical address 03FFFFF8 Hex. Only a "Read Word" access is legal and the AM* bit on the VME bus will indicate supervisor data access.

Level 3 Serial channels interrupt

Reading the 8-bit vector from the physical address 0130000 Hex will read from the SCC channel, issuing the interrupt request. The SCC channels are daisy chained with channel 0 having the highest priority.

Level 2 CIO interrupt

Reading the 8-bit vector from the physical address 0030000 Hex will read from the CIO circuit indicating which port is requesting service. The CIO ports are daisy chained as listed below with the highest priority first.

If a DataBoard interrupt scanner is used, it should be connected to XIRQ5* on the CIO port A.

CIO port/bit	Interrupt source
Counter/timer 3	User defined
Port A, bit 7	SCSI 0 interface interrupt.
Port A, bit 6	SCSI 1 interface interrupt.
Port A, bit 5	XIRQ5* DataBoard expansion.(Scanner)
Port A, bit 4	XIRQ4* DataBoard expansion.
Port A, bit 3	XIRQ3* DataBoard expansion.
Port A, bit 2	XIRQ2* DataBoard expansion.
Port A, bit 1	XIRQ1* DataBoard expansion.
Port A, bit 0	Diskette interface interrupt.
Counter/timer 2	-- user defined --
Port B, bit 2	SYSFAIL* from the VME subsystem.
Port B, bit 1	Console key in "OFF" position.
Port B, bit 0	DMA interrupt request.
Counter/timer 1	-- user defined --
Port C ,,	No interrupt. (NVRAM/Real Time clock).
Counter/timer 0	No interrupt.

Level 1 VME low level interrupt

At an interrupt from a VME source on this level, the 8 bit vector is read from the source at the physical address 03FFFFF2 Hex. Only a "Read Word" access is legal and the AM* bit on the VME bus will indicate supervisor data access.

5.11 Bus errors.

The hardware generates a bus error (BERR*) signal on the following conditions.

Note that bus errors caused by DMA accesses are trapped by the DMA and not the CPU.

NOTE! See the limitation described in the DMA section.

Bus errors are generated at:

- Illegal accesses detected by the PMMU.
- Parity error detected during read from the RAM memory, provided the parity check is enabled. Bus error can be generated both from read accesses from the DMA and from any CPU or from a VME master accessing the main memory. After a detected bus error, the parity syndrome byte should be read.
- VME-bus timeout at an access to the VME-bus after 512 retries, if the VME expansion backplane is not installed or if a bus master on the VME bus does not release the VME-bus.
- VME-bus timeout (11.5 microseconds) if the VME-bus has been granted but the addressed slave does not respond.

5.12 Watchdog with early warning and RTC interrupt reset.

The watchdog counter generates a system reset unless regularly pushed by software (within 1.2 seconds interval).

The watchdog can be pushed only in system mode by READING at the physical address 0010020 Hex. The data read is unspecified.

READ address to the watchdog is: 0010020 Hex.

An early warning signal is generated 1 second after the last watchdog push. This signal can generate a non-maskable interrupt if enabled by the jumber ST5.

RTC interrupts on level 6 for the system timing must be reset after detection by a write access to the same address which is used for the watchdog. The data written is ignored.

WRITE address to the RTC reset is: 0010020 Hex.

5.13 Real-Time clock with battery backup.

The MEM E050-16 real time clock (RTC) circuit is accessed serially through the CIO-port C. It is only accessible in system mode. Note that also the NVRAM is accessed through the CIO-port C. The port C data bits 2 and 3 select either device.

A 2.4V battery (type GE 013) is used for battery backup and retains the timing at power-off during at least 30 days.

A separate 32768 KHz crystal controls the timing. A tuning capacitor is provided for adustments (C22), which is near the 5 1/4" diskette interface connector.

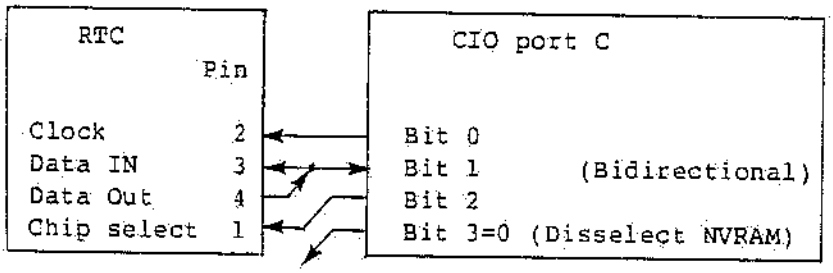
For programming details, see the manual for the MEM E050-16 circuit (ref 7). Below is a short general description.

Time data is transferred serially, using bit 0 in the CIO-port C as transfer clock and bit 1 to transfer the data bit by bit.

The RTC-circuit contains 6 time registers, each with one byte of data. A 4-bit command sent to the RTC selects a register and read/write operation, either for single byte transfer or for transfer of all 6 registers. If all registers are transferred, they are in the order: Hour, Minutes, Date, Month, Year, Day-of-week, Seconds.

Registers		Value
0	Seconds	00 .. 59
1	Minutes	00 .. 59
2	Hours	00 .. 23
3	Date	01 .. 28/29/30/31
4	Month	01 .. 12
5	Day-of-week	01 .. 07 (01 = Monday)
6	Year	00 .. 99
(7	Selecting register 7 gives transfer of all registers)	

The access address is: 0020000 Hex for port C data.
0020030 Hex for general CIO control.



Chip select: Low(0) to activate the RTC. High between commands.
Clock Bit-transfer clock. Rising edge transfers one data bit into the RTC, falling edge transfers a bit when reading from the RTC.
Data: Bidirectional data port.
Bit 3: = low(0) to dis-select the NVRAM.
Note: Data bits 4..7 on the CIO port C is a protect mask, when writing to the port. See the CIO datasheet.

5.14 NVRAM Non-Volatile RAM for parameter storage.

For non-volatile storage of 32 bytes of boot parameters, an NVRAM circuit of the type NMC9306 is used.

Data is erased/read/written as 16-bit words serially, using the CIO port C. It is only accessible in system mode. A word must be erased before writing new data. Erasing can also be done of the entire NVRAM with one command.

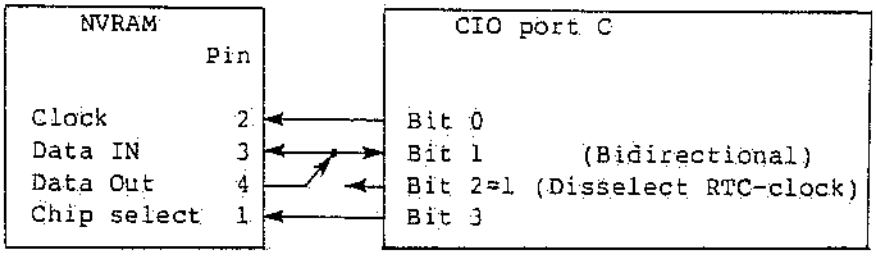
For programming details, see the manual for the NMC9306 circuit (ref 6). Below is a short general description. Note that also the real-time clock is accessed through the CIO-port C. The port C data bits 2 and 3 select either device.

Commands and data are transferred serially, using bit 0 in the CIO-port C as a transfer clock and bit 1 to transfer the data bit by bit.

Available commands are:

READ	Read one 16-bit word
WRITE	Write one 16-bit word
ERASE	Erase one 16-bit word
ERAL	Erase the entire NVRAM
EWDS	Disable erase/write
EWEN	Enable erase/write

The access address is: 0020000 Hex for port C data.
0020030 Hex for general CIO control.



Chip select:	High(1) to activate NVRAM. Low between commands.
Clock	Bit-transfer clock. Rising edge transfers one data bit.
Data:	Bidirectional data port.
Bit 2:	= high(1) to dis-select the real time clock.
Note:	Data bits 4..7 on the CIO port C is a protect mask, when writing to the port. See the CIO datasheet.

5.15 Display register with LED's

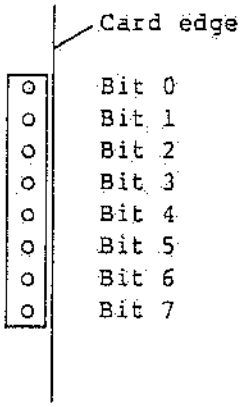
The computer board contains an array of 8 LED's to be used for system test and diagnosis purpose. The LED's are positioned close to the diskette interface and are controlled by writing an 8-bit byte to the physical address 0010010 Hex. Each bit controls one LED and a bit value '1' turns on the LED.

The recommended use is to let each 8-bit value indicate one defined system state.

Example: 8 bit values displayed when starting a DS90-2x system.

0 : Default system reset value.
1 : Boot program in EPROM started.
2 : CIO has been initiated and the boot-PROM copied to RAM.
3 : PMMU has been initiated and the parity error logic activated.
4 : NVRAM has been read.
5 - 8 : During loading of the stand-alone operating system

LED number 7 will flash if a memory error occurred during start-up.



The use of these LED's are system dependant and they may be used differently by any test program.

5.16 Serial communication channels.

Four (4) serial channels are available on the main board in two SCC circuits (28530A).

```
Channel 0 (SCC 0, port A) = /dev/lp       (line printer)
Channel 1 (SCC 0, port B) = /dev/console
Channel 2 (SCC 1, port A) = /dev/tty02
Channel 3 (SCC 1, port B) = /dev/tty03
```

Up to 3 expansion boards (type 5172-10) can be connected, each with 4 channels, if the mechanical design allows it, with the channel numbers 4..15. If more serial channels are required, VME terminal concentrator expansion boards are used.

The serial channels support asynchronous communication according to the V24(RS232C) standard. However the RI ring indicator input signal and external TRxC clock input is not supported. Furthermore the RTxC input signal on the connector is fed to the TRxC pin on the SCC circuit.

Baudrate is generated from a 1231 kHz clock signal input on the RTxC pin on the SCC circuits, allowing baudrates up to 76800 baud. This clock signal is independant of the CPU-clock.

Each serial channel can be separately protected through the PMMU system, using 4 kbytes page size.

Interrupt requests from the SCC channels are daisy chained on system level 3 and each channel can be programmed to give separate interrupt vectors. At interrupt the vector from the channel with highest priority is read from the physical address 0130000 Hex.

For programming details, see the SCC manual (ref 4).

The physical access addresses to the serial channels are as below. Byte mode shall always be used at access. Even 'n' is channel B and odd 'n' is channel A. 'n' = 0 .. F Hex.

```
010n000 Hex Control register channel code 'n'.
011n000 Hex Data    register channel code 'n'.
0130000 Hex Read the SCC interrupt vector.
```

Channels 0..3 are on the main board.

Channel	'n'	Name	Channel	'n'	Name	
0	1	lp	8	9	tty08	
1	0	console	9	8	tty09	**NOTE!**
2	3	tty02	10	11	tty10	'n' is not
3	2	tty03	11	10	tty11	equal to the channel
4	5	tty04	12	13	tty12	number!
5	4	tty05	13	12	tty13	
6	7	tty06	14	15	tty14	
7	6	tty07	15	14	tty15	

5.17 Direct memory access (DMA) logic.

The HD 68450 DMA controller is used. Three DMA channels (0..2) can work simultaneously, supporting high speed data transfer between the memory and the following I/O-devices.

Channel	Device
0	SCSI interface 0.
1	SCSI interface 1.
2	Diskette interface.
3	-- Not used --

For each device, a 16 bytes hardware buffer is used, with hardware controlled external handshaking. High speed burst data transfer is used between the DMA and the buffers.

DMA set up parameters:

The DMA accesses memory with physical addresses and every DMA cycle tranfers one long word (4 bytes). Therefore the memory address and byte count values stored in the DMA registers shall be according to the following rules.

Note that memory pages used at DMA must be locked in memory during the transfer.

- Tranfer count shall be equal to the number of long words to transfer (not the number of bytes). The mimimum transfer size is 4 long words (=16 bytes). The maximum block size is 256 kbytes (64 k * long words).
- The physical memory address loaded to the DMA 'MAR' register must be shifted right two steps in order to compensate the 2-bit address shift between the DMA and the real physical memory address.
- Single address mode.
- Byte operand transfer.
- Burst transfer mode.
- The PCL shall be programmed as abort input.
- The transfer direction from memory to device. The real direction of the transfer is controlled by hardware.
- Transfer on REQ* signal.
- Incrementing of the memory address.
- All channels must be programmed to the same priority level.
- The memory function code must be equal to the channel number (0..2) as the hardware uses the FC outputs in order to find which channel is actually served.
- The base function code must be equal to channel number + 4.
- The device function code is not used (single address mode).
- Any linked list table in the memory with setup address/count values must conform to the limitations:
  - -- All operands shall be located at physical memory addresses with the address bit PA2=1.
  - -- The first word operand must be located at a long word boundary.
  - -- Every next word operand must be offset by 8 bytes.

DMA register access:

DMA registers are addressed on the physical addresses:

DMA channel 0	040000xx Hex
DMA channel 1	040001xx Hex
DMA channel 2	040002xx Hex

At interrupt from the DMA, the DMA interrupt vector is read from the physical address 0430000 Hex.

The DMA registers can only be properly accessed using byte or word operations. (No "long word" access is permitted).

Any DMA register address ('xx' above) is a converted address, calculated from the register number ('Nr') in the DMA manual by the following formula:

'xx' = ((Nr AND 0FEH) * 4) + (Nr AND 1) + 4

DMA interrupt:

Any DMA channel can be programmed for interrupt generation. DMA interrupts are passed to the hardware level 2 through the CIO port B, bit 0. At an interrupt the CPU first reads the CIO interrupt vector at the physical address 0030000 Hex and detects the DMA interrupt on CIO port B, After this the DMA interrupt vector is read from the physical address 0430000 Hex in order to check which DMA channel has generated the interrupt.

Note that both normal and error interrupt vectors registers in the DMA shall be programmed with specific values to identify the interrupt source.

For further details on DMA programming, see the manual for the HD68450 DMA circuit (ref 2).

Parity error during DMA transfer:

If a parity error occurs during a DMA memory read cycle, the channel operation will be immediately aborted. The bus error signal does in this case not reach the CPU. After DMA abort, timeout will interrupt the CPU, which can detect the abortion in a DMA register and perform suitable corrections. If a device is accessed, it will still wait for more data.

NOTE!
Always check the parity syndrome register after each DMA transfer from the RAM memory, as a parity error in the last long word transferred will not be detected otherwise.

5.18 SCSI interfaces.

Two entirely independant SCSI interfaces are provided on the board, accessed with separate DMA channels and with different interrupt levels to achieve maximum performance. The SCSI interfaces are optimized for high speed data transfer between mass storage devices and the system RAM memory.

Internal high speed buffers (16 bytes= 4 long words) on the SCSI interfaces enable the use of burst mode in DMA transfer and direct writing of commands strings from the CPU without waiting for byte-wise transfer, minimizing the overhead of the system.

The SCSI buffers can be accessed in byte, word or long word mode. The buffer pointer and data will always be correctly accessed. External transfer on the SCSI busses are always in byte mode.

Each SCSI interface can be separately protected through the PMMU system.

The DMA channels used for the SCSI interfaces are:
DMA channel 0 for the SCSI 0
DMA channel 1 for the SCSI 1

The interfaces support multimaster operation on the SCSI bus as defined in the ANSI X3T9.2 specification. This makes it possible to share external devices, as 0.5 inch tape streamers or high capacity disks among a number of computers as well as to provide high-speed communication channels for computer to computer communication.

Each SCSI interface can be connected to an SCSI bus. Up to 7 external units can be connected to each SCSI bus and each unit on the bus shall have a unique identity number (0..6). The SCSI interface on the computer board are normally programmed to have the identity number 7.

The maximum bus load at data transfer over the SCSI channel, between a disk and the memory, will be lower than 15 % per channel as the DMA transfer rate is higher that the SCSI transfer speed.

SCSI programming:

For programming each SCSI interface consists of the following units:

- Interface command register
- Interface status register
- Buffer pointer register (auto-incremented at buffer access)
- 16 bytes buffer memory
- Transfer status register
- Associated DMA channel 0 or 1 (if used)

The buffer pointer register keeps the buffer memory address. It will be incremented modulus 16 on every access to the buffer. Buffer accesses can be issued by the CPU, the DMA or the interface logic. Access can be in byte, word or long word mode.

The buffer full flag (in the tranfer status register) toggles each time the last buffer address (15) is accessed. To set or reset the buffer full flag from the CPU, the last buffer location shall be properly accessed to toggle the flag.

The SCSI interfaces are accessed through the physical addresses:

SCSI 0 Command register	Write only :	0200000 Hex	
SCSI 0 Status register	Read only :	0200000 Hex	
SCSI 0 Buffer pointer	Read/Write :	0200020 Hex	**)
SCSI 0 Buffer	Read/Write :	0200030 Hex	**)
SCSI 1 Command register	Write only :	0210000 Hex	
SCSI 1 Status register	Read only :	0210000 Hex	
SCSI 1 Buffer pointer	Read/Write :	0210020 Hex	**)
SCSI 1 Buffer	Read/Write :	0210030 Hex	**)

**) The buffer pointer is autoincremented at buffer access.

Interrupts from the SCSI interfaces are detected on the CIO port A, bits 7 or 6. At an interrupt the CIO interrupt vector is read, the CIO port A is read and the appropriate SCSI registers are read to detect the source of the interrupt.

The communication sequence is always the following: - Calling unit obtains the bus - Select a target - Transfer a command - Optionally transfer data - Return two status bytes from the receiving unit. Interrupts are generated as soon as the interface needs service from the CPU. Normally at least the data transfer is controlled by the DMA.

SCSI commands

The SCSI interfaces recognizes the following commands. These are given by writing to the SCSI command register.

Command name	Code	Function
IDLE MODE	0 -	In Idle mode, the SCSI interface can become a target if selected by another SCSI bus master.
OBTAIN BUS	2 -	The interface tries to become the SCSI bus master. The command is either executed immediately if the bus is free or delayed until the bus is free.
SELECT TARGET	3 -	After the bus is obtained, this command selects another unit on the bus as target. The ID-number in the command (see below) shall be the target ID-number.
INITIATOR MODE	1 -	After selecting a target, this command sets up the interface to execute further transfer phases according to the handshaking controlled by the target.
TARGET MODE commands:		The command sets up the interface in target mode after another bus master has selected this interface as a target. Within the target mode, four submodes are defined:
CMD IN	4 -	Command block input.
DATA IN	6 -	Data input.
DATA OUT	7 -	Data output.
STATUS OUT	5 -	Status block output.

The command codes 0..3 are initiator commands, while 4..7 are target commands. Legal command sequencies are:

0 - 2 - 3 - 1 - 0	Standard initiator command sequence.
0 - 2 - 3 - 0	Idle when no response from target.
0 - 2 - 0	Idle when the bus can not be obtained.
0 - 4 - 5 - 1 - 0	Target mode: Receive command but no data transfer.
0 - 4 - 6 - 5 - 1 - 0	Target mode: Receive command and data.
0 - 4 - 7 - 5 - 1 - 0	Target mode: Receive command and transmit data.

SCSI command register Write only: SCSI 0: 0200000 Hex
SCSI 1: 0210000 Hex

Bit	Function
7	1 = Transfer supported by DMA during data phase.
6..4	Command codes as listed above.
3	1 = Assert RST* on the SCSI bus. "Bus clear" request.
2..0	ID-number (complemented). Own or selected target.

Bit 7 Controls the interrupt condition required to generate interrupt. When bit 7=1, data transfer is supported by DMA and interrupt will be generated:

* In Target mode: On "command received", "DMA completed" and on "target status transmitted".
* In Initiator mode: On "target disconnected" only.

When bit 7=0, data tranfer is controlled by the CPU and CPU action is requested by interrupt for each block of data or bus commands to transfer between the memory and the SCSI buffer.

Once the RST* is asserted on the SCSI bus, it shall stay set for at least 1 msec, or until the bus becomes free.

The own ID-number shall be included on all commands except the "Select target" command, which shall contain the target's ID. The ID shall be complemented, e.g ID=0 given as 7.

SCSI Interface status register Read only: SCSI 0: 0200000 Hex
SCSI 1: 0210000 Hex

The SCSI interface status register can be read at any time. It contains information from the SCSI bus.

Bit	Function
7	1 = SEL* line asserted on the SCSI bus.
6	1 = BSY* line asserted on the SCSI bus.
5	1 = CTRL* line asserted on the SCSI bus.
4	1 = DIR* line asserted on the SCSI bus.
3	1 = RST* line asserted on the SCSI bus.
2..0	ID-number, as received from the SCSI bus. (The ID is not complemented here. Compare the SCSI command register).

SCSI buffer pointer register Write only: SCSI 0: 0200020 Hex
SCSI 1: 0210020 Hex

The pointer register must be loaded in order to define the start address of the buffer memory prior to accessing it.

A special control bit is provided to enable/disable the interface handshake function. Transfer interrupt conditions do not generate interrupt if this bit is cleared.
The interface handshaking can be disabled to allow the CPU to handle some special conditions on the SCSI bus interface, which may be necessary when the interface is connected as a target.

Bit	Function
7	1 = Enable interface handshake function.
6..4	-- Reserved. Data is ignored. Should be 0. --
3..0	Buffer pointer value 0..F Hex.

SCSI transfer status register Read only: SCSI 0: 0200020 Hex
SCSI 1: 0210020 Hex

The transfer status register may be read at any time.

Bit	Function
7	1 = Transfer based interrupt condition has occurred.
6	1 = DMA operation completed on this SCSI interface.
5	1 = Pending REQ* on the SCSI bus.
4	1 = Buffer memory full flag.
3..0	Current buffer memory pointer value (0..F Hex).

SCSI control block alignment

For correct operation, control blocks (commands or status blocks) must be loaded to the buffer memory starting with a pointer value which assures that the "Buffer full" flag toggles when the last byte of the control block has been transferred.

The buffer pointer must point to the first byte of the control block prior to the transfer start.

SCSI interface interrupt conditions

The SCSI interface can generate interrupt on a number of conditions. Those conditions can be divided into two main groups, "bus phase conditions" and "transfer conditions".

Bus phase interrupt conditions, depending on the current active command.

Command	Condition
- Any	RST* asserted on the SCSI bus.
- Idle	Select condition with my ID on SCSI bus.
- Obtain	Select condition with my ID on SCSI bus.
- Obtain	Bus access granted condition.
- Select	Target connected condition.
- Initiator	Target disconnected.

Transfer interrupt conditions. These conditions result in interrupt only if the "Handshake enable" bit in the buffer pointer register is set.

Command	Condition
- Initiator	Data request from an external unit, after the DMA was completed at DMA supported data transfer, to allow immediate handling of additional incoming data.
- Initiator	Buffer full, during status request.
- Initiator	Buffer full, on input with no DMA support.
- Initiator	Buffer empty, on output with no DMA support.
- Cmd in	Buffer full.
- Data in	DMA completed, at DMA supported data transfer.
- Data in	Buffer full, at transfer without DMA support.
- Data out	Buffer empty and DMA completed, at DMA supported data transfer.
- Data out	Buffer empty, at transfer without DMA support.
- Stat out	Buffer empty.

5.19 Diskette interface.

The onboard diskette interface supports three 5 1/4 inch diskette drives. Only one at a time can be accessed. The drive select numbers shall be set to 0, 1 and 2 on the drives.

An internal high speed buffer (16 bytes= 4 long words) on the diskette interface enables the use of burst mode in DMA data tranfer and blockwise transfer at CPU controlled data transfer, minimizing the overhead of the system.

The buffer can be accessed in byte, word or long word mode, the buffer pointer and data will always be correctly accessed. External transfer to/from the diskette drives is always in byte mode.

DMA channel 2 is used for the diskette interface.

A WD1797 diskette drive interface circuit is used. Below is described special features on the interface, but refer to the WD1797 documentation (ref 9) for programming details.

Diskette interface programming

For programming, the diskette interface consists of the following units:

- Interface control register
- Interface status register
- Buffer pointer register (auto-incremented at buffer access)
- 16 byte buffer memory
- Buffer status register
- WD1797 diskette controller
- Associated DMA channel 2 (if used)

The buffer pointer register keeps the buffer memory address. It will be incremented modulus 16 on every access to the buffer. Buffer accesses can be issued by the CPU, the DMA or the WD1797 curcuit. Access can be in byte, word or long word mode.

The buffer full flag (in the buffer status register) toggles each time the last buffer address (15) is accessed. To set or clear the buffer full flag from the CPU, the last buffer location shall be properly accessed to toggle the flag.

NOTE!
The buffer full flag must always be cleared before issuing a data transfer command.

Data transfer between the WD1797 and system memory can be supported by DMA. However, in stand-alone mode of system operation, the CPU might handle the data transfer.

NOTE! When a DMA controlled data transfer has been initiated, it is not allowed to access any WD1797 register.

To find the "Transfer end" condition, the CPU should examine the contents of the floppy interface status register or wait for interrupt.

The diskette interface is accessed through the physical addresses:

Interface control register	Write only :	0220000 Hex	
Interface status register	Read only :	0220000 Hex	
Buffer pointer register	Write only :	0220020 Hex	**)
Buffer status register	Read only :	0220020 Hex	
Buffer access	Read/Write :	0220030 Hex	**)
WD1797 command register	Write only:	0230000 Hex	
WD1797 status register	Read only:	0230000 Hex	
WD1797 Track register	Read/write:	0230010 Hex	
WD1797 Sector register	Read/write:	0230020 Hex	
WD1797 Data register	Read/write:	0230030 Hex	

**) The buffer pointer is autoincremented at buffer access.

Interrupt conditions for the diskette interface

The interface generates interrupt on conditions specified in the WD1797 datasheet. The IRQ* signal from the WD1797 is detected on the CIO port A, bit 0.

Diskette interface control register Write only: 0220000 Hex

This register contains static signals, controlling the diskette drives, the WD1797 and the data separator.

Bit	Function
7	1 = Motor on, 0 = Motor off.
6	1 = Data transfer direction to the drive. 0 = Data transfer direction from the drive.
5..4	Drive select code. 0 = No drive, 1..3 = Drive 0..2.
3	1 = 360 rpm, 0 = 300 rpm on the 5 1/4" drive.
2	1 = Low data rate (250 kb/s MFM), 0 = 500 kb/s.
1	1 = FM recording(single density), 0 = MFM recording.
0	1 = Release RST on the WD1797. Asserted at power-on.

The drive selection code has the following values:

Code 0 : No drive selected. (A not-used SEL3* line on the connector is asserted).
Code 1 : Drive 0 (SEL0*)
Code 2 : Drive 1 (SEL1*)
Code 3 : Drive 2 (SEL2*)

Diskette interface status register Read only: 0220000 Hex

This register may be read at any time.

Bit	Function
7	1 = Drive not ready (RDY* signal from connector)
6	1 = Drive is write protected (Inverted WRPT*)
5..2	-- Reserved. Always 0.
1	1 = DRQ. Data request from WD1797.
0	1 = IRQ. Operation completed. Interrupt requested from WD1797.

Diskette buffer pointer register Write only: 0220020 Hex

The buffer pointer must be initiated to zero (0) before any data transfer command. This register contains also a control bit, which enables the buffer memory function when the data transfer is DMA-supported. The buffer memory must always be disabled after a completed DMA transfer, in order to prevent preloading of buffer memory.

Bit	Function
7	1 = Enable buffer memory function.
6..4	-- Reserved. Data is ignored. ---
3..0	Buffer pointer value (0..F Hex).

Diskette buffer status register Read only: 0220020 Hex

This register may be read at any time.

Bit	Function
7	1 = Mains (220/110V AC) is correct (UPS option)
6..5	-- Reserved. Always 0. --
4	1 = Buffer full flag.
3..0	Current value of the buffer pointer.

Bit 7 will be low (0) only if an active low signal is input on the ACLOW* pin in the power connector from an optional UPS system, to indicate power failure. This status bit should be checked regularly by the system.

Jumper for the 5 1/4 inch diskette interface

The ST1 jumper shall be CLOSED when the head load signal (HDLD*) shall be used on the connector pin 4. This is the default setting. The ST1 jumper is positioned below the diskette interface connector as shown in the figure in the installation section.

Diskette drive types

Different types of diskette drives and diskette types can be accessed, using different parameters. Software is available which can detect the format of a diskette by varying the parameters until it is possible to read the diskette. Generally single density 5 1/4" diskettes (160 KB and 80 KB) are not supported by the standard software.

Below are a few examples:

The abbreviations are:	DS/SS	Double/Single side
	DD/SD	Double/Single density
	DT/ST	Double/Single track (80/40)

5 1/4"	DS DD DT (80 tracks)	720 Kbytes (Standard)
	DS DD ST (40 tracks)	360 KB On DT-drives single track double density diskettes can only be read, not written.
	Normal data rate:	250 KHz (512 bytes/sector and 9 sectors per track).
	Motor speed:	300 rpm

5 1/4" IBM-PC/AT format with 1.2 Mbytes/diskette, which uses higher data rate and a special motor speed selected by signals to the drive.

DS DD DT	1.2 Mbytes unformatted
Data rate:	500 KHz (512 bytes/sector and 15 sectors per track).
Motor speed:	360 rpm

5.20 DataBoard 4680 expansion support.

An expansion subsystem can be connected to the 6P connector in the center of the 1121-30 board. Support is included for DataBoard and VME expansion subsystems.

The onboard logic includes support for efficient handling of DataBoard expansion systems. Direct support are available for up to four standard boards or three standard boards and an external I/O-expansion system, using up 32 boards.

A card select sequence is automatically performed at each I/O-access. A select code is output with the CS* strobe to select a DataBoard interface for each I/O-command given.

Special I/O-strobes are generated as support for an external I/O expansion system with interrupt scanning and for the card detection logic, EXP* and CSB*-read.

Each interface card is separately protected through the PMMU logic.

Card presence detection (CSB)

I/O-card detection logic on the expansion backplane returns information (CSB*) regarding the presence of selected I/O-cards, including the interrupt levels, both the direct levels on the expansion backplane and for cards in any external expansion system. To enable this, each DataBoard I/O-slot has separately wired CSB* and INT* wires. Five (5) different direct CSB*-signals can be recognized by the system, of which one is reserved for an external I/O-expansion system.

Note that only I/O-cards, generating a CSB* signal can be used with interrupt.

Interrupts

Four (4) direct DataBoard interrupt levels are supported, XIRQ1*, XIRQ2*, XIRQ3*, XIRQ4*. In addition a separate level, XIRQ5*, is reserved for any external I/O-expansion system, making it simple to identify this type of interrupt. Interrupts are detected through the CIO-port A on the system interrupt level 2.

The 4203-00 and 4202-00 boards are used for interrupt scanning on an external I/O-system, to provide individual detection of interrupts from up to 32 DataBoard interfaces.

Addressing commands

DataBoard I/O-strobes generated in the subsystem are defined by the physical address bits A4..A2, while the card select code (CS*) is defined by A19 ..A12.

A19 (CS* bit 7) is used by some DataBoard interfaces to select a secondary channel. A18 (CS* bit 6) generates special I/O-cycles for CSB-detection or interrupt scanning.

In the table below CS contains the card select code bits 0..5 and bit 7. As seen, standard I/O-strobes are accessed on the address: 0300000H + CS * 1000H + Strobe * 4

	Strobes	DataBoard strobes	Address in 1121-30
Read:	INP*	(INP 0)	0300000H + CS * 1000H + 0
	STAT*	(INP 1)	0300000H + CS * 1000H + 4
	OPS*	(INP 2)	0300000H + CS * 1000H + 8
	CSB*-read		0340000H + CS * 1000H + 0
	EXP*		0340000H + CS * 1000H +10H
Write:	OUT*	(OUT 0)	0300000H + CS * 1000H + 0
	C1*	(OUT 2)	0300000H + CS * 1000H + 8
	C2*	(OUT 3)	0300000H + CS * 1000H + 0CH
	C3*	(OUT 4)	0300000H + CS * 1000H + 10H
	C4*	(OUT 5)	0300000H + CS * 1000H + 14H

NOTE! Only byte operands are legal.

Special I/O-cycles

With A18=1 (CS* bit 6 =1), a special I/O-cycle is generated. The address bit A4 defines the type of action.

A4 =0 Read the CSB* card presence bits.

Bit	Function
7	Undefined.
6	Undefined.
5	0 = XCSB5* from external I/O-expansion system.
4	0 = XCSB4* from selected interface.
3	0 = XCSB3* from selected interface.
2	0 = XCSB2* from selected interface.
1	0 = XCSB1* from selected interface.
0	Undefined

A4 =1 Input with the EXP* strobe from the optional interrupt scanner. This could as example be reading a secondary interrupt level or a secondary CSB*-byte.

5.21 VME expansion support.

An expansion subsystem can be connected to the 6P connector in the center of the 1121-30 board. Support is included for DataBoard and VME expansion subsystems.

The VME extension makes it possible to attach a completely independant VME subsystem to the 1121-30 computer board. Such a subsystem, consisting of VME-compatible CPU, memory and interface boards, can use the VME bus resources as well as portions of the main system memory and I/O-resources. In addition, the processors on the main board can access all resources attached to the VME bus without restrictions.

The hardware localized on the VME backplane board supports the following functions:

- VME signal conditioning.
- VME bus arbitration.
- Protection of the main system resources against unauthorized access from the current VME bus master.
- Interrupt daisy chain lines.
- VME subsystem reset.
- VME bus timeout.

The standard VME bus electrical specifications are used on the VME expansion sockets. the address range is limited to 16 Mbyte and the data bus width is 16 bits.

The arbitration logic resolves VME bus aquisition using a "round robin" algorithm. VME bus requests issued by the main system are handled in the same way as those generated by VME requestors. Five different bus requests to the VME bus can be handled:

- From any of 4 request lines on the VME bus subsystem.
- Access from the main system to the VME bus.

Accesses to the main system from a master on the VME subsystem

The ability to access the main system resources from the VME subsystem is an important system feature, making it possible to significantly increase the system performance.

Separate logic provides physical address mapping and protection logic at access to the main system from bus masters on the VME system. This logic can only be accessed and changed from the main system.

Each of four (4) different bus masters on the VME-bus can have up to 1 Mbytes logical memory mapped into the main system memory through the address translation tables. The page size is 4 kbytes.

The VME bus subsystem is automatically reset at power on and the RST* signal is held until released by a software command from the main system. This assures that the VME system can not access any main system resources until the protection logic has been set up.

VME-access from the main system

When a CPU in the main system becomes a VME bus master, it can generate the following types of accesses:

- Byte or word access in 16 Mb range.
- Byte or word accesses in 64 kb range in short address mode.
- INTACK* accesses, generated by reading at the physical address of the VME interrupt vector.
- AS*-only accesses to the protection and translation tables.

Physical addresses for access to the VME-space:

Access to VME protection tables in main memory:	1000000 -	1FFFFFF Hex
Access in the 16 Mb range:	2000000 -	2FFFFFF Hex
Short address mode access (64 kb):	3000000 -	300FFFF Hex
Reading VME interrupt vector:	3FFFFF2	(Level 1)
	3FFFFF8	(Level 4)

The AM* bit combination on the VME-bus is asserted at all accesses from the main system and indicates "supervisor" data access on the VME bus subsystem, also when executing in user mode in the main system.

Accesses to non-responding slaves will result in bus errors, generated by the VME bus timeout logic (see below).

Access can be in byte, word or long word mode, but long word accessed will automatically be split by the CPU into word accesses.

Any physical address within the 16 Mbytes VME address space can be accessed from the main system.

When the "short address mode" is used during access to the VME-bus from the main system, the AM5 bit on the VME-bus will be asserted, indicating short address mode. The other AM bits always correspond to supervisor data access.

The AS* only accesses are used to access the protection and translation tables while preventing any VME-bus slave from responding. See below for details.

VME bus timeout

The VME bus timeout logic will issue a bus error when any VME bus master attempts to access a non-existing slave. Bus timeout is about 11.5 microseconds. The bus error shall be detected by the current VME bus master, which can be a master on the VME subsystem or the main system.

Interrupts on the VME-bus

Hardware interrupt requests can be issued from the VME-bus on the main system levels 1 and 4. These are recognized by the main CPU-plane on the 1121-30 board and handled there. Other interrupt requests on the VME bus must be handled by local VME resources.

When the main system reads the VME interrupt vector, an INTACK* cycle is generated on the VME-bus and the vector is read. The physical address for the VME interrupt vectors are:

Low level (1) VME interrupt vector: 03FFFFF2 Hex
High level (4) VME interrupt vector: 03FFFFF8 Hex

Only "word read" access is legal and the AM* bit combination will describe supervisor data access on the VME-bus.

Resource protection principle

Using an address translation and protection logic at accesses from the VME subsystem to the main system resources will provide the following features:

- A master on the VME subsystem will be able to reach any part of the main system address space, in spite of the limited addressing capability of the VME-bus.
- The main system resources can be protected against unauthorized access from the VME subsystem, allowing only a processor in the main system to set up or change the tables.

The tables translates addresses given on the VME-bus to physical addresses in the main system and provides protection on the page level (4 kbytes pages), i.e. any 4 kbytes page in the VME address space can be translated to any 4 kbytes area in the main system.

Four (4) tables can be defined at the same time, each with 256 pages, providing the possibility to use four different VME-bus masters with different mapping to the main system.

Only the processors in the main system can set up the tables. At power on the SYSFAIL* line on the VME-bus is asserted and is released by the main system first after initiating the tables. The SYSFAIL* line is controlled from the CIO port B, bit 4.

To set up the tables the main processor becomes the VME-bus master, but to prevent any VME-boards from responding to the address cycles on the VME-bus, the tables are accessed with AS*-only cycles.

For any current bus master on the VME-bus, the following rules shall be applied when accessing the main system through the tables.

- To access a resource in the main system, a VME-bus address in the range F00000 - FFFFFF Hex must be used. Addresses outside this space will access other VME-bus slaves. Totally any VME-bus master can have access rights to up to 256 pages in the main system address space.

- If access is allowed, the upper 12 address bits on the VME-bus will be translated into a 15-bits page number, forming the main system physical address together with the lower VME bus address bits.

- All semaphore areas handling communication between the main system and VME-bus masters must be located within the main system memory, as the hardware does not support Read-Modify-Write cycles on the VME-bus.

Protection table programming

The protection and translation tables are accessed from the main system at the physical address range 1000000 - 1FFFFFF Hex. The tables can be both read and written.

The table entry for the first page is at 1000000 Hex and each entry is offset by 4 kbytes. Each table entry is one word, containing the following data. The total size of the table is 1 kwords.

Bit	Function
15	1 = Access allowed, 0 = Protected.
14..0	Physical page location in the main system. Bits 14..0 is ignored if bit 15 indicates protected,

VME bus master BG line	Table address	Page number
BG 0 :	1000000 Hex	0
	1001000 Hex	1
	1002000 Hex	2
	.....	..
	.....	..
	10FF000 Hex	FF
BG 1 :	1100000 Hex	0
	1101000 Hex	1
	.....	..
	.....	..
	11FF000 Hex	FF
BG 2 :	1200000 Hex	0
	1201000 Hex	1
	.....	..
	.....	..
	12FF000 Hex	FF
BG 3 :	1300000 Hex	0
	1301000 Hex	1
	.....	..
	.....	..
	13FF000 Hex	FF

5.22 Referencies.

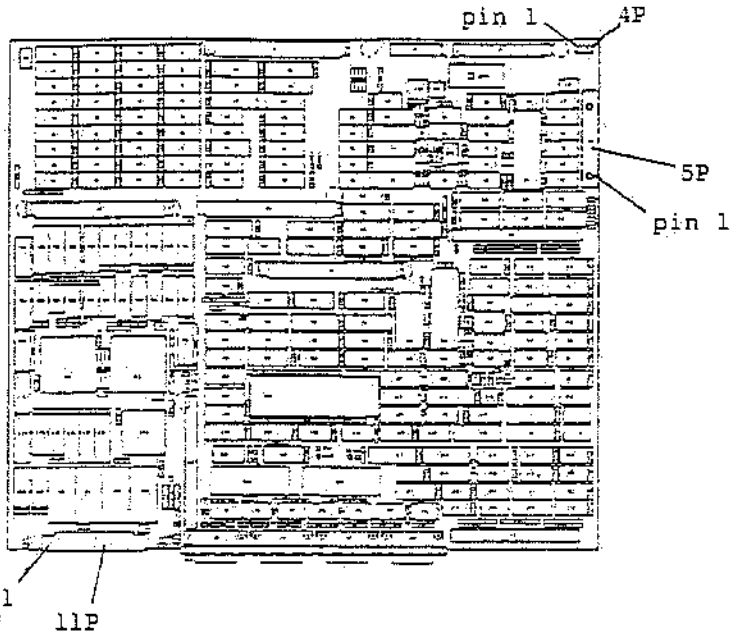
Below, MM indicates the DS90-2x maintenance manual.

1.	CPU	Motorola Semiconductor MC68020 Microprocessor manual.
2.	DMA	Hitachi HD68450 DMA
3.	FPU	Motorola Semiconductor MC68881 floating point processor.
4.	SCC	Zilog Z8530A SCC serial communication controller.
5.	CIO	Zilog Z8536A CIO counter/timer and parallel I/O-unit.
6.	NVRAM	National semiconductor NMC 9306 256-bit EEPROM datasheet.
7.	RTC	Microelectronic Marin MEM E050-16 1-bit real time clock timer.
8.	PMMU	Motorola Semiconductor MC68851 paged memory management unit.
9.	Floppy controller	Datasheet for WD1797 floppy controller circuit.
10.	Termination plugs	Diab 5213-00 memory termination plug Diab 5212-00 CPU termination plug See MM.
11.	Memory expansion	Diab 2020-30 4 Mbytes or 2022-00 8 Mbytes memory expansion module. See MM.
12.	CPU expansion	Diab 1120-30 CPU expansion module. See MM.
13.	Serial expansion	Diab 5172-10 serial expansion board See MM.
14.	VME/DataBoard back-plane	Diab VME/DataBoard backplanes, depending on the computer version. See MM.
15.	VME expansion rack	Diab 7183-00/7184-00 VME expansion system with the 5206-00 repeater board. See MM.
16.	DataBoard expansion rack	Diab 7182-00 DataBoard expansion system with the 4202-00/4203-00 adapter and interrupt scanner boards. See MM.

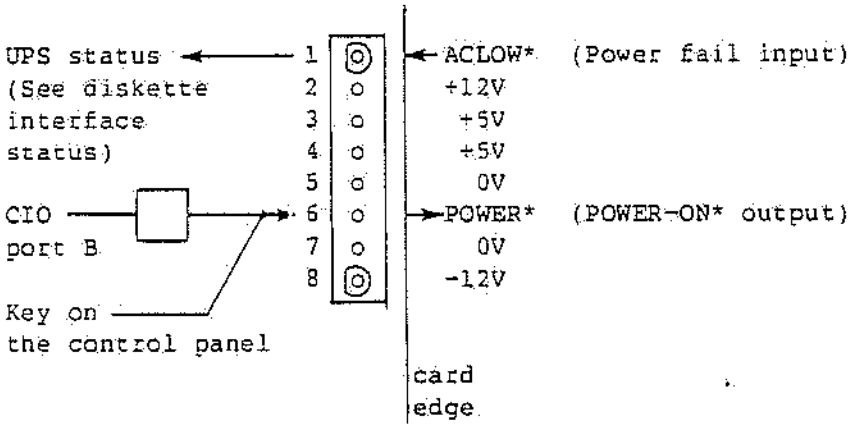
6. CONNECTORS

6.1 Power connectors 5P, 11P and 4P

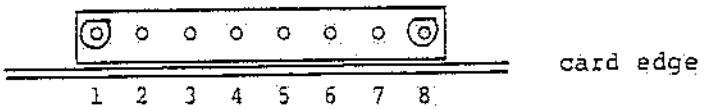
Positions on board:



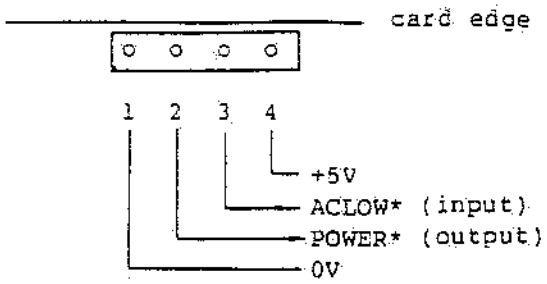
Pinning: 5P Power, standing on the board (Female)



Pinning: 11P Same as 5P. (Normally not mounted)



Pinning: 4P Power control



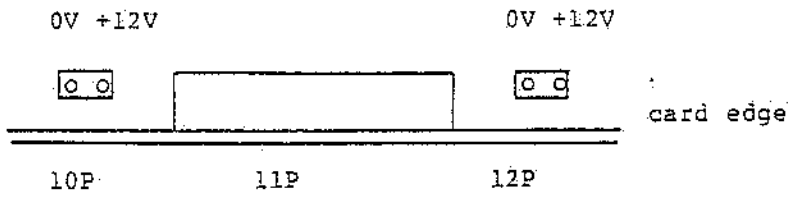
Notes: AMP connectors are used.

ACLOW* The input signal ACLOW* can optionally be connected to an external UPS system. An active low input signal shall indicate power failure.

POWER* The output signal POWER* shall control power ON/OFF. Power ON (active low output) can be generated directly by closing a control panel switch and can be kept ON by software (open collector output) during a controlled power down sequence.

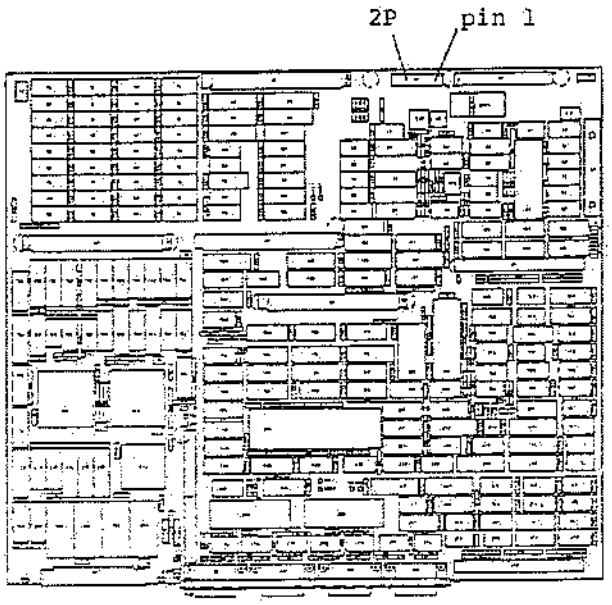
6.2 +12V power output connectors for fans (10P and 12P)

Two connectors are available close to the 11P power connector, having +12V power, to be used for the +12V fans on the expansion chassis. Note the pin assignments. If 10P is used as remote power control signal, it must be protected with a resistor.

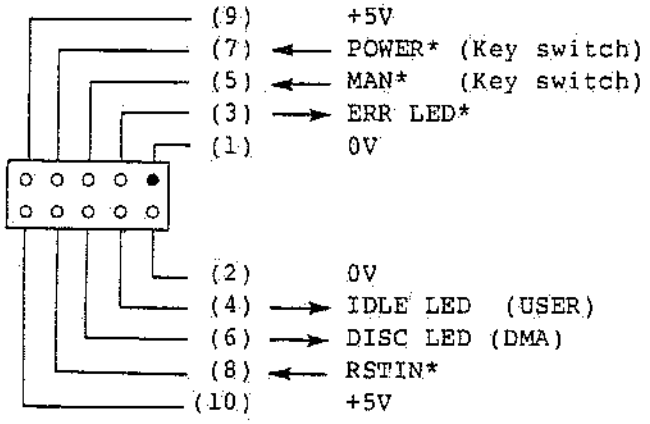


6.3 Control panel connector (2P)

Position
on board:



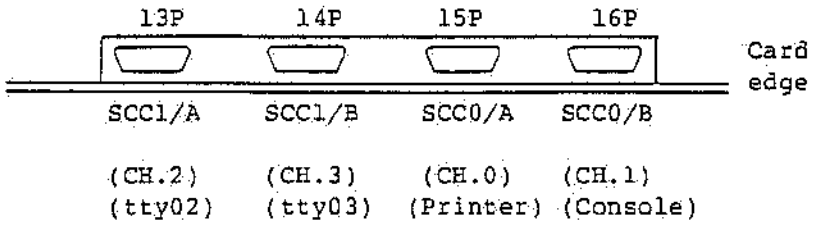
Pinning:



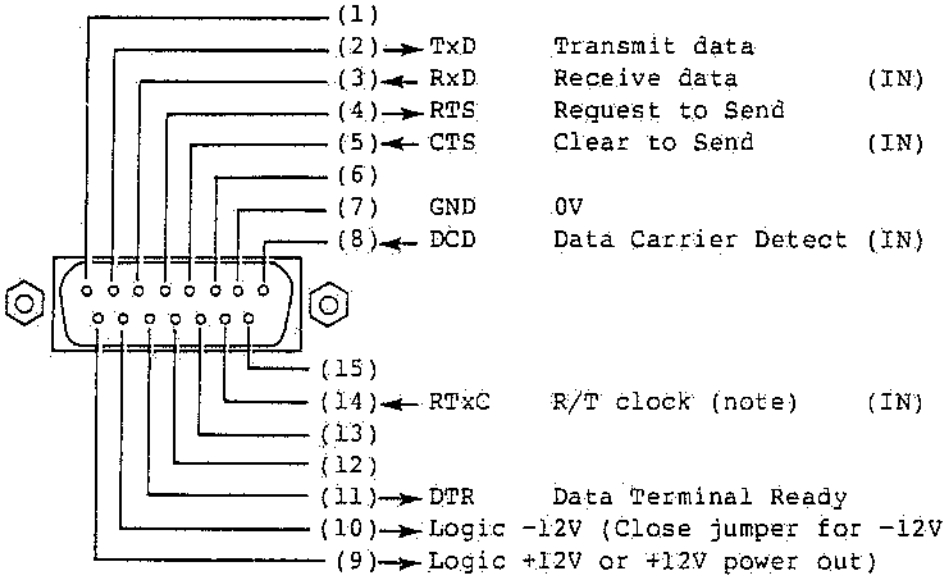
Notes: The connector is a 10-pin ribbon cable connector.

6.4 Serial V24 connectors (13P, 14P, 15P, 16P)

Position on board:



Pinning:



Notes: The RxD input has a 27 kohm pulldown resistor for higher noise immunity.

The connectors are DA15P connectors.

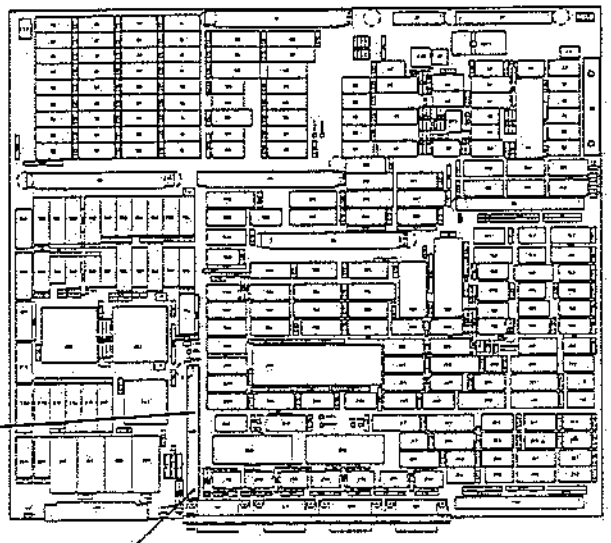
+12V,-12V pins are logic out for jumper purposes. Jumpers ST6,ST7 (13P), ST8,ST9 (14P), ST10,ST11 (15P) and/or ST12,ST13 (16P) can be closed to achieve +12V and/or -12V power output. Even jumpers are for +12V and odd jumpers for -12V.

Split speed is not supported. For split speed, use a an expansion board (DataBoard or VME).

The serial connectors on the expansion boards (5172-10) does not include the clock signal input (RTxC).

6.5 Connector for serial channel expansion board (18P)

Position on board:



Pinning:

IE2 ←	50	o	o	49	→ IE0
IE1 ←	48	o	o	47	→ CE2*
CE3* ←	46	o	o	45	→ CE4*
CE5* ←	44	o	o	43	→ CE6*
CE7* ←	42	o	o	41	→ IE3
	40	o	o	39	→ C*/D
	38	o	o	37	→ A/B*
	36	o	o	35	→ ZWR*
	34	o	o	33	→ ZRD*
	32	o	o	31	→ 1231 kHz
0V	30	o	o	29	← REQ*
	28	o	o	27	← INT* (to IRQ3*)
	26	o	o	25	→ PCLK* (4.166 MHz)
	24	o	o	23	→ ZIACK*
	22	o	o	21	D0
D1	20	o	o	19	D2
D3	18	o	o	17	D4
D5	16	o	o	15	D6
D7	14	o	o	13	0V
0V	12	o	o	11	0V
+12V	10	o	o	9	+12V
+5V	8	o	o	7	+5V
+5V	6	o	o	5	+5V
0V	4	o	o	3	0V
-12V	2	o	o	1	-12V

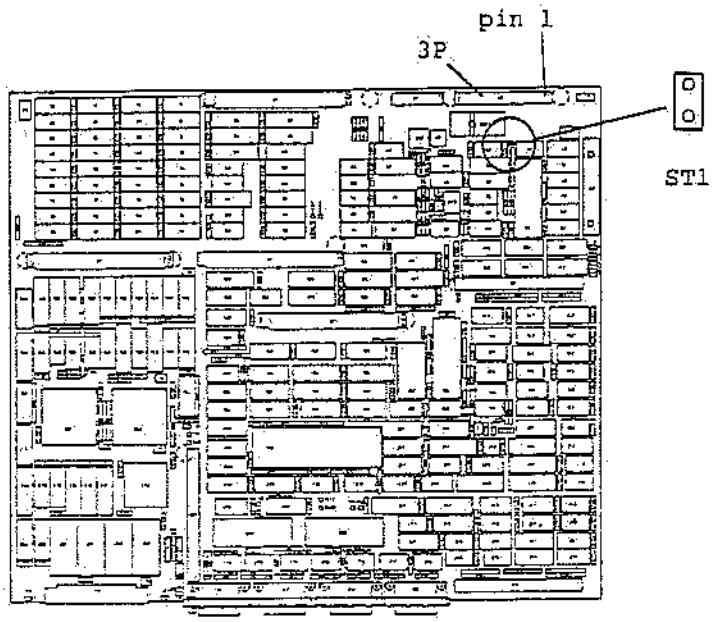
Notes: The expansion boards 5172-10 are mounted above the internal V24 ports, using mainly identical I/O connectors DA15P. However 5172-10 does not support external clocks. (Do not use 5172-00).

The connector is a 50-pin ribbon cable connector.

6.6 Diskette connector for 5 1/4" diskette (3P)

Up to two 5 1/4" drives can be connected to 3P.

Position on board:



Pinning:

	1	o o	2	→	LS*/LC* (motor speed control)
	3	o o	4	→	HDLD* (or no connect)
	5	o o	6	→	SEL3*
	7	o o	8	←	IP* input
	9	o o	10	→	SEL0*
	11	o o	12	→	SEL1*
0V	13	o o	14	→	SEL2*
Ground	15	o o	16	→	MOTOR*
	17	o o	18	→	DIRC*
	19	o o	20	→	STEP*
	21	o o	22	→	WD*
	23	o o	24	→	WG*
	25	o o	26	←	TRO0* input
	27	o o	28	←	WPRT* input
	29	o o	30	←	RDTA* input
	31	o o	32	→	SIDE*
	33	o o	34	←	RDY* input

Notes: HDLD* is normally to pin 4 through the ST1 jumper (see figure). For drives, not using HDLD*, the jumper ST1 can be removed. Old types of 5 1/4" drives, requiring RDY* on pin 6 can not be used.

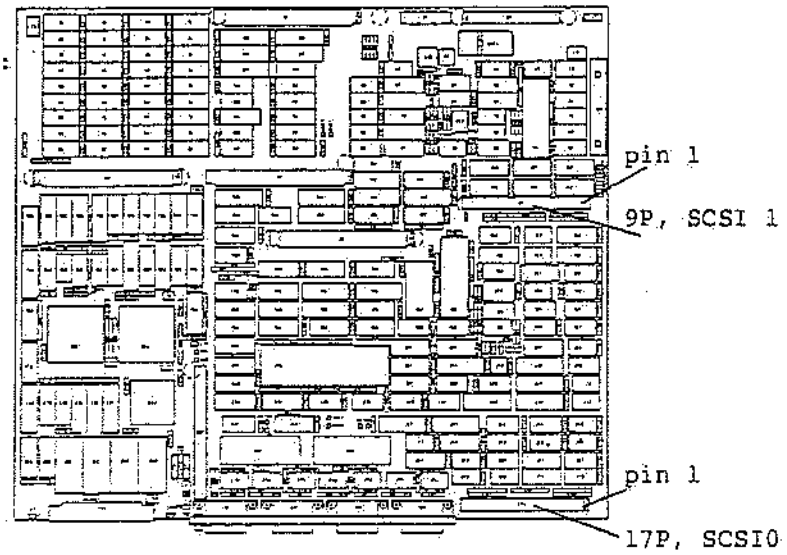
LS*/LC* controls for 5 1/4" diskettes motor speed. High = 360 rpm, while active low = 300 rpm normally.

The connector is a 34-pin ribbon cable connector.

6.7 SCSI connectors (9P and 17P)

Two separate independant identical SCSI channels.
SCSI 0: 17P connector, near the serial connectors.
SCSI 1: 9P connector.

Position on board:

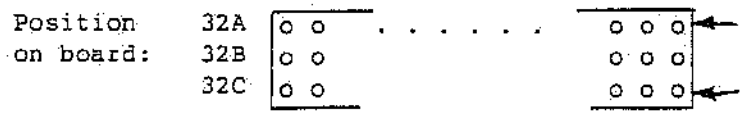


Pinning:

	1	o o	2		D0*
	3	o o	4		D1*
	5	o o	6		D2*
	7	o o	8		D3*
	9	o o	10		D4*
	11	o o	12		D5*
	13	o o	14		D6*
	15	o o	16		D7*
	17	o o	18		
	19	o o	20		
	21	o o	22		
	23	o o	24		
0V Ground	25	o o	26		
	27	o o	28		
	29	o o	30		
	31	o o	32		
	33	o o	34		
	35	o o	36	←→	BSY*
	37	o o	38	←→	ACK*
	39	o o	40	←→	RST*
	41	o o	42	→	MSG*
	43	o o	44	←→	SEL*
	45	o o	46	←→	C/D*
	47	o o	48	←→	REQ*
	49	o o	50	←→	I/O*

Notes: The connector is a 50-pin ribbon cable connector.

6.8 Expansion connector (8P) for VME or DataBoard

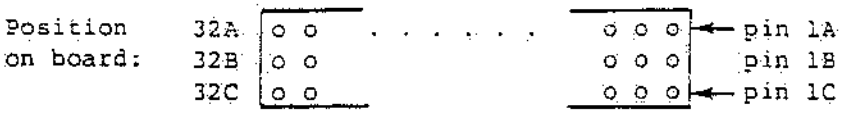


Pinning, as seen from the component side:

A	B	C	--A--		--B--		--C--	
o	o	o	1A	+5V	1B	+5V	1C	+5V
o	o	o	2A	+5V	2B	+5V	2C	+5V
o	o	o	3A	4680 AE*	3B	4680 DBE*	3C	XRST*
o	o	o	4A	16 MHz	4B	XATT*	4C	XINT4*
o	o	o	5A	XINT3*	5B	XINT2*	5C	XINT1*
o	o	o	6A		6B		6C	XINT0*
o	o	o	7A	XBERR*	7B	XD6	7C	XD7
o	o	o	8A	XD3	8B	XD4	8C	XD5
o	o	o	9A	XD0	9B	XD1	9C	XD2
o	o	o	10A	RA24	10B	RA25	10C	RA26
o	o	o	11A	RA21	11B	RA22	11C	RA23
o	o	o	12A	RA18	12B	RA19	12C	RA20
o	o	o	13A	RA15	13B	RA16	13C	RA17
o	o	o	14A	RA12	14B	RA13	14C	RA14
o	o	o	15A		15B		15C	
o	o	o	16A	RA9	16B	RA10	16C	RA11
o	o	o	17A	RA6	17B	RA7	17C	RA8
o	o	o	18A	RA3	18B	RA4	18C	RA5
o	o	o	19A	RA0	19B	RA1	19C	RA2
o	o	o	20A	RD15	20B	VMEEN	20C	VMIN*
o	o	o	21A	RD12	21B	RD13	21C	RD14
o	o	o	22A	RD9	22B	RD10	22C	RD11
o	o	o	23A	RD6	23B	RD7	23C	RD8
o	o	o	24A	RD3	24B	RD4	24C	RD5
o	o	o	25A	RD0	25B	RD1	25C	RD2
o	o	o	26A	RIZ1	26B	VS*	26C	VDS*
o	o	o	27A	RIZ0	27B	RW*	27C	VATR*
o	o	o	28A	IRQL1*	28B	IRQL4*	28C	SSA0*
o	o	o	29A	Clock*	29B	Clock	29C	SSA1*
o	o	o	30A	VME*	30B	4680 STB*	30C	4680 CS*
o	o	o	31A	0V	31B	0V	31C	0V
o	o	o	32A	0V	32B	0V	32C	0V

Notes: The connector is a C96 pin Euroconnector DIN41612.

6.9 Memory expansion connectors 1P and 7P



Pinning for 1P, as seen from the component side (1P is the connector close to the card edge):

A	B	C	--A--		--B--		--C--	
o	o	o	1A	+5V	1B	+5V	1C	+5V
o	o	o	2A	+5V	2B	+5V	2C	+5V
o	o	o	3A	0V	3B	0V	3C	0V
o	o	o	4A	0V	4B	0V	4C	0V
o	o	o	5A	0V	5B	0V	5C	0V
o	o	o	6A	MD6	6B	0V	6C	MD7
o	o	o	7A	MD4	7B	0V	7C	MD5
o	o	o	8A	MD2	8B	0V	8C	MD3
o	o	o	9A	MD0	9B	0V	9C	MD1
o	o	o	10A	0V	10B	0V	10C	0V
o	o	o	11A	P2Q	11B	0V	11C	P3Q
o	o	o	12A	P0Q	12B	0V	12C	P1Q
o	o	o	13A	0V	13B	0V	13C	0V
o	o	o	14A	MD14	14B	0V	14C	MD15
o	o	o	15A	MD12	15B	0V	15C	MD13
o	o	o	16A	MD10	16B	0V	16C	MD11
o	o	o	17A	MD8	17B	0V	17C	MD9
o	o	o	18A	0V	18B	0V	18C	0V
o	o	o	19A	MD30	19B	0V	19C	MD31
o	o	o	20A	MD28	20B	0V	20C	MD29
o	o	o	21A	MD26	21B	0V	21C	MD27
o	o	o	22A	MD24	22B	0V	22C	MD25
o	o	o	23A	0V	23B	0V	23C	0V
o	o	o	24A	MD22	24B	0V	24C	MD23
o	o	o	25A	MD20	25B	0V	25C	MD21
o	o	o	26A	MD18	26B	0V	26C	MD19
o	o	o	27A	MD16	27B	0V	27C	MD17
o	o	o	28A	0V	28B	0V	28C	0V
o	o	o	29A	P2D	29B	0V	29C	P3D
o	o	o	30A	P0D	30B	0V	30C	P1D
o	o	o	31A	0V	31B	0V	31C	0V
o	o	o	32A	0V	32B	0V	32C	0V

Notes: The connector is a C96 pin Euroconnector DIN41612.

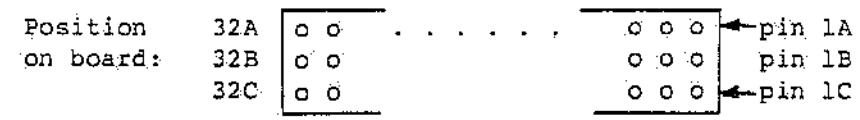
Pinning for 7P, as seen from the component side (7P is the connector close to the card center). The 5213-00 memory bus termination plug must always be mouted on 7P or on top of any expansion boards.

A	B	C	--A--	--B--	--C--
o	o	o	1A +5V	1B +5V	1C +5V
o	o	o	2A +5V	2B +5V	2C +5V
o	o	o	3A 0V	3B 0V	3C 0V
o	o	o	4A 0V	4B 0V	4C 0V
o	o	o	5A 0V	5B 0V	5C 0V
o	o	o	6A 0V	6B 0V	6C 0V
o	o	o	7A 0V	7B 0V	7C BA25
o	o	o	8A BA26	8B 0V	8C BA21
o	o	o	9A BA19	9B 0V	9C BA20
o	o	o	10A BA18	10B 0V	10C BA16
o	o	o	11A BA17	11B 0V	11C BA15
o	o	o	12A BA13	12B 0V	12C BA14
o	o	o	13A BA11	13B 0V	13C BA12
o	o	o	14A BA10	14B 0V	14C BA9
o	o	o	15A BA7	15B 0V	15C BA8
o	o	o	16A BA23	16B 0V	16C BA22
o	o	o	17A BA5	17B 0V	17C BA6
o	o	o	18A BA3	18B 0V	18C BA4
o	o	o	19A 0V	19B 0V	19C BA2
o	o	o	20A 0V	20B 0V	20C
o	o	o	21A Clock	21B 0V	21C Clock*
o	o	o	22A BA24	22B 0V	22C BW*
o	o	o	23A BIZ1	23B 0V	23C CCH*
o	o	o	24A 0V	24B 0V	24C
o	o	o	25A BIZ0	25B 0V	25C BA0
o	o	o	26A BA1	26B 0V	26C MC0
o	o	o	27A 0V	27B 0V	27C MC1
o	o	o	28A 0V	28B 0V	28C BPAS*
o	o	o	29A 0V	29B 0V	29C SSA0*
o	o	o	30A 0V	30B 0V	30C SSA1*
o	o	o	31A 0V	31B 0V	31C 0V
o	o	o	32A 0V	32B 0V	32C 0V

Notes: Up to three expansion memory boards can be mounted above the onboard memory.

The connector is a C96 pin Euroconnector DIN41612.

6.10 CPU-plane expansion connector 6P



Pinning, as seen from the component side:

A	B	C	--A--	--B--	--C--
o	o	o	1A +5V	1B +5V	1C +5V
o	o	o	2A +5V	2B +5V	2C +5V
o	o	o	3A BIZ1	3B BIZ0	3C BW*
o	o	o	4A BA25	4B BA26	4C BA27 not used
o	o	o	5A BA22	5B BA23	5C BA24
o	o	o	6A BA19	6B BA20	6C BA21
o	o	o	7A BA16	7B BA17	7C BA18
o	o	o	8A BA13	8B BA14	8C BA15
o	o	o	9A BA10	9B BA11	9C BA12
o	o	o	10A BA7	10B BA8	10C BA9
o	o	o	11A BA4	11B BA5	11C BA6
o	o	o	12A BA1	12B BA2	12C BA3
o	o	o	13A BD1	13B BD0	13C BA0
o	o	o	14A BD4	14B BD3	14C BD2
o	o	o	15A BD7	15B BD6	15C BD5
o	o	o	16A BD10	16B BD9	16C BD8
o	o	o	17A BD13	17B BD12	17C BD11
o	o	o	18A BD16	18B BD15	18C BD14
o	o	o	19A BD19	19B BD18	19C BD17
o	o	o	20A BD22	20B BD21	20C BD20
o	o	o	21A BD25	21B BD24	21C BD23
o	o	o	22A BD28	22B BD27	22C BD26
o	o	o	23A BD31	23B BD30	23C BD29
o	o	o	24A SSA1*	24B CLOCK	24C CLOCK*
o	o	o	25A SSA0*	25B SLRST*	25C NMI*
o	o	o	26A MC0	26B XRRUN*	26C XBERR*
o	o	o	27A MC1	27B BPAS*	27C BF/B*
o	o	o	28A INT51*	28B INT52*	28C INT53*
o	o	o	29A BRQ1*	29B BRQ2*	29C BRQ3*
o	o	o	30A GR1*	30B GR2*	30C GR3*
o	o	o	31A 0V	31B 0V	31C 0V
o	o	o	32A 0V	32B 0V	32C 0V

Notes: Up to three CPU-plane boards (1120-30) can be mounted above the onboard memory.

The connector is a C96 pin Euroconnector DIN41612.

7. TECHNICAL DATA

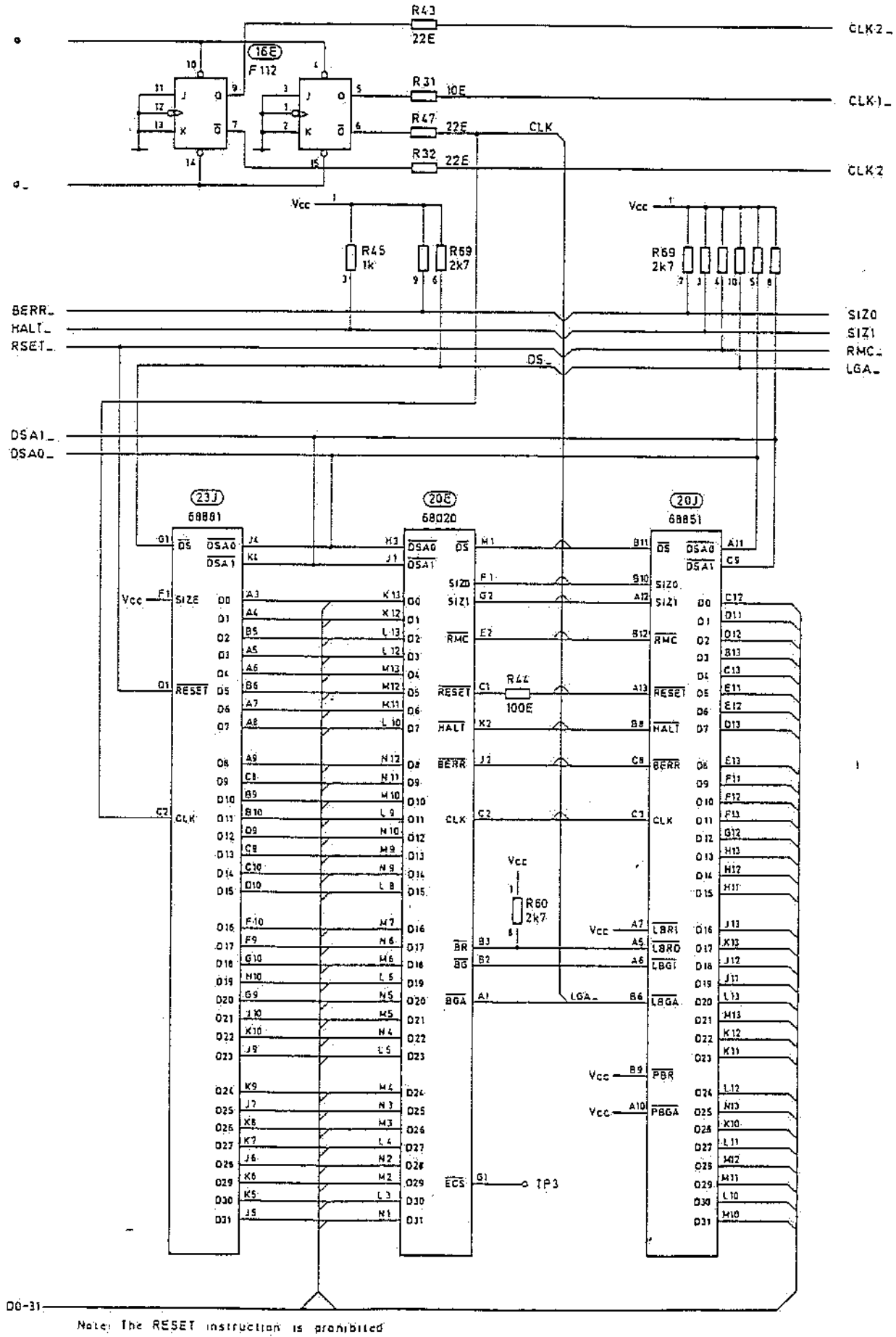
CPU-planes:	One CPU-plane on-board the 1121-30. Up to three more CPU-planes can be mounted, each with CPU, PMMU, FPU and cache memory. 1120-30 CPU plane boards.
CPU:	MC68020 32 bits processor.
PMMU:	MC68851 Paged memory management unit, using 4 kbytes page size, and virtual memory support, providing up to 2 Gbytes logical memory per process.
FPU:	MC68881 Hardware floating point processor.
DMA:	HD68450 Direct memory access module, directly accessing physical memory. Three independant DMA channels. The forth channel on HD68450 can not be used. DMA ch.0: SCSI-interface 0. DMA ch.1: SCSI-interface 1. DMA ch.2: Diskette interface.
Cache memory:	32 kbytes high speed cache memory. The cache is divided into 8 segments, using 16 bytes block size and immediate write through.
Memory:	4 Mbytes physical memory onboard. Up to 28 Mbytes total with three 2022-00 boards mounted (or 16 Mb using 2020-30). Memory chips: 1 Mbits. 100 ns access time, using type TC511000P-10 or equivalent. Prepared for: 64 Mbytes total memory space, using 4 Mbit chips.
Termination plugs:	The CPU bus and the memory bus require separate termination plugs always mounted. 5213-00 Memory bus termination plug. 5212-00 CPU bus termination plug.
Parity check:	Hardware parity check in main memory with 1 parity bit per 8-bit byte.
System clock:	16.67 MHz CPU-clock. No wait-states are used at cache access.
Peripheral clock:	1231 kHz as transfer clock to SCC circuits. 16 MHz available in the bus expansion connector.

Watchdog:	Should be pushed with max 1.2 sec interval. After 1 sec: Early warning signal which can generate interrupt. After 1.2 sec: System reset is generated.
Size:	325 * 385 mm. The height depends on optional mounted expansions.
Environment:	+10 .. +40 degrees C operating. 20% .. 80% humidity
Power requirement:	+5V +/-5% 11 A without expansion +12V +/-5% 300 mA without expansion -12V +/-5% 300 mA without expansion
Power control:	Output signal POWER* with open collector drive, non-isolated. Can also be direct from the control panel power switch. Active low is power-ON.
Power fail support:	"Power-low" input signal (ACLOW*) detected as a status bit. TTL-level, non-isolated active low.
I/O-protection:	Protection through the PMMU. Each of the following are separately protected: - System control through CIO. - Each serial channel. - SCSI-0, - SCSI-1, - Diskette interface. - Each "Card select" on a DataBoard expansion is separately protected. - Each page of the VME-bus.
Boot-PROM:	32 Kbytes in one 27256 EPROM. Optionally 64 kbytes in 27512 EPROM. The boot PROM contains the start-up program and a system serial number, unique for each system.
NVRAM:	Non-volatile RAM (32 bytes) for parameters. Circuit: NMC 9306. Allows typically 10.000 erase/write cycles.
Real-Time-Clock:	MEM E050-16 real time clock circuit with battery backup.
Battery:	2.4 V, type GE013 for the real-time clock only.

Control panel:	Support signals for LED's, power-on controls and Auto/Manual selection on an optional control panel. Connector: 10-pin ribbon cable connector with key and lock.
Display LED's	8 display LED's on-board for testing purpose.
Serial I/O:	4 serial full duplex asynchronous V24 (RS232C) channels onboard, using two SCC circuits (type Z8530). Fully buffered, using 1488/1489 circuits. Up to a total of 16 channels, with three expansion boards (5172-10) mounted. Baudrate up to 76800 Baud. Connectors: Standard DA15P connectors.
SCSI ports:	2 independant fully specified SCSI interfaces. 16 bytes = 8 words send/receive buffer. Multi-master configuration is supported with up to 8 units connected to the same SCSI-bus. Connectors: 50-pin Burndy connectors with key and lock.
Diskette interface:	Up to 2 minidiskette (5 1/4") drives can be connected. Only one drive is accessed at a time, supported by the DMA. 16 bytes = 8 words send/receive buffer. Connectors: 34-pin ribbon cable connector.
Interrupt logic:	7 levels of hardware interrupts, using autovectors. Extended levels by reading interrupt vectors from the different subsystems. Support for secondary interrupt levels on the DataBoard subsystem and for two interrupt levels on a VME subsystem.
Bus expansion:	Connector for mounting optional expansion backplanes. Example: - 5202/5203 DataBoard and VME expansion. (3 VME and 4 DB slots)

DataBoard support: The onboard hardware supports DataBoard I/O through an expansion backplane:
- Automatic CS* strobe at each access.
- Separate user access protection for each DataBoard interface.
- 4 DataBoard interrupt levels supported. Up to 32 levels with the 4202 interupt scanner.

VME support: Full support for VME-bus access from the main system.
Up to three bus masters on the VME-bus can access the main system resources through access protection and address translation tables. Each VME bus master can have 1 Mbyte logical memory in the main system address area.



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DATA INDUSTRIER AB Sweden

MC 68020 SBC
CPU data path

81-1121-30

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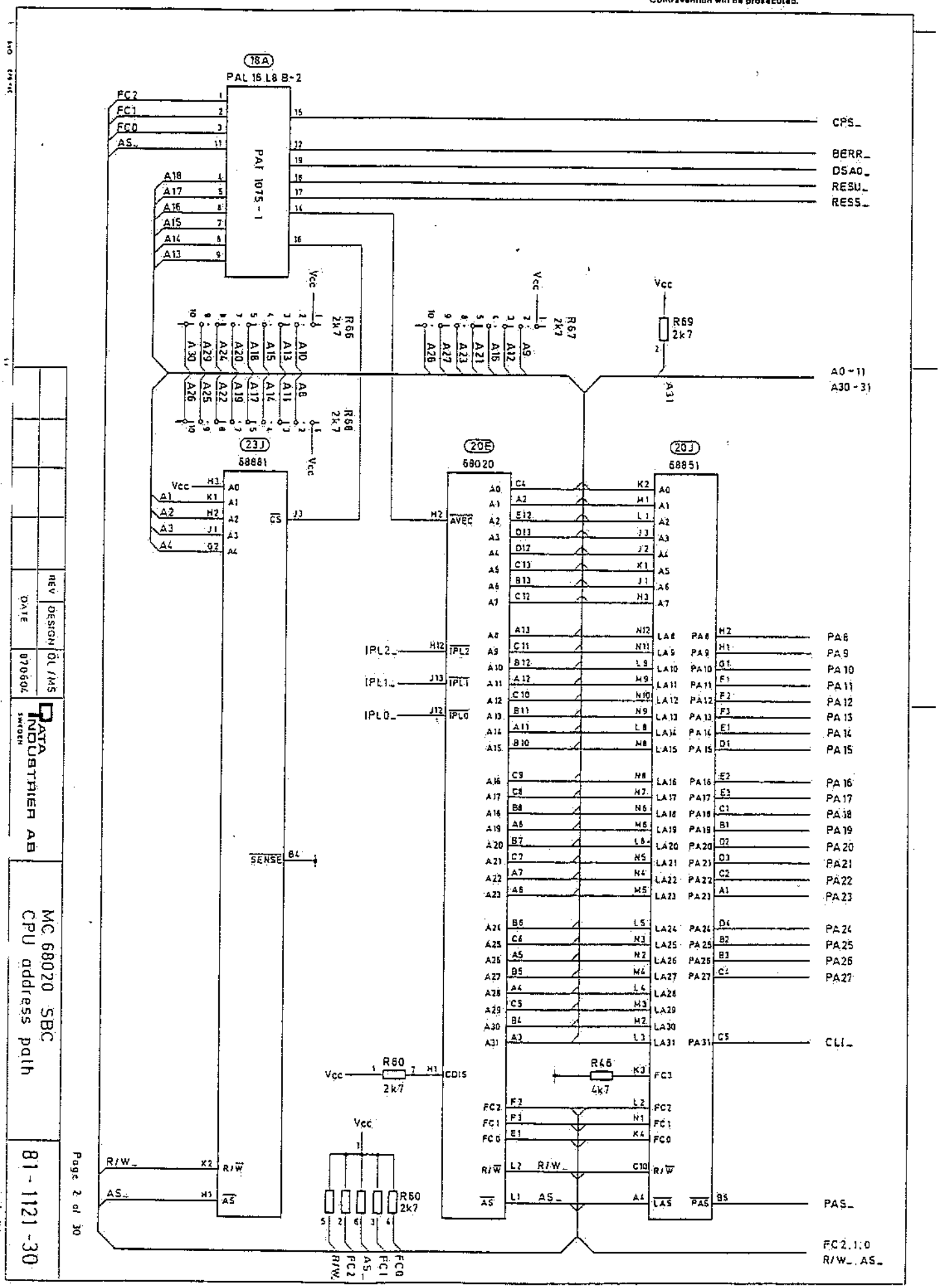

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DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
CPU address path

81-1121-30

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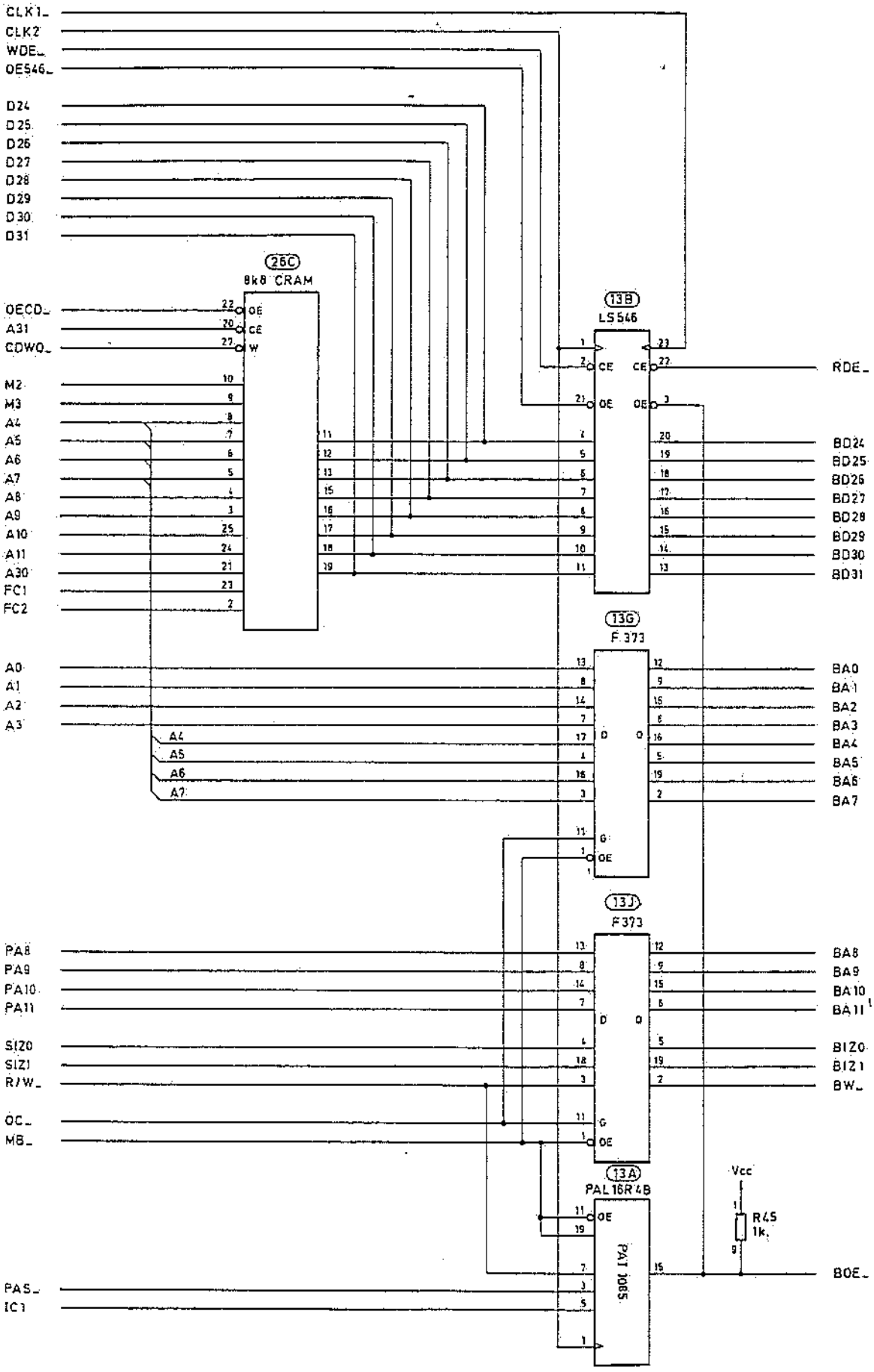

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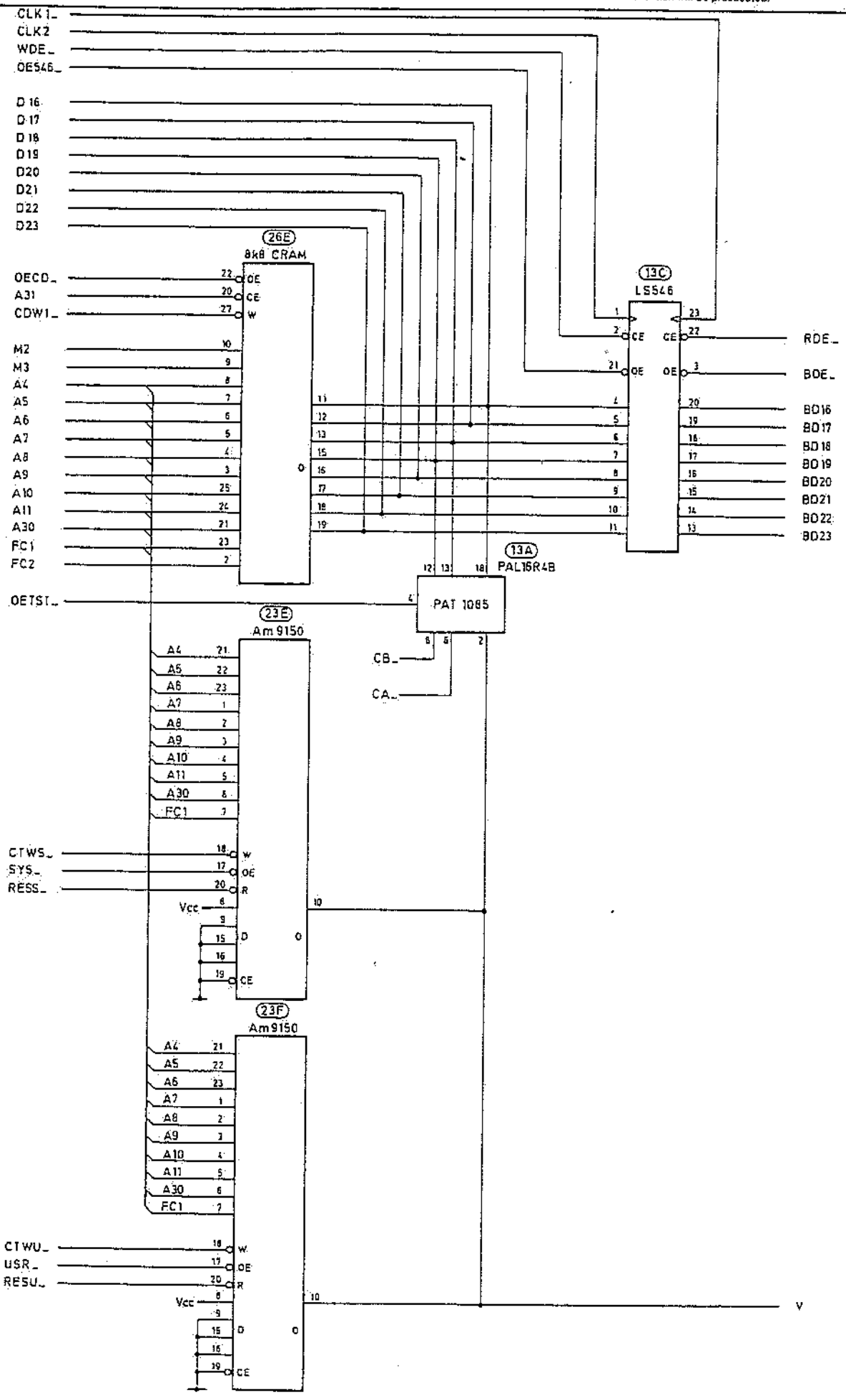
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Cache structure part 0

81 - 1121 - 30



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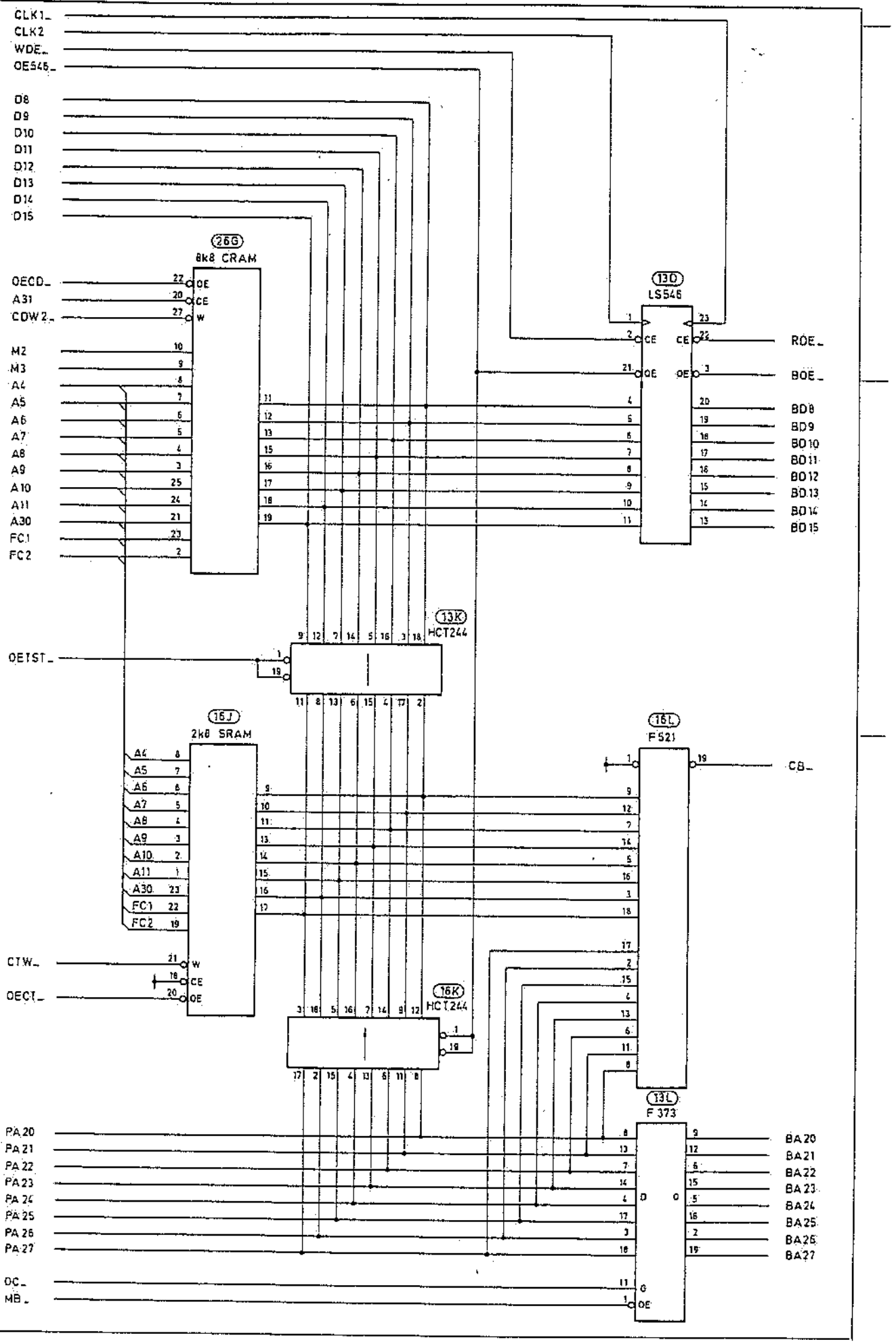
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Cache structure part 1

81-1121-30



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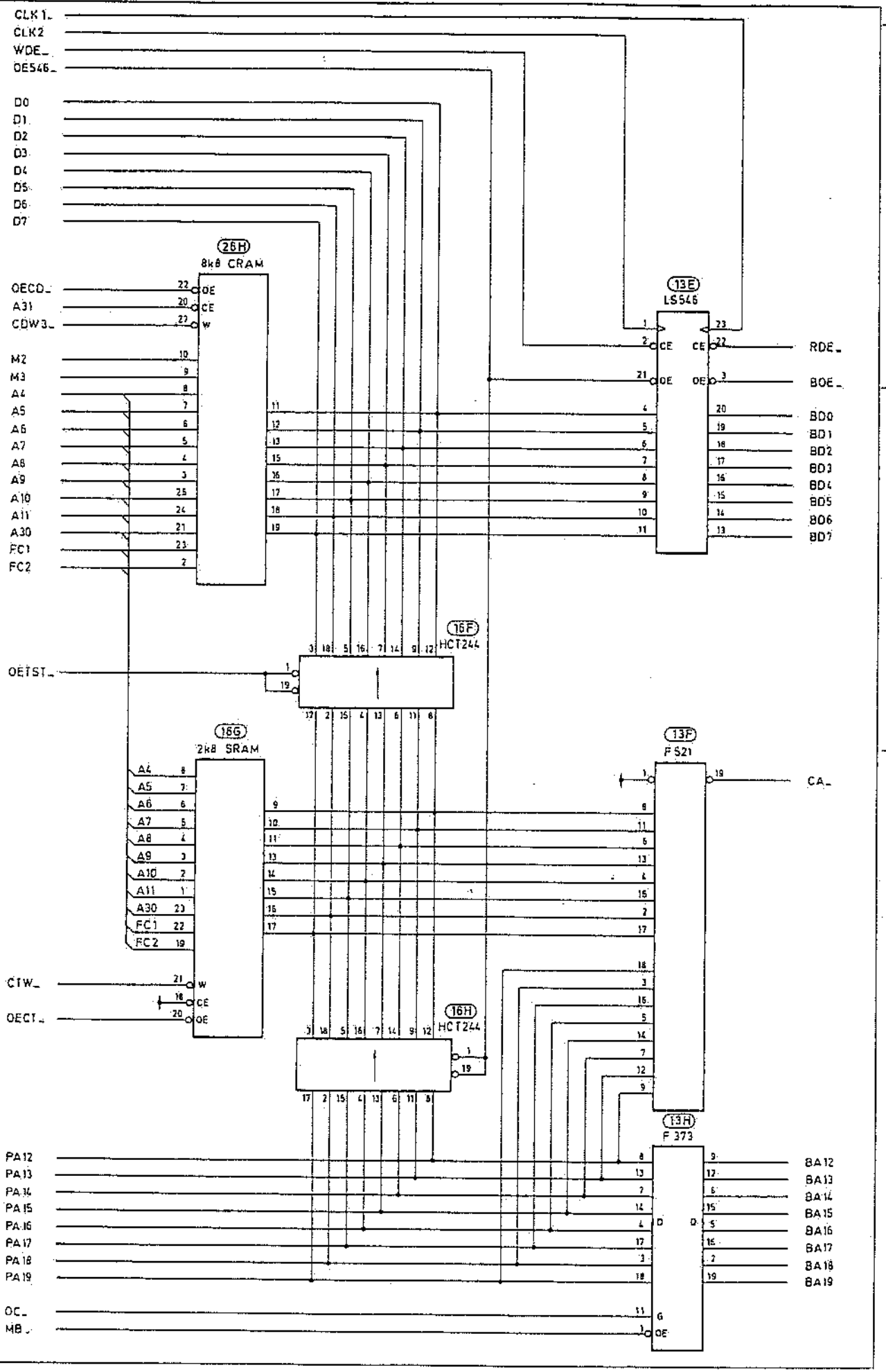
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Cache structure part 2

81 - 1121 - 30



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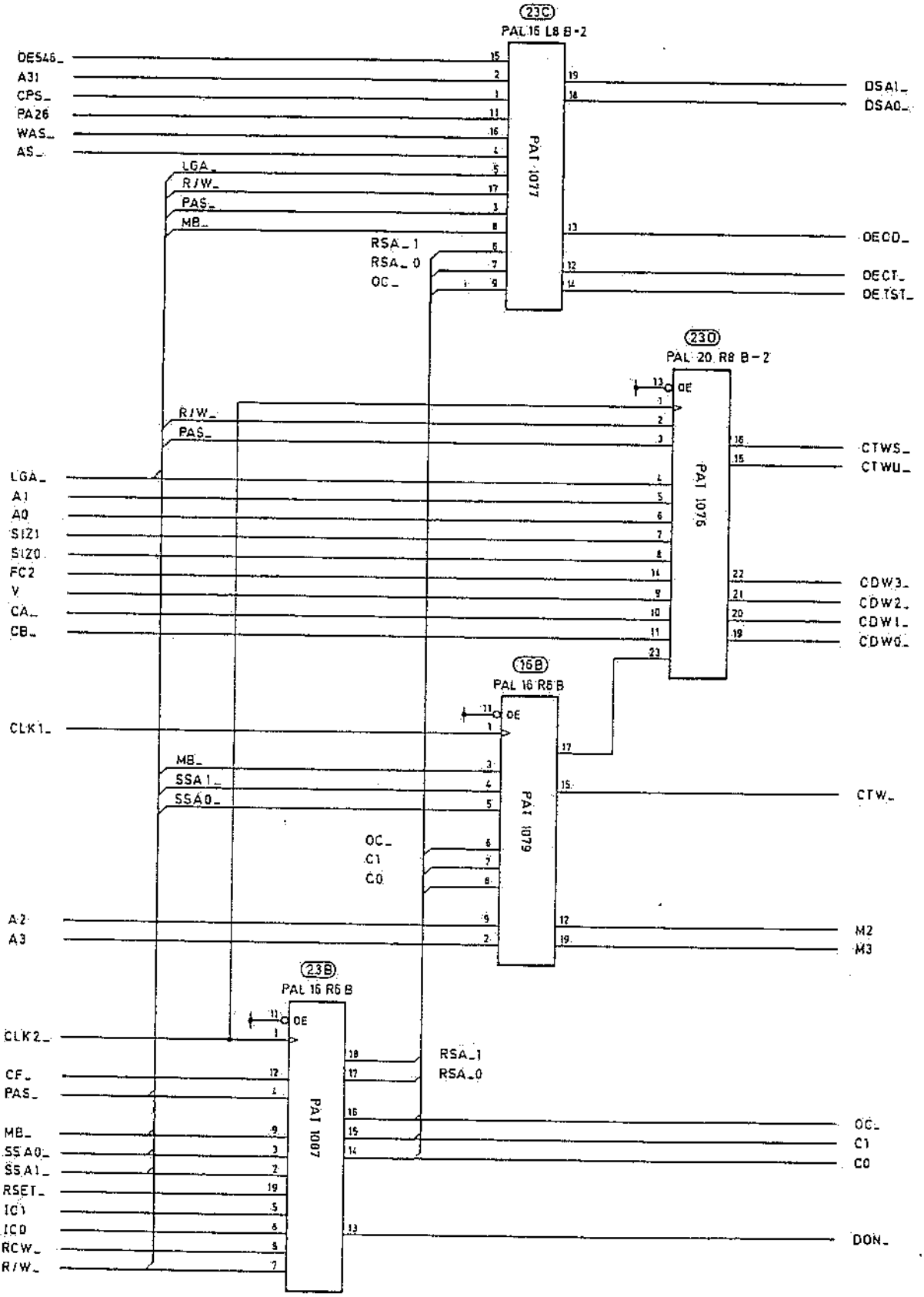
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC

Cache structure part 3

81-1121-30



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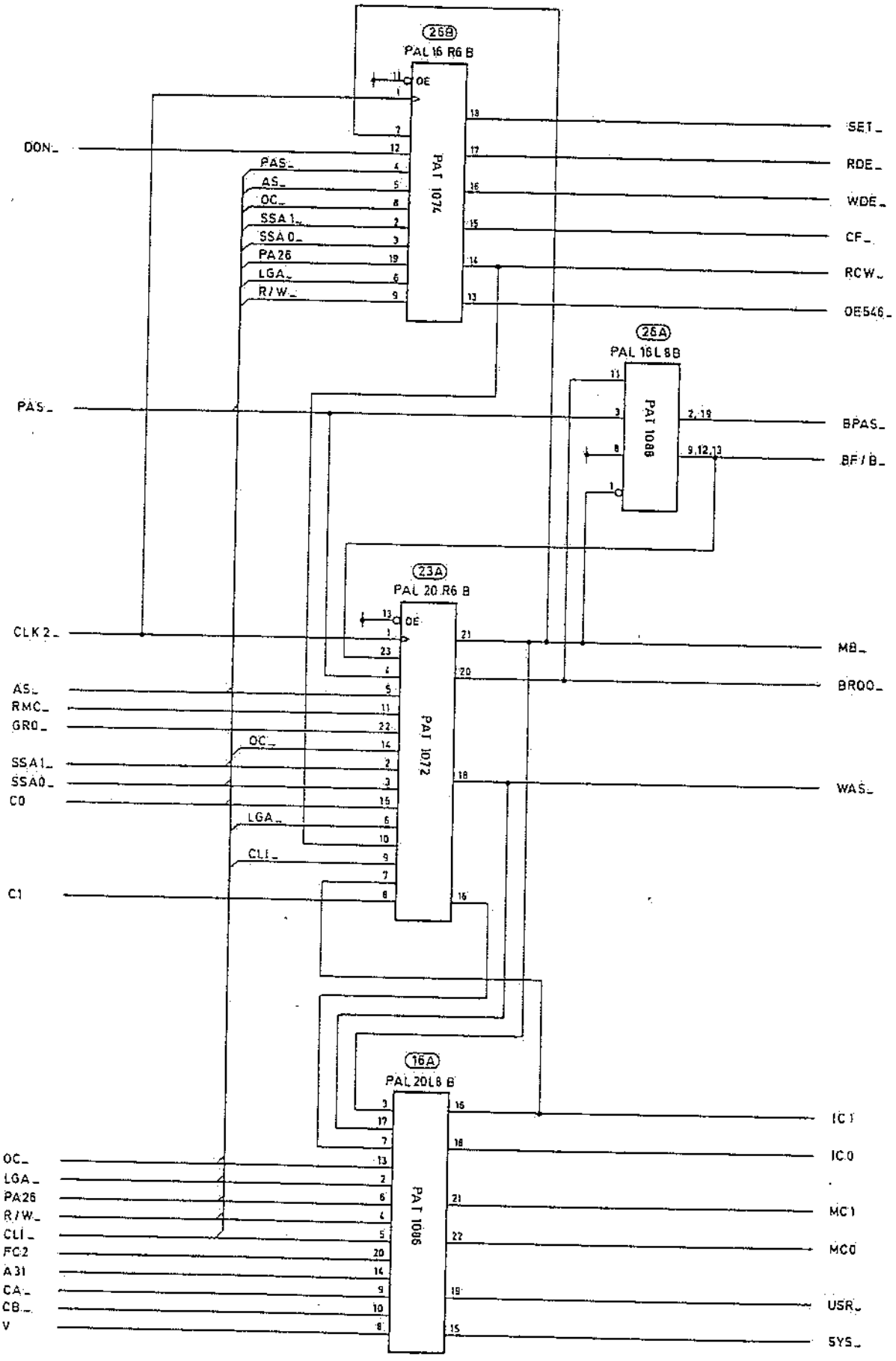
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC

CPU internal control

81 - 1121 - 30



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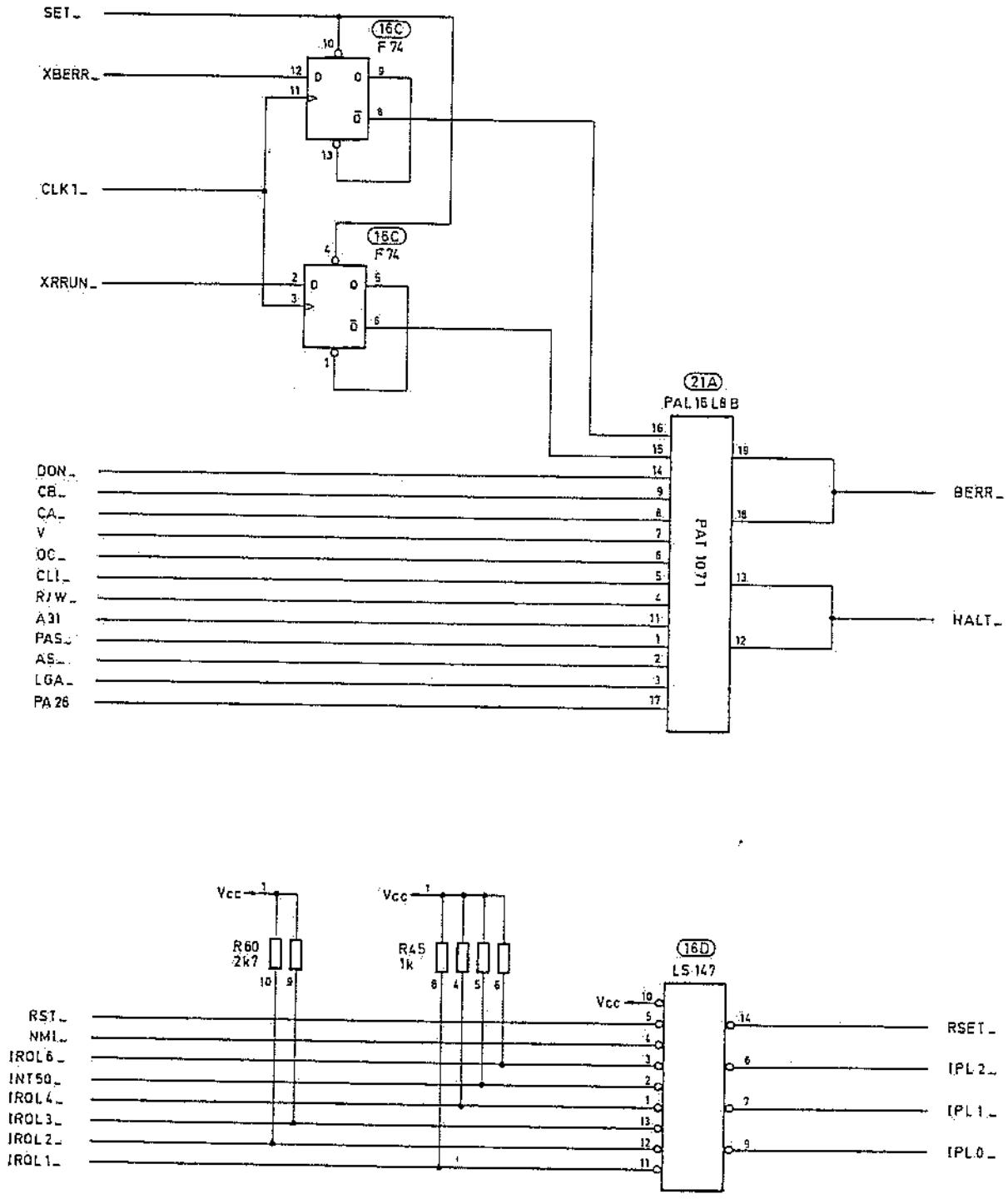
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
CPU bus control

81 - 1121 - 30



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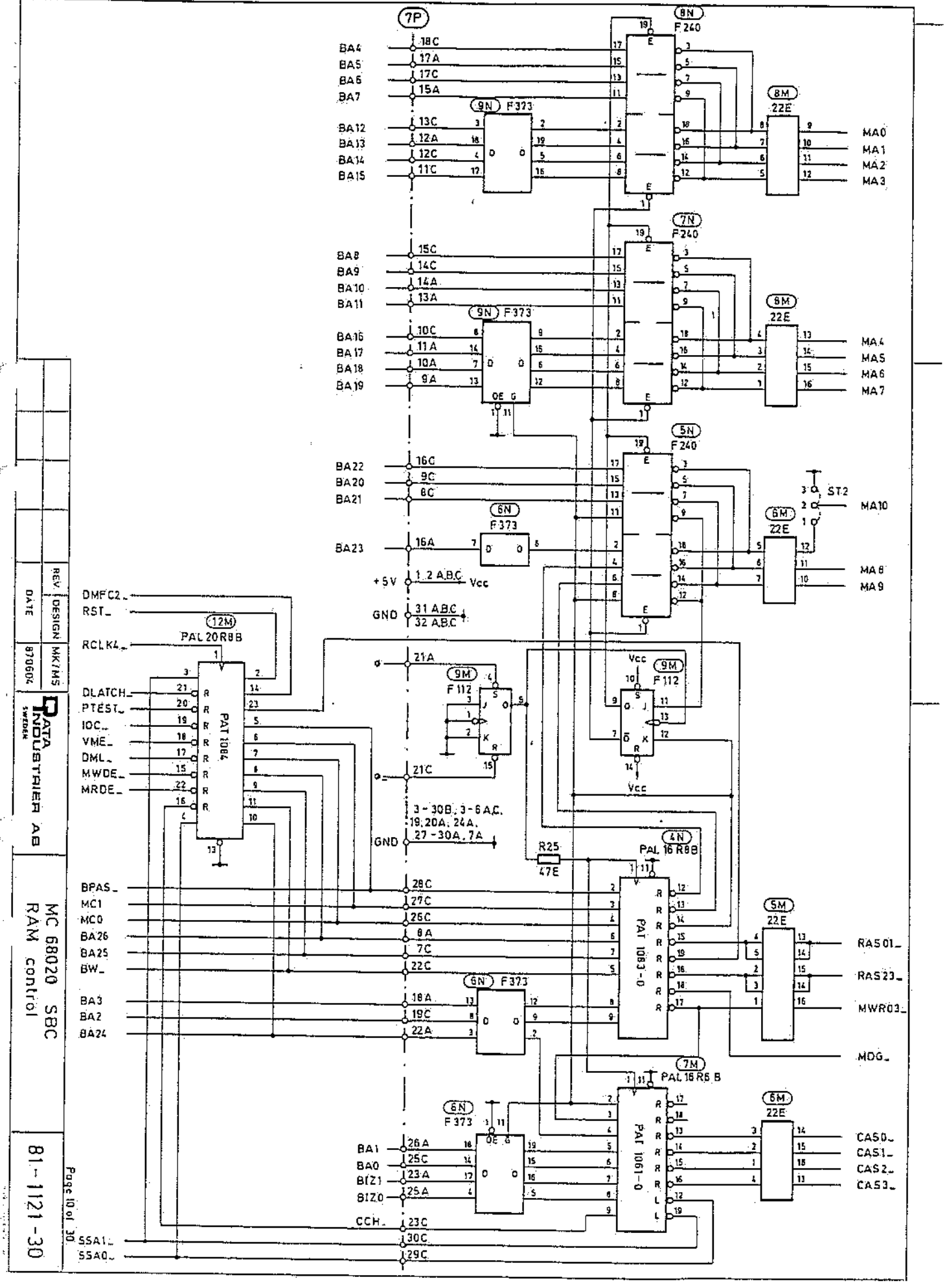
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
CPU exception control

81-1121-30



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MC 68020 SBC
RAM control

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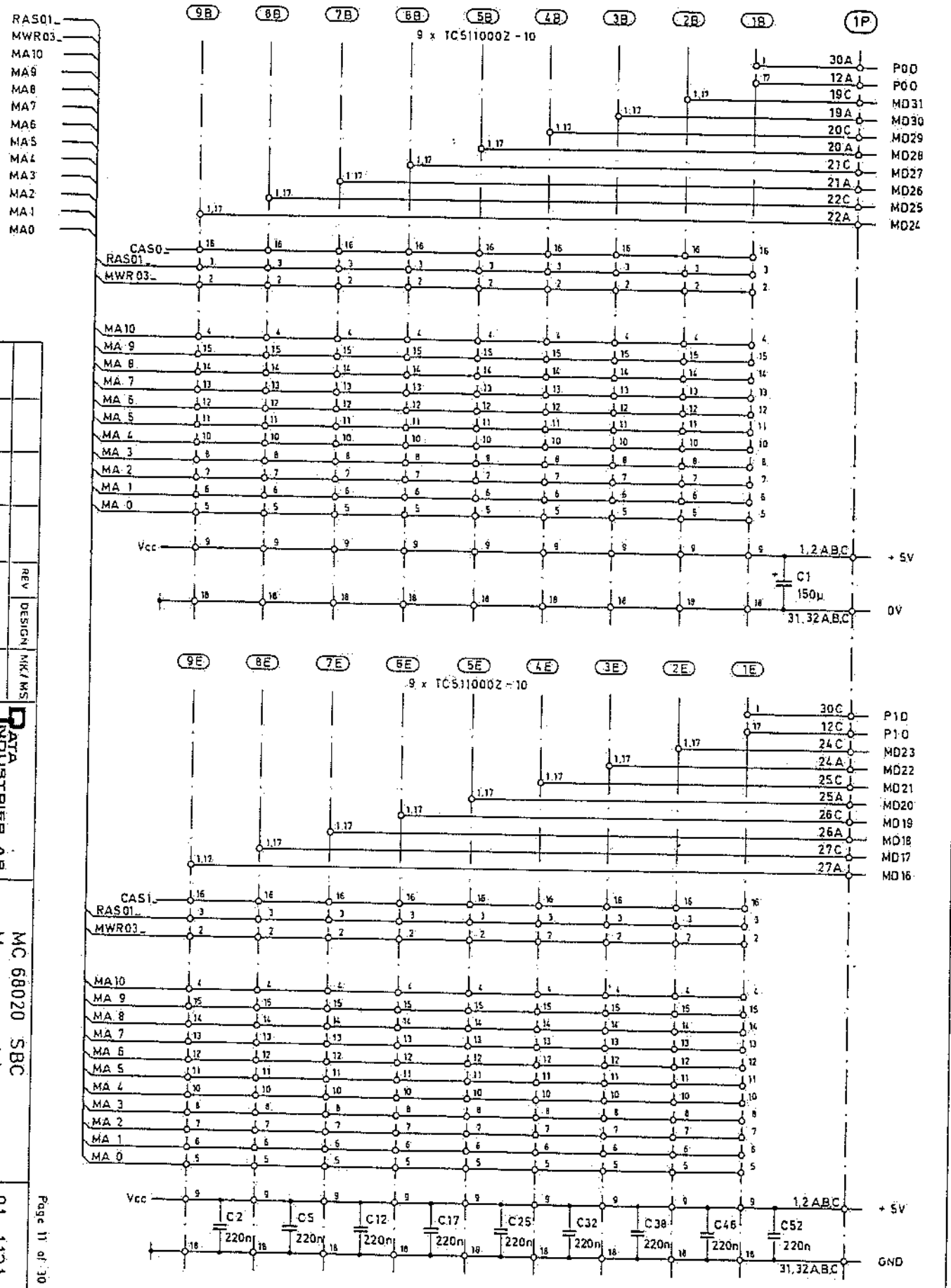

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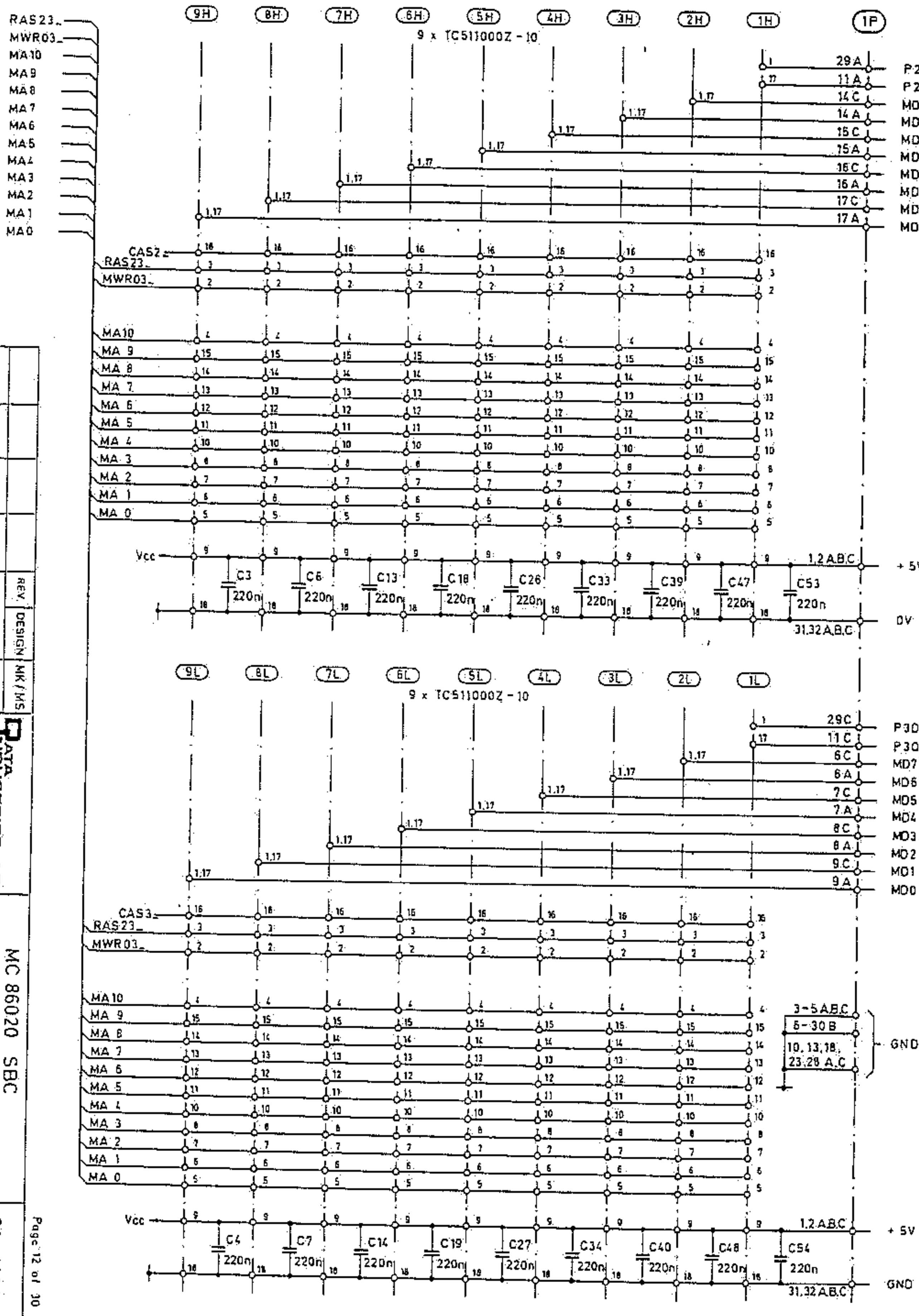
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Memory matrix part 01

81-1121-30



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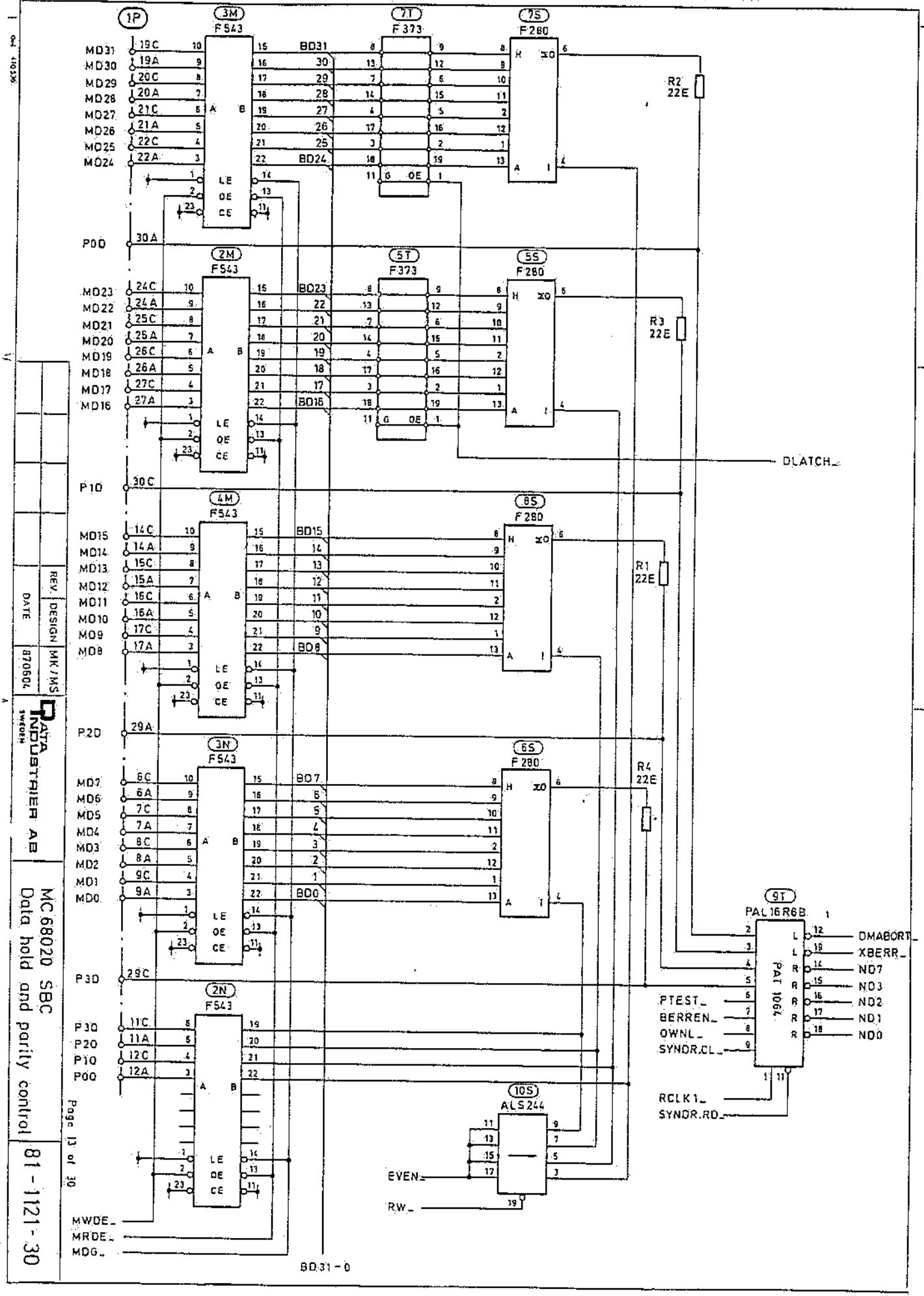
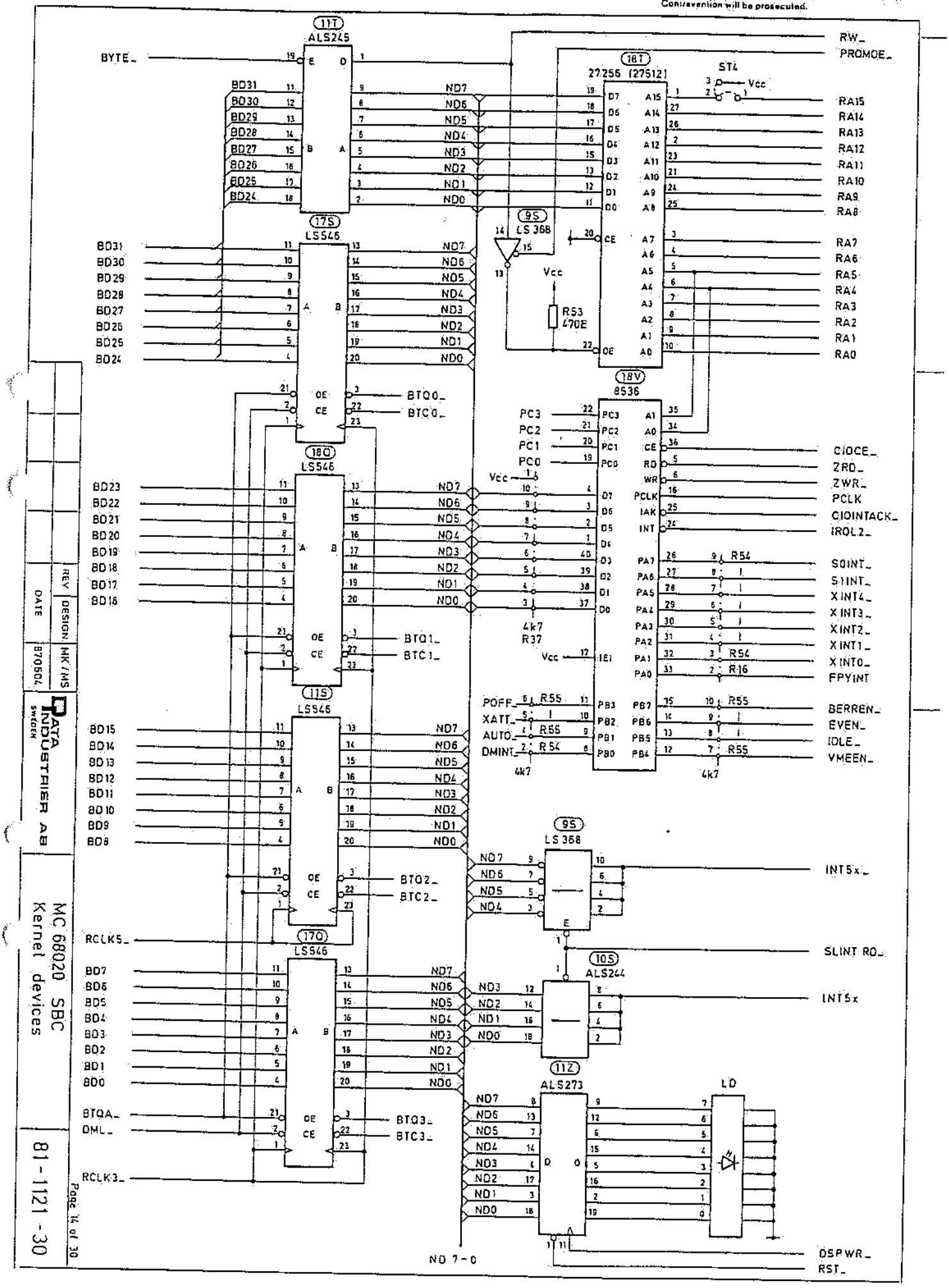
DATA INDUSTRIER - B
SWEDEN

MC 86020 SBC
Memory matrix part 23

81-1121-30





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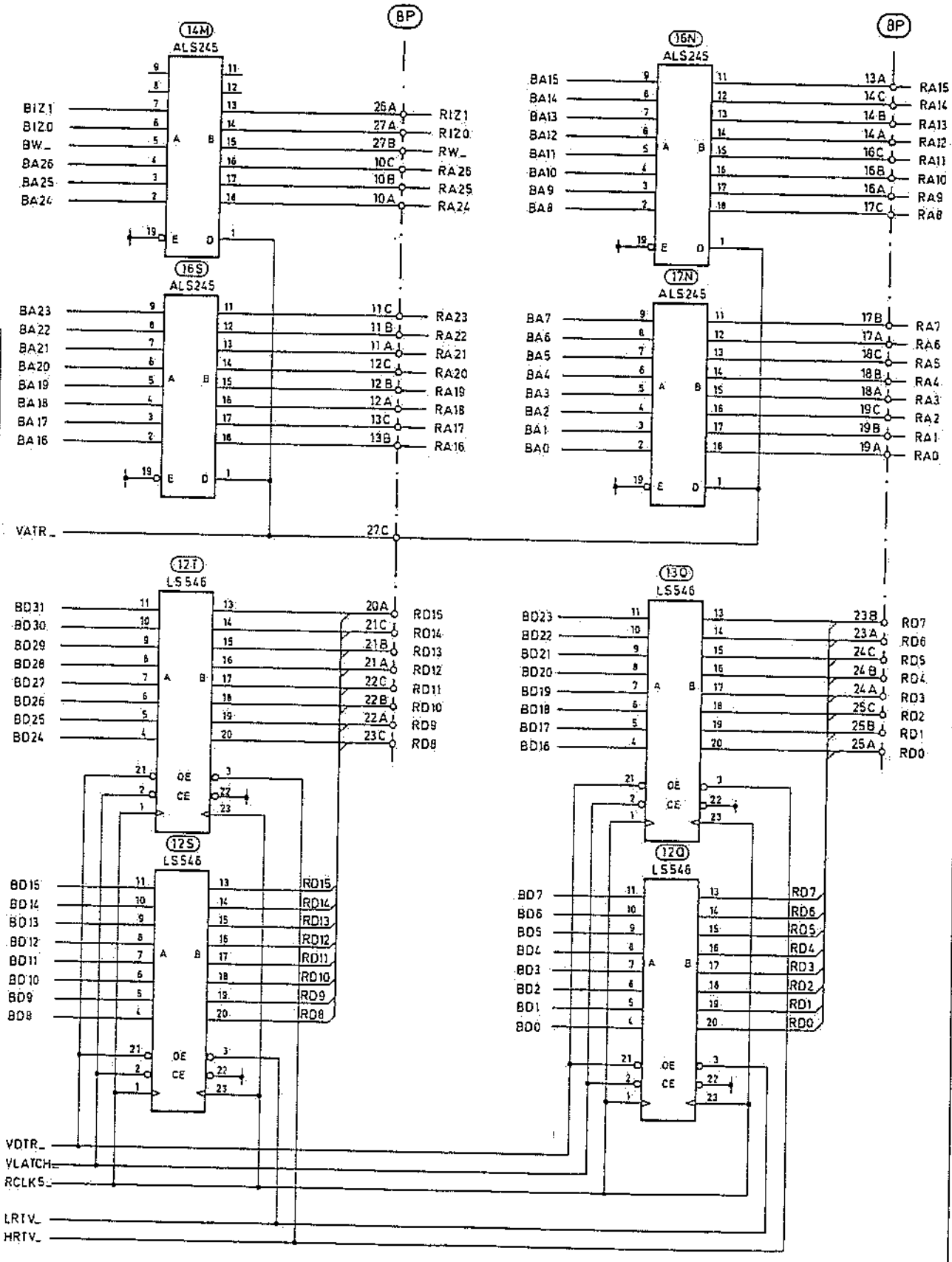
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Kernel devices

81 - 1121 - 30



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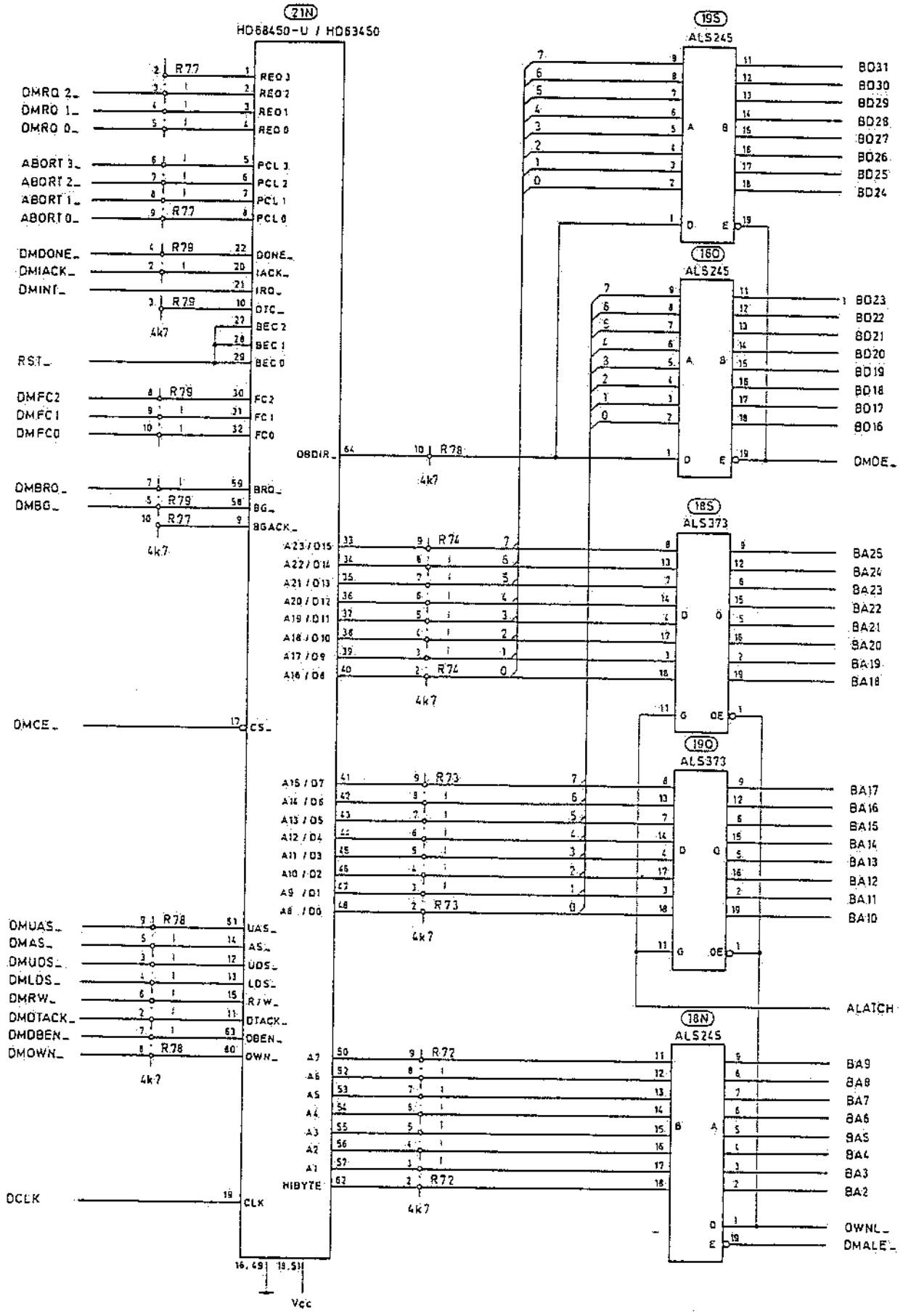
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Expansion buffers

81-1121-30



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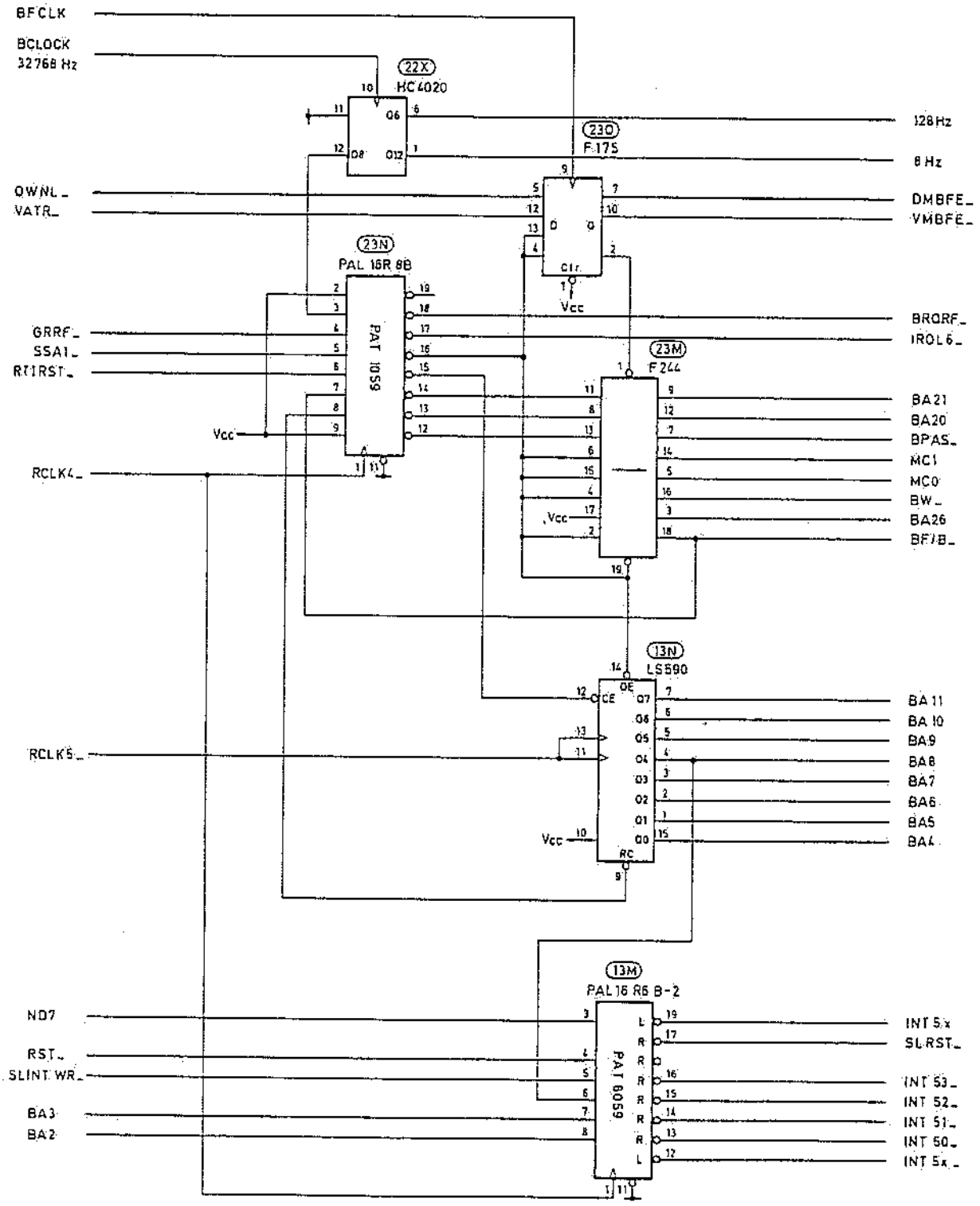
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
DMA structure

81 - 1121 - 30



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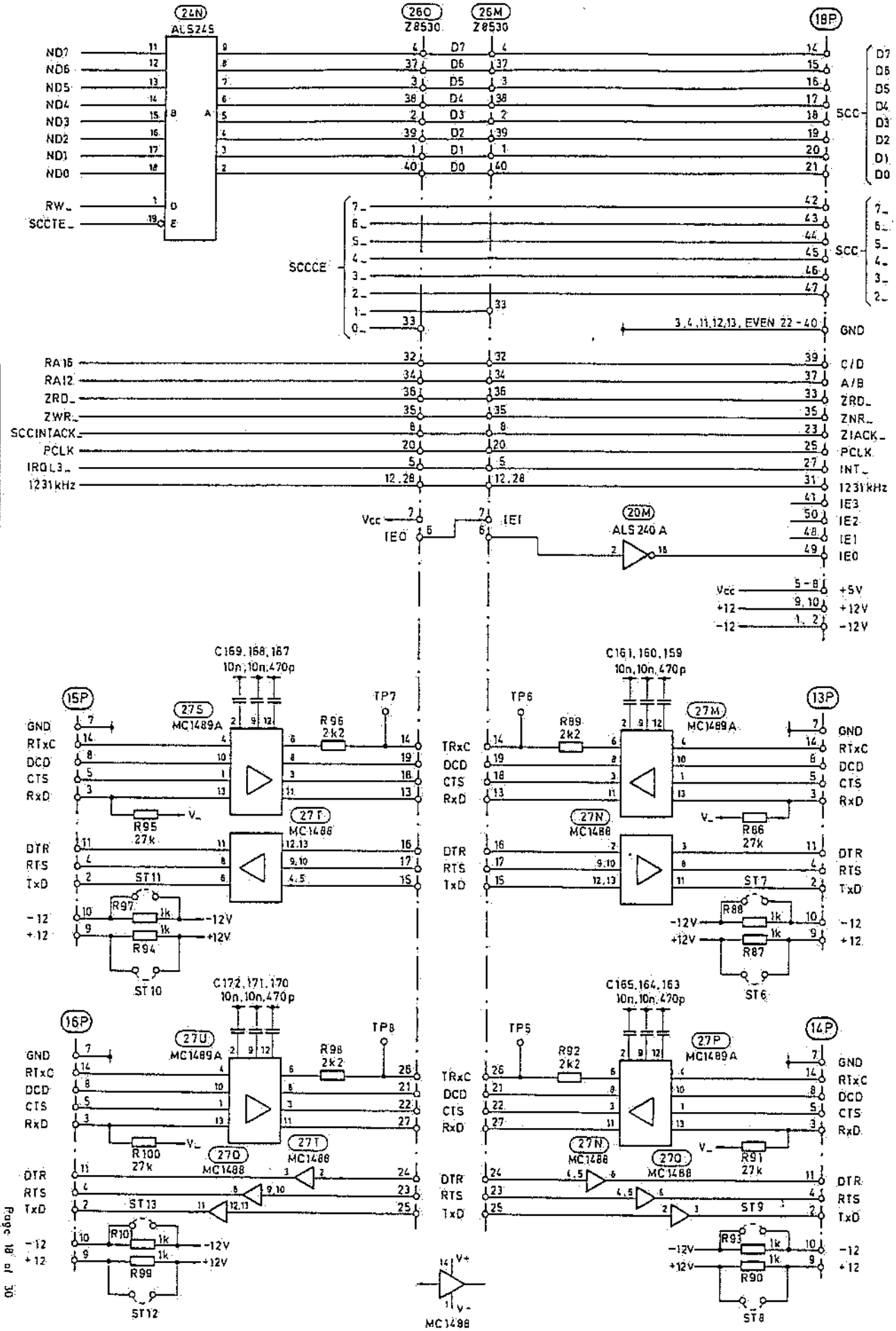
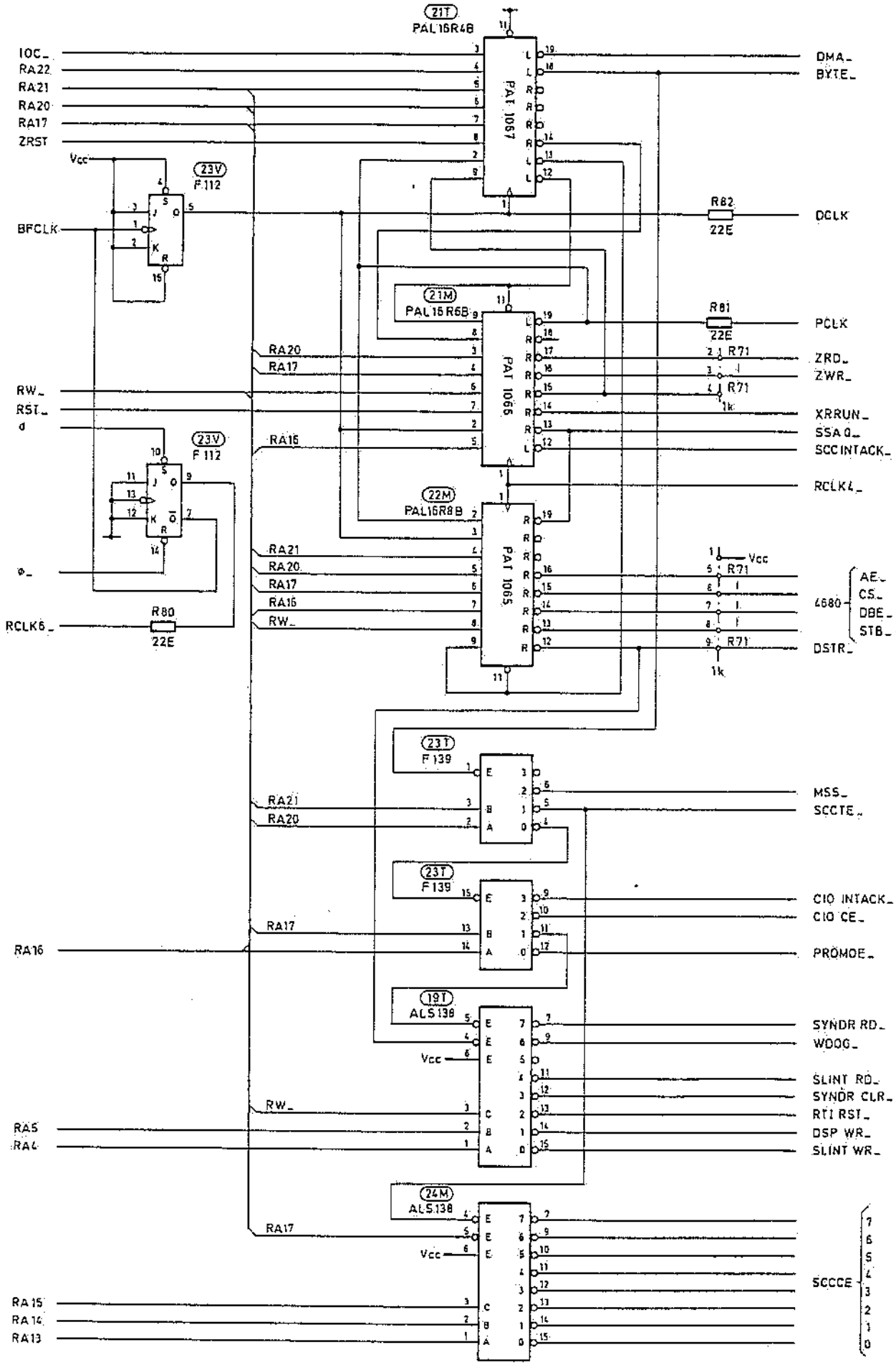
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Refresh control

81 - 1121 - 30





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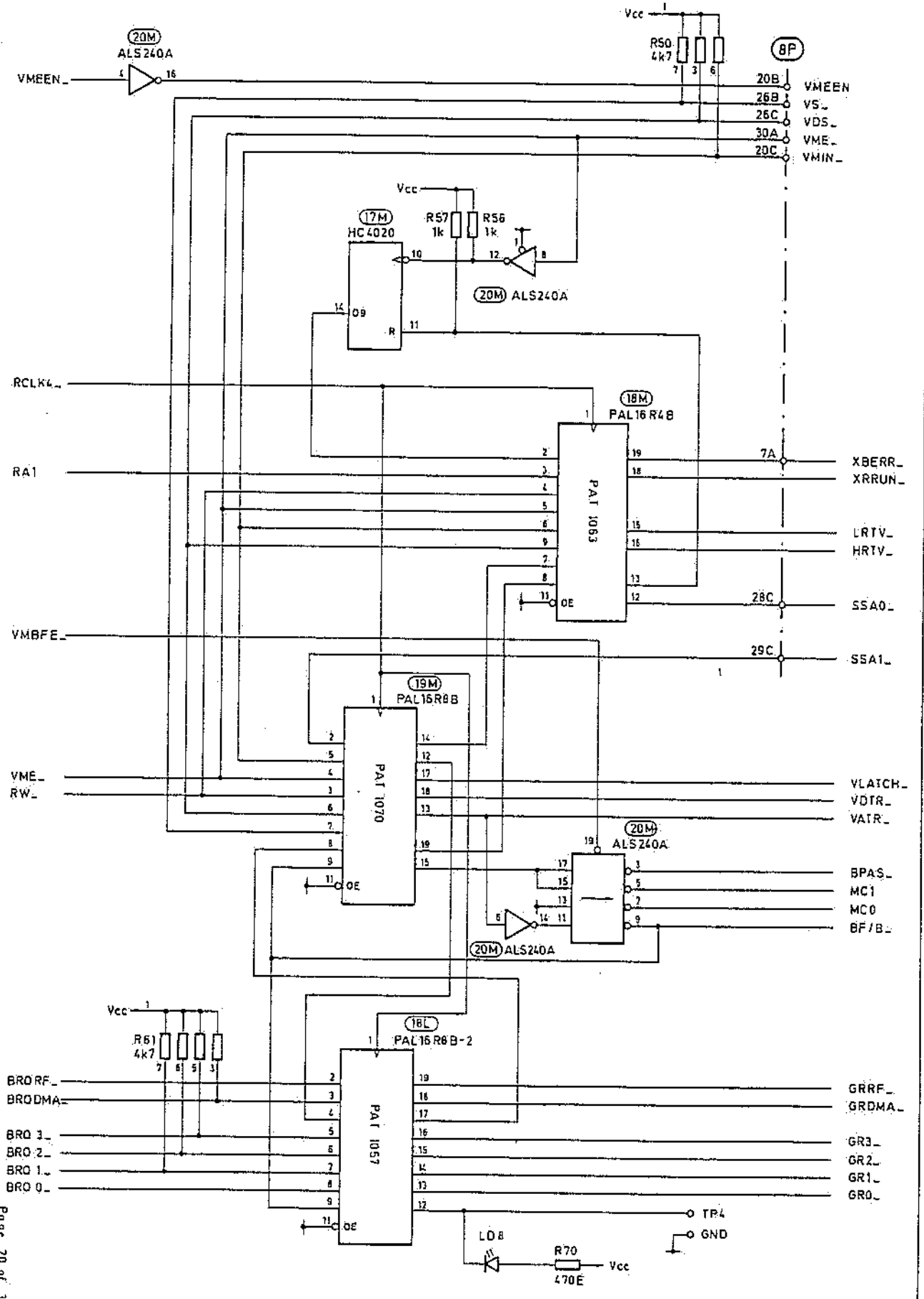
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
I/O part decoders

81 - 1121 - 30



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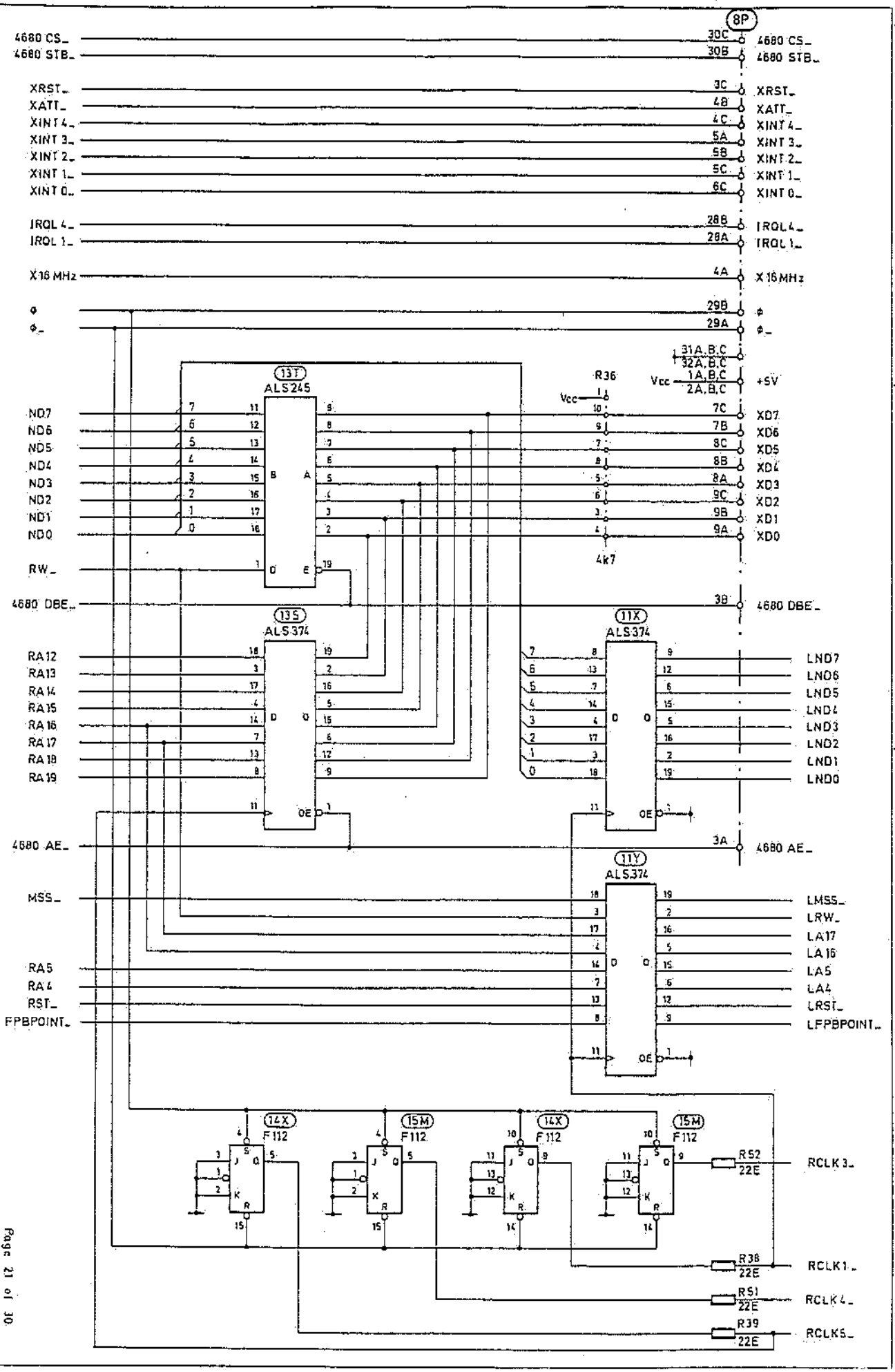
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Bus arbiter & expansion cont.

81-1121-30



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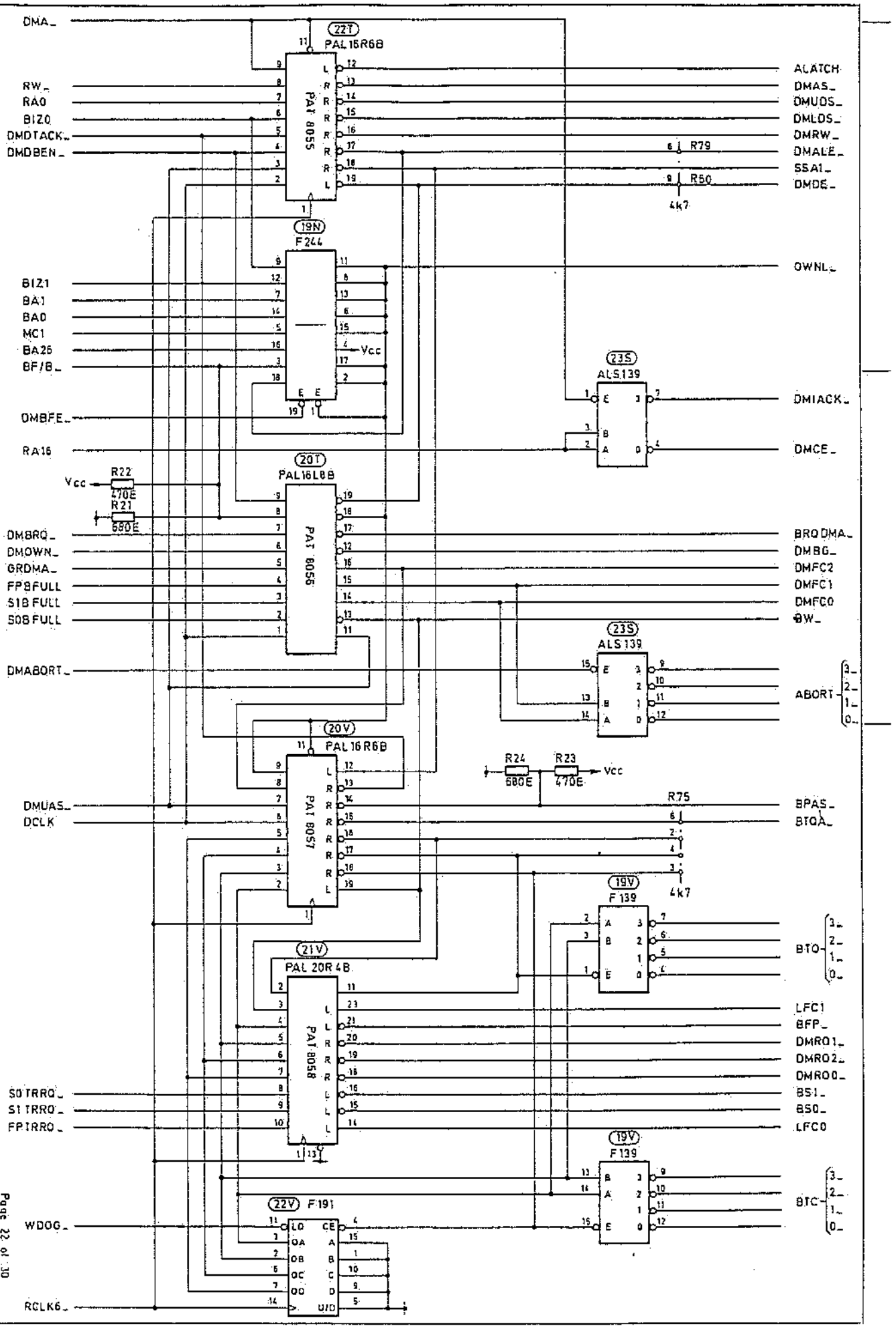
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
4680 interface & byte bus latch

81 - 1121 -30



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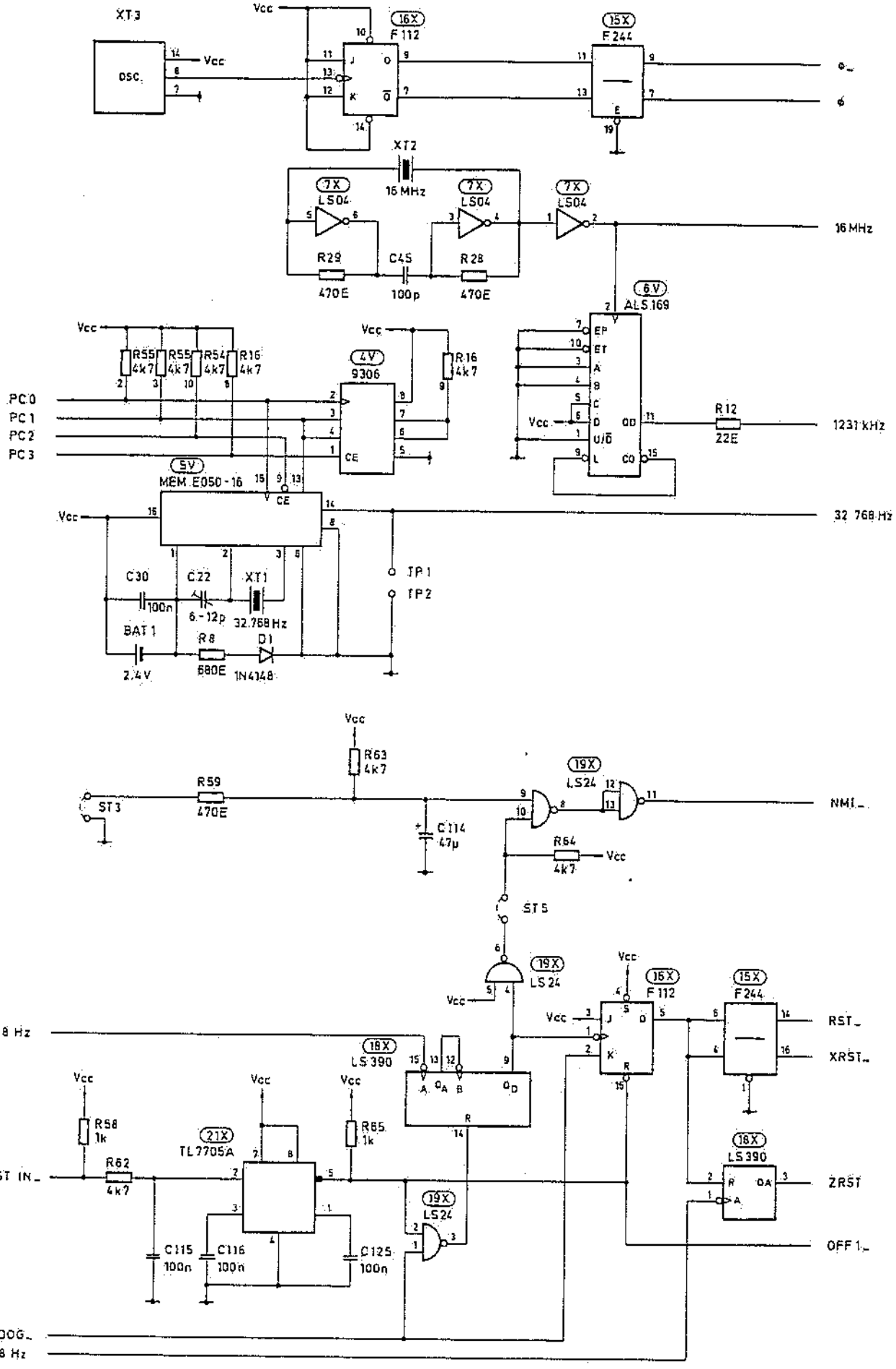
MC 68020 SBC
DMA control

81-1121-30



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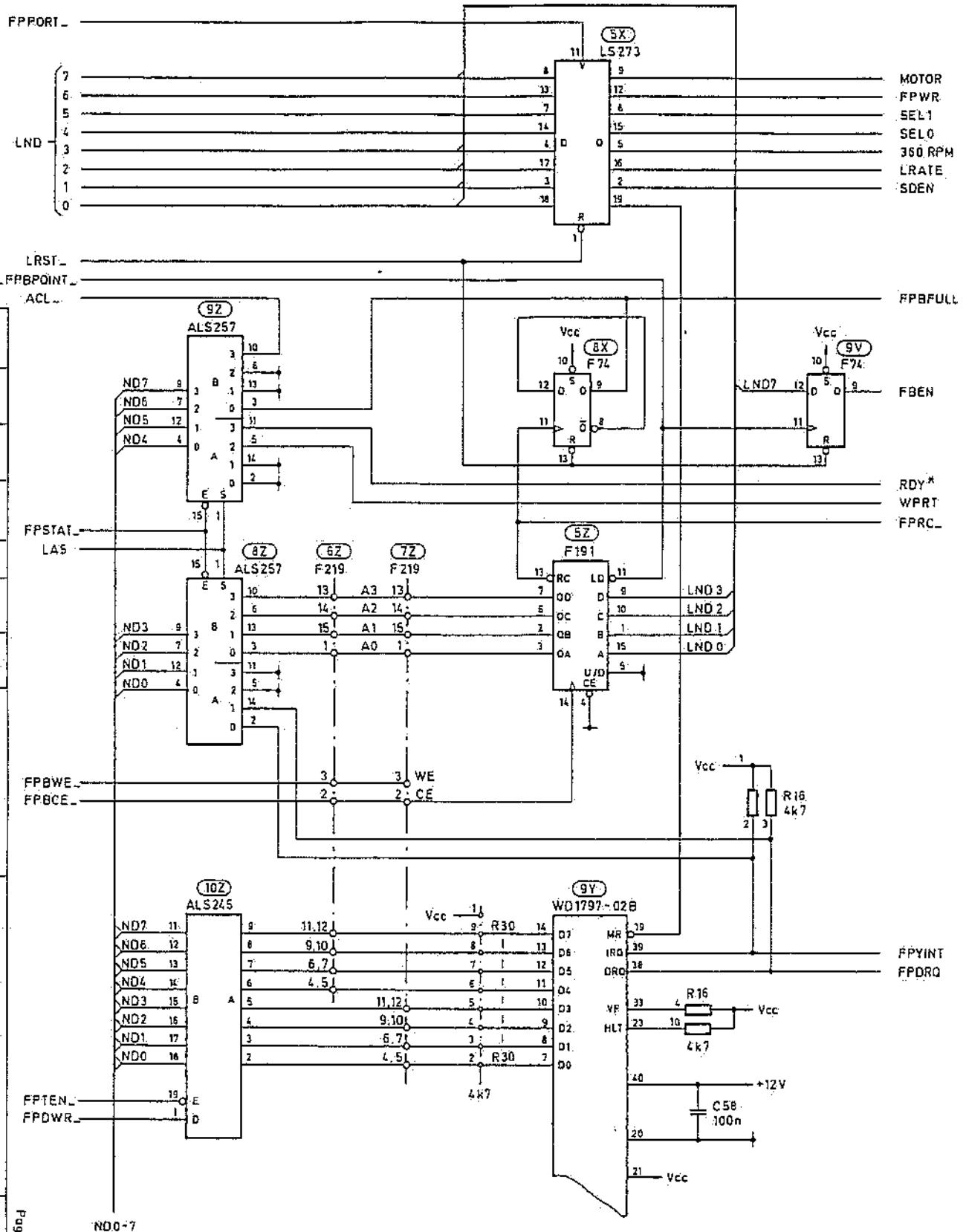
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Miscellanous control

81 - 1121 -30



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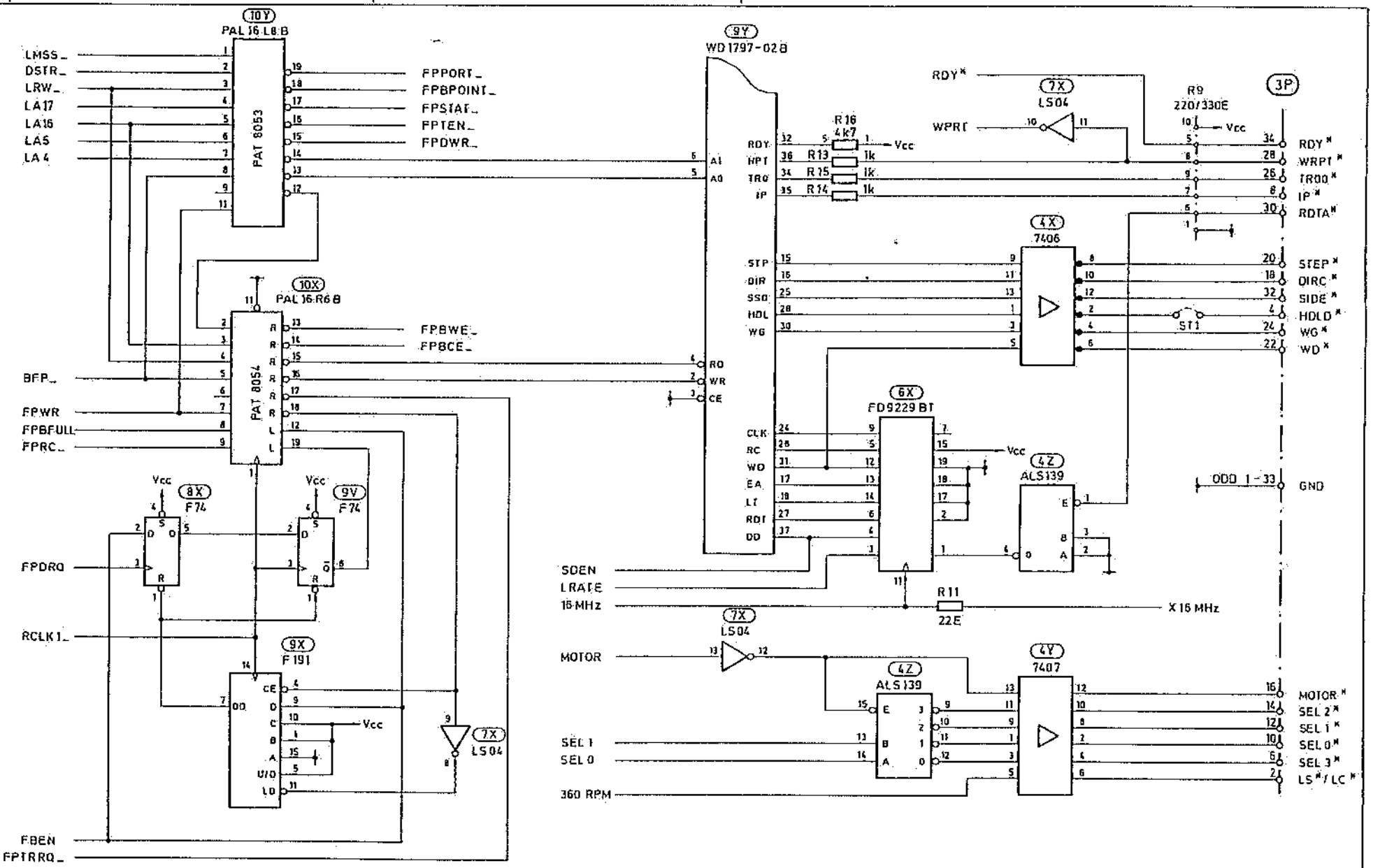
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Floppy buffer structure

81-1121-30



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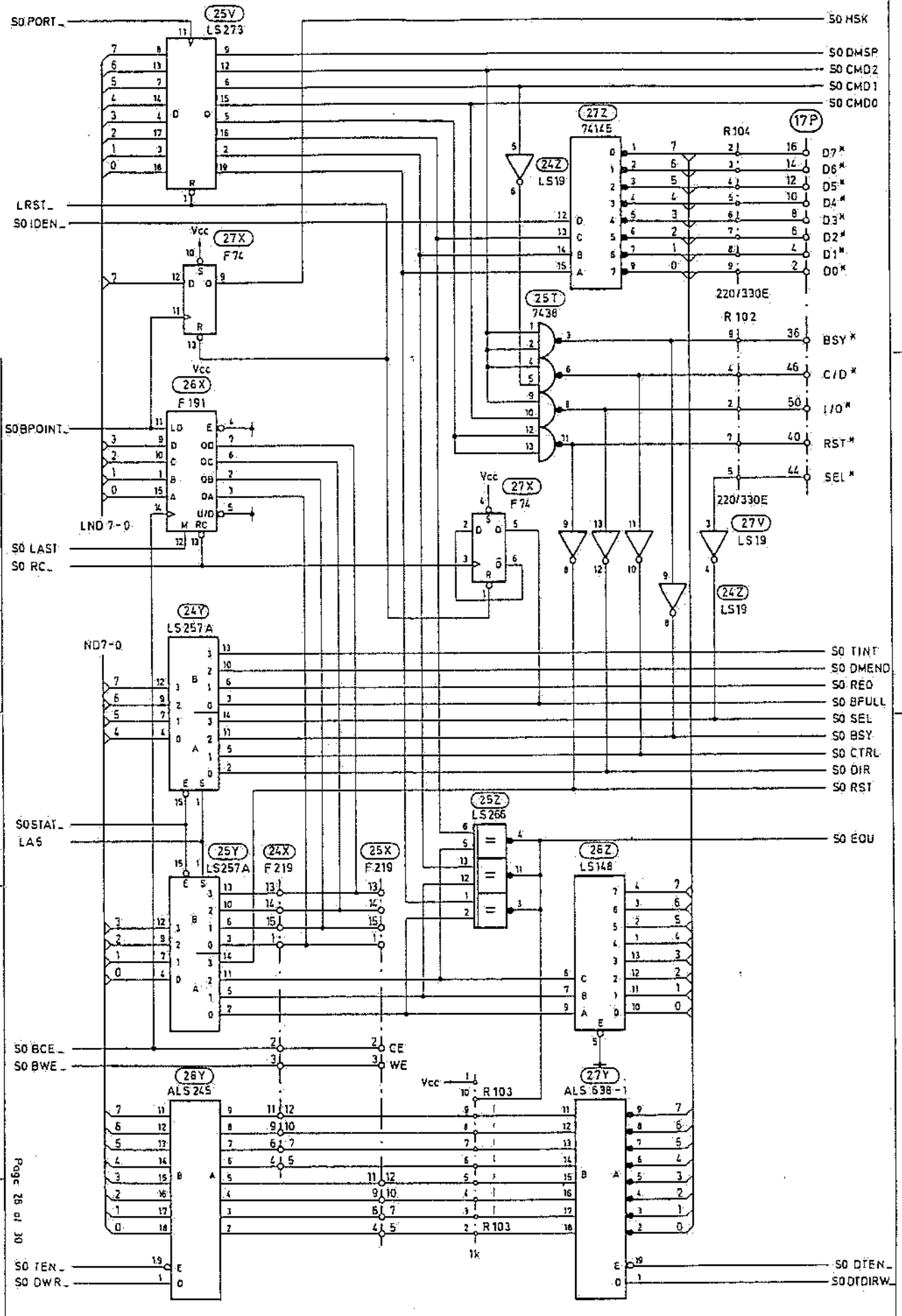
DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
Floppy interface

81-1121-30



DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
SCSI 0 structure

81-1121-30

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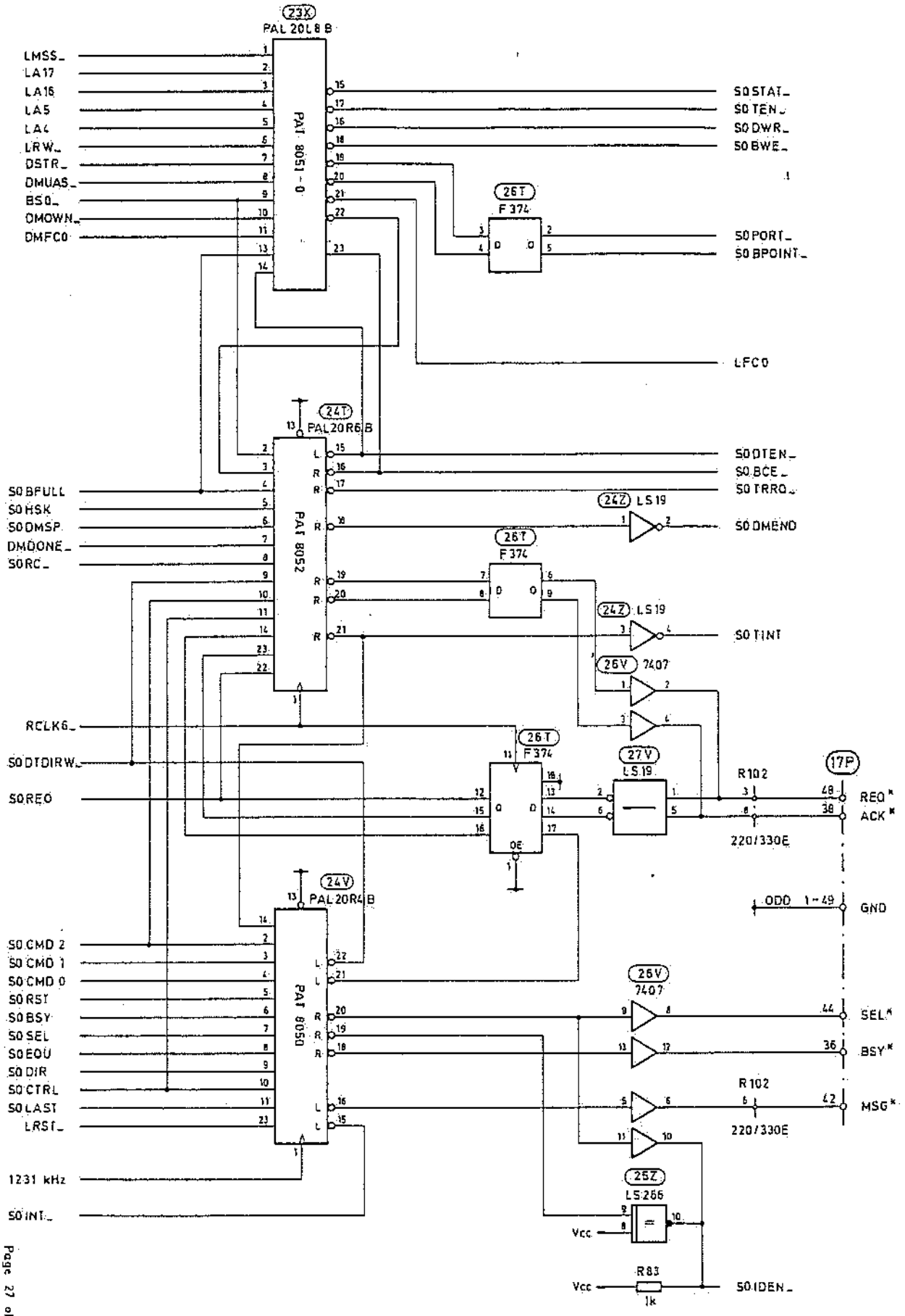

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DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
SCSI 0 control

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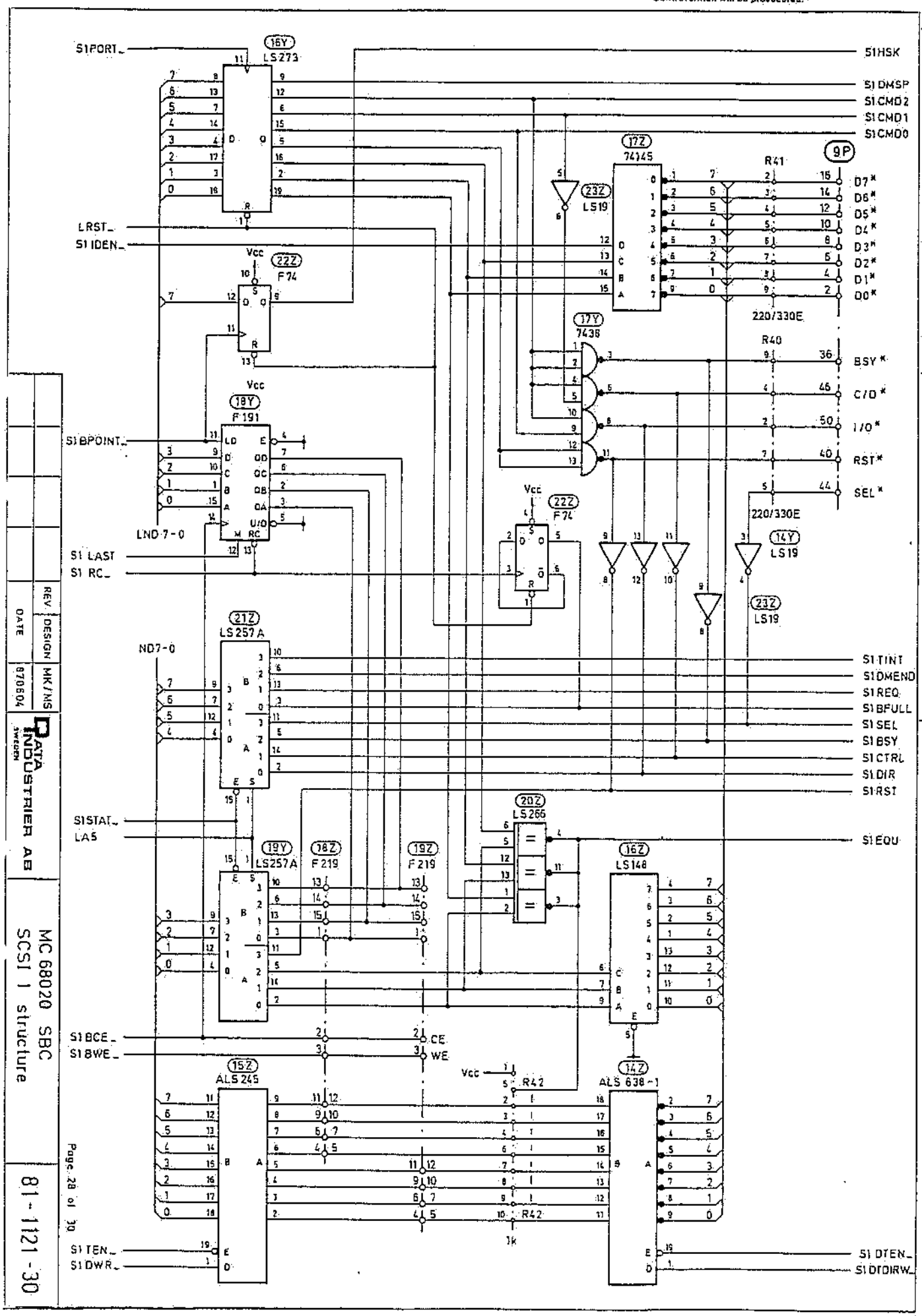

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DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
SCSI 1 structure

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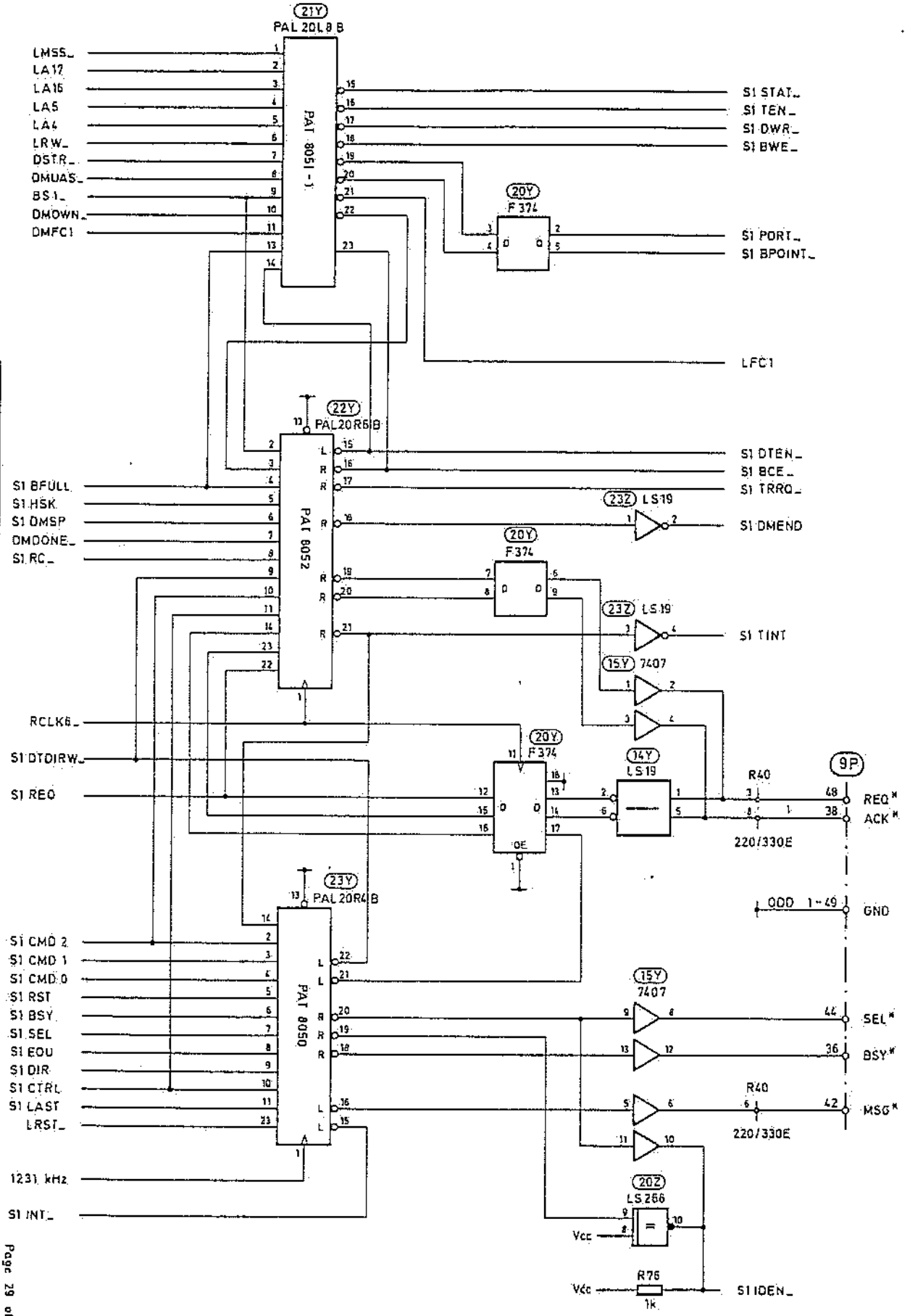

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DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
SCSI 1 control

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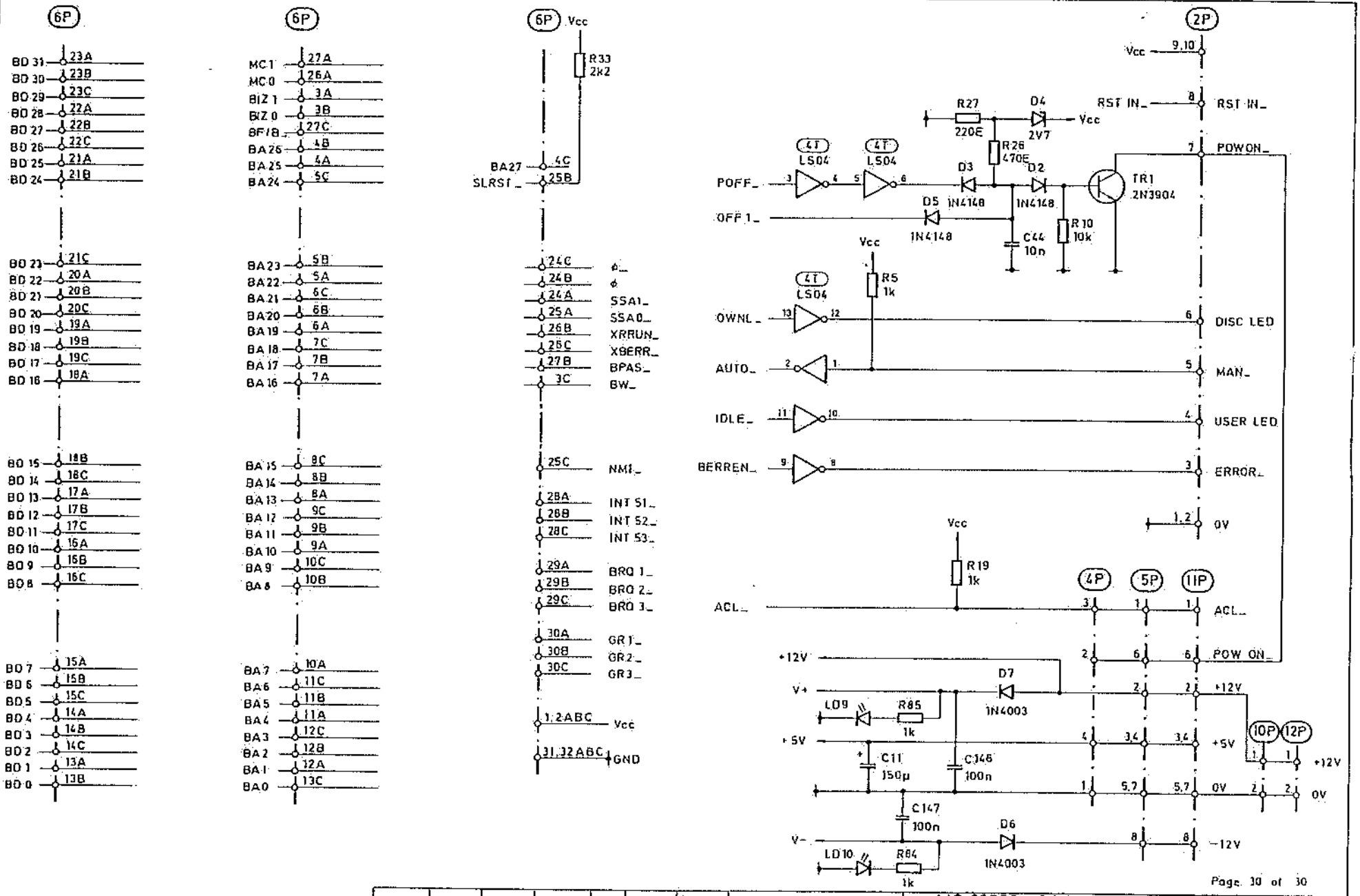

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DATA INDUSTRIER AB SWEDEN

MC 68020 SBC
CPU expansion bus & control panel logic

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DATA INDUSTRIER AB

CPU 68020 4MB

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