

DS90

1110-1x

DS90-1x Computer board

E

Diab Data AB

Box 2029 S-183 02 TÄBY  
SWEDEN

## Record of changes:

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**1. DESCRIPTION**

DS90-1x is a high performance low cost single board computer based on the 16/32 bits M68010 CPU, primarily intended to support industrial control and office automation applications.

The basic configuration is one large board (1110-1x) with the following resources. This board is described in this datasheet.

- M68010 CPU with 10 MHz clock, with no wait states.
- 512 KB up to 2 Mb memory. (Up to 4 Mb with mounted expansion. Includes error detection and correction.
- Two-level memory management unit, supporting up to 4 Mb virtual memory per process.
- DMA with 4 independant channels.
- Optional floating point processor (NS32081).
- 4 serial V24-ports. (Up to 12 ports with mounted boards.)
- Two high performance SASI interfaces. E.g. for Winchester disc and tape streamer.
- Floppy interface for up to two 5 1/4 inches -floppy drives and two 8 inches -floppy drives.
- Flexible interface expansion capability for DataBoard I/O, VME-boards, graphics and others, using a expansion backplane mounted on the basic board.

The two main versions of DS90-1x are:

- DS90-10 Business version, DataBoard and VME expansion, using the computer board version 1110-12.
- DS90-11 Industry version with DataBoard expansion, using the computer board version 1110-11.

The main components in a system are:

- 1110-1x Computer board, 2 Mb memory, 4 serial ports.
- 2107-00 2 Mb memory for direct mounting on 1110-1x.
- 5172-00 4 serial V24-ports. Two 5172-boards can be mounted on 1110-1x.
- 5173-00 Expansion backplane for the industry version for mounting on the 1110-11, with
  - 3 DataBoard I/O-positions.
  - 1 General expansion connector.
- 5175-00 DS90-11 Control panel.
- 5182-00/5183-00 DS90-10 Control panel.
- 5180-00/5181-00
  - Expansion backplane for the business version for mounting on the 1110-10, with
    - 4 DataBoard I/O-positions.
    - 2 VME-bus positions.
    - 1 Special expansion port.
- 7140-00 NS32081 FPU option.

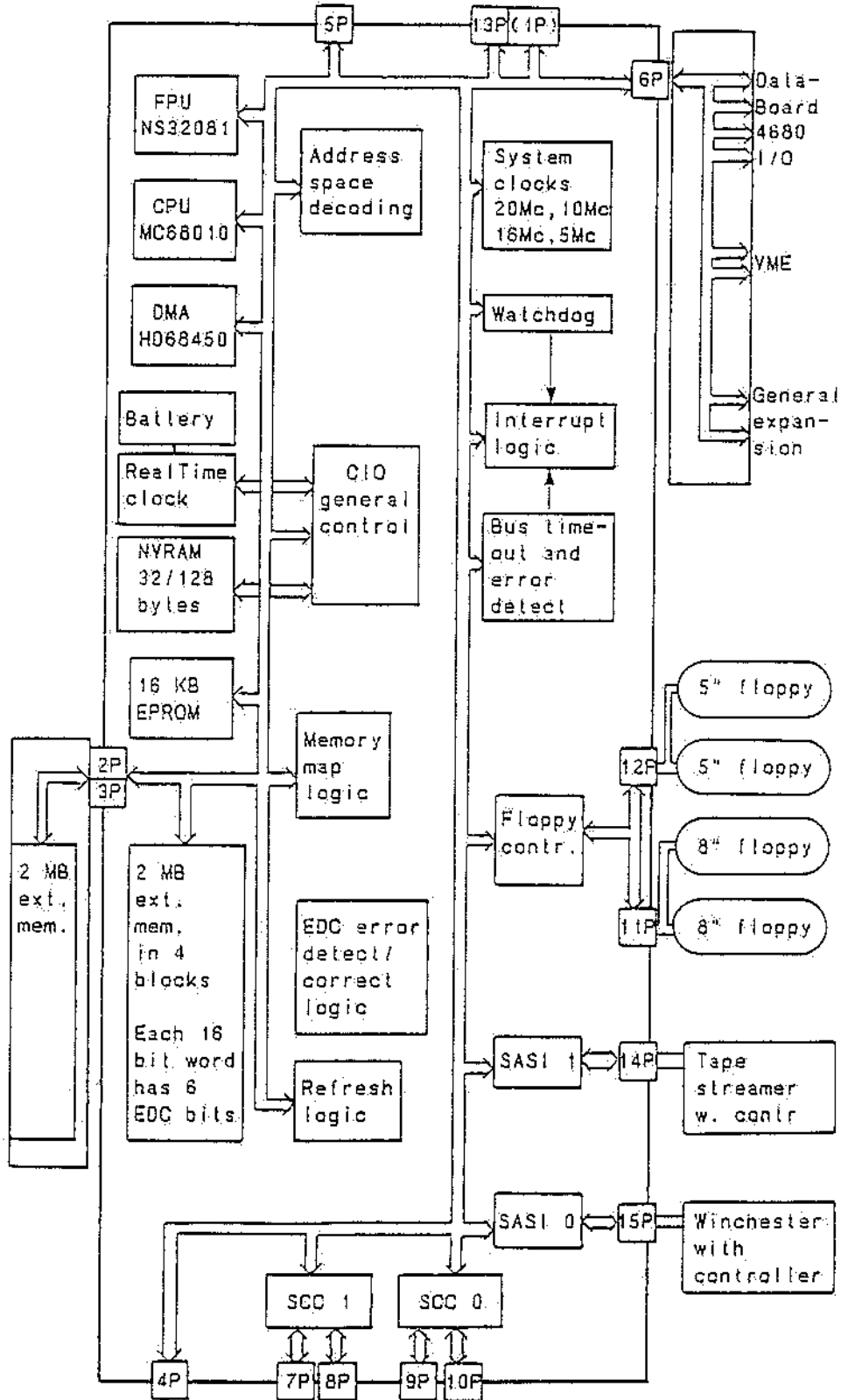
These are described in separate datasheets.

For further I/O-expansion a DataBoard I/O-expansion rack is available connected through the 4202/4203-00 adapters. Alternatively IQ/IO-systems for direct industrial level signals can be connected.

2. BLOCK DIAGRAMS

2.1 Hardware block diagram.

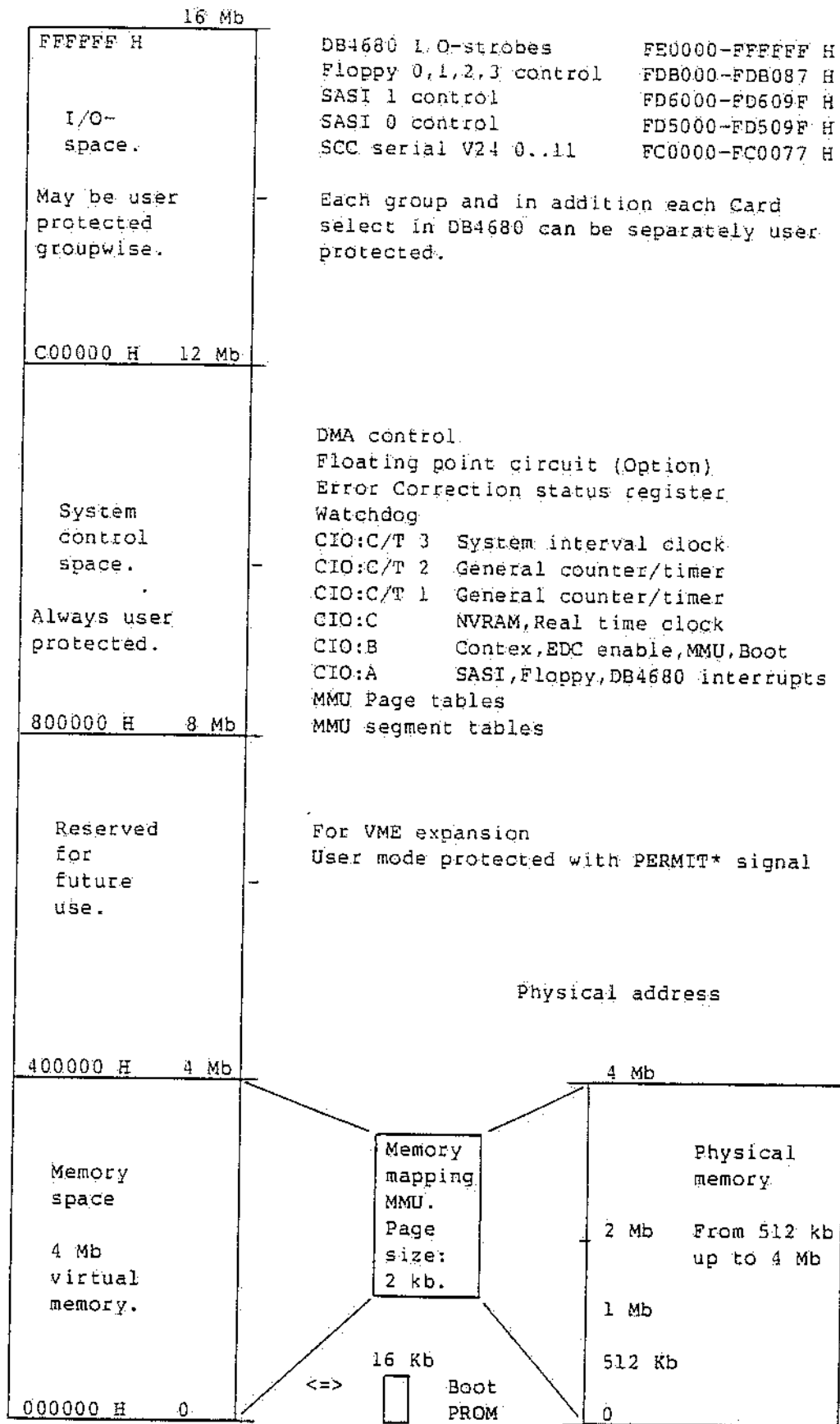
Control panel LEDs and Key Power supply



Expand to  
8 \* V24

4 \* V24  
Serial channels

2.1 Software environment. Logical addresses.



## 3. SUMMARY OF I/O AND SYSTEM SPACE ACCESS ADDRESSES

I/O-SPACE	Address range	2222	1111	1111	11		
		Bits	3210	9876	5432	1098	7654 3210
Data-Board:	FE0001-FFF8DD Hex	1111	111C	CCCC	C000	cc0S	SS01
	CS* bits:			5	4321	0	76
	Special CSB:						1 0
	EXP:						1 1
	I/O-strobe 0..5:						0 S SS
Floppy:	FDB001-FDB087 Hex	1111	1101	1011	0000	C000	0ww1
	WD1797 reg 0..3:					0	ww
	Ctrl-Stat reg:					1	00
SASI 1:	FD6000-FD609F Hex	1111	1101	0110	0000	C00b	bbbb
	Buffer word addr 0..15:					0	b bbbb
	Control with pointer:					1	b bbbb
SASI 0:	FD5000-FD509F Hex	1111	1101	0101	0000	C00b	bbbb
	Buffer word addr 0..15:					0	b bbbb
	Control with pointer:					1	b bbbb
SCC:	FC0001-FC0077 Hex	1111	1100	0000	0000	0SSS	0cD1
	SCC nr 0..7:					SSS	
	c (0=Ch.B, 1=Ch.A):						c
	D (0=Ctrl, 1=Data):						D

SYSTEM SPACE	Address range	2222	1111	1111	11		
	(Only system mode)	Bits	3210	9876	5432	1098	7654 3210
DMA:	830100-8301FF Hex	1000	0011	0000	0001	aaaa	aaaa
	Register 0..255:					aaaa	aaaa
FPU:	820100-8201FF Hex	1000	0010	0000	0001	aaaa	aaaa
	Register 0..255:					aaaa	aaaa
EDC:	810100 Hex	1000	0001	0000	0001	0000	0000
Watchdog:	810100 Hex (= EDC)	1000	0001	0000	0001	0000	0000
CIO:	800101-800107 Hex	1000	0000	0000	0001	0000	0pp1
	Port (0=C, 1=B, 2=A, 3=Ctrl):						pp
MMU:	800000-BFF880 Hex	1SSS	SSSS	Sppp	p000	P000	0000
	Segment 0..127:	SSS	SSSS	S		0	
	Page 0..15 in segm:	SSSSSSSS	Sppp	p		1	
	NOTE! CIO-B selects the process number (0..15):						
	Segment address = 800000+Segm*8000 Hex						
	Page address = 800000+Segm*8000+Page*800+80 Hex						

#### 4. HARDWARE CONFIGURATION AND INSTALLATION.

##### 4.1 Configuration

The 1110-1x computer board are mounted in different types of DS90-1x cabinettes, depending on the version. The industry version (DS90-11) is mounted in a 19 inches chassis with the DataBoard expansion as standard, while the business version (DS90-10) is mounted in a special cabinet with the VME and DataBoard expansions.

The 1110-1x board contains the following main parts:

General system control area with the CPU, DMA, Boot-PROM and the optional floating point processor.

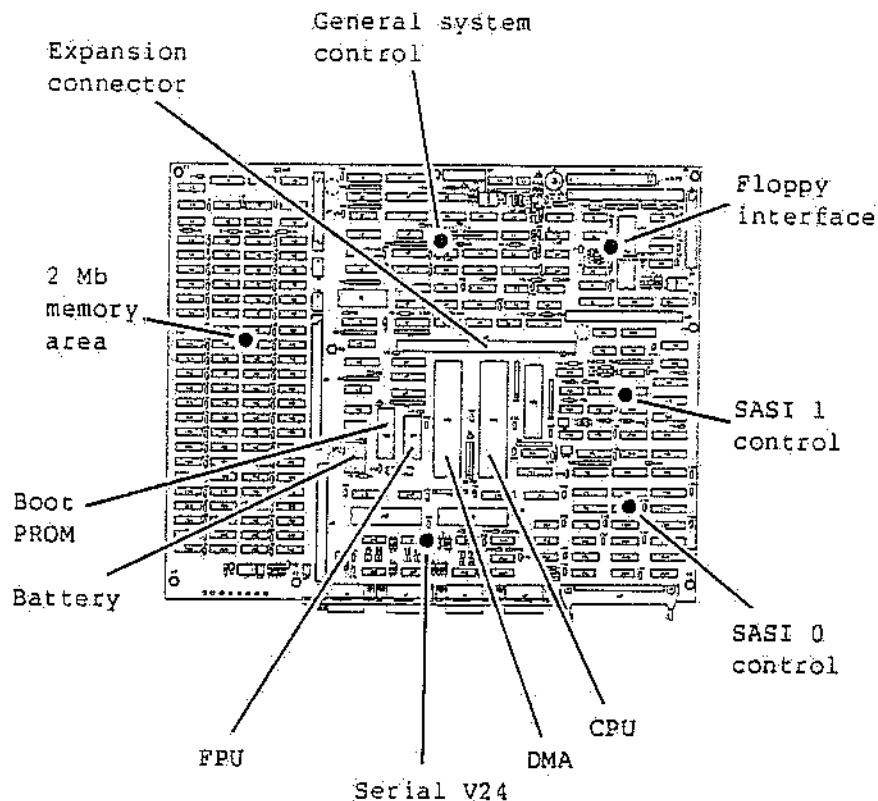
Memory area (2 MB). One expansion board (2 MB) can be mounted on the board, immediately above the standard memory.

Serial channels. Two expansion boards can be mounted on the chassis above this area, connected through a ribbon cable. These connectors are easily accessed from the back of the system.

SASI interfaces. Two independant interfaces.

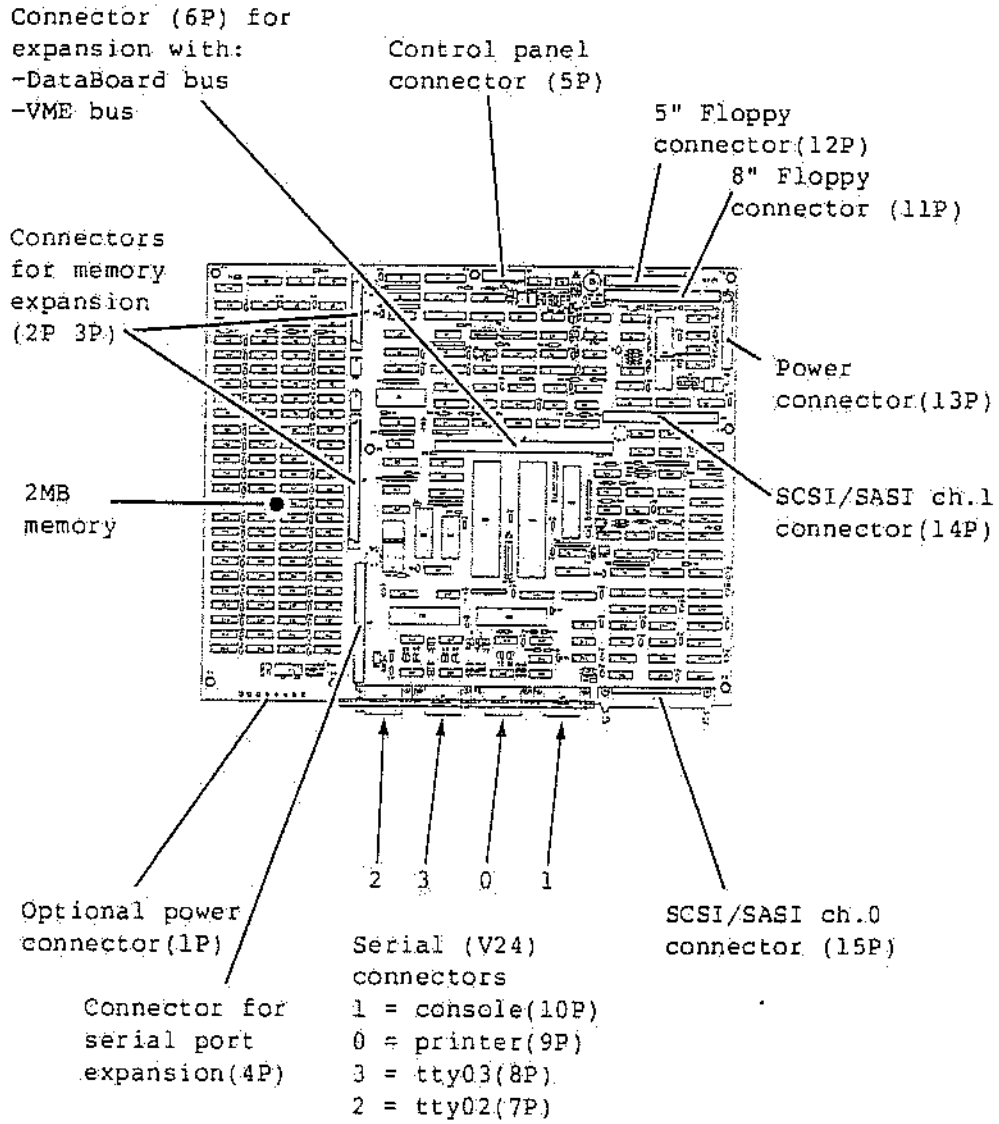
Floppy interface. One interface is used for both the 8 inches and the 5 1/4 inches floppy drives.

Through the expansion connector in the center of the board, different types of expansion systems can be connected, mechanically mounted on the chassis. Any expansion boards on an optional expansion backplane shall be inserted from the back of the system, above the serial channels (Example: DataBoard I/O-boards).



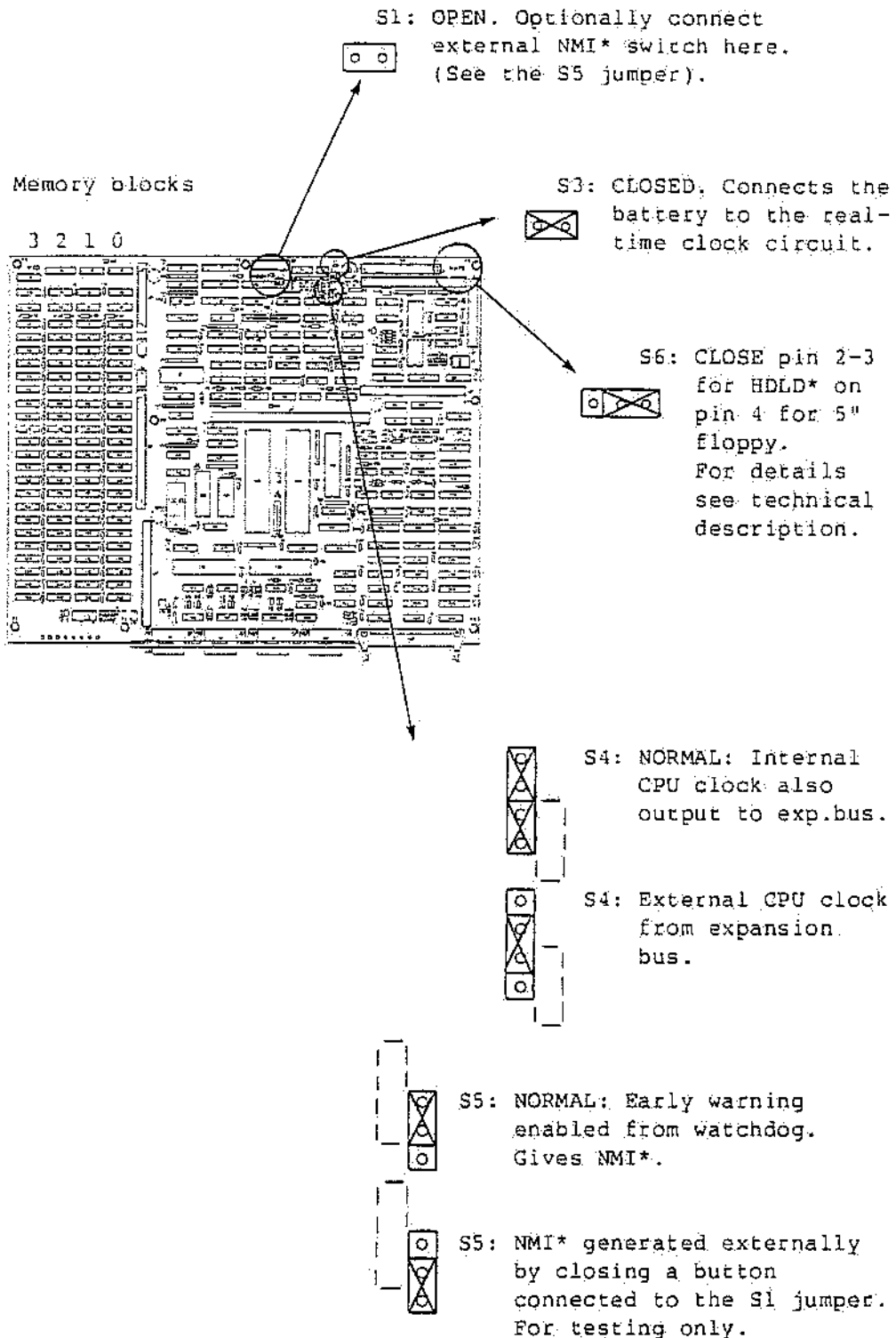


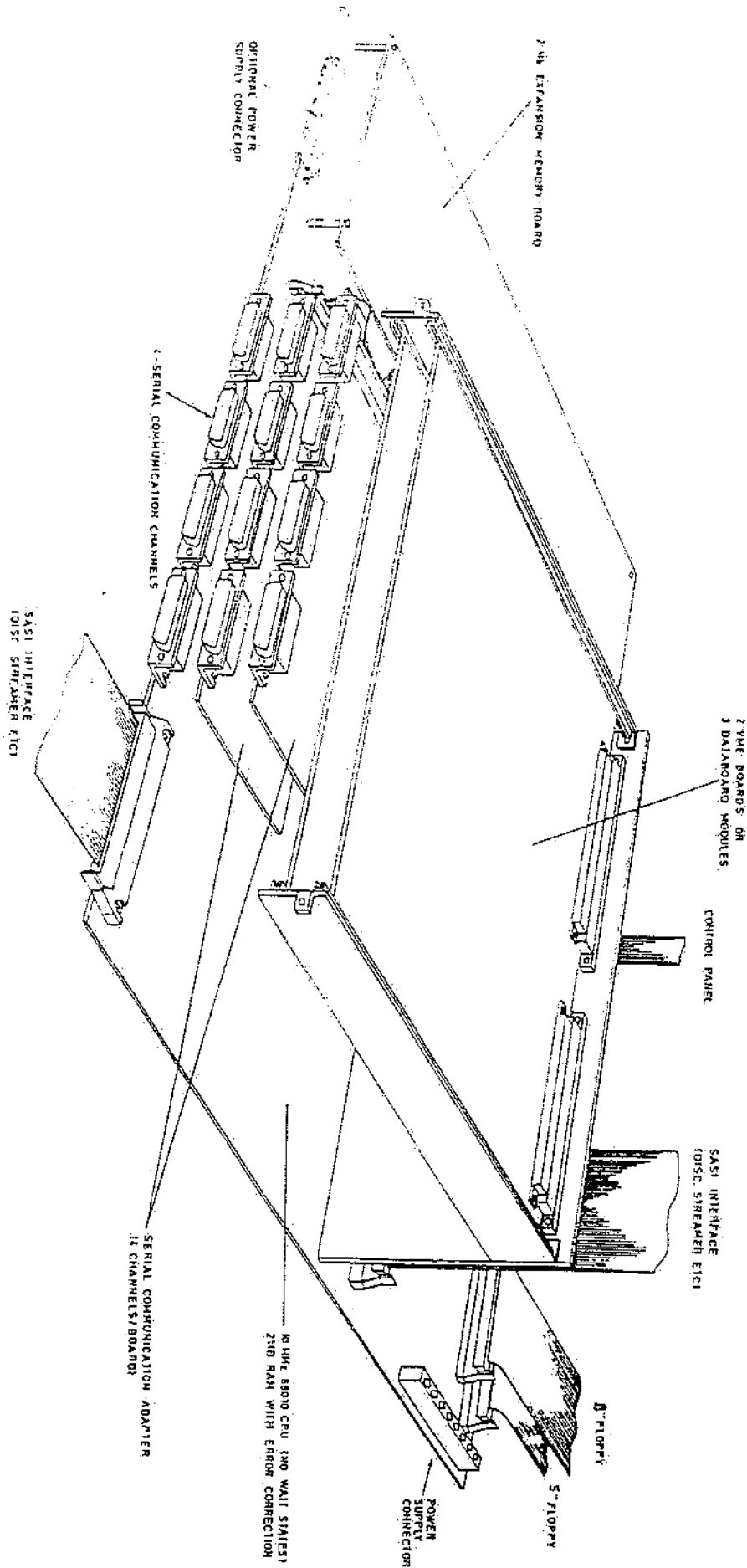
Connectors on the board



Jumpers and memory bank layout

The jumpers are shown below with their normal setting. For multipin jumpers, a dot indicates pin 1.





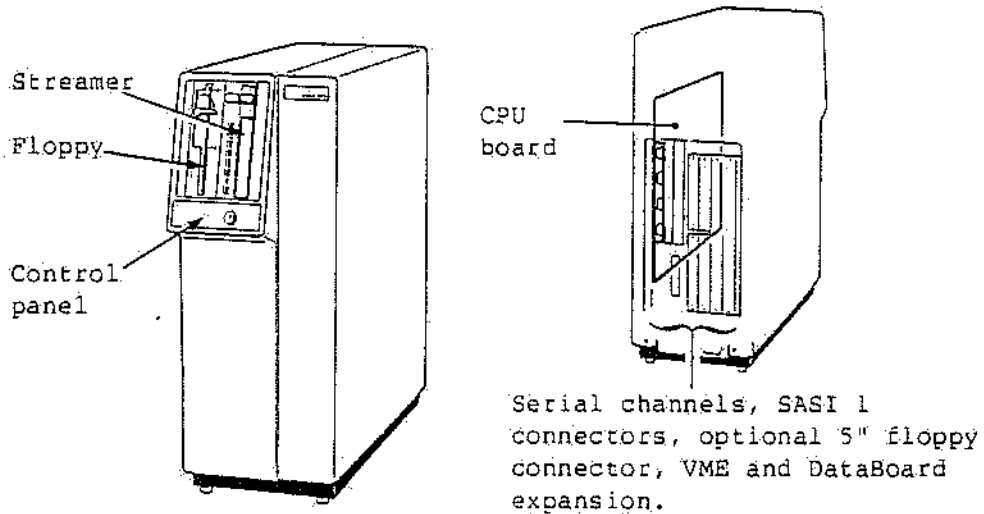
## 4.2 Installation

### Installing the 1110-1x mechanically.

#### Business version (DS90-10)

In the business version the computer board is mounted in a standing chassis. The 5180-00/5181-00 expansion backplane is standard with DataBoard and VME expansion.

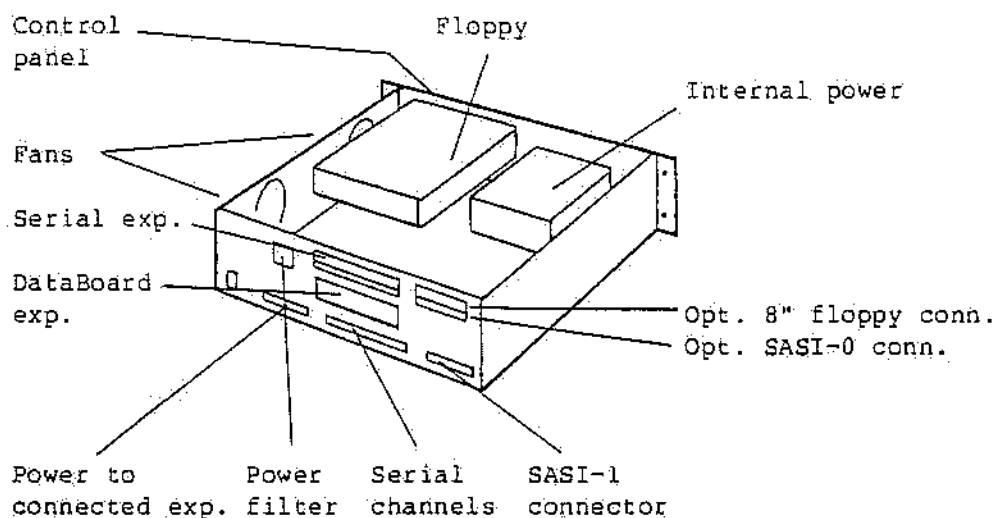
First mount any expansion memory directly on the board. Other expansions are mechanically mounted directly on the chassis. The computer board (1110-10) is mounted vertically with 8 screws.



#### Industry version (DS90-11)

In the industry version the computer board is mounted in a box for a 19 inches rack system. The 5173-00 DataBoard expansion backplane is standard.

First mount any memory expansion directly on the board. Other expansions are mechanically mounted directly on the chassis. The computer board (1110-11) is mounted on the bottom of the box with 8 screws.



Power connections.

Connect the power and the power control signals to either of the two available connectors, depending on the mechanical requirements. When an external power supply is used, the 1P connector on the back is used and the 13P connector is used with an internal supply.

The power control signals are:

- POWER\* Active low power-on signal from the computer board. Normally activated by the control panel switch. Alternatively a software command can pull this output low, through an open-collector, TTL-level non-isolated circuit.
- ACLOW\* Power-low input signal from external power fail detection circuitry. Active low means power low and will interrupt the computer. Non-isolated TTL-level input.  
NOTE! Must be high (+5V) from external source, during normal operation.

General comments on power connection to a computer system

- 1 - Always use transient filter circuitry on the mains connector.
- 2 - The following rules apply for equipments, connected directly without galvanic isolation between them:

Always connect all equipments to the same 220V AC phase. If the distance between different equipments are large and isolated communication is not used, a separate power cable should be provided to assure this requirement.

The chassis earth in all equipments should be interconnected and should only be connected to mains earth on one point in the system.

If possible, the 0V logic level should only be connected to the chassis earth on one point in the system. This point should be close to the computer power supply.

- 3 - Calculate the maximum current in the +5V and +12V/-12V cables and the total current in the 0V cables to assure that the cables selected supports this current without voltage drops.

Installing peripherals, expansions and options.

Normally turn the power off before connecting any equipments. Only the serial channels can be connected / disconnected on-line, with care.

- Control panel.
- Minifloppy (5 1/4 inches) drives.
- Standard floppy (8 inches) drives.
- Winchester drives and tape streamers.
- Terminals, printers, modems and other serial equipments.
- Floating point option.
- Boot-PROM.
- Battery.
- Memory expansion.
- Serial port expansion.
- Expansion backplanes.

Control panel

The control panel is connected through a ribbon cable to the board. Max cable length is 1 m.

Mini-floppy (5 1/4 inches) drives

Up to 2 minifloppy drives can be connected in parallel to the minifloppy connector (12P) through a ribbon cable. Max cable length is 2 m. The drive identity shall be set by jumpers on the drive controller to different values, normally 0 and 1. The S6 jumper is normally set to give the head load signal (HDL\*) on pin 4 in the minifloppy connector. For details, see the technical description.

Standard floppy (8 inches) drives

Up to 2 standard floppy drives can be connected in the same way as described for the mini-floppy above but to the 8 inches floppy connector (11P).

Winchester disc drives and tape streamers drives

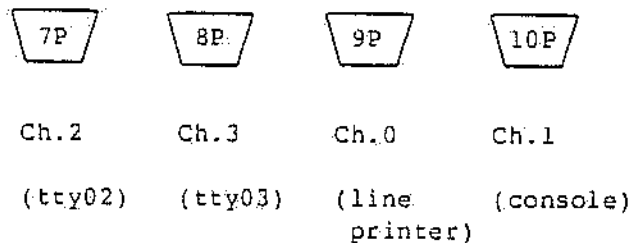
These are connected to the SASI connectors (14P and 15P). For highest performance one drive (with controller) should be connected to each SASI channel. The drive identities are set to 0 on both drives in this case. The following is standard:

SASI 0: Connector 15P: Winchester drive with controller.  
SASI 1: Connector 14P: Tape streamer or second winchester with controller.

It is possible to connect up to 8 units on each connector, with a different drive identity on each.

Terminals, printers, modems and other serial equipments.

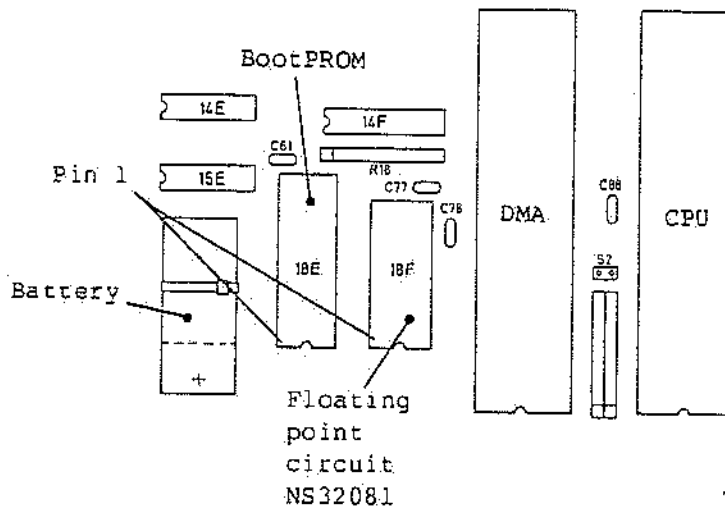
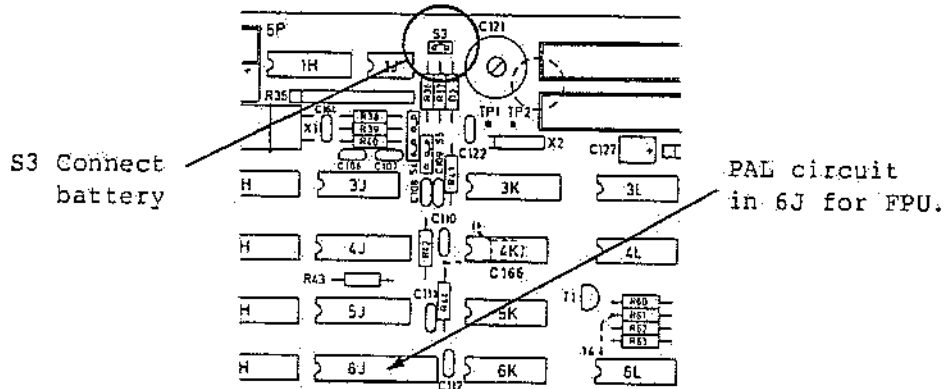
These are connected at the serial ports with standard connectors. The cables shall have DA15S connectors. See the connector section for the pinning. For system compatibility, the channels are used as:



Floating point option kit (7140-00).

The 7140-00 kit consists of an NS32081 FPP and an 8039 PAL circuit. The circuit NS32081 from National Semiconductor is installed in the 24-pin socket (18F) to the left of the DMA and CPU circuits. The PAL is inserted in the socket in position 6J. Note the orientation of the circuits according to the figure below.

Standard DNIX software will handle the floating point unit.

Boot-PROM

A standard boot-PROM is always delivered mounted in the system. The boot-PROM is of the type EPROM 27128 (16 kbytes) and is mounted in the 28-pin socket (18E) near the battery. See the figure above.

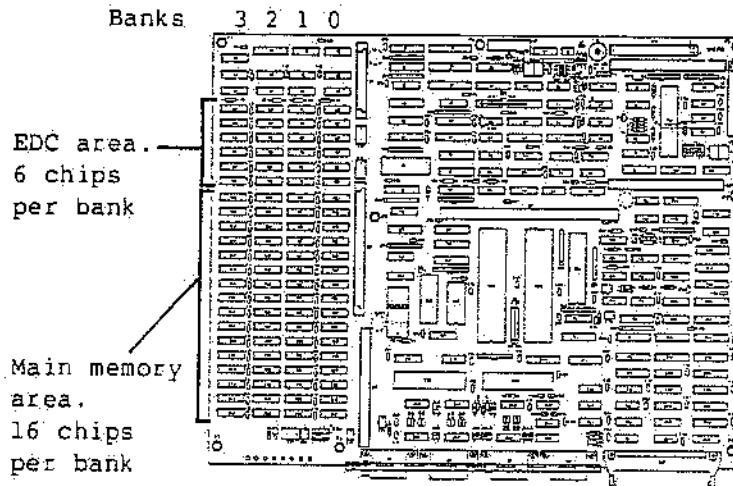
Battery

The battery is always delivered mounted in the system. The battery type is GE 013 or equivalent and the position and polarity is shown in the figure above. Be sure to open the S3 jumper while the battery is soldered and close it afterwards to connect the battery.



Memory expansion.

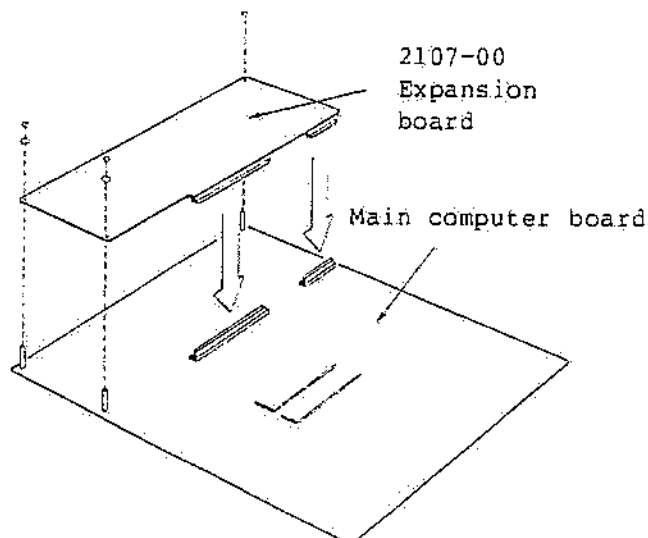
The onboard memory is 2 Mbytes as standard, but can be equipped in steps of 512 Kbytes banks, by inserting 256-bit RAM circuits. If the error detection and correction logic (EDC) is used, 6 extra chips is used for each bank, in addition to the 16 standard chips. The RAM circuits shall be 120 ns dynamic RAM. Example: HM50256P-12 or equivalent.



The same physical positions for the banks are used on the 2107-00 expansion memory board, with banks 4..7.

Bank 0	Range	0.0 Mb .. 0.5 Mb	Onboard the computer board.
1		0.5 Mb .. 1.0 Mb	
2		1.0 Mb .. 1.5 Mb	
3		1.5 Mb .. 2.0 Mb	
Bank 4		2.0 Mb .. 2.5 Mb	On the 2107-00 expansion board.
5		2.5 Mb .. 3.0 Mb	
6		3.0 Mb .. 3.5 Mb	
7		3.5 Mb .. 4.0 Mb	

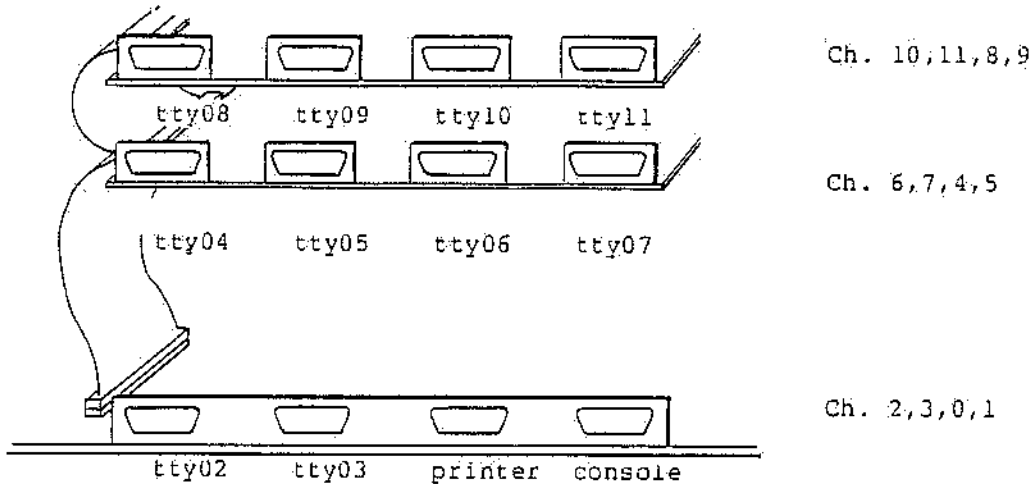
The 2107-00 memory expansion is screw mounted on top of the on-board memory on distances.



Serial port expansion.

One or two serial expansion boards (5172-00) can be mounted on the chassis back plate and connected through a ribbon cable to the 4P connector on the computer board. The expansion boards are mounted above the on-board serial channels, but in the present boxes, above any expansion slots for DataBoard interfaces.

On the expansion chassis, the tty device numbers (tty04, tty05, ... tty07 etc.) are in order, from left to right, in spite of the internal channel number order.

Expansion backplanes.

Expansion back planes are inserted in the expansion connector (6P) in the center of the computer board, with any expansion slots turned to the back above the serial channels.

Mechanically the backplane with its guides for the expansion slots are mounted on the chassis.

## 5. TECHNICAL DESCRIPTION

### 5.1 Processor, Clocks, Floating point option

#### Processor and system clocks

The Motorola MC68010 CPU is a 32-bit processor with 16-bit data bus and 24-bit address bus. A 4-channel DMA (HD68450) is used and an optional hardware floating point processor, described in separate sections.

The CPU clock is 10 MHz and the design allows normal memory access without wait-states, using 120 ns memory chips.

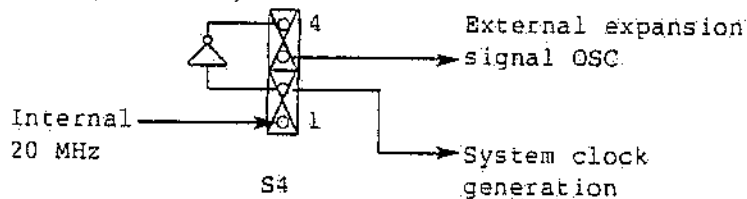
The CPU-clock is modulated to introduce a delay when:

- A byte-write is done and when
- The EDC circuit corrects a correctable memory error.

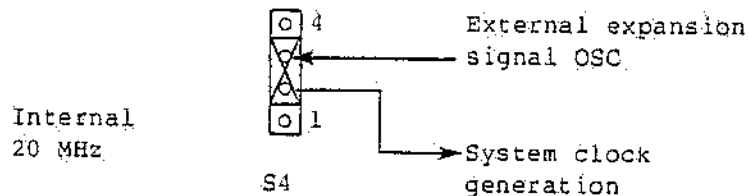
The 5 MHz peripheral clock is used for the SCC and CIO circuits.

A 20 MHz oscillator generates the CPU-clock, the peripheral clock, as well as memory refresh and other system timing signal. This frequency can be output to the expansion backplane. Alternatively, an external oscillator can be used, through the S4 jumper.

Internal clock (standard):



External clock:



A separate 16 MHz clock is used for the floppy interface and is also output on the expansion connector for VME bus applications.

A separated 32768 Hz crystal is used for the time-of-day clock.

#### Optional Floating Point Processor.

The NS32081 floating point processor from National Semiconductor is used as a slave processor. The CPU stores data and commands to the NS32081 registers for execution. The standard D-NIX system software contains fully transparent support for the FPU. For programming see the NS32081 datasheet (ref 3). The FPU is accessed in the address range:

820100 - 821FF Hex

## 5.2 MMU, EDC, system control

### Memory management unit (MMU)

The MMU provides address translation at memory access and access protection at both memory and I/O access. Flags are provided for virtual memory support. No distinction is made between CPU and DMA accesses.

Up to 4 Mbytes logical virtual memory per process is mapped through 2048 pages registers to the 4 Mbytes physical memory. Each page is 2 Kbytes and has two levels of protection attributes and flags. Bus errors are generated by hardware at protection violation. The flags are used when swapping pages in and out on external discs. See the following figures.

- Page attributes:
- Access protected page.
  - Write protected page.
  - User I/O permit (Only used in I/O-space)
- Page flags:
- Page has been accessed.
  - Page has been modified.

Write protected pages can be shared between different processes for efficient use of the physical memory.

A separate user PERMIT\* signal can be set for each process to allow a process in user mode to access certain system resources outside of the I/O-space on connected expansion systems. The expansion system logic shall ignore any access without the PERMIT\* signal, which will generate a bus timeout error to be trapped by the system.

Direct addressable map registers in hardware for up to 16 different processes speed up context switching. Only when more than 16 processes are active, some of the map registers need to be changed during context switch.

### MMU principle

A two-stage mapping principle is used where a 4-bit context register indicates the process. Each process can have up to 128 logical memory segments, each covering a logical area of max 32 kb in up to 16 physically discontinuous memory pages per segment.

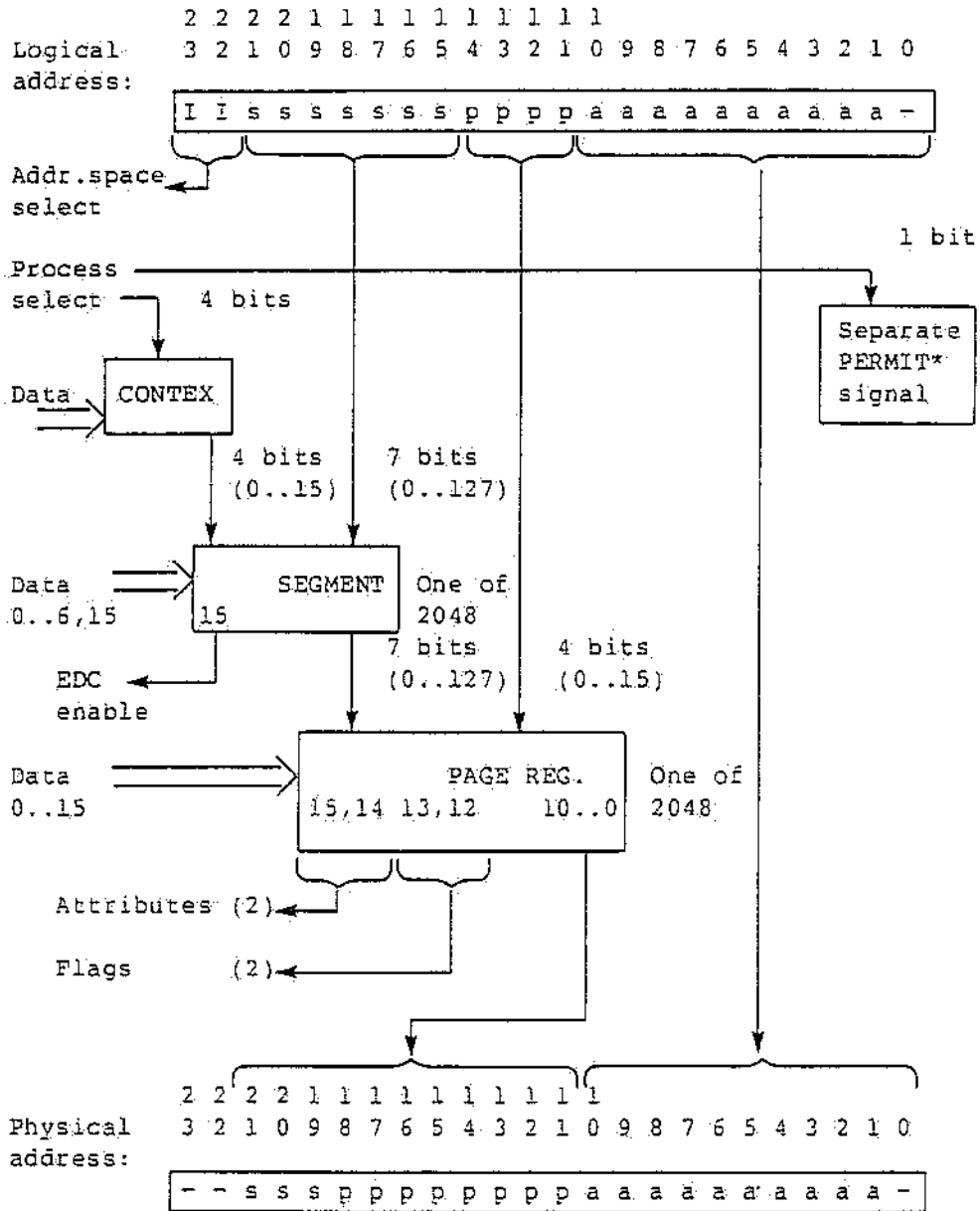
The mapping circuits can be disabled by software for direct access to certain parts of the physical memory. This is used at power-up to allow the system to test the memory and detect the actual physical memory size.

Note! At least one group of 16 pages always has to be "Nonexisting" to allow the system program to direct non-allocated logical segments to a "non-existing" area. Any access to this area will then by hardware generate a bus error to be trapped by the system program.

Note! The hardware automatically selects the process 0 registers when executing in system mode.

The MMU registers are only accessible in system mode and are located in the system control space.

Memory map principle:



Attributes in bits 15,14:

- 0 : Write protected page.
- 1 : Read/write memory.
- 2 : Non-existing (Not allocated page).
- 3 : User I/O-permit (Used in I/O space).

The flags are:

- Bit 13 : Page has been modified by write.
- Bit 12 : Page has been accessed.

General addr.spaces:

- 0.. 4 MB A23:A22 = 0:0 Memory access
- 4.. 8 MB A23:A22 = 0:1 Expansion area
- 8..12 MB A23:A22 = 1:0 System control
- 12..16 MB A23:A22 = 1:1 I/O-space.

Accessing the MMU registers.

As each process has its own segment and page registers, the context register must always be set up to the process number (0..15) before accessing the segment or page registers of this process.

CONTEX: Select one of 16 processes by the CIO port B, bits 0..3.

Access address: 800103 Hex (Byte mode)

Data	Function
D0..D3	Process 0..15.
D4	(1) PERMIT* User mode access permit signal to expansion connector.
D5	(1) Enable EDC interrupt on correctable memory errors. Also disables MAN reading. (0) Disable EDC interrupt and enable reading the MAN input, using CIO port bit 4.
D6,D7	MMU-mode. Shall be 0 (zero) at MMU access.

SEGMENT: First select the process with the context register. Then the segments of this process are accessed. Within a process, the logical address bit A21..A15 selects one segment.

Access address: Segment = 0..127.  
800000 + Segment\*8000 Hex (Word mode)

Data	Function
D0..D6	Segment pointer 0..127. Selects a group of 16 page register.
D7..D14	Ignored
D15	(0) EDC checking enable in this segment. (1) EDC checking disabled.

PAGE: First select the process with the context register. Then the pages of this process are accessed. Within a process, the segment select (A21..A15) and the page select (A14..A11) defines the physical address.

Access address: Segment = 0..127, Page = 0..15.  
800000 + 80 + Segment\*8000 + Page\*800 Hex (Word mode)

Data	Function
D0..D10	Physical address bits A21..All of the page.
D11	Unused
D12	Flag: Set 1 when the page is ACCESSED.
D13	Flag: Set 1 when the page is MODIFIED.
D15,D14	Attributes:
0 0	Write protected
0 1	Accessible read/write RAM
1 0	Non-existing page
1 1	User I/O-space permit (Only used in I/O-space)



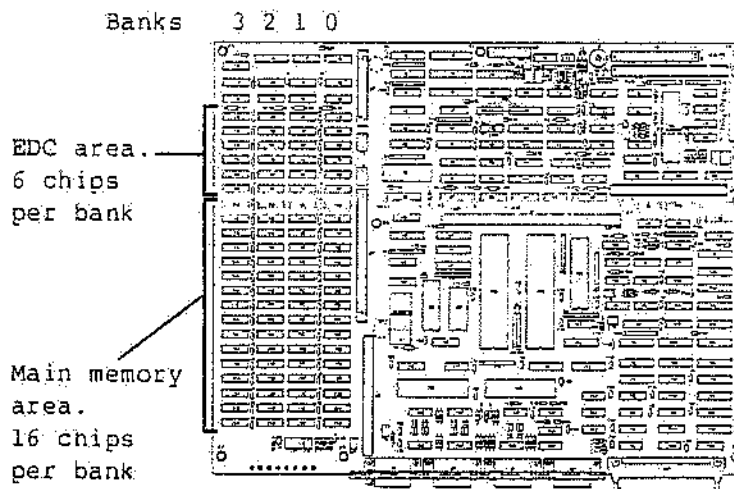
Memory matrix

The main board is equipped with 2.0 Mbytes dynamic RAM memory in 88 chips with 256 bits each.

The onboard logic for error detection and correction (EDC) requires 6 extra bits per 16-bit word.

The memory is divided into 4 memory banks, each 512 Kbytes. Within each bank, each chip provides one bit per data word.

Bank 0:	Address range	0 .. 512 kbytes.	
	Data bits	0 1 ... 15	EDC bits 0 ... 6
	Card position	25D 24D ... 10D	9D .. 4D
Bank 1:	Address range	512 kb .. 1.0 Mbytes.	
	Data bits	0 1 ... 15	EDC bits 0 ... 6
	Card position	25C 24C ... 10C	9C .. 4C
Bank 2:	Address range	1.0 Mbytes .. 1.5 Mbytes.	
	Data bits	0 1 ... 15	EDC bits 0 ... 6
	Card position	25B 24B ... 10B	9B .. 4B
Bank 3:	Address range	1.5 Mbytes .. 2. Mbytes.	
	Data bits	0 1 ... 15	EDC bits 0 ... 6
	Card position	25A 24A ... 10A	9A .. 4A





Error Detection and Correction Logic

At each memory write, the EDC logic automatically calculates and writes the 6 EDC checkbits for each word.

At each memory read, these bits are compared with the data bits. 1-bit and 2-bit errors can be detected, in which case the error address and the error type are stored in the Error Detection Status Register.

The EDC checking can be enabled/disabled separately for each logical memory segment, using bit 15 in the segment registers. Bit 15 = 0 enables EDC.

1-bit errors are automatically corrected, but an interrupt is generated to the CPU, if enabled, to allow the system program to read the Error Detection Status Register. Interrupt is enabled/disabled by bit 5 in the CIO-port B.

2-bit errors are fatal and can not be corrected. A bus error is generated. Bus errors during DMA access are trapped by the DMA, which only aborts any ongoing transfer.

As an option, it is possible to replace the EDC-check with parity check logic, requiring only 1 extra check bit per data word.

Error Detection Status Register

This 16-bit register contains information describing the type of error and the memory location of the last error detected by the EDC logic.

The contents of the EDS register is undefined if no error has occurred or when the EDC logic is disabled (or not included in the system),

The access address to the EDC register is: 810100 Hex.

Note! The watchdog counter is reset by reading the EDS register.

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

D S c c c c c c 0 0 B B B A A A

D = 1 Uncorrectable error (2-bit).

S = 1 Correctable error(1-bit). Also set at 2-bit errors.

cccccc Syndrome code (C5..C0), indicating the error type. See the EDC logic documentation (ref 8) for details.

BBBAAA Physical address bits A21..A16 of the error location. BBB is the memory bank (512 kb).

System control

The system control block provides all system control functions like accessing the MMU tables, context switching, interrupt control, DMA setup, watchdog support, support for system diagnostics and accessing the optional floating point processor. The system control address space is accessible in system mode only (area 8.. 12 MB).

General system control is performed through a CIO circuit (Z8536A).

The three CIO counters (1,2 and 3) are available for system timing. As standard, counter/timer 3 is used for system interval timing. Note however that the serial channels (SCC) have a higher interrupt priority than the CIO.

The CIO port A is used to detect interrupt signals from the SASI and floppy interfaces as well as from the DataBoard extensions. 4 DataBoard interrupt levels are supported. All are at the system interrupt level 3, as the CIO generates interrupts to the CPU on this level.

The CIO port C is used to access the onboard real-time clock and the NVRAM. Both are accessed serially, with a software generated transfer clock on one bit of the CIO-port.

For details on the CIO ports A and C, see sections about interrupts, NVRAM, Real-time clock, DataBoard expansion as well as the CIO manual (ref 5).

The CIO access addresses are:

CIO Port C data:	800101 Hex
CIO Port B data:	800103 Hex
CIO Port A data:	800105 Hex
CIO Control:	800107 Hex

The CIO port B is used for general system control.

Access address: 800103 Hex for Port B data.  
800107 Hex for general CIO control.

7 6 5 4 3 2 1 0

Port B m m E P c c c c

- Bit 0..3 Context register for process selection (Context switch).  
(cccc) These bits are programmed as inverted outputs. Note that context register 0 is always forced by hardware, independent of the CIO, when the processor works in system mode.
- Bit 4 - PERMIT\*. This is an optional extra context bit, (P) indicating if a process in user mode shall be able to access certain system resources outside of the normal I/O-space.  
Bit 4 high(1) => PERMIT\*
- The PERMIT\* signal is output on the expansion connector and logic on the expansion system shall detect access violation. In system mode, this signal is always output.
- MAN input. At power up, the CIO bit 4 is set up for input and will read the status of the MAN switch on the control keyboard (manual start-up mode). The MAN input signal is disabled when CIO-B bit 5 is set to 1.  
MAN is read as bit 4 = 1.
- Bit 5 High(1): Enables interrupts from the EDC logic (E) and disables the MAN input signal to CIO B:bit 4.  
Low(0): Disables EDC interrupts and enabled reading the MAN signal on CIO B:bit 4.
- Bit 6..7 These bits select one of 4 possible mapping (mm) modes. See the section about system boot for details.  
Bit 7 high(1) will turn on the ERR LED on the control panel and enable the bootPROM.

Bit 7 Bit 6

- |   |   |   |
|---|---|---|
| 1 | 1 | BootPROM enable, MMU disable. (Start-up).   |
| 1 | 0 | BootPROM enable, MMU enable.  |
| 0 | 1 | No bootPROM, MMU enable, Software generated power-off output signal, unless the control panel switch (POWER ON*) still is closed. |
| 0 | 0 | No bootPROM, MMU enable. (Normal execution).  |

### 5.3 Boot-PROM and start up, Interrupt system, Bus errors, Watchdog

#### Boot-PROM and Power-up sequence.

The system is restarted about 1 second after power-on or after a reset signal from the control panel switch or the watchdog circuits.

The Boot-PROM is one 27128 EPROM (16 Kbytes) with a start-up program, which at power-on automatically is mapped in from address 0 and up. All read accesses below 64K, during this phase, will access the boot-PROM.

The following sequence must be followed by the boot program at power up. Compare the table for the CIO port B on the last page.

- 1 - Power-on will enable the bootPROM and disable the MMU circuits, allowing direct access to the physical memory (Transparent mode).
  - .. Read at address <64K accesses the boot-PROM.
  - .. 7 pages (each 2 Kbytes size) in the physical memory are accessed directly for memory test. 0.5Mb, 1 Mb, 1.5 Mb, 2 Mb, 2.5 Mb, 3 Mb, 3.5 Mb.
  - .. No access attributes or flags in the MMU are used.
  - .. The EDC logic is disabled and the MAN switch can be read from the control panel.
- 2 - Set up the CIO ports.
- 3 - Test the memory and MMU circuits in transparent mode (MAP disabled).
- 4 - Enable MMU and set up map segments and registers to access low RAM at a high logical address (>64 Kbytes). Enable the EDC logic on the used memory segments by bit 15 in the MMU segment number.
- 5 - Copy the program from the BootPROM to RAM and compare to ensure correct copying.
- 6 - Reset the map registers to access low RAM with low addresses.
- 7 - Disable the bootPROM. Now the copy in RAM will be accesses at the same address and the program can continue to load the operating system.

Interrupt system

The interrupt system provides 7 system interrupt levels and 8 extended interrupt priority levels. Additional secondary levels can be added, using interrupt scanners on a DataBoard expansion.

Vectored interrupts are provided on the levels 2, 3, 4 and 5. Levels 1, 6 and 7 have autovectors. The M68010 CPU interrupt acknowledge cycle can be simulated for diagnostics.

The access address to the CIO port A for the extended interrupt detection is:

800102 Hex	for port A data.
800107 Hex	for general CIO control.

Below the interrupt levels are described, with the highest priority first..

IRQ7*	NMI* Non-maskable interrupt from the watchdog early warning signal or from an optional external button, as selected by the jumper S5.
IRQ6*	Power-fail warning (ACLOW*) from the power supply.
IRQ5*	Reserved. From the expansion slot.
IRQ4*	Serial communication channels. Interrupt vectors from the SCC and daisy chaining provides separate priorities with channel 0 highest.
IRQ3*	CIO system control, with the following internal priorities. Port A decodes extended interrupts. If an external DataBoard interrupt scanner is used, it shall be connected to the XIRQ5* DataBoard interrupt.
	Counter/timer 3 Normally used as system interval counter.
Port A	Bit 7 SASI 0 interface.
	Bit 6 SASI 1 interface.
	Bit 5 XIRQ5* DataBoard expansion (or scanner).
	Bit 4 XIRQ4* DataBoard expansion.
	Bit 3 XIRQ3* DataBoard expansion.
	Bit 2 XIRQ2* DataBoard expansion.
	Bit 1 XIRQ1* Graphics system expansion. This input shall be edge triggered.
	Bit 0 Floppy interface (5 <sup>1</sup> / <sub>8</sub> " )
Counter/timer 2	General counter/timer.
Port B	System control. No interrupts are used.
Counter/timer 1	General counter/timer.
Port C	NVRAM/RTC access. No interrupts used.
IRQ2*	Reserved. From the expansion slot.
IRQ1*	Correctable memory error from the EDC-logic. This interrupt can be disabled by bit 5=0 in CIO-port B. UN-correctable errors generate bus-error and not interrupt.

Bus errors, Bus timeout

The hardware generates a bus error (BERR\*) signal on the following conditions. It enables full support for the memory management with virtual memory as well as for the error detection and correction logic.

Note that bus errors caused by DMA accesses are trapped by the DMA and not the CPU. The DMA will then be aborted and the system program should detect the error by reading the appropriate register flag in the DMA.

Bus errors are generated at:

- Attempt to execute program code within the system control or I/O-spaces.
- Attempt to access system control space in user mode.
- Attempt to access an I/O-device or an I/O-device group in the I/O-space in user mode without access permission through the MMU logic. Appropriate MMU flags will be set for identification.
- Bus timeout at an attempt to access reserved space in user mode (through the expansion connector) without the PERMIT\* code (bit 4 in CIO port B).
- Attempt to access a logical memory page, defined in the MMU as non-existing. The 'accessed' flag will be set for virtual memory handling.
- Attempt to write to a write-protected logical memory page. The 'updated' flag will be set for identification.
- Bus-timeout (7.5 microseconds) at an attempt to access a non-implemented physical address.
- Uncorrectable memory error, detected by the EDC logic. The error address and type can be read in the Error Detection Status register. Correctable errors will only generate interrupt, if enabled.

Logical address space:	16 Mb	I/O-space including also DataBoard expansion
	12 Mb	
	8 Mb	System control space
	4 Mb	Reserved space for optional expansion
	0	Program/data memory

Watchdog with early warning

The watchdog counter generates a system reset unless regularly pushed by software (within 0.8 seconds interval).

The watchdog can be pushed only in system mode by READING at the address of the EDC error status register.

Access address to the watchdog (and EDC) is: 810100 Hex.

An early warning signal is generated after half the watchdog time (0.4 sec). This signal can generate a non-maskable interrupt if enabled by the jumper S5. The optional external NMI\*-switch should not be used when the early warning signal is enabled.

#### 5.4 Real-Time clock, NVRAM

##### Real-Time clock for time-of-day

The MEM E050-16 real time clock (RTC) circuit is accessed serially through the CIO-port C. It is only accessible in system mode. Note that also the NVRAM is accessed through the CIO-port C. The port C data bits 2 and 3 select either device.

A 2.4V battery (type GE 013) is used for battery backup and retains the timing at power-off during at least 30 days.

A separate 32768 KHz crystal controls the timing. A tuning capacitor is provided for adjustments (C121), which is near the 5 1/4" floppy connector.

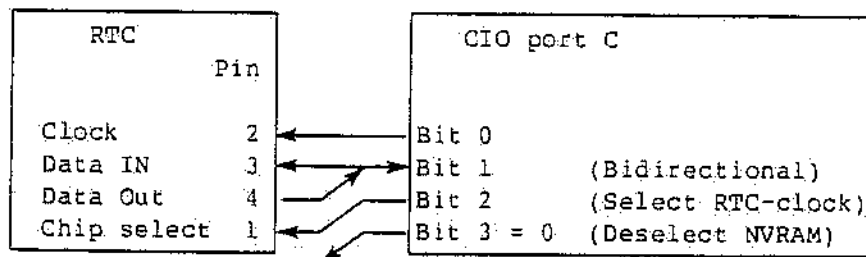
For programming details, see the manual for the MEM E050-16 circuit (ref 7). Below is a short general description.

Time data is transferred serially, using bit 0 in the CIO-port C as a transfer clock and bit 1 to transfer the data bit by bit.

The RTC-circuit contains 6 time registers, each with one byte of data. A 4-bit command sent to the RTC selects a register and read/write operation, either for single byte transfer or for transfer of all 6 registers. If all registers are transferred, they are in the order: Hour, Minutes, Date, Month, Year, Day-of-week, Seconds.

Registers	Value
0 Seconds	00 .. 59
1 Minutes	00 .. 59
2 Hours	00 .. 23
3 Date	01 .. 28/29/30/31
4 Month	01 .. 12
5 Day-of-week	01 .. 07 (01 = Monday)
6 Year	00 .. 99
(7)	Selecting register 7 gives transfer of all registers)

The access address is: 800100 Hex for port C data.  
800107 Hex for general CIO control.



Chip select: Low(0) to activate the RTC. High between commands.

Clock: Bit-transfer clock. Rising edge transfers one data bit into the RTC, falling edge transfers a bit when reading from the RTC.

Data: Bidirectional data port.

Bit 3: = low(0) to dis-select the NVRAM.

Note: Data bits 4..7 on the CIO port C is a protect mask, when writing to the port. See the CIO datasheet.



NVRAM Non-Volatile RAM for parameter storage

For non-volatile storage of 32 bytes of boot parameters, an NVRAM circuit of the type NMC9306 is used.

Data is erased/read/written as 16-bit words serially, using the CIO port C. It is only accessible in system mode. A word must be erased before writing new data. Erasing can also be done of the entire NVRAM with one command.

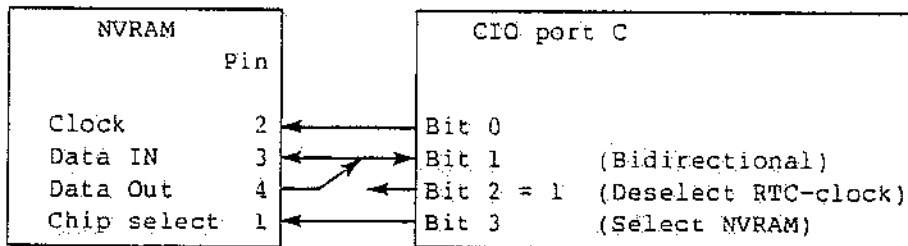
For programming details, see the manual for the NMC9306 circuit (ref. 6). Below is a short general description. Note that also the real-time clock is accessed through the CIO-port C. The port C data bits 2 and 3 select either device.

Commands and data are transferred serially, using bit 0 in the CIO-port C as a transfer clock and bit 1 to transfer the data bit by bit.

Available commands are:

READ	Read one 16-bit word
WRITE	Write one 16-bit word
ERASE	Erase one 16-bit word
ERALL	Erase the entire NVRAM
EWDS	Disable erase/write
EWEN	Enable erase/write

The access address is: 800100 Hex for port C data.  
800107 Hex for general CIO control.



Chip select: High(1) to activate NVRAM. Low between commands.

Clock: Bit-transfer clock. Rising edge transfers one data bit.

Data: Bidirectional data port.

Bit 2: = high(1) to dis-select the real time clock.

Note: Data bits 4..7 on the CIO port C is a protect mask, when writing to the port. See the CIO datasheet.

## 5.5 Serial channels, DMA, SASI, Floppy

Serial communication channels

Four (4) serial channels are available on the main board in two SCC circuits (Z8530A).

Up to 3 expansion boards (type 5172-00) can be connected, each with 4 channels, but with the present mechanical design only 2 boards can be mounted. Thus up to 12 serial channels are available. If more serial channels are required, use the DataBoard expansion possibility.

Channel 1 (SCC 0, port B) = /dev/console  
 Channel 0 (SCC 0, port A) = /dev/lp (line printer)  
 Channel 3 (SCC 1, port B) = /dev/tty03  
 Channel 2 (SCC 1, port A) = /dev/tty02

The 4 onboard channels support both synchronous and asynchronous communication, but the expansion channels (on 5172-00) can only use asynchronous communication. Instead they contain a special hardware split-speed generator.

Any serial channel (one at a time) can use DMA channel 3 for data transfer, which gives excellent support for local area networks.

Interrupt requests are on level 4 and each channel can be programmed to give separate interrupt vectors.

The peripheral clock, controlling the SCC circuits, is 5 MHz, allowing baudrate generation up to 19200 baud in asynchronous mode.

The serial channels can be access protected in user mode through the MMU attributes. Access enable in user mode can be defined for a process in the appropriate MMU register. All serial channels are affected as a group by a protection attribute.

For programming details, see the SCC manual (ref 4).

The access addresses to the serial channels are as below. Byte mode shall always be used at access.

Address: FC00nm Hex, where the Hex-digits 'nm' indicates the channel number and data/control selection.

n	0..7: SCC-chip (Each with 2 ports).
FC00n1	1 : Port B Control
FC00n3	3 : Port B Data
FC00n5	5 : Port A Control
FC00n7	7 : Port A Data

Example: console: SCC 0, Port B: Control with FC0001 Hex  
 (Ch. 1) Data with FC0003 Hex  
 tty02: SCC 1, Port A Control with FC0015 Hex  
 (Ch. 2) Data with FC0017 Hex

DMA logic

The HD 68450 DMA controller is used. Four DMA channels can work simultaneously, supporting data transfer between the memory and the following I/O-devices or for "fly-by" transfer between two I/O-devices. Alternatively any channel can be used for memory to memory transfers.

Channel	Device
0	SASI interface 0.
1	SASI interface 1.
2	Either floppy interface. or one DataBoard interface (One at a time).
3	One serial communication channel at a time.

The DMA addresses memory and I/O through the MMU logic, with full protection. DMA control access is only allowed in system mode. Memory pages used at DMA must be locked in memory.

The maximum block size used is 32 kbytes with the present software, using one MMU segment register per DMA channel.

If an uncorrectable memory error occur during a DMA memory read cycle, the channel operation will be immediately aborted. The bus error signal does in this case not reach the CPU. After DMA abort, timeout will interrupt the CPU, which can detect the abortion in a DMA register and perform suitable corrections. If a device is accessed, it will still wait for more data.

DMA channel 0 and 1, accessing the SASI interfaces, must be programmed for:

Single address  
Word operand  
Burst mode

The other channels must be programmed for:

Dual address  
Byte operand  
Cycle stealing mode

Access to the DMA-registers from the CPU is in word mode. For details, see the manual for the DMA circuit (ref 2).

The access addresses are: 830100 - 8301FF Hex, accessing 256 DMA register addresses (0..255).

SASI interfaces

Two entirely independant SASI interfaces are provided on the board, accessed with separate DMA channels and with different interrupt levels to achieve maximum performance.

The two SASI interfaces can have different user mode protections through the MMU logic. However, the direct DMA control can only be performed in system mode.

The interfaces are designed to be SASI bus masters only and up to 8 slaves devices can be connected to each interface.

Internal buffers on the SASI interfaces enable the use of burst mode in DMA transfer and direct writing of commands strings from the CPU without waiting for byte-wise transfer, minimizing the overhead of the system. The buffer area in each interface has 16 words (=32 bytes) for commands or data, directly addressable from the CPU or DMA in word mode. External transfer on the SASI bus is in byte mode. Full hardware support for DMA enables transfer block sizes up to 32 kb.

The DMA transfer speed can be up to 4 Mbytes/sec. The external transfer rate for buffered data is limited by about 100 ns delay per byte for the REQ\* / ACK\* signals and by the DMA transfer to/from the buffer, taking about 10 microseconds per 32 byte block. This design enables support for 5 Mbytes/sec winchester drives using interleave factor 1, while the DMA will occupy the system bus only 15% of the time.

The interfaces include certain test functions, by which external device signals can be simulated for automatic hardware tests.

The accesses addresses to the SASI interfaces are:

SASI 0	Buffer (0..15):	FD5000-FD501F Hex	(Word mode)
	Status reg:	FD5080 Hex	(Word mode)
	Control reg:	FD5080-FD509F Hex	(Word mode)
SASI 1	Buffer (0..15):	FD6000-FD601F Hex	(Word mode)
	Status reg:	FD6080 Hex	(Word mode)
	Control reg:	FD6080-FD609F Hex	(Word mode)

Control register:	D15	(0), High(1) simulates BSY* in. (Test only)
	D14	(0), High(1) simulates I/O* in. (Test only)
	D13	(0), High(1) simulates REQ* in. (Test only)
	D9	(1) Release RST* out signal, (1= Send RST*) RST* is also sent at system reset.
	D8	(1) GO command, (0) Release GO. NOTE! Access address = buffer pointer start value at the GO command.
D7..D0	0..128 SASI device select code. Use only values 0,1,2,4,8,16,32,64,128.	

Status register:	D15	(1) Interrupt request active.
	D14	(0) SASI BSY* input active.
	D9	SASI I/O* input 0=In, 1=Out to device.
	D8	(1) Buffer empty(at send), full(at receive).
	D7..D5	Always 0.
D4..D0	Buffer pointer 0..15.	

SASI communication principle

The 16-word buffer on a SASI interface is accessed as 16 words of memory. Note that the buffers MAY NOT be accessed by the CPU during the transfer phase, if DMA supports the transfer.

The procedure is as follows. The details on the access addresses and bit assignments are given in the programming section.

- 1- The status is checked to assure that no device is active on the SASI bus. (Command address STAT).
- 2- A command block is loaded to the buffer at a position leaving the last command byte at the end of the buffer. This enables the hardware to detect when the entire command has been sent.
- 3- The DMA channel (0 or 1, depending on which SASI interface is used) must be programmed for the desired block length (up to 32 KB) and in/out-direction, using single address and burst mode.
- 4- A GO command is given at a command address (CTRL), which in the address includes a buffer pointer (0..15) to the first byte to transfer. Data in the GO command shall contain also the device select byte for the external device to access.

Now a select sequence is performed automatically, followed by the transfer of the command and any requested data. The transfer is controlled by the REQ\* / ACK\* / BSY\* / I/O\* signal lines from the external device.

When the buffer is empty after sending a command or a 16-word block of data, or when the buffer is full after receiving a block of data, the "buffer full/empty" condition is set. This condition is used to issue a DMA request to load or unload the buffer.

The buffer pointer can at any time be read by the command STAT, together with other status information.

- 5- After the data transfer phase, the external device sends two bytes of status information. These are sampled in the first two bytes of the buffer, after which the device releases the BSY\* signals. Disconnecting BSY\* results in an interrupt to the CPU and a CTRL command shall be issued to clear the GO command bit. Clearing GO clears the interrupt request and allows reading the status bytes from the buffer. The CPU can by a STAT reading check the word count to assure that there really are two bytes in the buffer. The external device may also issue the two status bytes and disconnect at an error.

Floppy disc interface

The onboard floppy interface supports two 8 inches drives and two 5 1/4 inches drives. Only one at a time can be accessed. Required drive select numbers are:

8" Device 0 and 1  
5 1/4" Device 0 and 1

The DMA channel 2 is shared between the floppy interface and the DataBoard interface expansions.

The floppy interface can be accessed in user mode if unprotected in the MMU logic, but the DMA control requires system mode.

A WD1797 floppy controller circuit is used. Below is described special features on the interface, but refer to the WD1797 documentation (ref 9) for programming details.

In addition to the WD1797, a interface control register shall be set up, containing parameters like drive selection, motor control, data rate and others. A status register indicates if a disc has been replaced or if the disc is dual or single sided.

The access addresses are:


FDB001 Hex for WD1797 command/status register.  
FDB003 Hex for WD1797 track register.  
FDB005 Hex for WD1797 sector register.  
FDB007 Hex for WD1797 data register.  
  
FDB080 Hex for the control and status registers.


Control register:	D15, D14	Ignored.
	D13	(1) Low current.
	D12	(1) Postcompensation ON for 8" drives (LOI*). (1) Select motor speed 360 rpm on 5" drives. (0) on 5" drives gives 300 rpm.
	D11	(1) Motor on.
	D10	(1) Select 5 1/4" drive. (0)= 8" drive.
	D9	(1) Select drive number 1 (SEL1*).
	D8	(1) Select drive number 0. (SEL0*).
	D7..D6	Precompensation code (8" drives)
	D5, D4	Ignored.
	D3	(1) 250 KHz, (0) 500 KHz data rate.
	D2	(1) Head load time elapsed.
	D1	(1) Single density (FM), (0)=Double density.
	D0	(0) Reset WD1797

Status register:	D15..D8	Unspecified
	D7	(1) Diskette has been changed.
	D6..D1	Unspecified.
	D0	Dual sided diskette.

Jumper for the 5 1/4 inches floppy drive

For the 5 1/4 inches floppy connector, the S6 jumper shall be set for the correct configuration. The HDLD\* output signal is normally output on the connector pin 4.

S6  HDLD\* out on 5" connector pin 4 (Standard).

S6  No HDLD\* signal output on 5" connector.

Floppy drive types

Different types of floppy drives and diskette types can be accessed, using different parameters. Software is available which can detect the format of a diskette by varying the parameters until it is possible to read the diskette. Generally single density 5 1/4" diskettes (160 KB and 80 KB) are not supported.

The abbreviations are: DS/SS Double/Single side  
DD/SD Double/Single density  
DT/ST Double/Single track (80/40)

8"	DS DD SS SD Standard data rate:	1 Mbytes (Standard) 256 Kbytes (old IBM 3270) 500 KHz
5 1/4"	DS DD DT (80 tracks) DS DD ST (40 tracks)  Normal data rate: Motor speed:	730 Kbytes (Standard) 320 KB On DT-drives single track double density diskettes can only be read, not written. 250 KHz (512 bytes/sector and 9 sectors per track). 300 rpm
5 1/4"	DS DD DT Data rate: Motor speed:	IBM-PC/AT format with 1.2 Mbytes/diskette, which uses higher data rate and a special motor speed selected by signals to the drive. 1.2 Mbytes unformatted 500 KHz (512 bytes/sector and 15 sectors per track). 360 rpm

## 5.6 DataBoard, General expansion

### DataBoard expansion support

The onboard logic includes support for efficient handling of DataBoard expansion systems.

Clock signals are provided to allow logic on the expansion backplane to issue an automatic sequence CS\* strobe to select one DataBoard I/O-card for each data byte transferred.

Any interface card is separately protected or accessible in user mode through the MMU logic.

Four (4) direct DataBoard interrupt levels are supported, through the CIO-port A with the direct interrupt level IRQ3\*. On the expansion backplanes, support signals are generated to handle an external interrupt scanner, to provide individual detection of interrupts from up to 32 DataBoard interfaces. The 4202 and 4203 boards are used for external interrupt scanning.

The DMA channel 2 is shared between the floppy interface and any DataBoard expansion. One DataBoard interface or one floppy drive at a time can use DMA.

### Card presence detection (CSB)

I/O-card detection logic on the expansion backplane returns information (CSB) regarding the presence of selected I/O-cards, including the interrupt levels, both the direct level and any external expansion. To enable this, each DataBoard I/O-slot has separately wired CSB\* and INT\* wires. Note that only I/O-cards, generating a CSB\* signal can be used with interrupt.

### Addressing commands

A DataBoard interface is accessed in the system I/O-space, with the DataBoard card select code and I/O-strobe number in the address. The data bits (8-bits) for the transfer is on the low data bus internally (D0..D7). One address bit (A6) indicates a special I/O cycle, used to access the card detection logic (CSB) or to generate special strobes (EXP\*) for an external interrupt scanner. For more details, see the programming section and also the datasheet for the expansion backplane used (example: 5173-00).



Access addresses for DataBoard expansion

The access address to a port on the DataBoard expansion is in the range FE0001 - FFFF7F Hex. Address one DataBoard interface with the address below. Byte mode shall be used.

$FE0001 + (CS^* \text{ AND } 3F) * 800 + (CS^* \text{ AND } C0) + (\text{Strobe}) * 4 \text{ Hex}$
--

CS\* Bits 0..5 select one I/O-board (0..63).

Bit 6 is set (1) to generate the special I/O cycle for CSB detection and communication with the optional interrupt scanner.

Bit 7 is used by some DataBoard interfaces to selecting a secondary channel.

Strobe With CS\* bit 6 = 0, a standard DataBoard strobe:

Strobe	Read	Write
0	INP*	OUT*
1	STAT*	
2	OPS*	C1*
3		C2*
4		C3*
5		C4*

Special With CS\* bit 6 =1, a special I/O-cycle is generated. The access address 4 (Strobe bit 2) defines the type of action:

Strobe <4 Read the CSB\* card presence bits.

D7 Undefined.

D6 Undefined.

D5 (0) XCSB5\* from selected interface.

D4 (0) XCSB4\* from selected interface.

D3 (0) XCSB3\* from selected interface.

D2 (0) XCSB2\* from selected interface.

D1 Undefined

D0 Undefined

Strobe >=4 Input/output with the EXP\* strobe from/to the optional interrupt scanner.

General expansion support

External bus adapters can be connected to the expansion connector 6P.

The connector provides all general system signals from the CPU and DMA and in addition special support for access protection and DataBoard expansion control.

Examples of expansions are:

- Expansion for using DataBoard interfaces
- Expansion for using VME bus modules

Special support is available for DataBoard expansion as described earlier with 4 interrupt levels decoded. The DataBoard expansions are addresses in the normal I/O-space and protected by the MMU.

A PERMIT\* signal is available, automatically asserted in system mode but only with MMU permission (CIO-B bit 4 = 1), in user mode. External systems may not respond to bus cycles with PERMIT\* in-active.

A logical memory address area 4 .. 8 Mb is reserved for accesses in the general expansion area and two interrupt levels are reserved.

400000-7FFFFFF Hex	Reserved for expansion
IRQ5*	Interrupt level for expansion
IRQ2*	Interrupt level for expansion
PERMIT*	Special user mode permit signal

For DataBoard, see previous section.

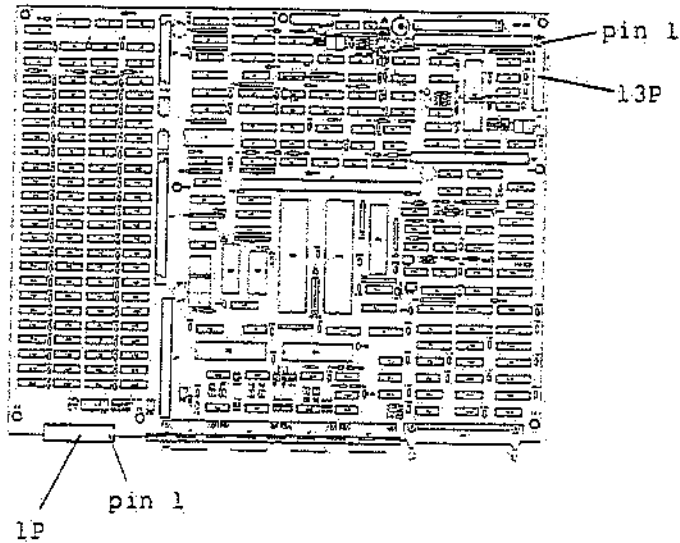
## 6. REFERENCES

1. CPU Motorola Semiconductor MC68010 Microprocessor manual.
2. DMA Hitachi HD68450 DMA
3. FPU (option) National Semiconductor NS32081 floating point processor.
4. SCC Zilog Z8530A SCC serial communication controller.
5. CIO Zilog Z8536A CIO counter/timer and parallel I/O-unit.
6. NVRAM National semiconductor NMC 9306 256-bit EEPROM datasheet.
7. RTC Microelectronic Marin MEM E050-16 1-bit real time clock timer.
8. EDC Specification of LS630 error detection and correction controller.
9. Floppy controller Datasheet for WD1797 floppy controller circuit.
10. Memory expansion Diab 2107-00 2 Mbytes memory expansion module datasheet.
11. Control panel Diab 5175-00 Control panel datasheet.
12. DataBoard expansion Diab 5173-00 expansion backplane.  
3 DataBoard I/O-slots.  
1 General expansion slot.
13. General expansion Diab 5180-00/5181-00 expansion backplane.  
4 DataBoard I/O-slots.  
2 VME board slots for single eurosize boards.  
1 Special expansion port.
14. DataBoard interrupt scanner Diab 4202-00 and 4203-00 DataBoard expansion boards.

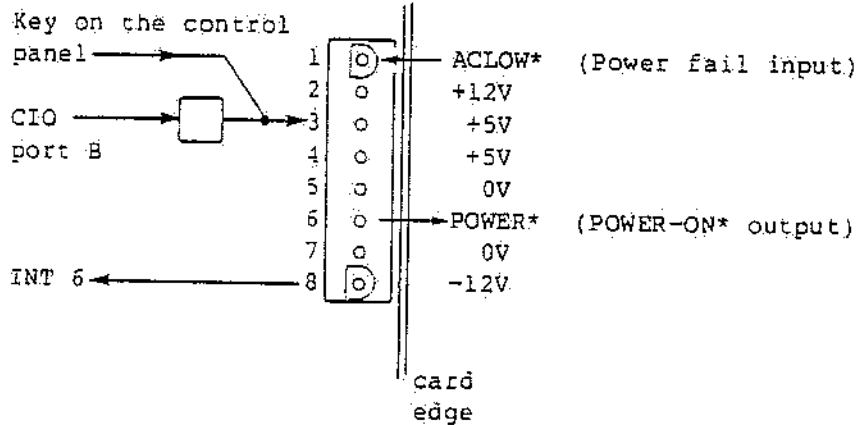
7. CONNECTORS

Power connectors 13P and 1P

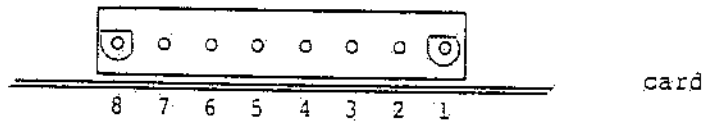
Positions  
on board:



Pinning: 13P Standing on the board (Female)



1P (Male)



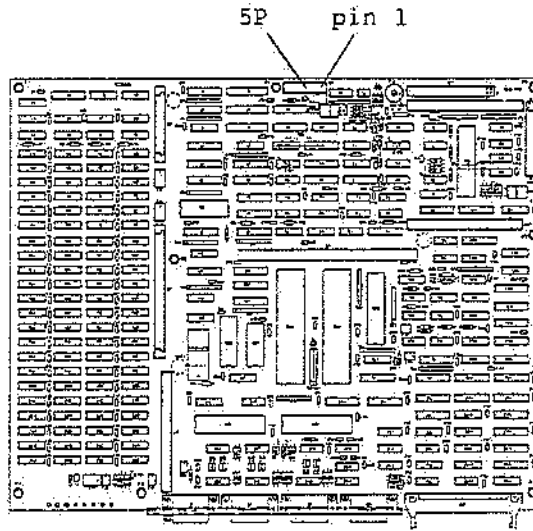
Notes: An AMP connector is used.

ACLOW\* The input signal ACLOW\* shall be connected to +5V logic level externally. A low signal on ACLOW\* generates an interrupt for power fail detection.

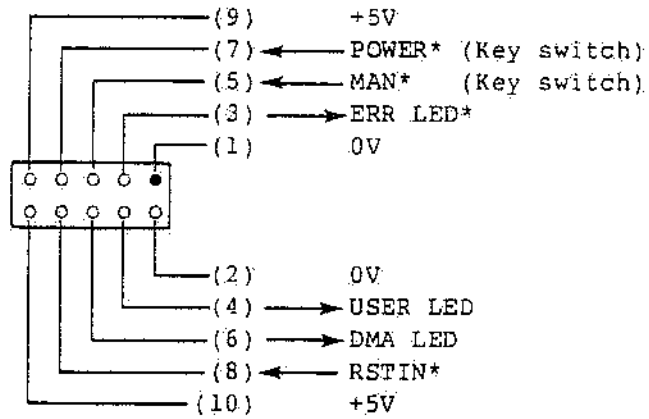
POWER\* The output signal POWER\* shall control power ON/OFF and can be generated by software (open collector output) or directly by closing a control panel switch.

Control panel connector (5P)

Position  
on board:



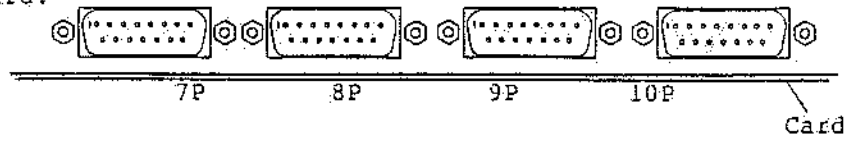
Pinning:



Notes: The connector is a 10-pin ribbon cable connector.

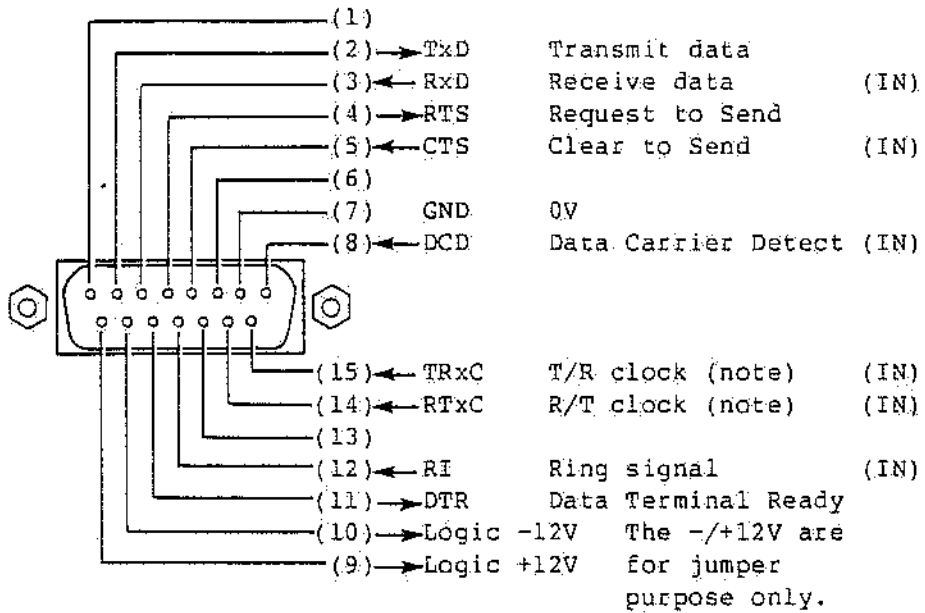
Serial V24 connectors (7P, 8P, 9P, 10P)

Position  
on board:



SCC1/A	SCC1/B	SCC0/A	SCC0/B
(CH.2)	(CH.3)	(CH.0)	(CH.1)
(tty02)	(tty03)	(Printer)	(Console)

Pinning:



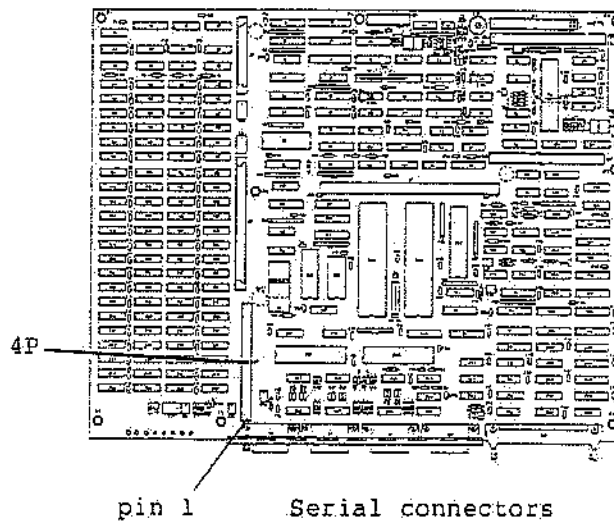
Notes: The RxD input has a 27 kohm pulldown resistor for higher noise immunity.

The connectors are DA15P connectors.

The serial connectors on the expansion boards (5172-00) does not include the clock signals input (TRxC, RTxC).

Connector for serial channel expansion board (4P)

Position  
on board:



Pinning:

IE2	←	50	○ ○	49	→	IE0
IE1	←	48	○ ○	47	→	CE2*
CE3*	←	46	○ ○	45	→	CE4*
CE5*	←	44	○ ○	43	→	CE6*
CE7*	←	42	○ ○	41	→	IE3
		40	○ ○	39	→	C*/D
		38	○ ○	37	→	A/B*
		36	○ ○	35	→	ZWR*
		34	○ ○	33	→	ZRD*
		32	○ ○	31	→	AUX (Reserved)
0V		30	○ ○	29	←	REQ*
		28	○ ○	27	←	INT*
		26	○ ○	25	→	PCLK* (5 MHz)
		24	○ ○	23	→	ZIACK*
		22	○ ○	21		D0
D1		20	○ ○	19		D2
D3		18	○ ○	17		D4
D5		16	○ ○	15		D6
D7		14	○ ○	13		0V
0V		12	○ ○	11		0V
+12V		10	○ ○	9		+12V
+5V		8	○ ○	7		+5V
+5V		6	○ ○	5		+5V
0V		4	○ ○	3		0V
-12V		2	○ ○	1		-12V

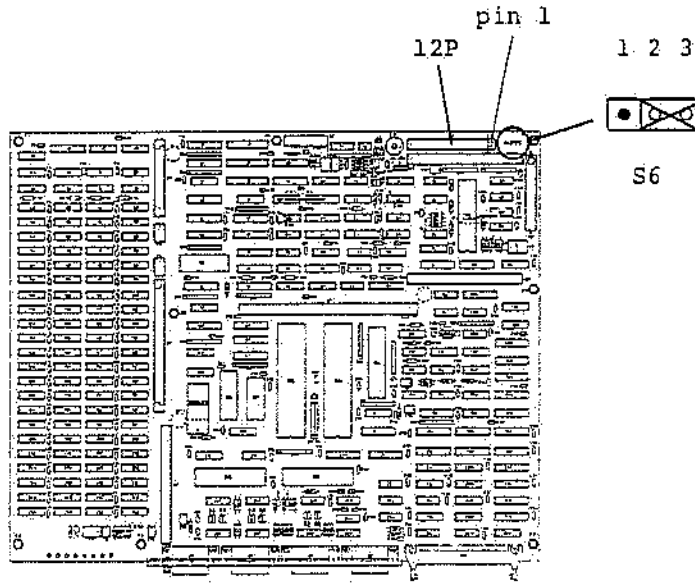
Notes: The expansion boards 5172-00 are mounted above the internal V24 ports, using mainly identical I/O connectors DA15P. However 5172-00 does not support external clocks.

The connector is a 50-pin ribbon cable connector.

Floppy connector for 5 1/4 inches floppy (12P)

Up to two 5 1/4" drives can be connected to 12P.

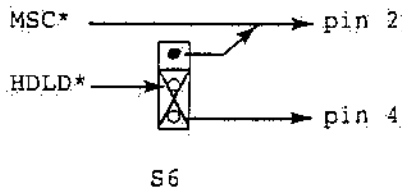
Position  
on board:



Pinning:

	1	○ ○	2	→ MSC* (motor speed control)
	3	○ ○	4	→ HDLD* (or no connect)
	5	○ ○	6	
	7	○ ○	8	← IP* input
	9	○ ○	10	→ SEL0*
	11	○ ○	12	→ SEL1*
0V	13	○ ○	14	
Ground	15	○ ○	16	→ MOTOR*
	17	○ ○	18	→ DIRC*
	19	○ ○	20	→ STEP*
	21	○ ○	22	→ WD*
	23	○ ○	24	→ WG*
	25	○ ○	26	← TRO0* input
	27	○ ○	28	← WPRT* input
	29	○ ○	30	← RDTA* input
	31	○ ○	32	→ SIDE*
	33	○ ○	34	← RDY* input

Notes: HDLD\* is normally to pin 4 through the S6 jumper (see figure). For drives, not using HDLD\*, the jumper S6 can be removed. Old types of 5 1/4" drives, requiring RDY\* on pin 6 can not be used.



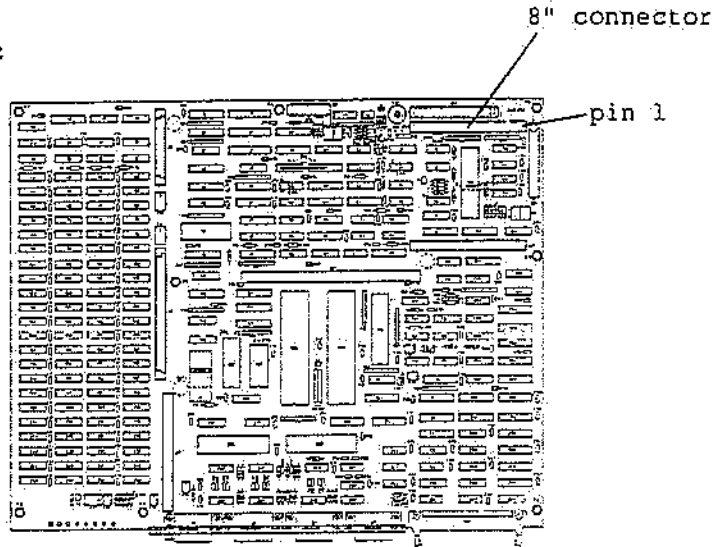
The connector is a 34-pin ribbon cable connector.



Floppy connector for 8 inches floppy (11P)

Up to two 8 inches drives can be connected to 11P.

Position  
on board:



Pinning:

	1	○ ○	2	→	LOI*	
	3	○ ○	4	→	MOTOR*	
	5	○ ○	6			
	7	○ ○	8			
	9	○ ○	10	←	DSD*	input
	11	○ ○	12	←	DCH*	input
	13	○ ○	14	→	SIDE*	
	15	○ ○	16			
	17	○ ○	18	→	HDL D*	
	19	○ ○	20	←	IP*	input
	21	○ ○	22	←	RDY*	input
0V	23	○ ○	24			
Ground	25	○ ○	26	→	SELO*	
	27	○ ○	28	→	SEL1*	
	29	○ ○	30			
	31	○ ○	32			
	33	○ ○	34	→	DIRC*	
	35	○ ○	36	→	STEP*	
	37	○ ○	38	→	WD*	
	39	○ ○	40	→	WG*	
	41	○ ○	42	←	TROO*	input
	43	○ ○	44	←	WPRT*	input
	45	○ ○	46	←	RDTA*	input
	47	○ ○	48			
	49	○ ○	50			

Notes: The connector is a 50-pin ribbon cable connector.

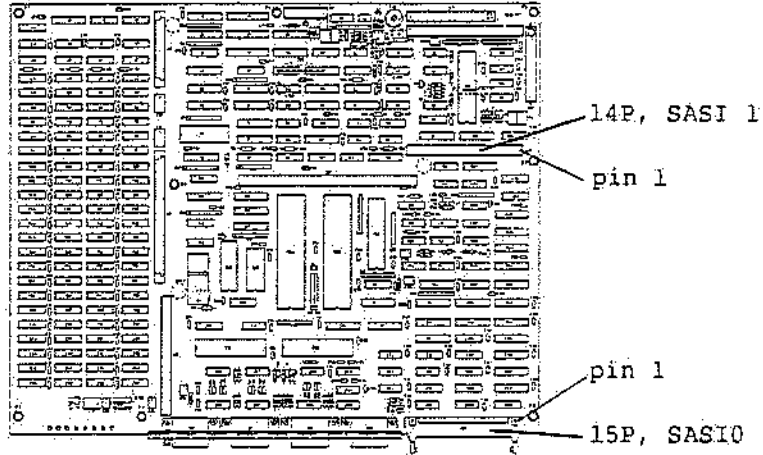
SCSI/SASI connectors (14P and 15P)

Two separate independant identical SASI channels.

SASI 0: 15P connector, near the serial connectors.

SASI 1: 14P connector.

Position  
on board:



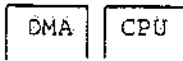
Pinning:

	1	○ ○	2	D0*
	3	○ ○	4	D1*
	5	○ ○	6	D2*
	7	○ ○	8	D3*
	9	○ ○	10	D4*
	11	○ ○	12	D5*
	13	○ ○	14	D6*
	15	○ ○	16	D7*
	17	○ ○	18	
	19	○ ○	20	
	21	○ ○	22	
	23	○ ○	24	
0V	25	○ ○	26	
Ground	27	○ ○	28	
	29	○ ○	30	
	31	○ ○	32	
	33	○ ○	34	
	35	○ ○	36	← BSY* input
	37	○ ○	38	→ ACK*
	39	○ ○	40	→ RST*
	41	○ ○	42	
	43	○ ○	44	→ SEL*
	45	○ ○	46	
	47	○ ○	48	← REQ* input
	49	○ ○	50	← I/O* input

Notes: Special test signals can simulate the control input signals for testing.

The connector is a 50-pin ribbon cable connector.

Expansion connector (6P)

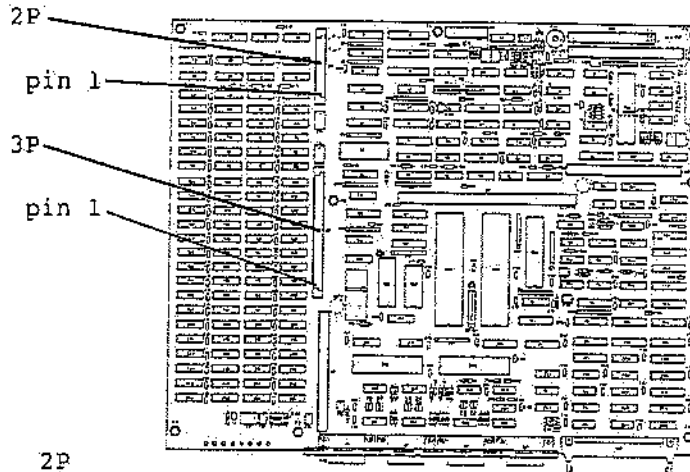


Pinning:

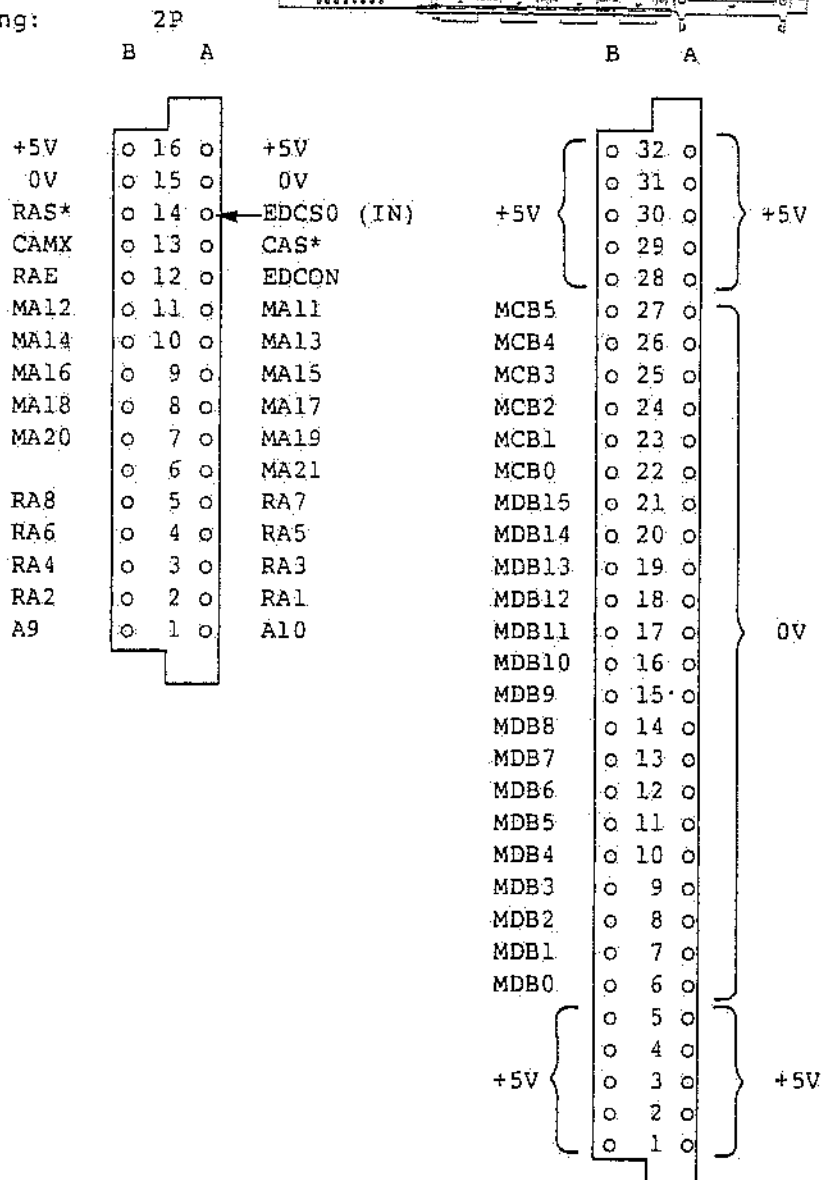
		A	B	
+12V	o	1	o	+12V
0V	o	2	o	0V
-12V	o	3	o	-12V
0V	o	4	o	16 MHz clock
(20 MHz) OSC	o	5	o	PREN
XIRQ4*	o	6	o	XIRQ5*
XIRQ2*	o	7	o	XIRQ3*
(CIO:B7)ERR LED	o	8	o	XIRQ1*
0V	o	9	o	0V
IPL0	o	10	o	IRQ2*
IPL2	o	11	o	IPL1
IRQ5*	o	12	o	ACL* (-ACLOW*)
PERMIT*	o	13	o	0V
FAS*	o	14	o	0V
BGI*	o	15	o	BERR*
FC2	o	16	o	FC0
A1	o	17	o	A2
A3	o	18	o	A4
A22	o	19	o	A23
A20	o	20	o	A21
A18	o	21	o	A19
A16	o	22	o	A17
A14	o	23	o	A15
A12	o	24	o	A13
A10	o	25	o	A11
A8	o	26	o	A9
A6	o	27	o	A7
0V	o	28	o	A5
XIOG*	o	29	o	0V
RST*	o	30	o	FC1
DONE*	o	31	o	ACK2*
AS*	o	32	o	R/W*
UDS*	o	33	o	LDS*
BGACK*	o	34	o	DTACK*
FCK	o	35	o	TRRQ*
0V	o	36	o	0V
BG0	o	37	o	BRQ*
D14	o	38	o	D15
D12	o	39	o	D13
D10	o	40	o	D11
D8	o	41	o	D9
D6	o	42	o	D7
D4	o	43	o	D5
D2	o	44	o	D3
D0	o	45	o	D1
0V	o	46	o	0V
+5V	o	47	o	+5V
+5V	o	48	o	+5V
0V	o	49	o	0V
0V	o	50	o	0V

Memory expansion connectors (2P and 3P)

Position  
on board:



Pinning:



Notes: A 2 Mbytes memory board (2107-00) can be mounted above the onboard memory.  
The 3P connector is a B64-pin Euroconnector DIN41612.  
The 2P connector is a 32-pin Burndy connector.

## 8. TECHNICAL DATA

CPU: MC68010 16/32 bits processor.

Floating point processor: Socket for optional NS32081, used as slave processor.

System clock: 10 MHz CPU-clock. No wait-states are used at memory access.  
Clock modulation is used at byte-write cycles and at correctable memory errors.  
Crystal: 20 MHz. Externally generated clock can be used instead, jumper selected.

Peripheral clock: 5 MHz for the SCC circuits.  
16 MHz available in the bus expansion connector.

Watchdog: Should be pushed with max 0.5 sec interval.  
After 0.5 sec: Early warning signal generates interrupt.  
After 1 sec: System reset is generated.

Size: 300 \* 375 mm.  
The height depends on optional mounted expansions.

Environment: +10 .. +35 degrees C operating.  
20% .. 80% humidity.

Power requirement: +5V +/-5% 7 A without expansion  
+12V +/-5% 300 mA without expansion  
-12V +/-5% 300 mA without expansion

Power control: Output signal POWER\* with open collector drive, non-isolated. Can also be direct from the control panel power switch.  
Active low is power-ON.

Power fail support: "Power-low" input signal (ACLOW\*) can generate interrupt. TTL-level, non-isolated active low.

Memory: 2 Mbytes physical memory onboard.  
Up to 4 Mbytes total with 2107-00 board mounted.  
Memory chips: 256-bits, 120 ns access time, using type HM50256P-12 or equivalent.

Hardware ECC: Using the LS630 circuit. Modified Hamming code. 1 bit error correction, 2 bit error detection, using 6 extra bits per 16-bit word.

Memory Management Unit (MMU) Two-level MMU, supporting up to 4 Mbytes virtual memory per process.  
Map registers for 16 simultaneous processes for fast "context".  
Direct access to physical memory in transparent mode.  
Page size: 2 Kbytes / page  
Attributes: Not-accessible  
Write-protected  
Flags: Accessed  
Modified

I/O-MAP: User protect attributes, with MMU, per I/O-group. System control space is always user protected.

- Serial I/O,
- SASI-0,
- SASI-1,
- Floppy,
- Each "Card select" on a DataBoard expansion is separately protected.

All 8-bit devices are connected to the lower half of the data bus and requires "odd" addresses.

Expansion area: The memory area for expansion can be user protected with the PERMIT\* signal.

Boot-PROM: 16 Kbytes in one 27128 EPROM.

NVRAM: Non-volatile RAM (32 bytes) for parameters.  
Circuit: NMC 9306.  
Allows typically 10.000 erase/write cycles.

Real-Time-Clock: MEM E050-16 real time clock circuit with battery backup.

Battery: 2.4 V, type GE013 for the real-time clock only.

Bus error logic: Hardware detection of bus errors and bus time-out (7.5 microsec).

DMA: 4 independant DMA channels, using the HD68450 circuit.  
The DMA accesses memory through the MMU.  
Standard block size is 32 Kbytes with present software support. (Max = 64 KB).

- DMA ch.0: SASI-interface 0.
- DMA ch.1: SASI-interface 1.
- DMA ch.2: Floppy interface OR a DataBoard interface, one at a time.
- DMA ch.3: One serial channel at a time.

Each channel can alternatively be used for memory to memory transfers.

**Control panel:**

Support signals for LED's, power-on controls and Auto/Manual selection on an optional control panel.

Connector: 10-pin ribbon cable connector with key and lock.

**Serial I/O:**

4 serial full duplex V24(RS232C) channels onboard, synchronous or asynchronous, using two SCC circuits (type Z8530). Fully buffered, using 1488/1489 circuits.

Asynchr: 75 baud ... >19.2 Kbaud, Also split speed.

Synchr: Up to 1 Mbit/sec.

Up to a total of 12 channels, with two expansion boards (5172-00) mounted. The expansion channels only support asynchronous communication. Logically a third 5172 board could be used, but is presently not supported by the mechanical design.

Connectors: Standard DA15P connectors.

**SCSI/SASI ports:**

2 independant SCSI/SASI interfaces.  
32 bytes = 16 words send/receive buffer.  
Up to 8 slave devices can be connected per port. Only single master configuration is supported.

Connectors: 50-pin Burndy connectors with key and lock.

**Floppy interface:**

Up to 2 minifloppy (5 1/4") drives and up to 2 floppy (8") drives can be connected. Only one drive is accessed at a time, supported by the DMA. The connectors are provided with key and lock.

Connectors: 5 1/4" - 34-pin ribbon cable connector.

8" - 50-pin ribbon cable connector.

Interrupt logic: Level 7: (NMI\*) from external button or from the watchdog early warning signal.  
Level 6: Power fail warning from the power supply (ACLOW\*).  
Level 5: Reserved. From expansion slot.  
Level 4: Serial communication channels.  
Level 3: System control. From the CIO.  
Extended priority levels are:  
7: Internal SASI 0  
6: Internal SASI 1  
5: DataBoard XIRQ5\*  
4: DataBoard XIRQ4\*  
3: DataBoard XIRQ3\*  
2: DataBoard XIRQ2\*  
1: Special expansion port  
0: Internal floppy interface  
Level 2: Reserved. From expansion slot.  
Level 1: Correctable memory error.

Bus expansion: Connector for mounting optional expansion backplanes.  
Examples:  
- 5173 DataBoard adapter (3 slots)  
- 5180/81 DataBoard and VME expansion.  
(2 VME and 4 DB slots)

DataBoard support: The onboard hardware supports DataBoard I/O through an expansion backplane:  
- Automatic CS\* strobe at each access.  
- Separate user access protection for each DataBoard interface.  
- The DMA channel 2 is shared between the floppy and DataBoard expansion.  
- 4 DataBoard interrupt levels supported.  
Up to 32 levels with the 4202 interrupt scanner.



### Boot-PROM contents.

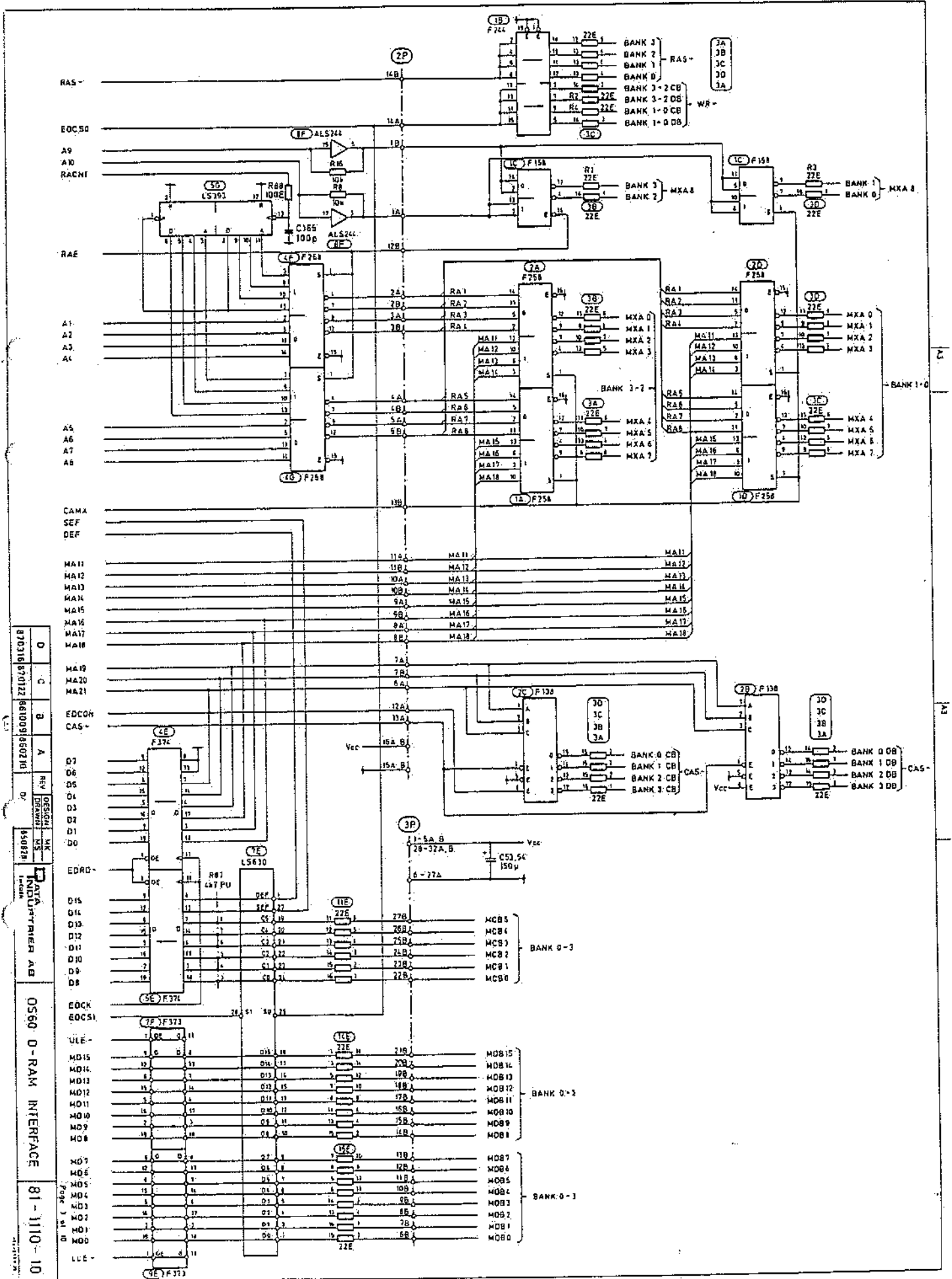
The Boot-PROM contains a start-up program, which does a hardware test of the system before it loads the operating system.

The Boot-PROM also contains the system serial number, which can be displayed with the DUNIX command:

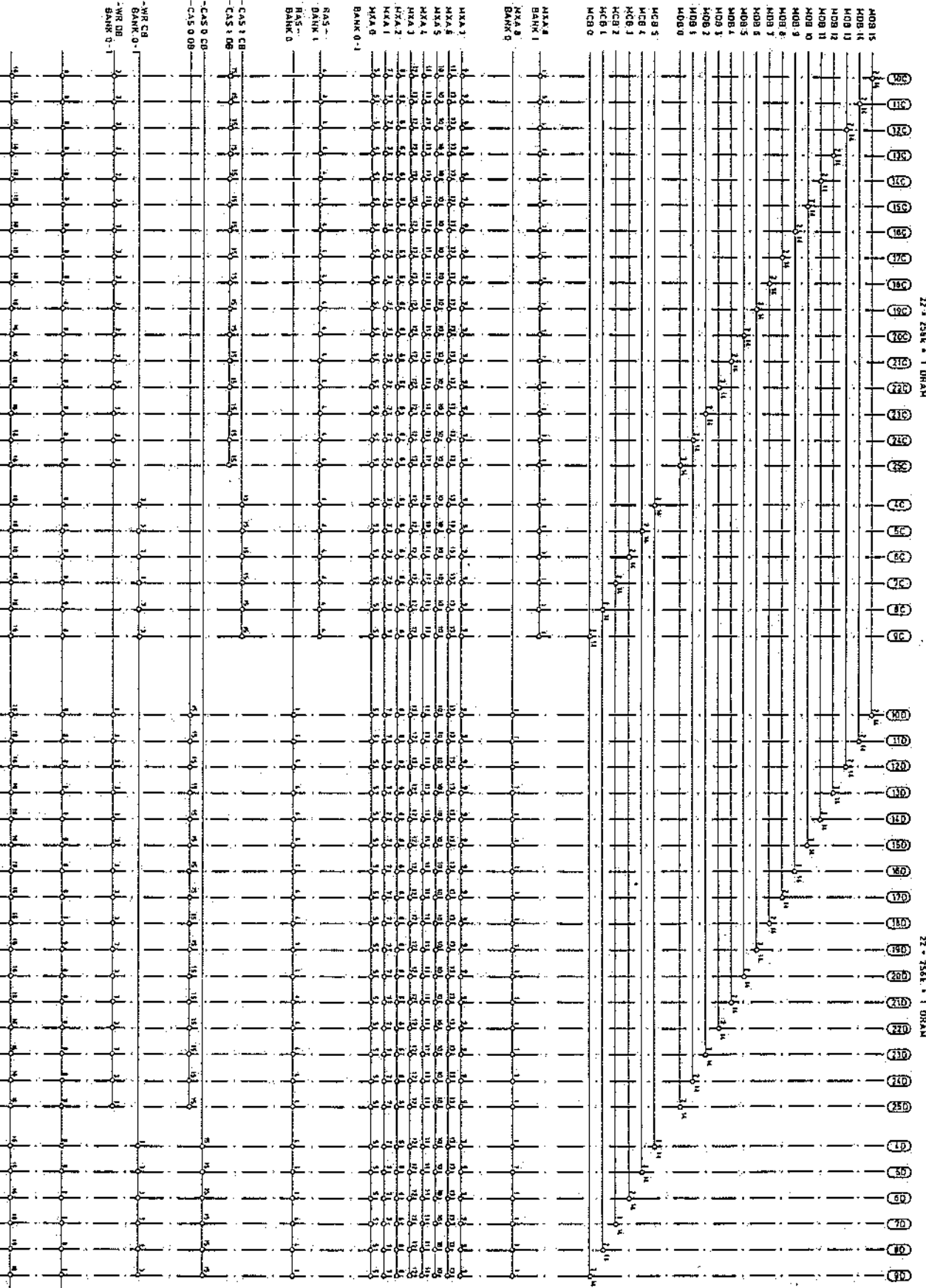
```
uname -u
```







0560 0-RAM INTERFACE  
81-1110-10

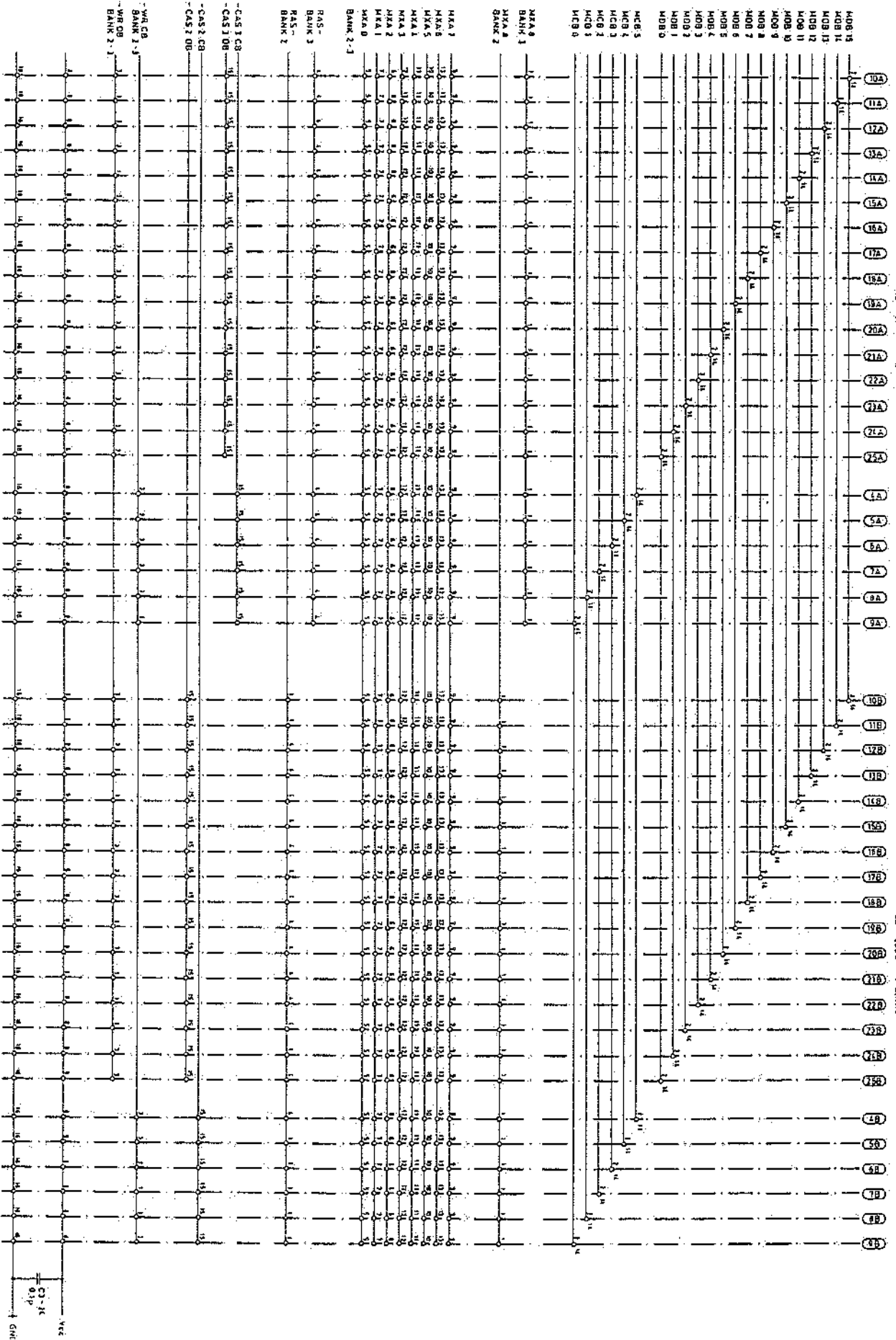


BANK 1

BANK 0

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REV	DESIGN	DATE	DATE	REV	DESIGN	DATE	DATE	REV	DESIGN	DATE	DATE
0	C	B	A	07016	870122	861009	860210	0	C	B	A
<p>0560 MEMORY MATRIX 1</p> <p>81-1110-10</p>											



BANK 1

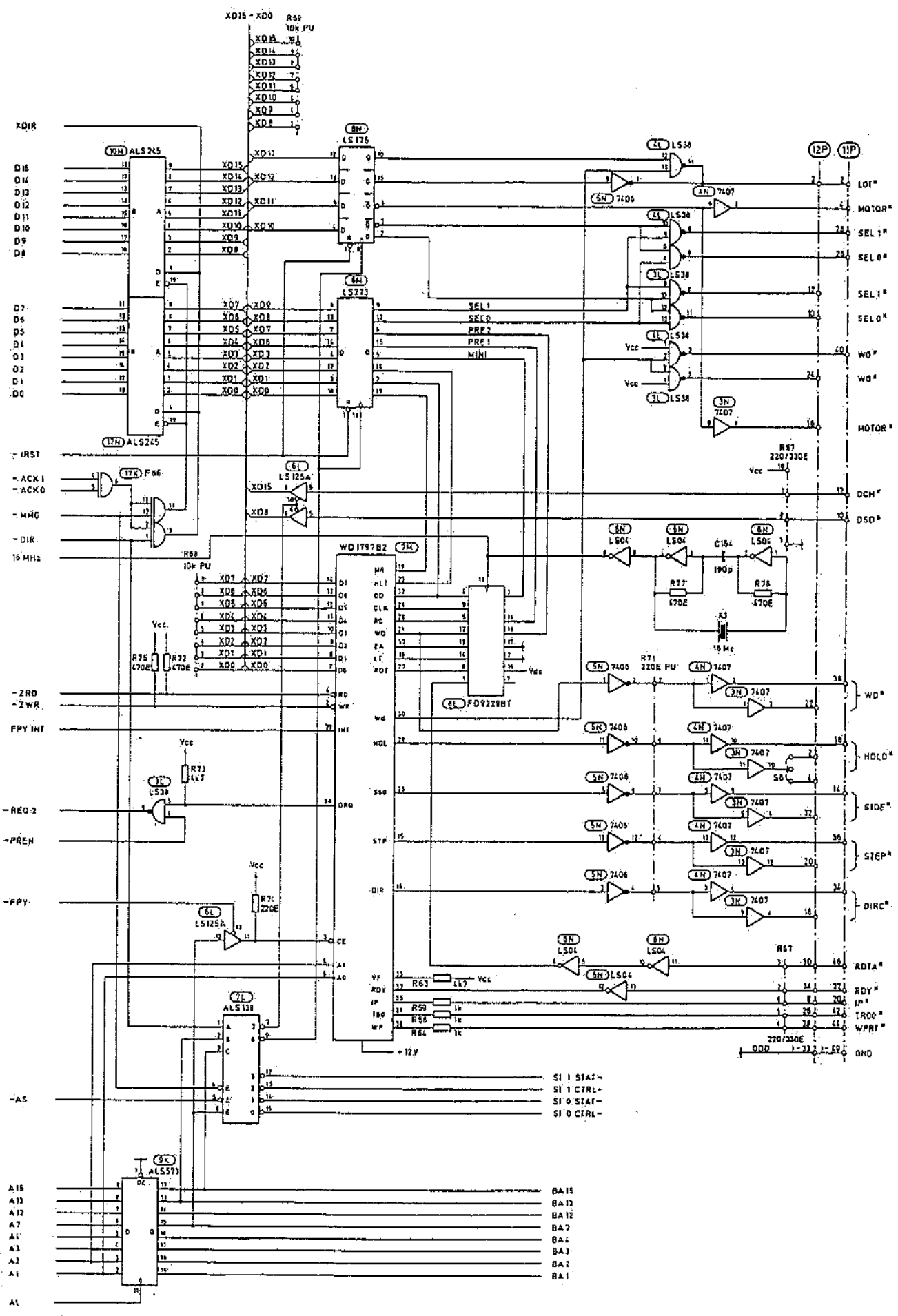
BANK 2

DESIGN NO.	REV.	DATE	DESIGNER	CHK'D	DATE
B70316	B70122	8/10/09	8/10/09		
DATA UNDERSTANDING					
OS60 MEMORY MATRIX 2					
81-1110-10					









DESIGN: [ ]  
 DRAWN: [ ]  
 CHECKED: [ ]  
 DATE: [ ]  
 OSGO FLOPPY INTERFACE  
 81-1110-10  
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