A Low/High Band Highly Linearized Reconfigurable Down Conversion Mixer in 65nm CMOS Process

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***Abstract*—This paper presents a universal down conversion mixer for a multistandard wireless receiver with adapted reconfigurability in the form of RF bandwidth, active/passive and IF bandwidth. In the proposed architecture RF bandwidth reconfigurability is reconfigured between low band (LB) RF frequency and high band (HB) RF frequency mixer modes. LB / HB reconfigurability is made through power switching the transconductance amplifier. Active / Passive reconfigurability is made through switching the input signal between gate and source terminal of input transistors and enabling/disabling the transimpedance stage at the output. The CMOS transmission gate (TG) switches are designed to provide optimum headroom in this low voltage design. The proposed circuit is designed in the UMC 65nm RFCMOS technology with 1.2V supply voltage. From the simulation results, the proposed circuit shows conversion gain of 22/26 dB and 25/31 dB, noise figure of 14.2/12.1 dB and 11.5/8.16 dB, IIP3 of 10/8.1 dBm and 6.4/3 dBm in LB and HB respectively where all these figures suggest passive/active mode. Hence this circuit will be much helpful in multi-standard receiver design.**

I. INTRODUCTION

With increasing demand, communication technology also needs improvement. In communication Low [1]and high RF frequency applications are having different power demands. So wideband receiver is also a wastage of power. On the other hand Internet of Things (IoT) enabled platform also demands multi-mode multi-standard transceiver enhance the performance through seamless connectivity between zigbee, bluetooth, Wi-Fi, UWB and cognitive radio interface. To meet above demand most of the smart systems already support an increasing number of radios, which turns into a significant increase in component count and cost[2]-[5]. Therefore, the easiest solution is a single re-configurable radio. To make the radio re-configurable researchers introduce the RF front-end transceiver with reconfigurable LNA[6]-[7], PA, PLL[8], mixer[9]-[10], and filter[11] etc. Most of the proposed re-configurable mixer have shown gain variability and Bandwidth tuning[12]-[13] through current variation, load tuning etc[9]-[11]. However, in multi-mode IoT systems, the other performances like noise figure, linearity reconfiguration need to be incorporated in mixer design. So our emphasis is to design a Mixer that can provide reconfigurability on these performances along with RF and IF bandwidth selection. In this regard, we propose a re-configurable down conversion mixer which switches between LB / HB and Active/Passive modes depends on performance requirement. Optimization between power can be achieved through switching between high and low frequencies.

The prime features of the re-configurable down conversion mixer are:

1) Reconfiguration between low band and high band with gain and noise tunability at IF stage.
2) Power switching is used to switch on or off Transconductance amplifier.
3) Reconfiguration in the single circuitry between active and passive modes is done to chose the mixer according to desired performance requirement.

Upto the best of our knowledge, first time one such work is being reported in IoT perspective and detail operation are described in following paragraphs as section II details the proposed architecture and simulation results are explained in Section III.

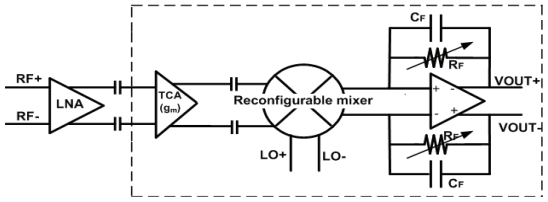

Fig. 1. Wide-band receiver front end.

II. ARCHITECTURE

The block diagram of wide-band RF front-end (demodulator) is shown in Fig. 1. The mixer is located after the LNA and downconverts the RF signal to a low IF signal. So it is required to design high input impedance g_m stage to avoid the loading effect and to provide high isolation between IF, LO and RF. Widely used active mixer suffer from poor linearily, especially when the supply voltage is low. The opposite side passive mixer can provide very good linearity with comparable noise performance. So according to demand Active/Passive reconfigurability is done. The differential ended RF input is taken by RF balun with 50 ohm input impedance termination. All the signal paths are fully differential in style to suppress the common mode noise and second order harmonic.

Reconfigurable front end mixer consists of two transconductance amplifier (LB / HB), two types of mixer (Active / Passive) in single circuitry and load stage. Transconductance amplifier that converts the RF input voltage into current is DC decoupled to switching stage. The mixer core output is directly coupled to transimpedance stage. IF voltage is built at the output of transimpedance amplifier after the RF current gets commutated in switching stage and passes to first order

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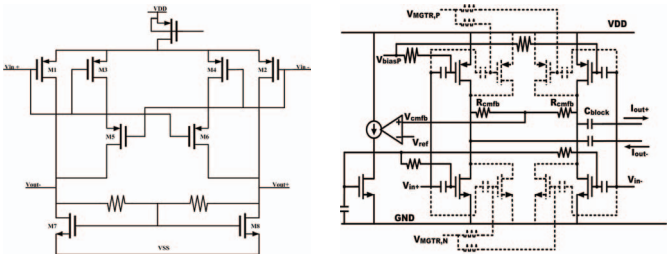


(a) Low Band TCA (b) High Band TCA

Fig. 2. Switch implementation using MOS

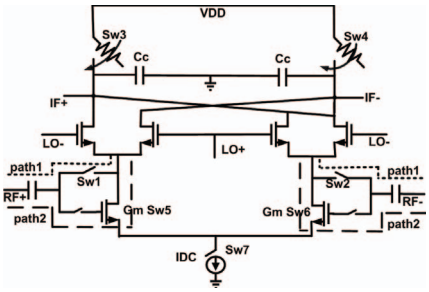
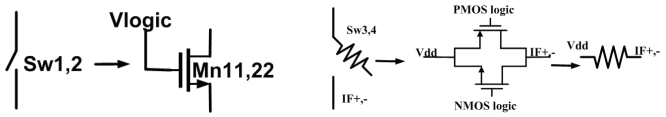


Fig. 3. Reconfigurable mixer.



(a) NMOS switch (b) resistive switch

Fig. 4. Switch implementation using MOS

RC low pass filtering. TIA offers a virtual ground node for the g_m stage, resulting in high linearity. Unlike narrow-band designs, C_{PAR} (parasitic capacitance at the output node of the transconductance stage) is minimized to allow a less stringent noise specification upon the op-amp which favourably gets translated into lower power consumption circuit design.

A. Transconductance Amplifier

A current switching passive mixer consists of transconductance stage, switching stage and transimpedance amplifier stage. Fully differential CMOS transconductors are employed for LB and HB to convert the input RF voltage signal to RF current as shown in Fig. 2. Post which the current signal is fed to the switching stage ensuring that second order nonlinearity is reduced by using fully differential topology. TCA is modeled to minimize the signal loss and enhance its linearity performance.

Fig. 2(a) shows a simplified circuit schematic of the g_m stage, where the main transistor pair M1 and M2 and auxiliary circuit M3-M6 are designed using PMOS that cancel the third order distortion of the main pair [1]. The g_m stage is designed to dissipate 2.7mA current from a 1.2V supply with .1 to 1.5G bandwidth.

Both PMOS and NMOS input stages use balanced input devices with no tail current as shown in Fig. 2(b). The use of multi-gated [14] input pair allows tuning to be done to achieve higher IIP3 with almost same bias current. HB g_m stage is designed to work from .6 to 5GHz. and dissipate 5.2mA current.

The common mode voltage is designed at VDD/2 for getting maximum swing. By setting VDD/2 common mode voltage, current can be minimized and parasitic capacitance at the output nodes of transconductor is optimized to the smallest possible value, thereby increasing the output impedance, for the purpose of improving the noise figure. The transconductance stage gain also reduces the overall noise of front end receiver.

B. Active / Passive Mixer

In this embodiment, modulator circuit is reconfigured between active and passive modes by switching between the output load, DC power supply and Gm stage (Gm MOS of active case) and current source shown in Fig. 3. Common source configuration is chosen because of compatibility with cases.

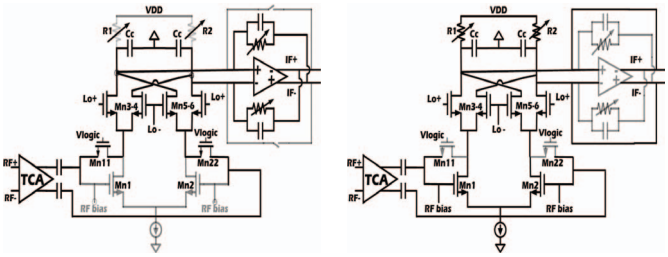
In passive mode, the frequency mixer or modulator circuit is simply composed of four NMOS transistors characterized by resistance (Ron) when switched on. Accordingly, in order to make the common-source input stage configuration suitable for both active and passive mode topologies, switch (Sw1-2) are implemented using NMOS which have been added between the gate and drain of the common source transistor (Gm MOS). TCA differential output current is applied at the drain of the transistor Mn11 and Mn22 (NMOS switch 1-2) to route to the mixer core for mixing in the current domain. Vlogic high or low is given at the gate of Mn11 and Mn22 to configure reconfigurable mixer to operate in active/passive mode as shown in Fig. 4(a). Specifically when there is no current flowing through the mixer core, Vlogic is set to high, thus causing input signal to flow directly through the switching stage as shown in path 1 to mix with LO signal. Width of NMOS is chosen to provide degeneration resistance, thus turning the overall mixer topology into a passive mode as shown in Fig. 5(a). Transistors thus operate as switch 1-2 as well as degeneration resistance R_{deg}(switch 1-2 resistance), thereby increasing linearity of passive mixer [5]. Capacitor Cc is a high-frequency compensation capacitor used to suppress the noise at higher frequency. The modulated signal is supplied from the mixer core without any load and directly coupled with transimpedance amplifier. The voltage conversion gain of passive mixer is

$$VCG = \frac{2}{\Pi} * g_m * Z_F \tag{1}$$

where Z_F is the feedback impedance of transimpedance amplifier, C_F parallel with R_F and g_m is the transconductance of transconductance amplifier.

Resistive switches 3-4 designed using transmission gate, made of PMOS and NMOS switch, are fully turned off so that drain of the switching MOS is directly connected to input MOS of transimpedance amplifier without any coupling capacitor. Switches 5-7 designed using NMOS will also be off when this circuit operates in passive mode.

In active mode, input stage of the frequency mixer or modulator circuit have a configuration that is a common source



(a) Passive mode (LB or HB) (b) Active mode (LB or HB)

Fig. 5. Reconfigurable mixer in passive and active mode

topology. This topology is chosen to provide better gain and low noise figure. Double balance gilbert cell architecture is used in active configuration when there is current flowing through input(Gm) MOS Mn1 and Mn2 (Sw 5-6). The bias voltage can be selected to control parameters of input stage or switching operation of Gm MOS switch 5-6 as shown in path 2. The Gm of MOS Mn1 and Mn2 can be changed by changing the value of bias voltage, thus varying the gain of mixer. The optimum value of bias voltage is so desired so that mixer consumes a minimal amount of current. Switch 7 has been designed using NMOS which is biased in saturation region to provide current source. Thus turning the overall topology into an active mode as shown in Fig. 5(b).

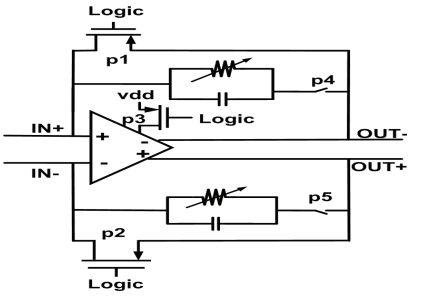
Transmission gate is used as a resistive switch connected between VDD and IF output as shown in Fig. 4(b). W/L of PMOS and NMOS is chosen so that some voltage drop occurs across it and act as a resistance. Transmission gate total resistance is $Rtol = R_PMOS||R_NMOS$. As it is connected to VDD so it acts as resistive load and Capacitor Cc is provided to act as a low pass filter in active mode operation of reconfigurable mixer. Gain of active mixer can be tuned by changing the resistance of transmission gate. The output of active mixer is directly passed to the output stage without going to TIA.

C. Transimpedance Amplifier

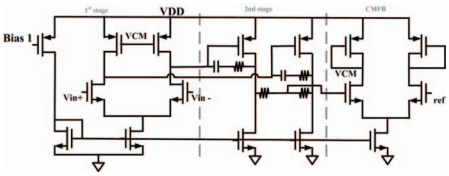
A simplified schematic of transimpedance amplifier is shown in Fig. 6(a). TIA consists of an operational transconductance amplifier with a feedback R_FC_F. R_F and C_F value is set according to IF frequency. A two stage miller compensated OTA topology is chosen for TIA design as shown in Fig. 6(b). First stage to provide high gain and second stage for high swing. So that structure can obtain both, high output swing and low input referred noise. Transimpedance amplifier is used to convert current to voltage output in passive mode operation. The TIA stage serves as load and anti-aliasing filter for the passive mixer. The TIA is designed in such a way so that very low impedance is provided at the passive mixer output. TIA input impedance is given by

$$Z_{in}(f) = \frac{2}{A(f)} * \frac{R_F}{1 + 2\Pi R_F C_F} \quad (2)$$

Where $A(f)$ is the open loop gain of the OTA. Due to high gain OTA bandwidth is limited and high frequency components suffer high impedance. In order to filter out high frequency components C_F is inserted. This is done for all signal current to flow into feedback R_FC_F from the mixer core. The TIA



(a) Schematic of TIA stage



(b) Schematic of OTA

Fig. 6. Transimpedance amplifier

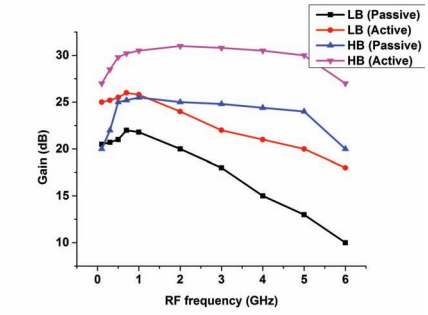


Fig. 7. Simulated conversion gain reconfigurable mixer vs RF frequency.

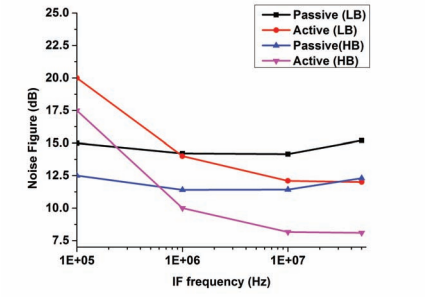
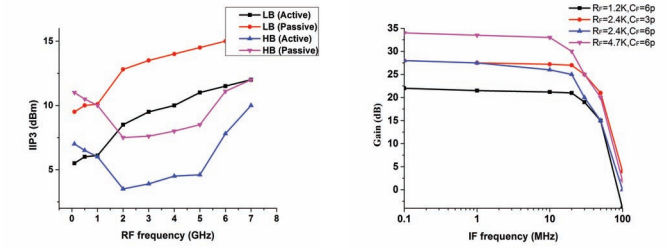


Fig. 8. Simulated noise figure vs IF frequency.

draws a total of 3.3mA from the supply. In case of active mixer operation TIA will be switched off to save power. In case of active mixer operation TIA will be switched off by switching off p3 switch to save power and p1, p2 will be on. p4 and p5 also implemented using MOS and switch on or off in case of passive and active respectively. The gain of the TIA can be tuned by changing the value of R_F and it provides another degree of freedom to configure the gain of the downconverter.

TABLE I. SIMULATION RESULTS AND COMPARISON

Parameters	Active(LB)(This work)	Active (HB) (This work)	Passive (LB) (This work)	Passive (HB) (This work)	[1]	[5]	[4]	[9]	[10]	[11]
Gain (dB)	26	31	22	26	19.5-21	22.5-25	35	9-24	1.2-17	3.5-20.5
Noise figure (dB)	12.1	8.16	14.2	11.4	11.4-12.4	7.7-9.5	10	NA	≥ 11	≥ 8
IIP3 (dBm)	8.1	3	10	6.4	8-9	≥ 7	11	3.5 to -12	8.6	≤ 8.5
Power(mW)	7.17	10.66	7.05	10.56	5.4	10(mixer + TIA)	20.25	2.4 to 18	5.9	5.6-9.6
Bandwidth(GHz)	.1 to 1.5	.6 to 5	.1 to 1.5	.6 to 5	.048-.86	1.55 to 2.3	.7 to 2.5	2 to 10	1 to 12	.7 to 2.3
Technology (CMOS)	65nm	65nm	65nm	65nm	130nm	180nm	130nm	130nm	130nm	180nm
Power supply	1.2V	1.2V	1.2	1.2	1.2	2	1.5	1.2	1.2	1.8



(a) IIP_3 of Reconfigurable mixer.

(b) voltage Conversion Gain of Reconfigurable mixer.

Fig. 9. Simulated linearity and Gain of reconfigurable mixer

III. SIMULATION RESULTS

Based on the qualitative description of the building blocks, using their insights related to operation, the RF front-end demodulator is simulated in CMOS 65nm process. The voltage conversion gain plot is shown in Fig. 7 with respect to RF frequency at 1MHz IF. The voltage conversion gain is close to 22/26 dB and 25/31 for LB and HB case respectively where these figures suggest passive/active mode.

The simulated double side band noise figure at 800MHz and 2GHz for LB and HB respectively is shown in Fig. 8. The Simulated noise figure for active/passive is 14.2/12.1 dB and 11.5/8.16 dB @ 5MHz in LB and HB case respectively.

The two tone linearity test result is shown in Fig. 9(a) for 2GHz and 800MHz LO frequency for HB and LB. Due to high conversion gain at low IF, the output compression point of the OPAMP, limits the input referred linearity of the circuit. 1dB-compression point of the circuit is limited by the output swing and varies with IF frequency. The simulated IIP_3 is 6.4/3dBm and 10/8.1 for HB and LB, where these figures suggest passive/active mode.

Fig. 9(b) depicts the voltage conversion gain of the proposed down conversion passive mixer of LB. By changing the value of R_F and C_F gain can be varied with constant bandwidth or by varying only R_F conversion gain can be varied with little variation in bandwidth.

IV. CONCLUSION

In this paper, a wide band Reconfigurable mixer is simulated in 65nm technology. A new concept of reconfiguration between Active / passive and LB / HB downconversion mixer is presented. This is an important design guideline for modern baseline deep sub-micron CMOS processes. Reconfigurable mixer is simulated in the frequency range .1GHz to 6GHz. The analytical results shows close to simulted results. With the exception of few very stringent standard, the architechture is suitable for both cases.

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