Allegro® PCB Router:
What's New in Release 15.5.1

Product Version 15.5.1
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Cadence Design Systems, Inc., 555 River Oaks Parkway, San Jose, CA 95134, USA

Contents

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What's New in Release 15.5.1

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  - Differential Pair Ripup Controls
  - Filter controls for Differential Pair Segments
- New Platform for the Mentor Board Station Translator
- New Demos

Differential Pair Autorouting Enhancements

Improved Gather Point Computation

The computation for locating gather points as well as pin to gather point routing has been improved.

For further details, see *Gather Point Location and Pin to Gather Point Routing* in the *Allegro PCB Router User Guide.*

Differential Pair Ripup Controls

Options have been added to allow you to suppress or enable the removal of routed differential pairs with conflicts by the `auto remove` command.

For further details, see the `auto remove pair` option for the `set` command in the *Allegro PCB Router Command Reference.*

Filter controls for Differential Pair Segments

Options have been added to allow you to suppress or enable the removal of differential pair segments by the `filter` command.

For further details, see the `filter_remove_diff` option for the `set` command in the *Allegro PCB Router Command Reference.*

New Platform for the Mentor Board Station Translator

The Mentor Board Station Translator is now supported on the Linux platform.

New Demos

The following new demos were created for Allegro PCB Router, Release 15.5.1:

- Creating a Basic Do File – Shows how to create a Do file using the on-board Rules Did FIle Editor.
- Using a Basic Do File – Shows how to set up and use a Do file to autoroute a design.

To access these demos, choose *Help – Documentation* from the main menu of Allegro PCB Router, then select the Demos tab on the Help page.

What's New in Release 15.5

Allegro PCB Router version 15.5 contains the following enhancements.

Allegro PCB Editor Integration Optimization

Additional Router Checks

The following new router checks are performed when the `specctra_checks` and `spif` commands are invoked from Allegro PCB Editor.

Check Name	Description
`checkDanglingConnections`	Checks for one or more dangling connections.
`checkRatTs`	Checks for one or more Rat-Ts with no `FIXED_T_TOLERANCE` property.
`checkXtalkTable`	Checks for the presence of a cross-talk table named `design_name.xtb` in the working directory if DRC for Xtalk is enabled.
`checkShapePadstacks`	Checks for one or more padstacks. Warns of potential performance degradation in the autorouter.

`checkHighNumberDRC`	Checks for 10K or greater DRCs. Warns of potential degradation while reading results from the autorouter.
`checkDiffPairConstraintArea`	Checks for differential pair nets within the constraint area. Warns if differential pair nets do not respect region rules in the autorouter.
`checkShapeVoids`	Checks for 7K or greater vertices in signal layer polygons. Warns of possible round-off and performance problems in the autorouter.

Rat-T Placement Optimization

A new `optimize_ts` command is available within Allegro PCB Editor that starts Allegro PCB Router in the background and optimizes the location of T-points. Upon optimizing the locations based on physical criteria, a Session file containing the new T-point locations is written.This file translates back into Allegro PCB Editor to update the design.

For further details, see *Optimizing Tpoint Location* in the *Allegro PCB Editor User Guide:Routing the Design.*

Blind and Buried Via Depth Control

Parameters that control fanout to blind or buried vias have been added to the Automatic Router Parameters dialog box (Fanout Tab) within Allegro PCB Editor.

Custom Route

A new `custom_route` command is available within Allegro PCB Editor that starts Allegro PCB Router in the foreground and runs a custom autoroute strategy. It enables you to improve the proficiency of the autorouter by:

- separating and then introducing rules strategically.
- providing feedback and allowing you to monitor and intervene in the autorouting process.
- allowing optional import of routing results back into Allegro PCB Editor upon completion.

For further details, see `custom_route` in the *Allegro PCB and Package Physical Layout Command Reference*.

Layersets

The following sections describe the enhancements that were made to Allegro PCB Router to properly align with layerset support in Allegro PCB Editor.

SPIF Update

The following enhancements were made to the interface between Allegro PCB Editor and Allegro PCB Router.

- DRC Check State Parameter

  If set to *Never,* SPIF will not translate layerset information to Allegro PCB Router.

- New Database Objects
  - Net
  - Xnet – Collection of all from/to into an identified group to provide Short Side Xnet exclusion.
  - Differential pair
- Bus Override Property

  Translates the layerset rule to all members of the bus but does not supply the Exclusive Layer Set switch.

DRC Alignment

The following DRC exclusions are provided to align with Allegro PCB Editor.

- Pin Escape exclusion

  Any part of wire segments and vias that are on the path from an SMD pin to a legal layerset such as:
  - a through hole via pin escape.
  - a sequence of wires and vias which stagger toward a legal layer as with blind and buried vias.
- Staggered Via exclusion

  A progression of blind and buried vias that stagger to a legal layer.

  Note: This extends beyond the pin escape exclusion.

- Short Side of Xnet exclusion

  Will not DRC flag surface routing connecting two pins on the short side of an Xnet.

Layerset Routing Exception Report

You can generate a report that lists nets that have routing not adhering to the layerset rule and not reported as a DRC due to an exception. The report lists the net name followed by a list of wires not adhering to layersets. The total exception etch length is provided at the end of the report.

For further details, see *Layer Set Reports* in the *Allegro PCB Router User Guide*.

Differential Pair Same Width Neck

Allegro PCB Router has been enhanced to analyze input data to identify differential pair wires that are necked at a constant line width and will set corresponding necking flags internally. Note that Allegro PCB Router is not required to support interactive necking. Therefore, those flags are set once during startup as the `.dsn` or `.ses` file is read in.

Directory and Filename Space Support on Windows® Platforms

In alignment with Allegro PCB Editor, Allegro PCB Router allows spaces to be used when specifying directory and file names on Windows® platforms. This covers the following items that may have locations containing spaces.

- Software installation
- Design data storage
- Access of temporary files

Allegro Platform Documentation

All Allegro platform products have enhanced access to product information. All Help menus were simplified to access *Documentation*, *Web Resources*, and product information (*About*). When you select *Help – Documentation*, a new Help page interface displays all product documentation in tabbed categories so that you can get the information you are looking for quickly.

- The *Documentation* tab lists user guide and reference information for key concepts and comprehensive point-of-need information. The Help page opens to this tab by default.

- The *Release Info* tab lists release-specific information such as What's New, migration documentation, system requirements, and so on.
- The *Best Practices* tab lists Cadence-recommended practices for key product features and tools.
- The *Tutorials* tab lists self-paced training lessons in a step-by-step format that teach you how to use the product.
- The *Demos* tab lists flash-based multimedia videos so that you can watch an example of how to use certain features or processes. Products with many demonstrations may have sub-categories from which to choose on the left-hand side of the *Demos* tab.

You can take a guided multimedia tour of our new information architecture by clicking on Discovering Allegro Platform Documentation. This 5-minute demonstration provides a quick tour of the user documentation that accompanies your installation of Allegro platform products.

Note: To view multimedia demonstrations, you need a compatible Flash player. For more information about Flash players that you can download for free, see http://www.macromedia/shockwave/.

New Demos

The following new demos were created for Allegro PCB Router, Release 15.5:

- Placing Components from a List – Shows how to place components using a component list.
- Placing Components By X,Y Location – Shows how to place components using Cartesian coordinates.
- Performing Basic Autorouting – Shows how to use basic autorouting commands.
- Using Smart Route to Determine Design Problems – Shows the benefits of using the Smart Route command.
- Autorouting Selected Connections – Shows how to choose connections to be routed.
- Autorouting Connections Within a Fence – Shows how to autoroute connections bounded by a hard fence.
- Setting Up the Interactive Routing and Editing Environment
- Routing a Connection Using Edit Route – Shows how to route a connection interactively.

What's New in Release 15.2

Welcome to the New Allegro System Interconnect Design Platform

Cadence launched the Allegro System Interconnect Design Platform to deliver tools that support a new generation co-design methodology, promoting collaboration across the entire system design chain. The Allegro platform also incorporates branding changes for all PCB and package applications, starting in the 15.2 software. The following table lists the pre-platform product names for PCB Router applications and their corresponding Allegro platform names. For more information about the Allegro platform, visit `www.cadence.com`.

Pre-platform Name	Allegro Platform Name
256 Layer SPECCTRA	Allegro PCB Router 256U 210
6 Layer SPECCTRA	Allegro PCB Router 6U 210
SPECCTRA Advanced Rules option	Allegro PCB Router ADV option 210
SPECCTRA Auto/Interactive option	Allegro Router Auto/Interactive option 220
SPECCTRA Design for Manufacturing option	Allegro PCB Router DFM option 210
SPECCTRA Expert	Allegro PCB Router 610
SPECCTRA High-Performance option	Allegro PCB Router HP option 210
SPECCTRA Performance option	Allegro Router Performance option 220

The following table lists the changes to documentation titles for the Allegro PCB Router.

Pre-platform Title	Allegro Platform Title
SPECCTRA Command Reference	*Allegro PCB Router Command Reference*
SPECCTRA Design Language Reference	*Allegro PCB Router Design Language Reference*
SPECCTRA Known Problems and Solutions	*Allegro PCB Router Known Problems and Solutions*
SPECCTRA Translator for Mentor Board Station and Board Station 500	*Allegro PCB Router Translator for Mentor Board Station and Board Station 500*
SPECCTRA Tutorial	*Allegro PCB Router Tutorial*

SPECCTRA User Guide	*Allegro PCB Router User Guide*
SPECCTRA: What's New in Release 15.1	*Allegro PCB Router: What's New in Release 15.2*
Mentor Graphics Board Station (v.5.0.8)	No change
Mentor Translator Product Notes	No change
Mentor Translator Known Problems and Solutions	No change
Migration Guide for PCB and IC Packaging to Release 15.0 and 15.1	*Migration Guide for Allegro Platform Products Release 15.0, 15.1 and 15.2*
PCB and IC Packaging Properties Reference	*Allegro Platform Properties Reference*
PCB and IC Packaging Documentation Roadmap	*Allegro Platform Documentation Roadmap*

PCB Router version 15.2 contains the following enhancements.

- Z-Axis Delay
- Turbo Stagger option
- Pin Delay
- Multiple Matched Groups
- Dynamic F1 Help

Z-Axis Delay

To more accurately account for delay in your designs, the Z dimension of vias and PTH pins can now be included in timing path DRC calculations. You can include the conducting portion of a via or pin in DRC calculations for differential pair, phase tolerance, propagation delay, and relative propagation. The length of the conductive path of the hole is included in the actual length for the applied rule. The Z-dimension length is calculated by accumulating the number of the copper layer and dielectric thicknesses over the conductive path of the hole. The entry and exit copper layers are excluded from the calculation. For example, if a through hole via on a 10 layer PCB is used to connect a signal from layer 1 to layer 4, the unit length of the via would be:

```
VIA (Z LENGTH) = L2 + L3 + D1 +D2 +D3 where L = Layer and D = Dielectric.
```

Turbo Stagger option

A turbo stagger switch on the Options section of the Router setup tab improves routing performance though staggered pin connector fields. f left unset, the router may route around the connector, thus increasing lengths of routed traces.

Pin Delay

The Pin Delay feature manages the timing paths from the die of one package to the die of another package, or packages. Die-to-die timing paths across a printed circuit board will factor inter-package delay into timing and delay requirements. A new PIN_DELAY property allows delay values, such as inter-package length, to be entered across the PCB Editor tools. In the PCB Router, this feature is driven from the schematic or board level.

Multiple Matched Groups

Guidelines for source synchronous buses require their nets/pin pairs to reside in multiple matched groups. Prior to 15.2, Allegro PCB Editor restricted a pin pair to only one matched group. 15.2 removes this restriction as nets/pin pairs can reside in more than one matched group. PCB Router has been enhanced to align with Allegro PCB Editor.

Dynamic F1 Help

Allegro PCB Router 610 now supports dynamic F1 Help on active commands. You can display documentation by pressing the F1 function key while the command is running and Allegro PCB Router 610 is the active window.

Example:

1. Choose *Edit – Undo.*
2. Press F1.

   Documentation for the *Undo* command displays in your Web browser.

Note: Dynamic F1 Help does not support some standard Windows® commands such as New, Open, and Save As.

What's New in Release 15.1

SPECCTRA version 15.1 contains the following enhancements.

- Elongation Self-Coupling
- Linux Support
- New Windows® Update Process
- New Known Problems and Solutions Process

Elongation Self-Coupling

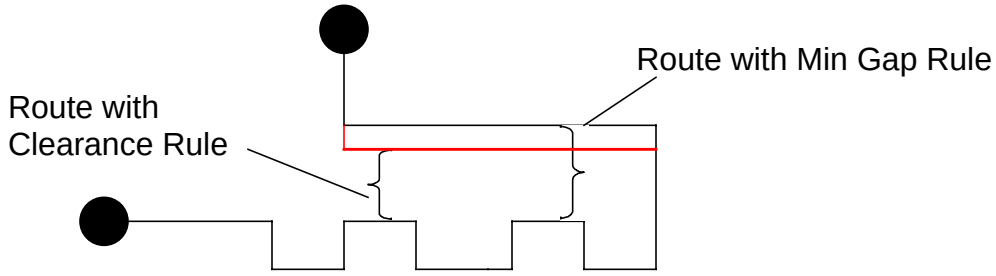
A new Do file command set option, `set selfcouple`, lets you control how closely the same connection routes to itself when the router produces a series of elongation patterns.

The new self-coupling functionality does not operate by default, thereby maintaining existing SPECCTRA functionality for current users. Currently, the *Min Gap* rule only applies within the elongation pattern itself during auto routing. By enabling the self-coupling functionality, SPECCTRA uses the *Min Gap* or *Min Time* parameter in a more expanded role.

The router identifies any same-connection wiring that is too close to elongation patterns within itself, thereby violating the *Min Gap* parameter, which exists in multiple levels of SPECCTRA's timing rule hierarchy, as follows:

- PCB
- Class
- Class Layer
- Group Set
- Group Set Layer
- Net
- Selected Net
- Net Layer
- Group
- Group Layer
- Fromto

- Fromto Layer



You can specify the *Min Gap* parameter in the *Elongation tab* of the **Timing Rules** dialog box that displays using *Rules - <hierarchy level> - Timing* (or specify the parameter in the **PCB Timing Rules** dialog box itself for the PCB level or in the **Net Length Timing Rules** dialog box itself for the Net Layer level).

A new Do file command, `report selfcouple`, generates `selfcouple.rpt,` which lists *Fromto Name, Min Gap Rule, Actual Gap, Start* and *End Location,* and *Layer* for all self-coupling violations that occur, even if you have not set the self-couple condition to on.

Linux Support

Linux Redhat 7.3 and 8.0 are supported for PSD release 15.1.

New Windows® Update Process

Beginning with version 15.1, updates for PCB and IC Packaging products can be installed directly from the Internet or downloaded to your local Windows machine for installation. Windows updates only replace changed files on a full previous installation; you no longer have to uninstall your product to reinstall an update.

Update files are located on `downloads.cadence.com` and have a version number like 15.1.001 where the last number will increment with each new update. Product updates are cumulative so you need only obtain the latest version, even if your 15.1 software is a few revisions from the current version.

New Known Problems and Solutions Process

Known Problems and Solutions documents will be posted on SourceLink. In an effort to provide you with up-to-date and accurate data, the known problems and solutions will be reviewed and updated at regular intervals; they will no longer be installed with the software's documentation set. Check SourceLink for the latest information about your products.

What's New in Release 15.0

SPECCTRA version 15.0 contains the following enhancements.

- Alignment with Allegro's New Dynamic Shapes
- Alignment with Allegro's New Differential Pair Functionality
- Virtual Pin (T-Points) Functionality
- Layersets
- Licensing
- Allegro to SPECCTRA Interface (SPIF) Enhancements
- PCB Enterprise Publications

Alignment with Allegro's New Dynamic Shapes

SPECCTRA supports Allegro's dynamic shapes, allowing for user control of:

- via pop through a shape
- wire plow during fanout

Note: SPECCTRA will not automatically heal the shapes. This is left for Allegro to do after importing the routing back into Allegro.

Alignment with Allegro's New Differential Pair Functionality

SPECCTRA is aligned with and fully supports Allegro's new differential pair functionality.

Following is the complete list of differential pair properties for 15.0

- Primary Gap
- Line Width

- Neck Gap
- Neck Width
- Coupling Tolerance (+)
- Coupling Tolerance (-)
- Minimum Spacing
- Gather Control
- Max Uncoupled Length
- Phase Control
- Phase Tolerance

These new constraints are available for nets, classes, groups, groupsets and fromtos. DRC markers and reports have been updated to include these constraints. GUI support for defining pin to pin (fromto) pairs has been added to SPECCTRA.

Note: For backward compatibility, SPECCTRA will still read the old differential pair definitions and rules for releases prior to 15.0.

For information on how to best implement differential pairs in your PCB designs, see *Best Practices: Working with Differential Pairs*.

Virtual Pin (T-Points) Functionality

The way SPECCTRA handles virtual pins has been improved. In the past, designers would get the best results by moving the T-Points to the desired location in Allegro, applying a Fixed T Tolerance in order to save the location, and forcing SPECCTRA to route to the virtual pins at the predetermined locations.

The dynamic movement of virtual pins has been enhanced in 15.0. You can now allow SPECCTRA to determine the location for virtual pins, eliminating the need to move T-Points in Allegro. By not applying a Fixed T Tolerance, you can let SPECCTRA determine the location for virtual pins and allow the router to dynamically move them if necessary during later routing passes. You can still pre-place critical T-Point locations if you wish, by applying the Fixed T Tolerance and allowing SPECCTRA to do the virtual pin placement for the less critical nets.

Layersets

Layerset functionality provides the ability to define routing layer "sets" and use them to better control routing. Designers have the need to define a number of layer pairs that they prefer to route certain nets or busses on and restrict routing from layers not in the "set". This is usually related to the similar impedance values of those particular layersets.

Similar to Use Layers, you can now assign layersets to a Class, Group Set, Net, or Group.

Layersets can be enabled or disabled.

- With layersets disabled, the router will route the assigned items on any of the layersets assigned (if there are more than one). However, once a net is started on a particular layerset, it will remain on those two layers and not bounce around between available layersets.
- With layersets enabled, the router will route all of the assigned items on only one of the layersets assigned (after having chosen the best one for routability).

Licensing

Licensing in SPECCTRA has been rewritten in 15.0. The principal features are:

- the ability to choose a SPECCTRA license based on PSD suite licenses that are available.
- a GUI for product license choice.
- SPECCTRA product license is locked to the PSD suite.
- Non-Allegro customers have a choice of 6 layer, 256 layer or PX3800 licenses.
- PSD suites cannot be upgraded with legacy features.

Allegro to SPECCTRA Interface (SPIF) Enhancements

Along with the necessary changes to support differential pairs and dynamic shapes, the following interface enhancements have been made.

- In Route Automatic and Route By Pick, users can now choose elongation patterns.
- In Route Automatic and Route By Pick, miter passes can now be specified.

PCB Enterprise Publications

Cadence is continually improving the quality and quantity of our documentation content, getting you the information you want and need. We provide several ways in which to access the documentation: the product's Help menu, dialog box help buttons within the product, the Cadence online documentation library, and SourceLink.

In release 15.0, the PCB information set is unified in the Cadence online documentation system (CDSDoc). Unifying the information set enables us to devote more time to improving the quality and quantity of content in our documentation. Release 15.0 will let you perform a single search to find anything you need.

We are also standardizing the command reference format for better navigation and organization of PCB product information.

The following documents have been added to SPECCTRA Release 15.0 product information:

- *SPECCTRA Command Reference*

  The SPECCTRA Command Reference is a comprehensive source of information for both menu and console commands in the Place and Route environments. Console commands are fully described using syntax diagrams and command examples. This book also serves as the content source for the context-sensitive online help providing dialog box descriptions and related procedures.

- *SPECCTRA User Guide*

  The SPECCTRA User Guide contains high-level procedural and conceptual information that is especially pertinent to the novice user. Introductory information regarding user interface usage, file management topics and work flow diagrams are also included.

- *PCB and IC Packaging Documentation Roadmap*

  This document describes a high-level overview of the PCB Systems design flow and directs you to appropriate documentation for each step in the flow. It also contains information about the documentation set by product, providing brief descriptions of each document.

The following document has been eliminated from the SPECCTRA Release 15.0 product information:

- *SPECCTRA Installation and Configuration Guide*

  Note: For information on installing and configuring SPECCTRA, you should now refer to the following documents.

  - *Cadence Installation Guide*

- *PCB and IC Packaging Software Requirements*

You can get information about your Cadence products in the following ways.

- Open the *Help* menu or click on product *Help* buttons
- Launch CDSDoc on Windows from the *Start* menu or on Unix by typing: `release/tools/bin/cdsdoc`
- Search SourceLink

Information You Need	**Where to Find it**
What is new in a release	What's New or Product Notes in CDSDoc or SourceLink
What is changed from one release to another	Migration Guide in CDSDoc or SourceLink
Answers to problems or bugs in a release	FAQs on SourceLink
Answers to frequently asked questions	FAQs on SourceLink
How to install Cadence tools	Installation Guide in CDSDoc or SourceLink
Platform and operating system requirements	Installation Guide in CDSDoc Installation area on SourceLink

Previous Releases

Chronology of the SPECCTRA 10.0 Releases

- Version 10.2 -- April 2002
- Version 10.1.1 -- September 2001
- Version 10.1 -- May 2001
- Version 10.0.2 -- April 2001
- Version 10.0 -- November 2000

What's New in Release 10.2

SPECCTRA version 10.2 contains the following enhancements:

- Mitering
- Allegro to SPECCTRA (SPIF) interface
- New do file behavior
- Propagation delay and elongation patterns
- Matched length
- Quality improvements

Mitering

The following improvements have been made to the miter feature:

- Mitering of differential pairs is more efficient. In prior versions, Miter would only miter to a minimum set back, which sometimes caused multiple jogs on long paths. With version 10.2, the system automatically determines when a single, longer miter can be used, resulting in much smoother, longer 45s.
- Recursive mitering has now been introduced. Up to and including version 10.1.1, Miter ran a single pass, only working on one net at a time, often failing to miter many 90s. The Miter function also did not re-miter any 45s, once they had already been mitered. To circumvent this deficiency, users would often create custom Do files that would run multiple miter passes with various setback parameters. Starting with version 10.2, Miter will automatically execute 4 passes, with each pass able to re-miter existing 45s to their

maximum. The results are significantly better with a reduced number of overall bends, whether 90 or 45, and longer, smoother 45s. This capability has also been extended to recognize nets coming out of pin fields such that Miter will, through re-mitering, eliminate unnecessary bends. This new capability will take longer than in prior releases. However, the overall results will be much better. We suggest that you try miter without your old multiple pass do files and compare the results.

Allegro to SPECCTRA (SPIF) interface

In response to requests from our power users for more flexibility and control with the Allegro/ SPECCTRA interface (aka SPIF), SPECCTRA version 10.2 with Allegro version 14.2 will now split the design information into three files:

- The ***[boardname]*.dsn** file is now trimmed down to contain only the basic information and general PCB rules.
- A ***[boardname]*_rules.do** file is now created which contains all of the design rules.
- A ***[boardname]*_forget.do** file is also created which contains forget statements for all of the rules in the *[boardname]*_rules.do file.

This new methodology has two main goals:

1. By splitting out the rules information into a separate Do file, power users can more easily create and manipulate this information to obtain an optimized strategy.
2. For the user who runs completely through Allegro, the separate Do file provides better optimized data for SPECCTRA. The data is optimized in three ways:
   - Redundant class and class-class rules within the hierarchy are eliminated.
   - Regions (generated from Allegro Constraint Areas) which are not necessary are removed.
   - Padstacks utilizing power and signal layer definitions are compressed.

   As a result, the load time for Do files is improved by optimizing the rule computations. Load times are also greatly improved due to the suppression of the display of .do file contents to the SPECCTRA output window.

This change will impact the user flow when using SPECCTRA through the Allegro UI in the following ways:

- *SPECCTRA – By Pick* will function no differently than in previous versions - the changes are transparent.

- *SPECCTRA – Route Automatic* will function no differently than in previous versions - the changes are transparent.
- *SPECCTRA – Interactive Editor* will invoke SPECCTRA as it has in previous versions, and will automatically load the corresponding *[boardname]*_rules.do file. This process should also be transparent and have no impact.
- *Export – SPECCTRA* will now output the three files as specified above. In the case when you invoke SPECCTRA independently, you now MUST load the file *[boadname]*_rules.do manually. Otherwise, your design will have only the default PCB rules specified. In this case, SPECCTRA will warn you at the time of invocation.

For more information, see the Allegro online manuals (specifically: *Allegro/APD Design Guide: Routing, Chapter 6 - Automatic Routing with SPECCTRA*).

New do file behavior

The **do** command no longer echoes each command in the SPECCTRA output window. This has been shown to significantly slow down the reading of a Do file on Windows operating systems. Errors and warnings, however, still show up in the output window. If you want to see the commands echoed, a new -vdo switch ("verbose" Do file) has been incorporated which will provide the same behavior as in prior releases.

Propagation delay and elongation patterns

Propagation delay and elongation patterns are now handled more efficiently and with greater user control over the process.

- A new GUI has been implemented for Elongation controls, allowing the user more control over the desired results. All four elongation patterns, Meander, Sawtooth, Accordion, and Trombone, can now be independently selected. Parameters for min and max amplitude, run length, and gap can be set.
- **Meander** elongation has now been implemented. Meander routing will not use any regular pattern, such as accordion or trombone to hit the target length. Instead, the router will add length by routing with a longer path, outside of the Manhattan area. Please experiment with this new functionality as it may effect convergence and "wrong-way" routing. It may best be used on isolated nets that are most susceptible to self-coupling.
- A new option has been added to create **Sawtooth** elongation patterns. In version 10.2, Sawtooth now accepts a Gap control which will result in a "flattened" top with a length specified by the Gap parameter.

In addition, quality improvements have been made such that gap, min and max amplitude, and run length (for trombone) are now enforced more strictly during routing.

See the SPECCTRA online Help system for more details.

Matched length

Throughout the 10.x releases, we have made continuous improvements to the Matched Length routing capabilities. With the completion of version 10.2, we anticipate that users should see more accurate routing patterns and better convergence on nets with matched length.

Quality improvements

As part of our Quality Initiative, we are committed to tracking and working on the user community's Top PCR's.

The following list shows just some of the PCRs that we have fixed in this release. These PCRs are in addition to those uncovered during normal testing and those related to major focus areas.

- 349729:

  accordion does not follow the setting rules

- 359790:

  SPECCTRA wont route to pinescapes

- 360856:

  Check takes 14X longer in v10 than v9

- 362128:

  miter causes length conflicts

- 362164:

  SPECCTRA reports unroutes on offset blind via in smd pad

- 362173:

  Miter not working as expected when net has length rule

- 362232:

edit_critic_wire creates length violations on mitered accordion

- 362649:

  Shield segment that cross region not written to session, wire

- 365059:

  How to setup miter to not leave small 90 bends

- 368032:

  Router puts thru via in pad against v10.1 default

- 369100:

  Timing rules change after route

- 376459:

  SPECCTRA routes differently when class has override value

- 376815:

  Unrts when end of protected preroute is on forbidden layer

- 382930:

  SPECCTRA produces unroutes on nets with non zero max stub

- 383512:

  Many Thru-vias in smd pads violate 10.1 default

- 383711:

  Filter removes differential pairs with 200+ priority

- 386772:

  Net with the ECL property are reported as unconnects

- 399790:

  Segmentation fault after copying tracks

- 401836:

  SPECCTRA fails to autoroute certain nets

- 408082:

  Matched length with Delta doesn't work with Autorouter

- 408228:

  SPECCTRA crashes after trying to edit `rules.do` in sp editor

What's New in Release 10.1.1

SPECCTRA version 10.1.1 contains the following enhancements:

- Miter Enhancements
- Matched length
- Propagation delay and elongation controls
- Quality improvements

This version is available only through our dedicated web site http://www.specctra.com.

This web site has been dedicated to our user community. The site demonstrates our commitment to sustaining SPECCTRA's world class status as the only autorouting environment that is able to handle today's most complex designs.

Miter Enhancements

With prior releases of SPECCTRA, Miter did not always produce results that were ideal for manufacturing. Also, Miter results would not always adhere to all constraints, especially electrical constraints such as differential pairs and length controlled nets. These mitering deficiencies could pose a significant delay in the cycle time of a board design if manual clean-up was required.

For this release of SPECCTRA 10.1.1, Miter has been significantly enhanced to produce far better diagonalization of traces in open areas, into pins and vias, and on traces with electrical constraints.

Specifically...

- Miter will now produce many more mitered 45 degree corners than in previous releases. This is the result of applying more intelligent methods to determine optimal setbacks from the corners.
- The miter function will now generate longer mitered connections to produce cleaner, more manufacturable routing patterns.

- Mitering produces improved 45 degree pin entries for both circular and rectangular pins, including SMD pins. For rectangular pins, miter will now create clean diagonals from the corner locations.
- Differential pairs are now fully recognized and mitered, adhering to all constraints. This is a significant improvement for high speed designs where differential pairs are widely used. The new algorithm will also adjust length accordingly to meet min, max, and matched length.
- Miter has been enhanced to adhere to both minimum and maximum length rules, to ensure that the length rules are not violated. Miter will automatically add length, if space is available, in cases where mitering reduced length below the minimum tolerance.
- Other enhancements were made to the general quality of mitering, based on customer feedback.

Matched length

The SPECCTRA algorithms for adding length to individual nets of a matched pair or group has been significantly enhanced with 10.1.1.

In the past, when SPECCTRA was required to follow a matched length rule, the lengths of the routes being matched would grow larger as more route passes ran. The main cause for this was that at some point, one of the routes being matched was put in with a length that was outside of the matched length tolerance. The router then attempted to meet this longest connection with every other net in the pair or group, resulting in the overall length growing. This was referred to as length creep.

In this release, SPECCTRA will not exhibit this problem. It will efficiently match the length to optimal length specifications.

Propagation delay and elongation controls

SPECCTRA now handles propagation delay and elongation patterns more efficiently, and users have greater control over how these processes work. In past releases, users did not have the appropriate controls to manage elongation and, as a result, were sometimes forced to use manual editing to clean up the routing.

- New elongation controls, min gap, min amplitude, max amplitude, and max run length, have been added to allow better control.

  Note: The new Meandor and Sawtooth patterns will be available in the upcoming 10.2 Release.

- The values for gap, and for minimum and maximum amplitude for Accordion and Trombone are now enforced more strictly during routing.

Quality improvements

At the 2000 CCT User's Group conference, we committed ourselves to making continuous quality improvements in SPECCTRA. As part of this initiative, we are committed to tracking and working on the user community's Top 25 PCRs.

The following list shows just some of the PCR's that we have fixed in this release. These PCRs are "in addition to" those uncovered during normal testing and those related to major focus areas.

- 365069:

  SPECCTRA aborts with system error during route pass 1

- 361112:

  Router crashes at start of fanout or route pass

- 366919:

  Some system variables change from integer to string type on Windows platform

- 360915:

  Buried via gap check broken in v9 and v10

- 365060:

  Net and Pin System Variables do not work in v8, v9, and v10

- 361314:

  Router does not follow ordered nets in some cases

- 376815:

  Unroutes when end of protected preroute is on forbidden layer

- 374243:

  SPECCTRA guides going to the wrong locations

- 351242:

  Documentation error for set `stub_viols_cost` command

- 388810:

Fanout creates redundant vias on BGA

- 361317:

  Can't turn off match_fromto in *Rules – group – timing* form

- 361321:

  Can't turn off matched or relative length/delay using GUI

- 365011:

  Length conflicts are not ignored when protected

- 377574:

  Need Length report to display selected nets/fromto rules

What's New in Release 10.1

SPECCTRA version 10.1 contains the following enhancements:

Differential pair routing

The default value for length_gap is now the wire-to-wire clearance instead of twice the wire width. Users still have the ability to modify this value.

What's New in Release 10.0.2

SPECCTRA version 10.0.2 contains the following enhancements:

- Differential pair routing
- Via control
- Performance improvements
- GUI improvements
- General routing
- Quality improvements
  - Differential pair improvements and fixes
  - Fanout improvements and fixes

- High Speed improvements & fixes
- Via in Pad improvements & fixes
- Miscellaneous improvements & fixes:

Differential pair routing

Differential pair routing has been significantly improved. With pair averaging OFF SPECCTRA will now adjust the length of each member of the differential pair independent of the other. Matched length constraints assigned to the pair are met. A preference is given to add the additional length along the segments between the pin and the gather point. However, the additional length may be added anywhere along the paired wire.

Via control

SPECCTRA now allows users to specify if thru vias may be used at SMD pads. The default setting is to NOT allow thru vias. This rule exists at the PCB rules hierarchy level. Users who wish to specify a specific via for use at SMD pads still have the attach via rule.

Performance improvements

- Performance improvements include better convergence rates and faster run times on designs with a significant number of differential pairs.
- Load times for design files are faster. This is very noticeable on large designs.

GUI improvements

The PCB Wiring Rules dialog box has been enhanced to provide controls for using vias at SMD pads.

General routing

Users will gain significant improvement in the areas of fanout, differential pairs, shielding, and high speed routing. Significant work has been done in these areas for this release.

Quality improvements

The ongoing "Quality Initiative" for SPECCTRA has resulted in many improvements and fixes for the 10.0.2 release. The list includes but is not limited to the following list of PCRs.

Differential pair improvements and fixes

- 31047, 32333, 360028 & 354955:

  Differential pairs with length constraints are not routing to correct length. "Gather points" need to be more intelligently established.

- 30224 & 360853:

  Fanout of differential pairs does not keep escapes for pair on same side of component pins.

- 30593:

  Setting pair averaging on results in length violations that do not resolve.

- 32890:

  Setting pair averaging off caused all pair length rules to fail.

- 34074:

  SPECCTRA cannot route differential pairs in a design that has staggered pins.

- 33359:

  The differential pair routing does not obey the "pad_to_turn_gap" spacing rule.

- 32070:

  Differential pairs were adopting the "class_class" gap instead of obeying the pair gap. The "class_class" rule was overriding the pair gap.

- 31685:

  Noexpose property on components causes differential pairs to break.

- 32295:

  With 'set dp_snap_to_grid 1' all differential pair 45's are off the wiring grid. Now when you 'set dp_snap_to_grid 1' the router will snap to the grid and maintain the pair gap as close as possible.

- 360022 & 360022:

  Wires that were not part of a differential pair were being affected by the "dp_snap_to_grid" setting.

- 28322:

  Filter does not work on differential pairs.

- 30225:

  Clean unroutes some differential pairs.

Fanout improvements and fixes

- 356051:

  Power fanout does not obey the "via_share" settings.

- 33004:

  Fanout is using the default via-test rule for via clearance instead of the via-via clearance.

- 33110:

  When using fanout with the "depth opposite" option, it created staggered via violations.

- 346942:

  When there is a via in pad rule on an SMD padstack fanout is not using a thru via to connect to the planes.

- 346929 & 346940:

  Fanout is using blind and microvias, which do not directly connect to the planes. The guides disappear until the fanout wires are read back into the design.

- 346938:

  Fanout puts in a redundant blind via when a thru via is the only selected via and the only via which makes a connection to the ground plane.

- 354950, 357754, 356399 & 359749:

  Fanout from existing vias produces unacceptable results. Multiple thru vias were being added when "fan extension" was allowed.

- 357712:

  When running fanout with "direction out" specified, the via grid value gets altered.

- 360859:

  Fanout is creating wire to track keepout errors.

High Speed improvements & fixes

- 30244:

SPECCTRA does not follow elongation keepout. Tromboning found in keepout.

- 32312:

  SPECCTRA is not converging where there is an elongation keepout under an IC. There is sufficient room for the routing.

- 359691, 352921, 357292, 359754, 34140 & 32327:

  Several problems related to virtual pins, complex T-point topologies and Virtual pins with only two guides attached to them.

- 26833:

  Router does not re-route when order violations exist.

Via in Pad improvements & fixes

- 347178 & 30800:

  Router creates many blind vias that hang off SMD pads and also violates via in pad rules by using thru vias under SMD pads. SPECCTRA was not placing via in pad due to an error in the interpretation of the rules hierarchy.

Miscellaneous improvements & fixes:

- 349893:

  Copy route reporting violation and not performing copy even though there was adequate space.

- 347857:

  SPECCTRA was crashing when issuing a report selected command with a power net selected.

- 29469:

  There is a mismatch in the number of order violations reported by "status Report" and "Check results transcript".

- 359410:

  SPECCTRA exhausts available memory while routing this design.

- 33594:

  Length report is issuing erroneous errors when pair averaging is on.

What's New in Release 10.0

SPECCTRA version 10.0 contains the following enhancements:

- Automatic Routing
- Edit Route
- Differential Pair Routing
- Interactive Routing
- Placement
- Timing Control
- Performance Improvements
- Usability Improvements
- GUI Improvements
- General Routing

Automatic Routing

Fanout now accommodates length restrictions by routing in the direction of the guide.

Edit Route

Same net checking is supported in Edit Route but not in move mode. Move mode checks notches only when moving a wire to a same net via. You can not push accordion shape wires. You can also turn on or turn off same net checking in the Interactive Routing Setup dialog box.

Differential Pair Routing

Since version 7.1, SPECCTRA has snapped the wires of a differential pair to grid, sometimes causing the separation between the two to be greater than the pair gap. This was especially noticeable after the wires were mitered. In SPECCTRA 10.0, the pair gap is again enforced at the expense of the wire grid. You can override the current default behavior, prefer gap over grid, with the following commands: set dp_snap_to_grid 1 and set dp_snap to grid 0. The set

dp_snap_to_grid 1 snaps to the grid at the expense of the pair gap. The set dp_snap_to grid 0 is the default.

Interactive Routing

You can now access change connectivity mode through the Interactive Routing Menu or the Polygon Editing Menu.

Placement

You can replace the outline of an existing room keeping the same room name. Replacing the outline preserves any rules defined for the room.

Timing Control

The circuit command now includes relative timing rules.

- The relative_delay and relative_length rules constrain the delays and lengths of fromtos in a group relative to the length or delay of a reference fromto.
- The relative_group delay and relative_group_length rules constrain the delays and lengths of groups in a group_set relative to the length or delay of a reference group.

Performance Improvements

- The bus command is enhanced to create a slant bus when pins are slightly offset.
- A user-selectable option allows you to improve routing performance around staggered pins in some designs.
- The autorouter now routes from protected pre-routes.
- General improvement to the smart_route command produces better routing results in designs.

Usability Improvements

- Querying about a design object now shows more detailed information in a Measure dialog box.
- You can now interactively set all grids from a single dialog box by using View - Display Grids.

- The traffic light indicator was removed.
- The graphical ruler now displays a tick mark for each starting point and a distance number for each ending point.

GUI Improvements

- Menu and dialog box enhancements
  - Simplified Interactive Routing Setup dialog box that now includes General, Measure, Bus, Style, and Move/Copy options.
  - Simplified Placement Setup dialog box that now includes General, Alignment, Move/Measure options.
  - *View – Visit* provides greater usability and more information about visited objects and conditions.
  - A measure dialog box which opens when you click or drag the pointer in the work area.
- Display improvements
  - The highlight command highlights nets by class.
  - The layers panel now groups layers by function.

General Routing

- You can now specify the layer on which the smd_escape control applies in the change command.
- You can now select and unselect components attached to specified nets using on_nets.