Analysis of SiC Technology in Two-Level and Three-Level Converters for Aerospace Applications

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Abstract

There is a growing need for highly efficient, power dense DC-AC converters to supporta number of futuremore electric aircraft technologies. SiC has been identified as a potentialtechnology to improve the efficiency of these converters.To analyse the semiconductorlosses, this paper presents the semiconductor loss equations for the two-level converter (2LC), three-level neutral point clamped converter (3LNPCC) and the three-level T-Type converter (3LTTC).Based on the equations and current datasheet information,it is identified that SiC technology offers significant reductions in losses compared with traditional Si devices. The paper also discussesa number of hybrid device combinations to achieve the benefits of high efficiency in SiC technology and low cost of Si technology.Based on the semiconductor losses the converter efficiencies in the SiC 2LC and the 3LTTCs are about3-4%higher than in the Si 2LC for a 42 kW threephase converter operating at a 25 kHz switching frequency.

1 Introduction

The concept of electrifying auxiliary systems on-board an aircraft that were previously powered through mechanical, hydraulic and pneumatic means is known as the more electric aircraft (MEA) concept. Some of the key benefits ofthe MEA concept include improving fuel efficiency and reducing the maintenance costs[1].As a result of this technology change, a number of new electrical power system architectures are being developed including AC and DC sub-systems which require a range of power electronic converters to form the interconnections[1, 2].

DC-AC converters are likely to perform many of the power conversion functions in a MEA power system, such as engine starting and active rectification functions in the generator converters, control of high speed pumps and flight control actuators, and synthesizing an AC electrical system for the hotel and auxiliary loads. Thereforethere is a growing need for high efficiency DC-AC converters capable of operating at powers in the kWsrangeand at fundamental frequencies of400 Hz and above [1, 2].High efficiency is essential to minimize the size of the converter and reduce fuel burn.

New SiC devices offer lower on state and switching losses compared with traditional Si devices[3]and are therefore a candidate technology for future high performance converters. The three-level T-Type converter (3LTTC) and the three-level neutral point clamped converter (3LNPCC) have been reported to offer efficiency gains of 1-2% over the two-level converter (2LC) with Si devices [4]. Therefore this paper seeks to examine the performance of the 2LC, 3LNPCC andthe 3LTTC when using SiC technology for typical MEA applications.Initially, analytical equations to estimate the semiconductor losses in the converters are described. Then based on the loss equations, converters are analysed at a range of power levels and switching frequencies that would be required on-board an aircraft. The analysis is first performed for converters with Si devices and then with SiC devices and finally combinations of Si and SiC devices.

2 DC-AC Converter Topologies

Figure 1shows the converter legs of the topologies considered in this study. The complete converters will have three legs for a three phase converter and a greater number for multiphase systems.
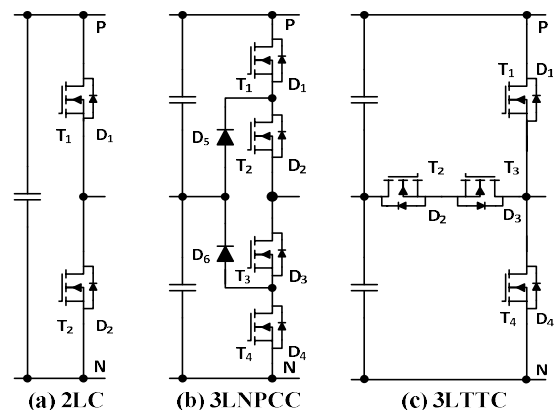

Figure 1: Converter legs of topologies analysed in this paper

3 Analytical Loss Model

The analysis focuses on the semiconductor losses and excludes any passive component losses such as in the DC link capacitors and any filter inductors. Hard switching is assumed and only conduction and switching semiconductor losses have been considered sincegate drive losses are comparably small in IGBT and MOSFET devices.Sinusoidal PWM (SPWM)is assumed due to its simplicity and also due to the absence of a common mode output voltage component, which enables the

neutral of the output to be grounded, a requirement in some MEA systems architectures[5].

The analysis of semiconductor losses is explained generally for the transistor and diode pair T_1 and D_2 in the 2LC of Figure 1 and the general results are then adapted for other topologies. Figure 2 presents the key waveforms for the 2LC where a low switching frequency to fundamental frequency ratio is assumed for clarity. The PWM voltage of the converter leg, V_{PWM} in Figure 2b is generated by SPWM, comparing the modulating waveform, $m(\theta)$ with the carrier signal, V_{tri} in Figure 2a. The line current I_L, and the currents in T_1 and D_2 are shown in Figure 2b, 2c and 2d. φ is the angle of the current with respect to the fundamental PWM voltage and t_1 is the conduction time of T_1 in each switching period.
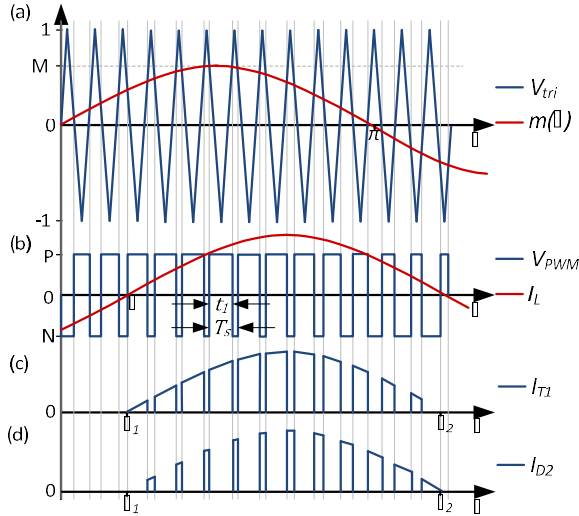

Figure 2: Key waveforms in the 2LC

3.1 Conduction Losses

The conduction losses $P_{c,sc}$ in T_1 averaged across a switching cycle may be approximated by eqn.(1).

$$P_{c,sc}(\theta) = \left(v_o + r_o \hat{I}_L \sin(\theta - \varphi)\right)\left(\hat{I}_L \sin(\theta - \varphi)\right)\alpha(\theta) \quad (1)$$

where v_o and r_o are the initial device voltage drop and incremental resistance respectively, $\hat{I}_L$ is the amplitude of the line current, θ is the angle of the line current and $\alpha(\theta)$ is the device duty ratio function defined for transistor T_1 as,

$$\alpha(\theta) = \frac{t_1(\theta)}{T_s} \quad (2)$$

where T_S is the switching period. The average transistor conduction losses P_c in eqn. (3) are then obtained by integrating eqn.(1) across the positive half-cycle of the line current waveform.

$$P_c = \frac{1}{2\pi} \int_{\theta_1}^{\theta_2} P_{c,sc}(\theta)\, d\theta \quad (3)$$

3.2 Switching Losses

The device switching losses are obtained using the datasheet values for turn on and turn off energy losses and assuming they may be scaled linearly according to the actual device

voltage and current[3]. The switching energy loss per switching period in T_1 may therefore be written as $E_{s-T1}(\theta)$.

$$E_{s-T1}(\theta) = \left(E_{on} + E_{off}\right)\left(\frac{\hat{I}_L \sin(\theta - \varphi)}{I_{ref}}\right)\left(\frac{V_{sw}}{V_{ref}}\right) \quad (4)$$

where E_{on} and E_{off} are the datasheet transistor turn on and turn off energy losses at current and voltage levels I_{ref} and V_{ref} respectively. V_{sw} is the actual transistor off state voltage in the circuit under consideration. In a similar way the reverse recovery energy $E_{s-D2}(\theta)$ in diode D_2 may be expressed as,

$$E_{s-D2}(\theta) = E_{rr}\left(\frac{\hat{I}_L \sin(\theta - \varphi)}{I_{ref}}\right)\left(\frac{V_{sw}}{V_{ref}}\right) \quad (5)$$

where E_{rr} is the datasheet energy loss under conditions of I_{ref} and V_{ref}. The average power dissipation is obtained by integrating eqns. (4) and (5) across the positive half-cycle of the line current waveform and multiplying by the switching frequency giving,

$$P_{s-T1} = \frac{f_s}{2\pi} \int_{\theta_1}^{\theta_2} \left(E_{on} + E_{off}\right)\left(\frac{\hat{I}_L \sin(\theta - \varphi)}{I_{ref}}\right)\left(\frac{V_{sw}}{V_{ref}}\right) d\theta \quad (6)$$

$$P_{s-D2} = \frac{f_s}{2\pi} \int_{\theta_1}^{\theta_2} E_{rr}\left(\frac{\hat{I}_L \sin(\theta - \varphi)}{I_{ref}}\right)\left(\frac{V_{sw}}{V_{ref}}\right) d\theta \quad (7)$$

3.3 Derivation of $\alpha(\theta)$ and Device Losses

The transistor duty ratio function $\alpha(\theta)$ for the 2LC topology is determined by the naturally sampled SPWM modulation function depicted in Figure 2, which shows the triangular carrier waveform and the sinusoidal modulating waveform $m(\theta) = M\sin(\theta)$. The current in the conducting devices T_1 and D_2 are shown in Figures 2c and 2d, assuming current is flowing out of the leg. By assuming that $m(\theta)$ is constant within a switching cycle, from the geometry of Figure 2a expressions may be written down for the duty-ratio functions of devices T_1 and D_2 as shown in Table 1. Similar expressions may be written down for devices T_2 and D_1 by considering the negative half cycle of the output current, however due to symmetry the total converter losses may be obtained by doubling the result from the positive half cycle of the current.

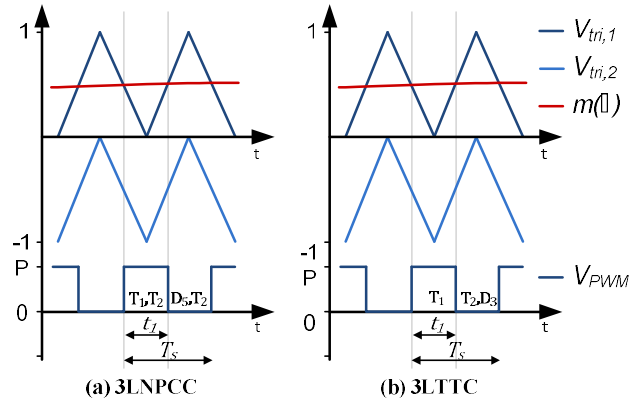
(a) 3LNPCC   (b) 3LTTC

Figure 3: Calculation of duty ratio function, $\alpha(\theta)$ for the 3LCs

Phase disposition SPWM [6] is used to generate the switching signals in both the 3LNPCC and the 3LTTC as illustrated in

Figures 3a and 3b.The conducting devices during each period are shown on the PWM waveform.

Table 1: Duty ratio function, α(θ) for the 2LC

Device	T_1	D_2
$\boldsymbol{\theta_1}$ **to** $\boldsymbol{\theta_2}$ $\boldsymbol{\alpha(\theta)}$	φ to $\pi+\varphi$ $[1+m(\theta)]/2$	φ to $\pi+\varphi$ $[1-m(\theta)]/2$

Table 2: Duty ratio function, $\alpha(\theta)$ for the 3LTTC

Device	T_1	D_4	T_2 and D_3	
$\boldsymbol{\theta_1}$ **to** $\boldsymbol{\theta_2}$ $\boldsymbol{\alpha(\theta)}$	φ to π $m(\theta)$	π to $\pi+\varphi$ $-m(\theta)$	φ toπ $1-m(\theta)$	π to$\pi+\varphi$ $1+m(\theta)$

Table 3: Duty ratio function, $\alpha(\theta)$ for the 3LNPCC

Device	T_1	T_2		D_5		D_3	D_4
$\boldsymbol{\theta_1}$ **to** $\boldsymbol{\theta_2}$ $\boldsymbol{\alpha(\theta)}$	φ to π $m(\theta)$	φ to π 1	π to $\pi+\varphi$ $1+m(\theta)$	φ to π $1-m(\theta)$	π to $\pi+\varphi$ $1+m(\theta)$	π to$\pi+\varphi$ $-m(\theta)$	π to$\pi+\varphi$ $-m(\theta)$

For the 3LNPCC in Figure 3a where I_L is assumed to be flowing out of the leg, transistors T_1 and T_2 are conducting when the modulating function $m(\theta)$ is greater than the upper carrier signal $V_{tri,1}$, whilst D_5 and T_2 are conducting when $m(\theta)$ is greater than $V_{tri,2}$ but less than $V_{tri,1}$.Though not shown in Figure 3a, when $V_{PWM} = N$ and $I_L > 0$ D_3 and D_4 will conduct. The resulting duty ratio functions for the positive half cycle of current I_L are shown in Table 3.

Figure 3b shows the conducting devices in the 3LTTC for the same conditions. T_1 conducts when $m(\theta) > V_{tri,1}$, and T_2 and D_3 conduct when $m(\theta)$ is greater than $V_{tri,2}$ but less than $V_{tri,1}$. When $V_{PWM} = N$ and $I_L > 0$, D_4 will conduct. Table 2 lists the resulting duty ratio functions for the positive half cycle of current I_L.

By substituting the duty ratio functions and conduction angles θ_1, θ_2 in Table 1-3 in to the general loss eqns. (3), (6) and (7) for each device the average loss equations for the 2LC, 3LNPCC and 3LTTC may be derived as given in Table A1 [7, 8] in the Appendix A.

4 Device Selection

A typical MEA DC-AC converter specification is assumed for device selection, $V_{dc} = \pm 270$ V, $V_{ac} = 115$ V line-neutral, 400 Hz, three phase, 0.85 power factor load and ajunction temperature (T_j) of 125°C. Assuming the devices are operated at around 50 % of their voltage rating, the 2LC and the 3LNPCC require 1200 V and 600 V devices respectively, whereas the 3LTTC requires 1200 V devices for T_1 and T_4 and 600 V devices for T_2 and T_3. Devices with continuous current ratings in the range of 250-300 A were selected for each of the three topologies as listed in Table 4. In each case all Si and all SiC modules were selected, with trench gate and field stop IGBTs being used in the Si modules and MOSFETs in the SiC modules.

In addition hybrid module options were also selected for each topology. SiC anti parallel diodes and Si IGBTs are used in the 2LC hybrid module, whilst in the 3LNPCC all Si devices are used with the exception of the neutral point clamping diodes which are SiC. Two hybrid options are selected for the 3LTTC, SiC devices are used in the phase leg (T_1, T_4, D_1 and D_4) and Si IGBTs in the neutral leg (T_2 and T_3), in the first hybrid option Si diodes are used for D_2 and D_3 whilst in the second hybrid option D_2 and D_3 are SiC components.

The selected modules allow at least 42 kW to be delivered by each converter, with output powers of up to 60 kW being achieved in most of the configurations as discussed in the following section.

Table 4: Proposed device combinations with $I_{rating-T}$ and $I_{rating-D}$ calculated at $T_j = 150$°C and $T_{case} = 25$°C.

Topology	Device Selection	Device Name	Manufacturer	V_{rating}(V)	$I_{rating-T}$ (A)	$I_{rating-D}$ (A)
2LC - Si	T_{1-2} - Si , D_{1-2} - Si	SKM200GB12T4	Semicron	1200	295	210
2LC - Hybrid	T_{1-2} - Si , D_{1-2} - SiC	GA100XCP12-227	GeneSiC	1200	200	85
2LC - SiC	T_{1-2} - SiC , D_{1-2} - SiC	APTMC120AM08CD3AG	Microsemi	1200	275	205
3LNPCC - Si	T_{1-4} - Si , D_{1-4} - Si	APTGT200TL60G	Microsemi	600	270	165
	D_{5-6} - Si	Part of Module	Microsemi	600	-	212
3LNPCC - Hybrid	T_{1-4} - Si , D_{1-4} - Si	APTGT200A60T3AG	Microsemi	600	290	230
	D_{5-6} - SiC	APTDC902U601G	Microsemi	600	-	160
3LNPCC - SiC	T_{1-4} - SiC , D_{1-4} - SiC	APTMC120AM08CD3AG	Microsemi	1200	275	210
	D_{5-6} - SiC	APTDC902U601G	Microsemi	1200	-	160
3LTTC - Si	$T_{1\&4}$ - Si , $D_{1\&4}$ - Si	SKM200GB12T4	Semicron	1200	295	210
	$T_{2\&3}$ - Si , $D_{2\&3}$ - Si	APTGT200A60T3AG	Microsemi	600	290	230
3LTTC - Hybrid 1	$T_{1\&4}$ - SiC , $D_{1\&4}$ - SiC	APTMC120AM08CD3AG	Microsemi	1200	275	210
	$T_{2\&3}$ -Si , $D_{2\&3}$ - Si	APTGT200A60T3AG	Microsemi	600	290	230
3LTTC- Hybrid 2	$T_{1\&4}$ - SiC , $D_{1\&4}$ - SiC	APTMC120AM08CD3AG	Microsemi	1200	275	210
	$T_{2\&3}$ - Si	APT150GN60B2	Microsemi	600	215	-
	$D_{2\&3}$ - SiC	APTDC902U601G	Microsemi	600	-	160
3LTTC - SiC	$T_{1\&4}$ - SiC , $D_{1\&4}$ - SiC	APTMC120AM08CD3AG	Microsemi	1200	275	210
	$T_{2\&3}$ - SiC , $D_{2\&3}$ - SiC	APTMC120AM08CD3AG	Microsemi	1200	275	210

5 Converter Efficiency Analysis

This section analyses the efficiency of the three converters in Figure 1, based solely on the semiconductor losses using the device selection listed in Table 4for identical specifications as listed in Section 4. The efficiency is calculated using the equations in Table A1of Appendix A for two operating conditions, with the first being at a fixed power of 42 kW and at different switching frequencies, the second being at different power levels and at a fixed 25 kHz switching frequency.This forms the basis for understanding the semiconductor losses ata range of power levels and switching frequencies required for applications on-board a MEA.Figures 4to11 illustrate the converterefficiency obtained for the three topologies at different power levels and switching frequencies. The extremities of the lines in all figures indicate the thermal limits of the differentsystems assuming a case temperature of 70°C.
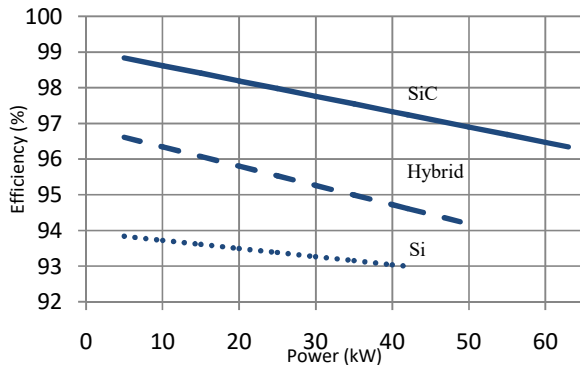
Figure 4: Efficiency vs power for 2LC (f$_s$ = 25 kHz)
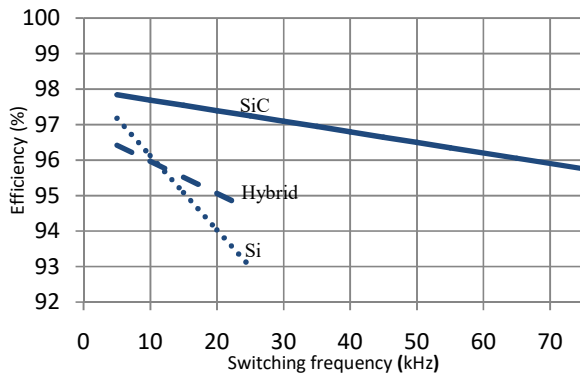
Figure 5: Efficiency vs switching frequency for 2LC (P = 42 kW)

The results for the Si-2LC, Figures 4and5, show the lowest efficiency at all power levels with a switching frequency of 25 kHz, however at low switching frequencies below 12 kHz, the Si converter performs better than the hybrid option. This is due to the high switching losses in the1200 V Si IGBTsand diodes. The hybrid-2LCimproves the efficiency by replacing the Si diodes with SiC diodes. The very low reverse recovery effects in SiC diodes result in lower switching losses, which is particularly evident at high switching frequencies. At low switching frequencies the hybrid option has lower efficiency due to the increased on state voltage in SiC diodes. A greater

loss reduction is seen in the all SiC-2LC as the SiC MOSFETs have a lower on state voltage and very low switching losses. Due to these reasons, the SiC-2LC shows the highest efficiency in Figures 4 and 5. For example in Figure 4, at 42 kW the SiC-2LC has a 97.3 % efficiency, a significant increase compared to the other two level options. Furthermore the performance advantage of the all SiC converter is greater at high switching frequencies.The performance advantage of the SiC option is slightly exaggerated in these results since the SiC modules are over rated for the nominal 42 kW specification. This was due to the limited number of high power SiC modules currently offered by manufacturers. Nevertheless a lower rated SiC module would still offer a significant performance improvement over Si technology.
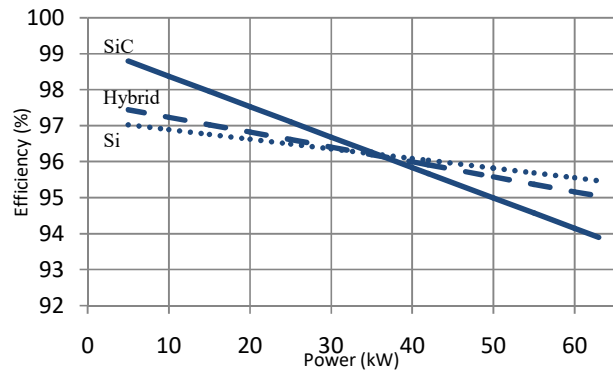

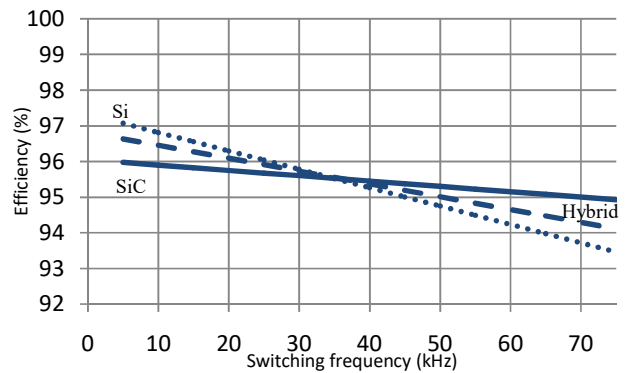Figure 6: Efficiency vs power for 3LNPCC (f$_s$ = 25 kHz)

Figure 7: Efficiency vs switchingfrequency for 3LNPCC (P = 42 kW)

A similar pattern is seen in the results for the 3LNPCC, Figures 6 and 7, however the Si and hybrid options show higher efficiency than the two level designs due to the use of 600 V IGBTs and diodes, which have lower on-state and switching losses than 1200 V devices. Due to the limited availability of 600 V SiC devices, 1200 V components were used in the SiC 3LNPCC circuit. As a result, at power levels greater than 36 kW with 25 kHz switching frequency the Si 3LNPCC has the highest efficiency, however the SiC converter has the best performance at very high switching frequencies.
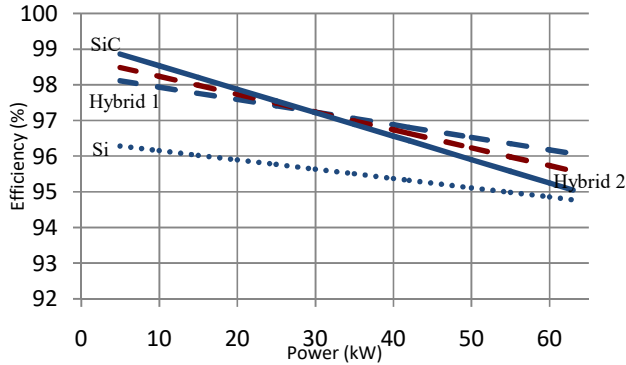
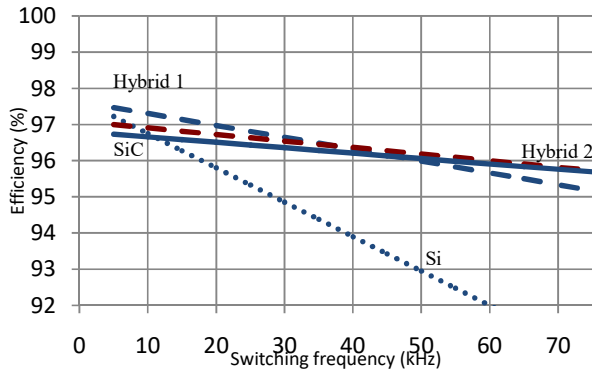Figure 8: Efficiency vs power for 3LTTC (f_s = 25 kHz)

Figure 9: Efficiency vs switchingfrequency for 3LTTC (P = 42 kW)

As shown in Figures 8 and 9, the SiC-3LTTC shows a significant efficiency improvement over the Si-3LTTC at all power levels with a switching frequency of 25 kHz.At switching frequencies below 12 kHz and at 42 kW power throughput the Si system has a higher efficiency than the SiC design. The hybrid options which use SiC devices in the main phase leg and 600 V Si IGBTs in the neutral leg have similar performance to the all SiC design, but have higher efficiency above 32kW with a 25 kHz switching frequency. This is due to the lower conduction losses in the 600 V Si devices in the neutral leg.

The hybrid-2 option differs from the hybrid-1 option in that SiC diodes are used in the neutral leg, as a result the hybrid-2 option has a slightly lower efficiency at high power and 25 kHz switchingfrequency, but a higher efficiency for very high switching frequencies and at 42 kW throughput.
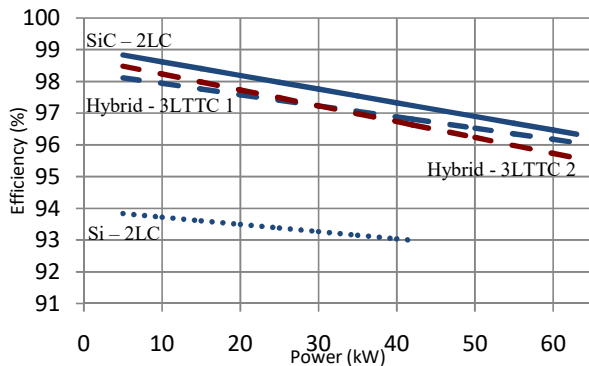

Figure 10: Efficiency vs power (f_s = 25 kHz)

Figures 10 and 11 show a comparison between the hybrid 3LTTC options and the two-level all Si and all SiC designs. The all SiC 3LTTC option is not shown as its component cost is likely to be higher but it doesn't offer an obvious performance benefit. Compared with the Si 2LC, the SiC 2LC and the hybrid 3LTTCs show a substantial performance improvement over a wide operating range. However, the SiC 2LC has the highest efficiency figure amongst the options considered in this study.
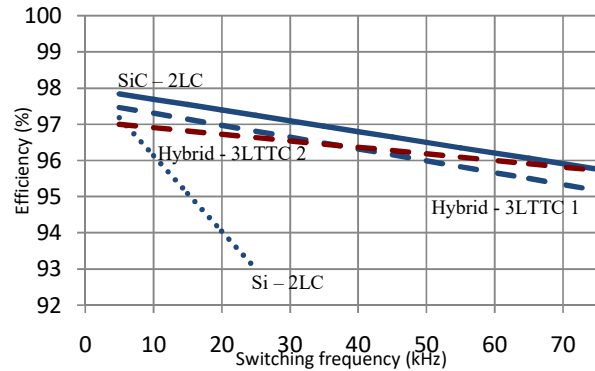

Figure 11: Efficiency vs switchingfrequency (P = 42 kW)

6 Conclusion

Among the proposeddevice combinations, the SiC-2LC has the lowest semiconductor losses for the power levels and switching frequencies considered in the study. The SiC and hybrid 3LTTCs also offer significant improvements in efficiency when compared with a Si 3LTTC and also a Si 2LC. The choice of the 3LTTC is likely to depend on the power level and the switching frequency of the specific application. But the performance gain must be traded against the increased complexity and cost, and in this regard the hybrid options may be an attractive compromise.

Further work is needed to analyse the passive component requirements and associated losses in the converter. The three level topologies are likely to have reduced filter requirements when compared with two-level circuits, which may result in a narrowing of the efficiency difference between the converters.

This study has also indicated a role for lower loss 600 V devices in multi-level topologies, for example a 600 V SiC MOSFET or GaN device may offer improvements in the efficiency of the three-level topologies that have been examined.

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Appendix A

Table A1: Device losses in the 2LC, 3LNPCC and the 3LTTC

Conduction Losses - 2LC[7]

$$P_{c-T1,T2} = \frac{v_{o,T}\hat{I}_L}{2\pi}\left[1 + \frac{M\pi}{4}\cos(\varphi)\right] + \frac{r_{o,T}\hat{I}_L^2}{2\pi}\left[\frac{\pi}{4} + \frac{2M}{3}\cos(\varphi)\right]$$

$$P_{c-D1,D2} = \frac{v_{o,D}\hat{I}_L}{2\pi}\left[1 - \frac{M\pi}{4}\cos(\varphi)\right] + \frac{r_{o,D}\hat{I}_L^2}{2\pi}\left[\frac{\pi}{4} - \frac{2M}{3}\cos(\varphi)\right]$$

Switching Losses - 2LC[7]

$$P_{s-T1,T2} = \frac{f_s}{\pi}\left(E_{on} + E_{off}\right)\left(\frac{V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{ref}}\right)$$

$$P_{s-D1,D2} = \frac{f_s}{\pi}E_{rr}\left(\frac{V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{ref}}\right)$$

Conduction Losses - 3LNPCC[7]

$$P_{c-T1,T4} = \frac{v_{o,T}M\hat{I}_L}{4\pi}[\sin(\varphi) + (\pi - \varphi)\cos(\varphi)] + \frac{r_{o,T}M\hat{I}_L^2}{4\pi}\left[\frac{8}{3}\cos^4\left(\frac{\varphi}{2}\right)\right]$$

$$P_{c-D1,D4} = \frac{v_{o,D}M\hat{I}_L}{4\pi}[\sin(\varphi) - \varphi\cos(\varphi)] + \frac{r_{o,D}M\hat{I}_L^2}{2}\left[\frac{4}{3\pi}\sin^4\left(\frac{\varphi}{2}\right)\right]$$

$$P_{c-T2,T3} = \frac{v_{o,T}\hat{I}_L}{\pi}\left[1 - \frac{M}{4}(\sin(\varphi) - \varphi\cos(\varphi))\right] + \frac{r_{o,T}\hat{I}_L^2}{4}\left[1 - \frac{8M}{3\pi}\sin^4\left(\frac{\varphi}{2}\right)\right]$$

$$P_{c-D2,D3} = \frac{v_{o,D}M\hat{I}_L}{4\pi}[\sin(\varphi) - \varphi\cos(\varphi)] + \frac{r_{o,D}M\hat{I}_L^2}{2}\left[\frac{4}{3\pi}\sin^4\left(\frac{\varphi}{2}\right)\right]$$

$$P_{c-D5,D6} = \frac{v_{o,D}\hat{I}_L}{\pi}\left[1 - \frac{M}{4}(2\sin(\varphi) - (2\varphi - \pi)\cos(\varphi))\right] + \frac{r_{o,D}\hat{I}_L^2}{4}\left[1 - \frac{4M}{3\pi}(1 + \cos^2(\varphi))\right]$$

Switching Losses - 3LNPCC[7]

$$P_{s-T1,T4} = f_s\left(E_{on} + E_{off}\right)\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{ref}}\right)\left(\frac{1 + \cos(\varphi)}{2\pi}\right)$$

$$P_{s-D1,D4} = f_s E_{rr}\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{mes}}\right)\left(\frac{1 - \cos(\varphi)}{2\pi}\right)$$

$$P_{s-T2,T3} = f_s\left(E_{on} + E_{off}\right)\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{ref}}\right)\left(\frac{1 - \cos(\varphi)}{2\pi}\right)$$

$$P_{s-D2,D3} = 0$$

$$P_{s-D5,D6} = f_s E_{rr}\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{ref}}\right)\left(\frac{1 + \cos(\varphi)}{2\pi}\right)$$

Conduction Losses - 3LTTC[8]

$$P_{c-T1,T4} = \frac{v_{o,T}M\hat{I}_L}{4\pi}[\sin(\varphi) + (\pi - \varphi)\cos(\varphi)] + \frac{r_{o,T}M\hat{I}_L^2}{4\pi}\left[\frac{8}{3}\cos^4\left(\frac{\varphi}{2}\right)\right]$$

$$P_{c-D1,D4} = \frac{v_{o,D}M\hat{I}_L}{4\pi}[\sin(\varphi) - \varphi\cos(\varphi)] + \frac{r_{o,D}M\hat{I}_L^2}{2}\left[\frac{4}{3\pi}\sin^4\left(\frac{\varphi}{2}\right)\right]$$

$$P_{c-T2,T3} = \frac{v_{o,T}\hat{I}_L}{\pi}\left[1 - \frac{M}{4}(2\sin(\varphi) - (2\varphi - \pi)\cos(\varphi))\right] + \frac{r_{o,T}\hat{I}_L^2}{4}\left[1 - \frac{4M}{3\pi}(1 + \cos^2(\varphi))\right]$$

$$P_{c-D2,D3} = \frac{v_{o,D}\hat{I}_L}{\pi}\left[1 - \frac{M}{4}(2\sin(\varphi) - (2\varphi - \pi)\cos(\varphi))\right] + \frac{r_{o,D}\hat{I}_L^2}{4}\left[1 - \frac{4M}{3\pi}(1 + \cos^2(\varphi))\right]$$

Switching Losses - 3LTTC[8]

$$P_{s-T1,T4} = f_s\left(E_{on} + E_{off}\right)\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{ref}}\right)\left(\frac{1 + \cos(\varphi)}{2\pi}\right)$$

$$P_{s-D1,D4} = f_s E_{rr}\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{ref}}\right)\left(\frac{1 - \cos(\varphi)}{2\pi}\right)$$

$$P_{s-T2,T3} = f_s\left(E_{on} + E_{off}\right)\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{ref}}\right)\left(\frac{1 - \cos(\varphi)}{2\pi}\right)$$

$$P_{s-D2,D3} = f_s E_{rr}\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}_L}{I_{ref}}\right)\left(\frac{1 + \cos(\varphi)}{2\pi}\right)$$