# Carnegie Institute of Technology

## COMPUTATION CENTER

ATHENA

# REFERENCE GUIDE

# ATHENA

# USERS MANUAL

PUBLISHED ON OCTOBER 22,1968

BY

PS08
JP40
JY08
GS33
CP05

VERSION I

# SECTION XI
# COMPUTER SET CONSOLE, OA-2654/GSK-1

11-1. GENERAL.

11-2. The Computer Set Console, OA-2654/GSK-1 (computer console) switch and indicator panels are shown in figure 11-1. The console is only operable when the computer set is in the Maintenance or Hold Maintenance condition. The lower panel contains the operational pushbuttons and operation-indicator lamps, while the upper panel contains the flip-flop indicator lamps, and/or manual set pushbuttons and manual clear pushbuttons. The flip-flop indicator lamps themselves are the manual set pushbuttons. That is, to manually set a given flip-flop, the indicator lamp bulb of that flip-flop is depressed. The operational pushbuttons and operation-indicator lamps on the lower panel are as follows (read in order from left to right):

TOP ROW

a. DRUM TEST CLOCK, S129, figure 1-27, T.O. 21-SM68-2D-6-1: Permits the selection of either CP0 or CP1 pulses. (Amber)

b. CLOCK PULSE 0, S128, figure 1-27, T.O. 21-SM68-2D-6-1: Causes only CP0 pulses to be issued. (Used in conjunction with DRUM TEST CLOCK.) (White)

c. CLOCK PULSE 1, S127, figure 1-27, T.O. 21-SM68-2D-6-1: Causes only CP1 pulses to be issued. (Used in conjunction with DRUM TEST CLOCK.) (White)

d. DOOR OPEN ROW 1, DS126, figure 1-65, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates a door open condition in row 1 of the computer. (Red)

e. DOOR OPEN ROW 2, DS125, figure 1-65, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates a door open condition in row 2 of the computer. (Red)

f. DOOR OPEN ROW 3, DS124, figure 1-65, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates a door open condition in row 3 of the computer. (Red)

g. HIGH TEMP TAPE, DS123, figure 1-65, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates a condition of high temperature in the perforated tape reader assembly. (Red)

h. HIGH TEMP POWER, DS122, figure 1-65, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates a condition of high temperature in the power supply section. (Red)

i. HIGH TEMP DRUM, DS121, figure 1-65, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates a condition of high temperature in the magnetic drum storage unit. (Red)

j. AIR FAULT, DS120, figure 1-65, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates improper air flow in the power supply section. (Red)

k. POWER SUPPLY FAULT, DS119, figure 1-65, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates that conditions are not correct in the power supply section. (Red)

l. SYNC FAULT, DS118, figure 1-4, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates the reception of an abnormal sync pulse, which is a partial or cycle sync pulse timing fault. (Red)

m. COMP FAULT, S117, figures 1-13 and 1-19, T.O. 21-SM68-2D-6-1: Indicator lamp and manual clear pushbutton which indicates a computer fault condition (i.e., Arithmetic Overflow, Invalid instruction, Tape Reader fault). The pushbutton will clear this condition. (Red)

n. TARGET-REF and 1 through 10, S116 through S106, figure 1-34, T.O. 21-SM68-2D-6-1: Indicator lamps and pushbuttons which select a given drum group sector in the magnetic drum storage section which is then referenced during a program by a coefficient jump instruction. During guidance operations, target trajectory constants are stored in those drum group sectors corresponding to the target pushbuttons labeled 1 through 10. The drum group sector corresponding to the TARGET REF pushbutton is normally loaded with "reference target" constants. These constants correspond to an imaginary target which is used during guidance simulation operations when the computer and radar equipment are checked for proper operation. (All indicators white.)

o. DISTR PULSE RATE, S105, figure 1-1, T.O. 21-SM68-2D-6-1: Indicator and pushbutton which selects the "pulse" rate of operation. At this rate one main pulse at a time is issued. (White)

p. DISTR CYCLE RATE, S104, figure 1-1, T.O. 21-SM68-2D-6-1: Indicator and pushbutton which selects the "cycle" rate of operation. At this rate one group of main pulses (MP0 through MP7) is issued at a time. (White)

q. NORMAL RATE, S103, figure 1-1, T.O. 21-SM68-2D-6-1: Indicator and pushbutton which selects the normal rate of operation. At this rate successive main cycles are continuously issued. (Green)

r. MAINT, DS102, figure 1-15, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates that the computer is in the Maintenance condition. (White)

s. STANDBY, DS101, figure 1-15, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates that the computer is in the Standby condition. (Green)

MIDDLE ROW

a. MARGINAL CHECK, DS146, figure 1-15, T.O. 21-SM68-2D-6-1: Indicator lamp which indicates that one of the rotary switches positioned beneath this indicator is at other than its NORMAL position and thereby introducing marginal conditions into certain circuits. (Amber)

b. INHIBIT-ADVANCE PAR, S145, figure 1-25, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which inhibits the advancement of the program address register (PAR). (Amber)

c. INHIBIT-DTR TO PCR, S144, figure 1-5, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which inhibits the transfer of an instruction word from the drum transfer register (DTR) to the program control register (PCR). (Amber)

d. INHIBIT-DRUM WRITE, S143, figure 1-1 and 1-15, T.O. 21-SM68-2D-6-1: Indicator and pushbutton which removes the voltage of the magnetic drum write amplifiers and thereby inhibits any drum writing operation. (Amber)

e. INHIBIT-TAPE REVERSE, S142, figure 1-21, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which, when a VERIFY operation is initiated, inhibits the tape from starting forward once it has reversed itself to the starting position. (Amber)

f. INHIBIT-COMP FAULT STOP, S141, figure 1-3, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which inhibits the computer from stopping when the following conditions are detected: (1) Invalid instruction, (2) Overflow fault, (3) Any tape reader fault (IPB, CPB, Feedhole, Verify, or Resume), and (4) Tape reader End of Block or End of Tape stop code. (Amber)

g. INHIBIT-AUDIBLE ALARM, S140, figure 1-65, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which inhibits the audible alarm from sounding when a door opens, high temperature, power supply, or air fault occurs. (Amber)

h. SIMULATOR, S139, figure 1-33, T.O. 21-SM68-2D-6-1: Indicator and pushbutton which selects certain logic circuits to enable input signals and data to be received from the Simulator-Verifier, SM-203/GSK-1, or the radar equipment. When the pushbutton is depressed such that the indicator lamp is lit, input signals and data are received from the simulator. When the indicator lamp is extinguished, input signals and data are received from the radar equipment. (White)

i. TAPE READER 1, S138, figure 1-15, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which selects circuits in the computer to receive information from tape reader number 1. (White)

j. TAPE READER 2, S137, figure 1-15, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which selects circuits in the computer to receive information from tape reader number 2. (White)

k. TAPE BLOCK NUMBER, figure 1-43, T.O. 21-SM68-2D-6-1: Four dial knobs which select the block identification number used in loading information into the magnetic drum storage via the perforated tape reader.

l. READY, S136, figure 1-1, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which master clears the computer. (White)

m. HOLD MAINT, S135, figure 1-15, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which, if the computer is already in the Maintenance condition, can be used to select circuits to hold the computer in the Maintenance condition. In this condition the missile guidance console is inhibited from control (alternate action switch; a second push will release Hold Maintenance). (Amber)

BOTTOM ROW

a. CORE READ, S183, figure 1-15, T.O. 21-SM68-2D-6-1: Rotary switch which introduces marginal conditions into the core storage circuits to test the operation of these circuits. (Lights MARGINAL indicator above it when at other than its NORMAL position.)

b. DRUM TIME, S182, figure 1-15, T.O. 21-SM68-2D-6-1: Rotary switch which advances or delays (in time) the mark and timing pulses in the magnetic drum storage circuits. (Lights MARGINAL indicator above it when at other than its NORMAL position.)

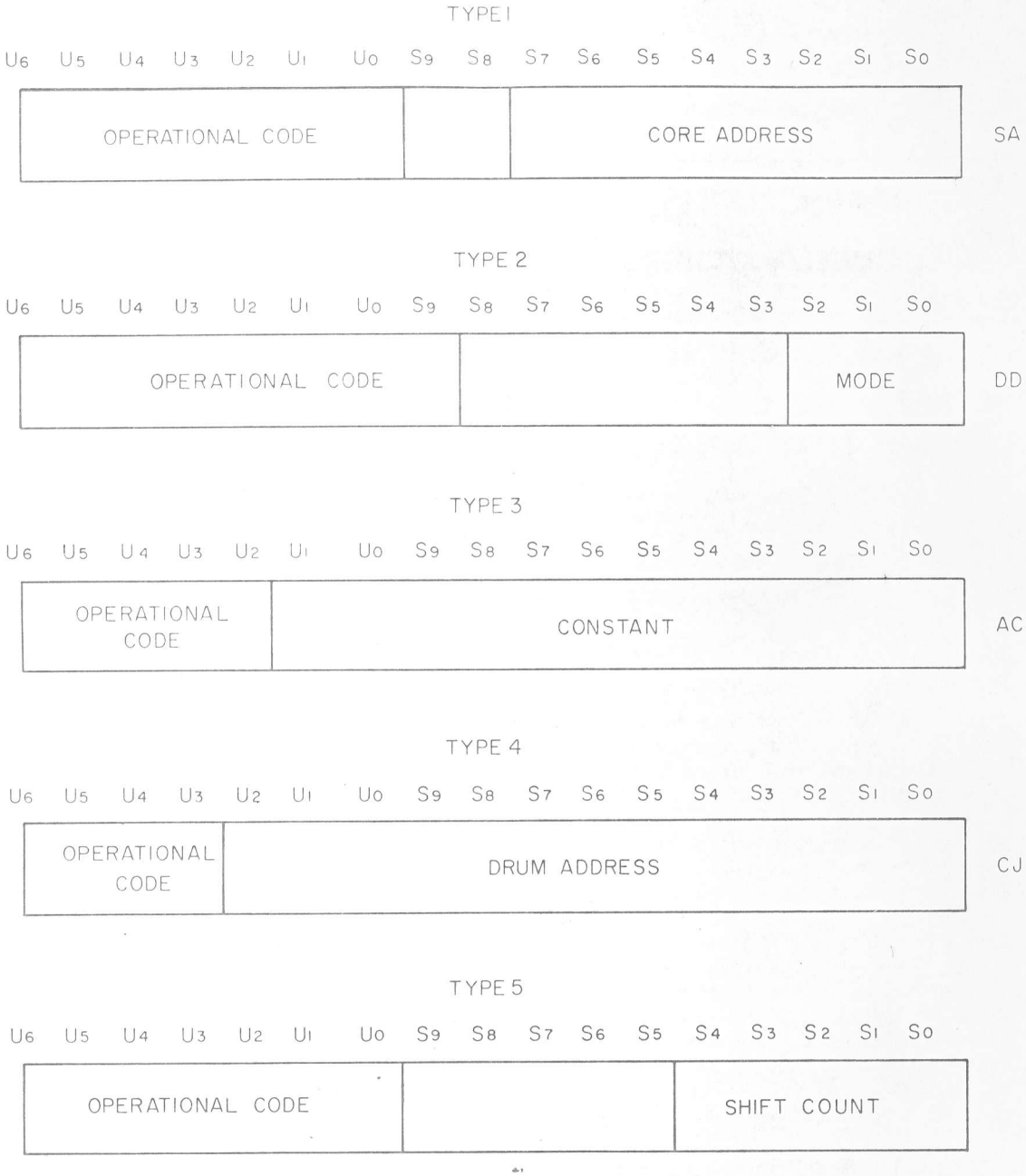
c. DRUM READ, S181, figure 1-15, T.O. 21-SM68-2D-6-1: Rotary switch which increases or decreases the width of the read signals (the signal received by the read amplifiers when a bit is read from the magnetic drum). (Lights MARGINAL indicator above it when at other than at its NORMAL position.)

d. OSC SPEED, R101, figure 1-2, T.O. 21-SM68-2D-6-1: Knob used to control the speed of the low speed oscillator used in conjunction with the DIST CYCLE RATE or DIST PULSE RATE selections. (5 to 20 cps)

e. PARTIAL SYNC, S175, figures 1-4 and 1-15, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which introduces a partial sync pulse into the program sync circuits. (White)

f. CYCLE SYNC, S174, figures 1-4 and 1-15, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which introduces a cycle sync pulse into the program sync circuits. (White)

g. TEST JUMP, S173, figure 1-19, T.O. 21-SM68-2D-6-1: Indicator lamp and pushbutton which enables circuits




NOTE:
$U_0$ THROUGH $U_6$ REPRESENT $U^{01}_{00}\ u^{00}_{00}$ THROUGH $U^{01}_{06}\ u^{00}_{00}$

$S_0$ THROUGH $S_9$ REPRESENT $S^{00}_{00}$ THROUGH $S^{00}_{09}$

Figure 5-40. Types of Program Words

| INSTRUCTION | OCTAL CODE | $U^{01}_{06}{}^{u}{}^{00}_{06}$ through $U^{01}_{00}{}^{u}{}^{00}_{00}$ | INSTRUCTION DESCRIPTION |
|---|---|---|---|
| WC | 000 | 00 000 00 | Wait for computation cycle sync. |
| EP | 002 | 00 000 01 | Enter parameters by adding conditionally the contents of the constant register to the accumulator. |
| SA | 004 | 00 000 10 | Store the contents of the accumulator in magnetic core storage. |
| SI | 006 | 00 000 11 | Store the input data in magnetic core storage. |
| LB | 010 | 00 001 00 | Transmit word in magnetic core storage to the buffer core storage in the Signal Data Recorder Set, AN/GSH-4. |
| WM | 012 | 00 001 01 | Transmit word in magnetic core storage to the buffer core storage in the Signal Data Recorder Set, AN/GSH-4 and then write the contents of buffer core storage on magnetic tape. |
| PC | 014 | 00 001 10 | Select Plotter mode and transmit to the X register the cross range data in magnetic core storage. Transmit nine bits in $X_{14-22}$ to the display register in bit positions $J_{20-28}$. |
| PA | 015 | 00 001 10 | Transmit to the X register the altitude data in magnetic core storage. Transmit ten bits in $X_{13-22}$ to the display register in bit positions $J_{10-19}$. |
| PD | 016 | 00 001 11 | Transmit to the X register the down range data in magnetic core storage. Transmit ten bits in $X_{13-22}$ to the display register in bit positions $J_{00-09}$. |
| DD | 017 | 00 001 11 | Transmit data from a designated source to a designated display destination via the display register. |
| TS | 020 | 00 010 00 | Transmit to the X register the steering order from magnetic core storage. Transmit ten bits in $X_{12-21}$ to the steering register. |
| TA | 022 | 00 010 01 | Transmit to the X register the acceleration data from magnetic core storage. Transmit ten bits in $X_{00-09}$ to the acceleration register. |
| TD | 024 | 00 010 10 | Transmit to the X register the discrete data from magnetic core storage. Transmit twelve bits in $X_{00-11}$ to the discrete register. |
| LV | 026 | 00 010 11 | Transmit to the X register the vernier count from magnetic core storage. Transmit seven bits in $X_{00-06}$ to the vernier counter. |
| TP | 060 | 00 110 00 | Clear accumulator and add the quantity in magnetic core storage. |
| TN | 062 | 00 110 01 | Clear accumulator and subtract the quantity in magnetic core storage. |
| AD | 064 | 00 110 10 | Add to contents of accumulator the quantity in magnetic core storage and place results in accumulator. Check for overflow. |
| SB | 066 | 00 110 11 | Subtract from the contents of the accumulator the quantity in magnetic core storage and place the results in the accumulator. Check for overflow. |
| TQ | 102 | 01 000 01 | Left Shift the quantity AQ by K places ($0 \leq K \leq 37_8$). After shifting place algebraic sign from $A_{24}$ to $A_{23}$. |

Figure 5-45. Repertoire of Instructions (Sheet 1 of 2)

| INSTRUCTION | OCTAL CODE | $U_{06}^{01\ 00}{}_{u}{}_{06}$ through $U_{00}^{01\ 00}{}_{u}{}_{00}$ | INSTRUCTION DESCRIPTION |
|---|---|---|---|
| LS | 104 | 01 000 10 | Left Shift the quantity AQ by K places ($0 \leq K \leq 37_8$). Check for overflow during shifting. |
| RS | 106 | 01 000 11 | Right Shift the quantity AQ by K places ($0 \leq K \leq 37_8$). Algebraic sign in $A_{23}$ is retained and transferred to $A_{22}$. |
| MP | 110 | 01 001 00 | Multiply the contents in the accumulator by the quantity in magnetic core storage and place the result in AQ. This instruction requires 13 instruction time periods. |
| DV | 112 | 01 001 01 | Divide the contents of AQ by a quantity in magnetic core storage and place quotient in Q and the absolute value of the remainder in the accumulator. This instruction requires 25 instruction periods. |
| OC | 114 | 01 001 10 | If an overflow has occurred since the last OC, OJ, or WC instruction, store this information. |
| CX | 12- | 01 010 xx | Transmit the rightmost 12 bits of instruction word to the X register at bit positions $X_{00-11}$. |
| CA | 14- | 01 100 xx | Transmit the rightmost 12 bits of instruction word to the X register at bit positions $X_{12-23}$. Clear the accumulator and add the quantity in X to the accumulator. |
| AC | 15- | 01 101 XX | Transmit rightmost 12 bits of instruction word to the X register at bit positions $X_{12-23}$. Add quantity of X to the accumulator. |
| UJ | 20- | 10 00D DD | Unconditional Jump. |
| SJ | 22- | 10 01D DD | Sign Jump; jump if quantity in accumulator is negative. |
| ZJ | 24- | 10 10D DD | Non-Zero Jump; jump if quantity in accumulator is not zero. |
| OJ | 26- | 10 11D DD | Overflow Jump. |
| TJ | 30- | 11 00D DD | Test Jump, selective in Maintenance condition only. Automatic selection when simulator is selected and simulator power is on. |
| MS | 32- | 11 01I II | Manual Stop, selective in Maintenance condition or in Standby condition for preguidance operations only. |
| WP | 34- | 11 10D DD | Wait for Partial Cycle Sync. |
| CJ | 36-,37- | 11 11D XX | Co-efficient Jump. Jump to a drum group sector in drum groups zero, one, or two for an octal code of "36" or drum groups four, five, and six for an octal code of "37"; the specific sector being determined by the TARGET pushbutton selected. |

NOTE: D = DRUM ADDRESS
X = CONSTANT
I = IDENTIFICATION

Figure 5-45. Repertoire of Instructions (Sheet 2 of 2)

e. An output from the DISC R -12 flip-flop now sets the COUNT HOLD flip-flop (K 00/06) and satisfies an ND input to inverter K 22/10 so that on the next CP1, CLOCK COUNT flip-flop is cleared and the operation of the vernier counter terminated.

10-35. DATA DISPLAY. (See figure 10-24.) The data display circuits are composed of a display register, the mode selection, the digit selection, the printer translator, shift counter, print control timing, and display select. The display register stores and displays the data which is to be displayed, plotted, or printed. The mode selection circuits determine whether the data contained in the display register will be displayed or printed. The display select circuit switches the data contained in the display register from the plotters to the display indicators on the radar Signal Data Recorder-Monitor Set and supplies a print or space enable to the printer. The digit selection circuits are used only during printing. These circuits select which bits in the display register are to be printed. The printer translator translates the output of the four most significant stages of the display register into decimal or octal characters. The shift counter is used in the print operation to shift each digit over to the digit 7 position since this is the input to the print translator and the printer. The print control timing sets up the timing sequence for print operation. The display select circuit switches the data contained in the display register from the plotters to the display indicators.

10-36. Display Register.

37. The display register (figure 1-35, T.O. 21-SM68-2D-6-1) is a 32-bit register which receives its input from control inverters x 03/00 through x 03/23, the Q register, and Command Timing Control. There are two general types of instructions used for data display. These are the plot instructions (Plot Altitude (PA), Plot Cross Range (PC), and Plot Down Range (PD) instructions) and the display (Display Data (DD)) instruction. The plot instructions transmit data from magnetic core storage directly to the plotter of the radar signal data recorder-monitor set through the display register. The DD instruction transmits data from the A1 and Q1 registers to a selected display mode through the display register. These outputs may be monitored on the computer console. On a PA instruction the altitude information to be plotted is transferred from the address in MCS, given in the eight lower order bits of the instruction, into the X register (on MP1) where it is stored in stages X 00/13 through X 00/22. The outputs are available through control inverters x 03/13 through x 03/22 and are transferred into stages J 60/10 through J 60/19 of the display register and are transmitted to the radar signal data recorder-monitor set through line drivers Y 34/10 through Y34/19 (outputs J80215 thru J80222, J80224, and J80225) (see figure 1-60, T.O. 21-SM68-2D-6-1) and line drivers Y 34/60 through Y 34/69. On a PC instruction the cross-range information to be plotted is transferred from the address in MCS, given in the eight lower-order bits of the instruction, into the X register (on MP1) where it is stored in stages X 00/14 through X 00/22. The outputs are available through control inverters x 03/14 through x 03/22 and are transferred into stages J 60/20 through J 60/28 of the display register (on MP4). The output of these stages of the display register are transmitted to the radar signal data recorder-monitor set through line drivers Y 34/20 through Y 34/28 (outputs J80226 through J80234) (see figure 1-60, T.O. 21-SM68-2D-6-1). On a PD instruction, the down-range information to be plotted is transferred from the address in MCS, given in the eight least-significant lower-order bits of the instruction, into the X register (on MP1) where it is stored in stages X 00/13 through X 00/22. The outputs are available through control inverters x 03/13 through x 03/22 and are transferred into stages J60/00 through J60/09 of the display register (on MP4). The outputs of these stages of the display register are transmitted to the radar signal data recorder-monitor set through line drivers Y 34/00 through Y 34/08 (outputs J80205 through J80214) (see figure 1-60, T.O. 21-SM68-2D-6-1) and Y 34/50 through Y 34/58.

10-38. On a DD instruction the miss distance data or target identification data is transferred from the A1 and Q1 registers to the display register. The three lower order bits of the DD instruction identify the output mode (see figure 10-25). The miss distance data contains 31 bits and is contained in A 00/08 through A 00/00 and Q 00/22 through Q 00/00 and is transferred into the X register on MP1. The miss distance is then transferred into the display register on a Q 00 through X 08 Command (MP4). The data may be printed out in either octal or decimal form depending whether the output mode selected is 2 (decimal) or 3 (octal). For octal printout, the data is transmitted to the display register in spread form (see figure 10-26). The target identification data consists of 20 bits and is contained in Q 00/19 through Q 00/00 and is transferred directly into the display register on a Q to DR Command (MP4). The set outputs of J 60/00 through J 60/28 are applied to line drivers Y 34/00 through Y 34/28 which transmit data to the radar signal data recorder set. The set outputs of J 60/00 through J 60/19 are also applied to line drivers Y 34/50 through Y 34/69 which transmit target identification data to the radar signal data recorder set.

10-39. Mode Selection.

10-40. When a Display Data (DD) instruction is translated in the main control translator (MCT) the three least significant bits of the instruction word designate whether a display or a print operation will be performed.

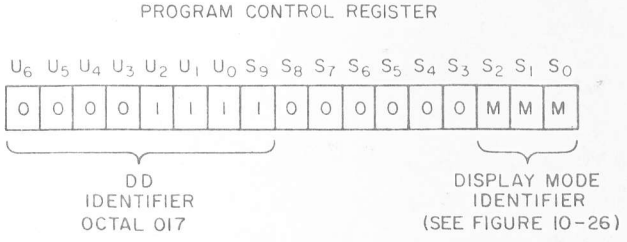



Figure 10-25. Program Word for Display Data Instruction

| MODE (m) | SOURCE | DESTINATION | FUNCTION |
|---|---|---|---|
| 1 | $A^{00}_{08-00}$ and $Q^{00}_{22-00}$ | Signal Data Recorder | Display target identification |
| 2 | $A^{00}_{08-00}$ and $Q^{00}_{22-00}$ | Printer | Print in decimal |
| 3 | $A^{00}_{23-00}$ (SPREAD) | Printer | Print in octal |
| 4 | No transmission of data | Printer | Printer spaced |
| 5 | $A^{00}_{08-00}$ and $Q^{00}_{22-00}$ | Signal Data Recorder | Display miss distance |

Figure 10-26. Display Data Modes

There are five display modes (m) coded 1, 2, 3, 4, and 5. Modes 1 and 5 are used for display purposes while 2, 3, and 4 are used for printing. Sometimes the display mode designator is made equal to zero which is normally used to affect a change from the plotter mode to a display mode. The source, destination, and function of the calculated or programmed data for these modes are given in figure 10-26.

10-41. A description of the functions of the modes is as follows:

a. Mode 1 displays a 20-bit target identification data in the display register and energizes Y 32/40 (Target Identification relay) to provide a common for the target identification circuits (radar signal data recorder set).

b. Mode 2 places in the display register the data contained in the Q1 register and the nine least significant stages of A1 register and then prints this data out in decimal form.

c. Mode 3 places the data in the A1 register into the display register in octal grouping as illustrated in figure 10-27.

d. Mode 4 causes the printer to space a line without any transfer of data to the display register.

| STAGES | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4th | | | 4th | | | | 4th | | | | 4th | | | | | 4th |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 |
| | 1 | 1 | 1 | | 1 | 1 | 1 | | 1 | 1 | 1 | | 1 | 1 | 1 | |
| | | | | 4th | | | | 4th | | | | 4th | | | | |
| 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 1 | 1 | 1 | | 1 | 1 | 1 | | 1 | 1 | 1 | | 1 | 1 | 1 | | |

Figure 10-27. Octal Spread in Display Register

e. Mode 5 displays 29 bits of miss distance data and energizes Y 32/41 (miss distance relay) which provides the plotter common for the plotters (radar signal data recorder set).

10-42. Display Select Circuit.

10-43. The display select circuits, J 02/01-03 (figure 1-37, T.O. 21-SM68-2D-6-1), form a three stable state circuit similar to those in operational control. This circuit is used to switch the data contained in the display register from the plotters to the display indicators of the Signal Data Recorder Monitor Set. Double inverter J 02/00 clears the three stable stage devices whenever any of its inputs go positive. During a plotting operation (PA, PC, or PD instruction) MP2 energizes relay Y 32/42 closing contacts 21A and 22A which apply the plotting board common return to the plotting board control circuits. Likewise, during mode 1 the target identification common return is applied to the target identification control circuit. In mode 5 the common for the miss distance is applied to the miss distance control circuits. During modes 2, 3, and 4, the Print or Space Enable is generated.

10-44. PRINTER CONTROL. An eight-digit printer, normally adjusted to print 32 to 34 lines per minute, is used during a program operation to provide a printed record of calculated data from the computer. Means are provided whereby the printer can either print in decimal or octal representation.

10-45. The various circuits which control a printing operation are shown in block form in figure 10-28. Three principal circuits are shown: printer control (P), shift counter (SK), and display register (DR).

10-46. A printing operation is initiated when a Display Data (DD) instruction, set up in the Program Control Register, as illustrated in figure 10-25, is translated by the main control translator. The three least significant bits of the program word identify the display mode which determines both the source and destination of the data to

be displayed, as illustrated in figure 10-26. Five modes, coded 1, 2, 3, 4, and 5 are used for display purposes, three of which (2, 3, and 4) concern the digital printer. Figure 10-26 illustrates that a DD instruction causes a transfer of data from the appropriate register or registers in the arithmetic section of the display register (DR) where it is then sent to the printer. When a mode 4 code is employed, no transmission of data occurs and the printer spaces a line.

10-47. Once a printing operation is being performed, it must be completed before another printing operation can be initiated. However, a Plot instruction, Display Target Identification (mode 1), or Display Miss Distance (mode 5), will clear out the display register and shift counter and cause the printer to print out whatever number of digits it has received. Hence, these operations will interrupt the printing operation with the subsequent partial loss of the word being printed.

10-48. DISPLAY REGISTER DURING A PRINT OPERATION. The display register's (DR) 32 stages may be considered as eight groups of four bits each. (See figure 1-35, T.O. 21-SM68-2D-6-1.) Each group can hold one binary-coded decimal digit or one octal digit. During a mode 3 DD instruction (octal) data from the accumulator register (A1) in the arithmetic section which is transferred to the display register is "spread." By "spread" is meant that every fourth stage of DR does not receive a transfer of data, but is left cleared. (See figure 10-27.) Hence, in each group representing one octal digit, the highest order bit is always zero. In other words, 24 stages in the A1 register, after transfer, occupy 32 stages in the display register.

10-49. The most significant four bits of DR, representing one octal or decimal digit are translated into the digit enable and sent to the printer first. After this each successive lower order four-bit group is transferred to the four most significant stages of DR, translated into a digit enable and then sent to the printer (see figure 10-28).

10-50. SHIFT COUNTER. The shift counter (SK) (figure 1-40, T.O. 21-SM68-2D-6-1) is used to supply enables to the display register (DR) which cause the proper digit to be shifted to the four higher order stages of that register at the appropriate time. Once the shift counter is initially cleared, its counting operation is performed in two steps as follows:

a. SK 2 ⟶ SK 1

b. SK 1 + 1 ⟶ SK 2

With the exception of the first or seventh digit transfer, the SK 1 + 1 ⟶ SK 2 signal is provided each time the PRINT START 2 flip-flop, J 71/02 j 70/02, becomes set. In like manner the SK 2 ⟶ SK 1 signal is produced each time the PRINT START 3 flip-flop, J 70/01, becomes set. A translator composed of single inverters k 52/01 through k 52/07 provides an enable for each count that appears in rank 2 of SK with the exception of the cleared or zero count $(000)_2$.

10-51. DIGIT SELECTION. The digit selection circuits are used to transfer the contents of four successive stages of the display register (DR), to the four most significant stages, J 60/31 through J 60/28 of DR, starting with stages J 60/27 through J 60/24. This data is transferred on each count of the shift counter (SK) beginning with the count of $001_2$. Figure 10-30 shows the count and what data is transferred. This is also shown in block form in figure 10-28.

10-52. PRINTER TRANSLATOR. The printer translator (see figure 1-44, T.O. 21-SM68-2D-6-1) translates the data contained in the four most significant stages of the display register into 10 characters (0 through 9) during mode 2. During the printout of a decimal number, the first digit (digit seven) sent to the printer is used to print out the plus or minus sign. If the first digit translated is an eight, the plus (+) sign will be printed out. Likewise, if the first digit translated is a nine, the minus (-) sign will be printed out. For octal numbers, the most significant bit of the binary coded octal number is used to determine the sign of the number. If this bit is a "1", a negative number is represented; likewise, if this bit is a "0", a positive number is represented.

10-53. PRINT CONTROL TIMING. The timing sequence for a printing operation in which the Display Data instruction is coded for mode 2 is shown in figure 10-31. The same timing sequence is involved for a DD instruction coded mode 3, with the exception that in this latter case, the transfer of data is from the 24 stages of the accumulator register (A1). A low-speed oscillator designated as the printer control timing pulse generator, (TPG) is used to control the timing of each digit transfer to the printer (see figure 10-32). This oscillator may be adjusted to operate within the range 5-20 cps and slows down the digit transfer operation to a rate the printer is capable of handling. The decoding of a DD instruction of Modes 2, 3, or 4 generates a Print Or Space Enable signal from the output of J 82/00 which sets the PRINT INIT (Print Initiate) flip-flop. J 80/00, on MP2 since the PRINT ON flip-flop, J 81/01 j 80/01, is not set at this time. The set output of PRINT INIT sets PRINT ON on MP6, which applies a Print On = 0 (-) back to command timing control inhibiting these circuits from issuing another print initiate signal during the time that the printing operation is being performed. The set output of PRINT INIT, J 80/00, is also applied to an AND input to the START SYNC flip-flop, J 71/05 j 70/05, which is set by a CP0 on the first positive excursion of the double inverted output of the TPG. The output of the TPG is inverted and shaped by the two inverters, J 72/08 and j 72/07, before enabling the AND input to START SYNC. The PRINT START 1 flip-flop, J 70/03, is set on the next CP1 during the negative excursion of the TPG, since at this time the negative AND inputs of j 74/01 are satisfied and the output of j 74/01 together with the set side of the START SYNC and PRINT INIT flip-flops, and the clear side of the PRINT flip-flop satisfies the input AND. On the next CP0, PRINT START 2 is set by the outputs of PRINT START 1, and START SYNC is cleared. On the next CP 1, PRINT START 1 is cleared, the PRINT START 3 J 70/01 is set. PRINT START 2 is cleared on the next CP0 which sets the TRANSL ENABLE flip-flop, J 71/00 j 70/00. PRINT START 3 is cleared by the output of J 74/05 on the next CP1 since the AND input is satisfied by the set output of TRANSL ENABLE. On the next positive excursion of the TPG,

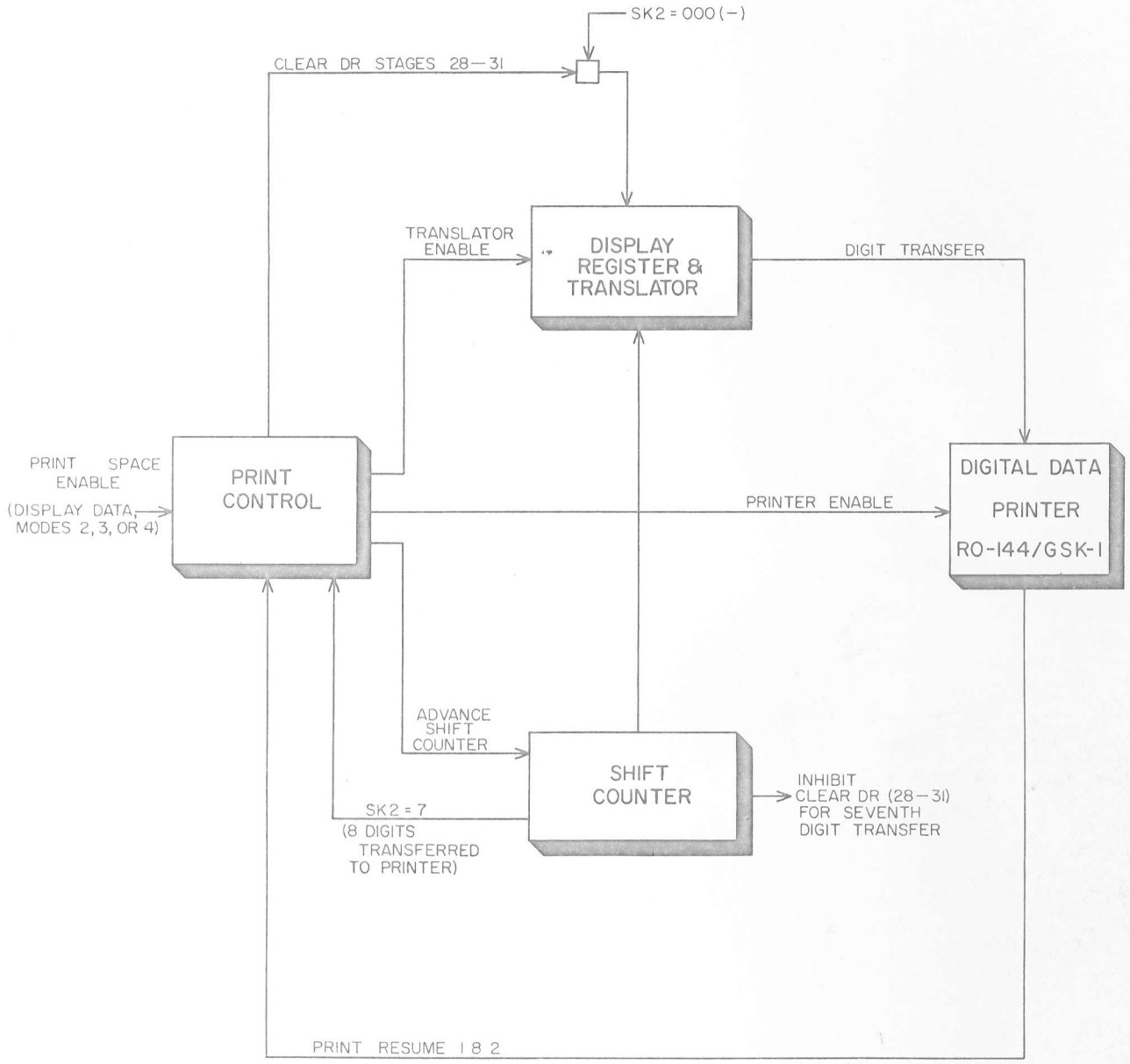



Figure 10-28. Print Control, Block Diagram

TRANSL ENABLE is cleared and on CP0 the whole series of operations explained previously begins again. All three of the PRINT START flip-flops are used to time the signals associated with the digit transfer to the printer and to generate the subsequent print signal.

10-54. Seventh Digit Transfer.

10-55. The first digit (digit seven) transfer is different than the other seven in that neither the shift counter (SK) is advanced, nor are the four higher order stages of the display register (DR) cleared. See timing sequence in figure 10-31. This is necessary since should these two steps occur, the first transferred digit would be lost. The SK DELAY flip-flop J 70/04 inhibits the two above-mentioned steps from occurring for the first digit transfer. This flip-flop must be set in order for SK to be advanced, or the four higher order stages of DR cleared. When the PRINT START 3 flip-flop J 70/01 becomes set, it will enable the SK 2→SK 1 transfer (which does not advance the count in SK) and the TRANSL ENABLE (translator enable) flip-flop J 71/00 j 70/00 to be set. When the TRANSL ENABLE flip-flop becomes set, it will enable the SK DELAY flip-flop to be set at CP1 time. At the time the TRANSL ENABLE flip-flop is set, the translator is enabled to supply the first or seventh digit to the printer. Had the SK 1 + 1→SK 2 signal been allowed to happen when the PRINT START 2 flip-flop became set, the SK would have been advanced and the sixth digit would have been present in the four higher order stages of DR instead of the seventh digit.

10-56. For each digit, the START SYNC flip-flop is set when the timing pulse generator's (TPG) output goes

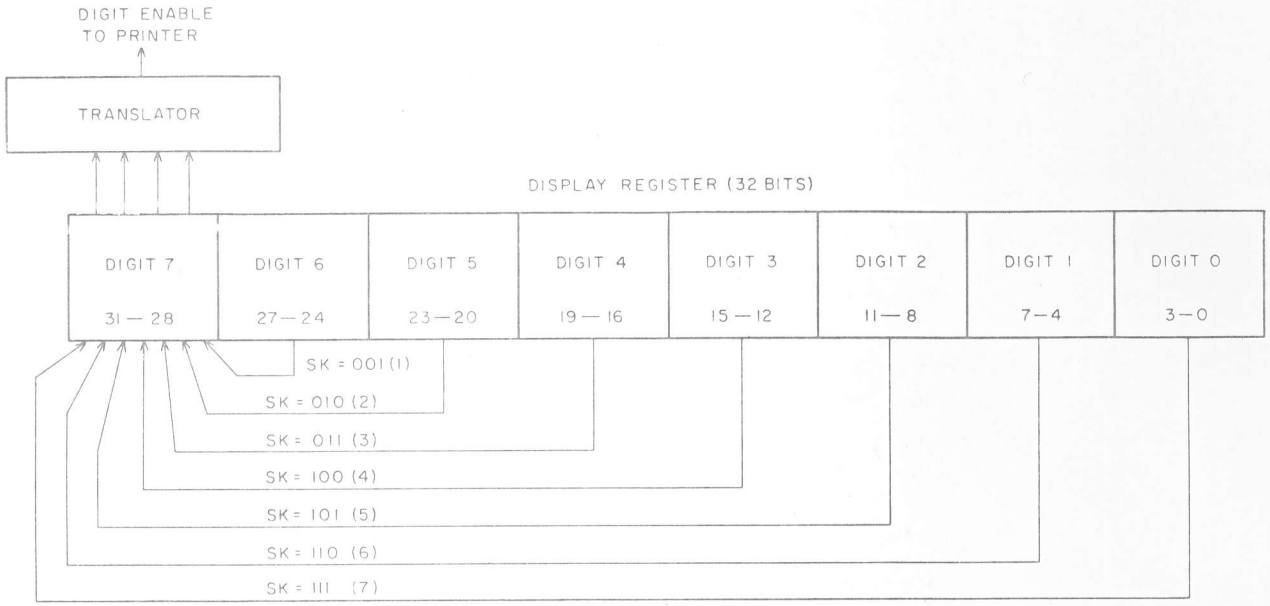



Figure 10-29. Display Register, Block Diagram

positive, and on the following half cycle, when its output goes negative, the PRINT START 1, 2, and 3 flip-flops will be set. These flip-flops will advance SK (except for the seventh digit transfer) and cause the TRANSL ENABLE flip-flop to become set. Each time the TRANSL ENABLE flip-flop is set, the translator is enabled to supply a digit to the printer. Each time the output of TPG goes positive (at the time when the START SYNC flip-flop is set), the TRANSL ENABLE flip-flop is cleared.

10-57. Print Out.

10-58. After all eight digits have been translated and supplied to the printer the count in rank 2 of the shift counter (SK) will equal seven $(111)_2$. When SK 2 equals seven $(111)_2$ and the PRINT START 1 flip-flop is again set, the PRINT flip-flop, J 80/02, will be set and cause the printer to print out the eight-digit word. This is shown in the timing sequence of figure 10-31. Following this, the PRINT START 2 flip-flop will be set and cause the SK 1 + 1→SK 2 transfer to occur which results in SK 2 receiving a count of zero $(000)_2$. The PRINT START 3 flip-flop cannot be set because it is inhibited by the action of the PRINT flip-flop being set.

10-59. When the printer starts its print-out operation, it will send the Print Resume 1 signal to the printer control circuits. This signal will cause the PRINT RES (print resume) flip-flop J 80/03 to be set which in turn enables the AND input to single inverter J 82/01. (See figure 10-33.) Also, when the PRINT RES flip-flop becomes set, the high Print signal from single inverter j 82/06 goes low. (See figure 1-40 in T.O. 21-SM68-2D-6-1.) The Print signal is used to energize the Print solenoid; hence, when this signal is terminated, the Print solenoid is de-energized. The Print Resume 1

| COUNT | DATA SHIFTED TO $J^{60}_{31-28}$ |
|---|---|
| 0 0 1 | $J^{60}_{27-24}$ |
| 0 1 0 | $J^{60}_{23-20}$ |
| 0 1 1 | $J^{60}_{19-18}$ |
| 1 0 0 | $J^{60}_{15-12}$ |
| 1 0 1 | $J^{60}_{13-08}$ |
| 1 1 0 | $J^{60}_{07-04}$ |
| 1 1 1 | $J^{60}_{03-00}$ |

Figure 10-30. Data Transfer in Display Register

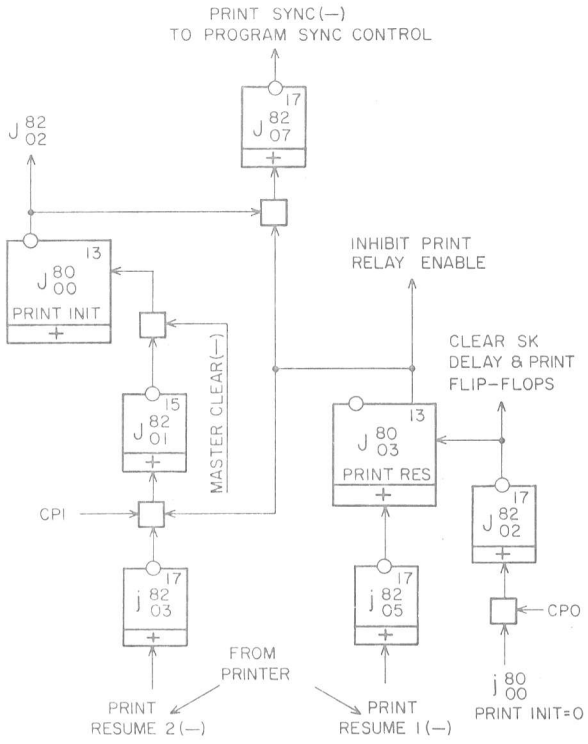



Figure 10-33. Print Resume, Simplified Logic Diagram

signal indicates that the Print solenoid has started the printing operation. This signal is received from a microswitch on the printer and occurs when the switch is in its actuated position. (See figure 1-44, T.O. 21-SM68-2D-6-1.) At all other times, when the switch is not actuated, the Print Resume 2 signal will be received. Once the print operation is started, the Print solenoid is immediately de-energized. This is necessary in order to allow the mechanical linkage (associated with this solenoid) time to return to its non-actuated position. If the Print solenoid were allowed to remain energized until the PRINT flip-flop became cleared, a series of printing operations would result in rapid succession because of the slow moving mechanical linkage. Therefore, it is necessary that the Print solenoid receive power only until the print operation is started. When the printing operation is completed, the Print Resume 2 signal will be received and provide a second enable to the AND input of single inverter J 82/01. On the next CP1, the PRINT INIT flip-flop will be cleared. This is illustrated on figure 10-30. This method of resume signals is employed in order to provide a means of delaying a pulse from a mechanically actuated switch as well as overcoming the difficulty of contact bounce. On the following CP0 after the PRINT INIT flip-flop is cleared, the PRINT RES, PRINT, and SK DELAY flip-flops will be cleared. When MP0 is generated, the PRINT ON flip-flop will be cleared. With all flip-flops now cleared, the print control circuits are ready for another print initiate signal.

10-60. When the PRINT INIT flip-flop is cleared (on a CP1 when the Print Resume 2 signal is received) and the PRINT RES flip-flop is set, the AND input to single inverter J 82/07 will be completed. The low output from this single inverter is the Print Sync signal which is applied to the program sync control (SYNC) circuits. The only time that this signal will affect the SYNC circuits is when the computer is in the Maintenance or Hold Maintenance conditions. During maintenance operations, a Wait Partial instruction may be programmed after a Data Display instruction (coded to produce a printing operation) and thereby hold up the computer while the printing operation is in progress. The Print Sync signal will re-start the computer.

10-61. MODE 4 OR INTERRUPTION. A Data Display (DD) instruction coded mode 4 will cause the printer to space a line. This is accomplished by setting the PRINT flip-flop J 80/02 without any digit transfer to the printer. (See figure 10-32.) Hence, the printer has nothing to print and consequently spaces a line. This will occur on an MP2 after this mode has been translated from the DD instruction. When a printing operation is being performed, the PRINT INIT flip-flop will be set. Should a Plot instruction, Display Target Identification (mode 1), or Display Miss Distance (mode 5) be initiated at the time the print operation is in progress, the PRINT flip-flop will again be set. This is accomplished by a Clear DR SK command (on MP1) from command timing control which completes an AND input to the PRINT flip-flop. The digits which were transferred to the printer by the time this command was received will be printed. The shift counter (SK) and the display register (DR) will be cleared to receive the new data.

**Note**

If the printing operation is interrupted while a printer digit solenoid is energized, a mechanical interlock prevents printing until the digit solenoid is released. A premature Resume signal may be generated clearing the print control circuits even though the digits have not been printed. Thus, all printer programs should start with a space (mode 4) instruction to clear the printer mechanically.

The initiation of these display or plot instructions will interrupt the printing operation and clear all circuits associated with the print operation.

10-62. DIGITAL DATA PRINTER, RO-144/GSK-1.

10-63. GENERAL. The digital printer is an on-line electromechanical output device which prints out the contents of the 32-bit display register (DR). During the preguidance phase, the digital printer may be programmed to print out target identification and constant register data routed to the display register. This provides a check that the target identification and constant register data inserted previously are correct and have been received in correct form by the computer. During the post-guidance phase, after the missile warhead has begun its free flight ballistic trajectory, the computer is programmed to predict cross-range and down-range miss