AN11075

Driving I²C-bus signals over twisted pair cables with PCA9605

Rev. 1 — 19 August 2011 Application note

Document information

Info	Content
Keywords	I2C-bus, 2-wire bus, twisted pair cables, LED lighting, communication cables, Cat5e, Cat6, Fast-mode, Fast-mode Plus, Fm+, inter-IC, SDA, SCL, PCA9605, RS-485, CAN bus
Abstract	The availability of powerful I²C buffers that drive their I/Os on both sides to a nominal ground or ‘zero offset’ logic level allows the removal of noise introduced into one section of a larger bus system. That ‘regeneration’ of clean I²C signals enables building long I²C buses by combining together relatively short bus sections, each say less than 20 meters, using such buffers or multiplexers that contain them. Conventional twisted pair communication cabling with its convenient connectors, and a ‘modular’ I²C system approach, make large system assembly easy. Each drop point or node can be individually selected for bidirectional data communication with the Master just by using normal I²C software addressing. As an example, a system is described for control of LED lighting displays and it is suggested that the power for the LEDs, and the I²C control system, might be economically provided using ‘extra low voltage’ distribution at 48 V using either the control signal cable or similar low cost wiring in a manner similar to that used in ‘Power over the Ethernet’ systems. The simplicity and flexibility of this approach makes it attractive to consider as an alternative to other control systems such as RS-485 or CAN bus.

Revision history

Rev	Date	Description
v.1	20110819	application note; initial release

Contact information

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1. Introduction

The wide availability of very low cost communications hardware, such as Cat5e or similar multi-pair cables with modular connectors, makes it attractive for extending an I^{2}C-bus beyond its traditional application, as an internal bus, into a competitive and attractive LAN that possibly also uses ‘Power over Ethernet’ concepts.

Typical applications can include directly interconnecting the ‘local’ I^{2}C-buses that already exist within pieces of equipment without adding the complexity of converting the I^{2}C protocol into another data format and back again. I^{2}C signaling can just replace, for example, RS-485 or similar signaling systems and hardware.

2. Discussion

Twisted pair cables are intended for balanced signal applications with 100 Ω terminations while I^{2}C uses unbalanced, ground referenced, signals with restrictions on the available drive and terminations. The objective of this application note is to present an arrangement that allows those low cost cables to be used and still allow data rates to approach 1 Mbit/s.

The 30 mA static sink capability of PCA9605 enables it to sink the currents necessary to drive 5 V signals and maintain reasonable noise margins over lengths of at least 20 meters between nodes.

Only two cable pairs are required, one each for SDA and SCL, so the remaining two pairs are connected to lower the ground and supply line impedances.

Waveforms are improved and more current can be available for powering other circuitry via the cable.

To maximize signaling integrity (noise margin) over cables that can vary in conductor diameter/resistance, it is proposed to limit the cable length to 20 meters but this is very conservative and should not be taken as indicative of the typical lengths that could be driven. Probably that limit is well over 100 meters. The system limitation is likely to be set by other factors such as power distribution losses in the cable cores. Each core has a resistance around 1.8 Ω for 20 m.

Figure 1 shows the typical signal transmission arrangement for SCL and SDA. Slave devices may also be directly connected on the cable side of each buffer. Slaves with 30 mA drive capability may be directly connected, but slaves with less drive capability will need their SDA signal buffered as shown in Figure 5.

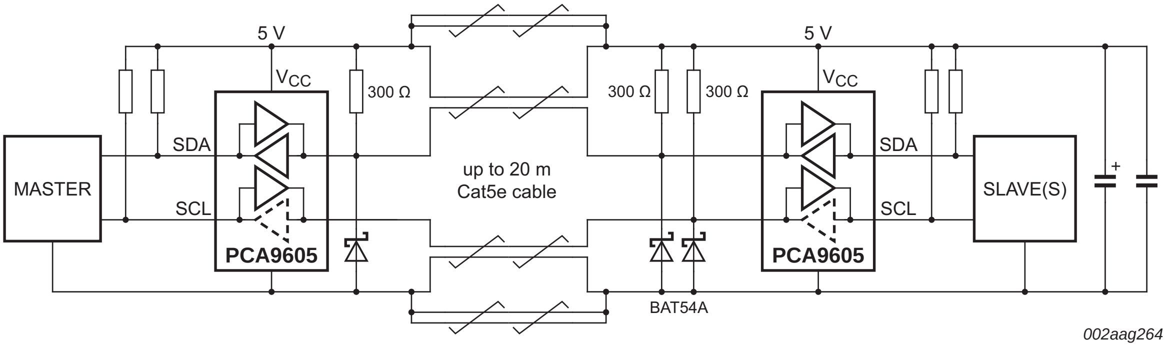
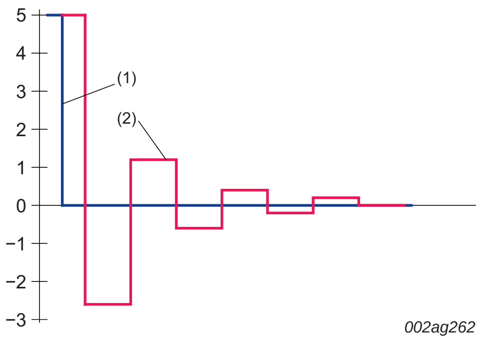


Fig 1. Driving twisted pair cables with PCA9605

3. Technical details

When a cable with 100 Ω characteristic impedance is driven from a source or terminated into a load that is other than 100 Ω, then the cable output signals will be distorted. For example, if the SCL cable was driven to ground from the relatively low impedance (few Ohms) of the FET switch in PCA9605 while the cable is terminated only by the 300 Ω pull-up as shown in Figure 1, then the received LOW signal would swing below 0 V to a level around –2.5 V as shown in Figure 2 and then alternate positive/negative before settling to its final static LOW near 0 V.

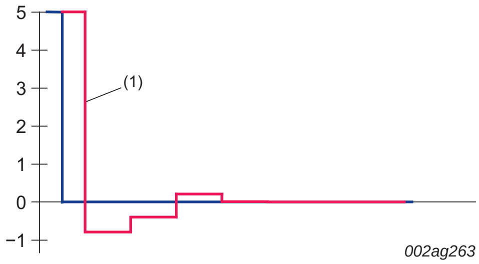


(1) Input drive voltage

(2) Output voltage

Fig 2. Cable input drive and output

While a first attempt to driving the cable involved using cable terminations that approached the characteristic impedance as the means to avoid this overshoot and ringing, it was found that the increased drive current levels led to greater cross-coupling of one signal into the other. An alternative is to use Schottky diode clamps as shown in Figure 1 at any ‘receiving’ end of the cable to minimize the negative voltage at the receiving IC. Figure 3 shows the theoretical output for the same 300 Ω termination when the receiving end is clamped by a junction diode (e.g., IN4148). Section 9 “Appendix 1: Calculating bus delays and using a graphical method to predict transmission line signals” gives details of the graphical method used to predict these cable waveforms.



(1) Cable output

Fig 3. Cable output with junction diode clamp

4. Determining the allowable system clock speed

The original I²C-bus specifications were intended to apply to systems with relatively small capacitance and short wiring inside one enclosure. The bus timing specifications therefore do not expect signal delays between the ICs in the system.

The availability of bus buffers gives a system designer freedom to build large systems with large capacitance and to use long cables to link widely separated I²C-bus systems. It is just necessary for the designer to recognize that introduced delays may mean the clock speeds need to be reduced below the maximum ratings of the individual building blocks.

I²C-bus data bit transfer is similar to read/write operations on a static RAM memory. There are requirements for data set-up times relative to the SCL clock edges equivalent to the read/write strobe of memory.

In its simplest terms, the device delivering data must not change the data bit on SDA while SCL is HIGH and it must change the data bit to its new valid state before the next rising edge of SCL. When the master and slave are separated as in Figure 1, and delays are introduced, it necessary to ensure that the LOW period of the clock (SCL) is long enough for the I²C timing to be met.

Suppose the buffers and cable in Figure 1 delay the SCL by 300 ns so the slave receives the SCL falling edge 300 ns after the master made the change. The slave will respond by changing the data bit it places on SDA, but it takes time before that new data is received back at the master. If the new data is also delayed, through the buffers and cables, by 300 ns then the simplest system design approach will simply add 600 ns to the I²C-bus LOW period requirement. For a Fast-mode system, with 1300 ns LOW, that would be increased to 1900 ns. The total SCL period would be increased from 2500 ns to 3100 ns so the fastest speed becomes 323 kHz.

Appendix 1 (Section 9) describes in more detail the different delays that can apply to the SCL and SDA signals, for different sequences of HIGH and LOW bits, and shows how the full top speed may still be achieved provided the I²C driver components are selected to have faster response than the minimum implied in the I²C specifications. For example their manufacturer may provide data sheet guarantees slightly faster than the ‘worst case’ or they may be parts specified to run in faster modes, for example Fm+.

5. ESD considerations

Long, unshielded, communication cables — probably fitted with unshielded connectors for low cost and convenience — may require more ESD protection than buffer ICs can provide.

One effective protection method is called ‘rail to rail’ clamping. First ensure that the 5 V supply is ruggedly bypassed using ceramic capacitors, as well as electrolytic or tantalum, and is fitted with a 5.6 V Zener diode or other form of limiting device to ensure the supply cannot be increased above a safe DC value. Then fit diode clamps from the bus lines to both supply and ground as shown in Figure 4. Those diodes can be diodes specified for guaranteed rail-to-rail ESD protection or could be low cost 1 A rectifier diodes that, in practice, have high ESD tolerance. Note that the Schottky diodes provide no ESD protection and may also need to be protected by the larger diodes. The Schottky diodes just guarantee the Absolute Maximum ratings of the ICs (for correct operation) are met. ESD is a separate issue.

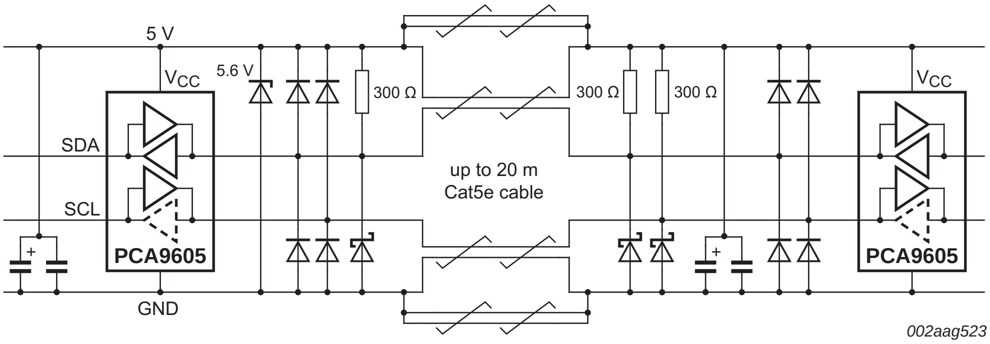


Fig 4. Protecting the bus against severe ESD

6. Including logic power distribution on the cable carrying I^{2}C signals

The distribution of the I^{2}C signals uses only four of the available eight cores in a typical communication cable such as Cat5e. Provided the remaining cores are used only for carrying low noise power supplies, they can provide an attractive means of distributing power to the controlled modules in a system.

The only point to note is that each of the cable cores has a resistance of about 10 Ω / 100 m so using three in parallel with a 20 m cable would give a total resistance less than 0.67 Ω in the ground. It is advised to keep the total voltage drop on the ground less than 200 mV because any drop decreases the noise margin on the logic LOW level.

That still allows a current of 300 mA in any 20 m cable ground and since the maximum drain of any one module will be less than 50 mA (mostly bus pull-up current) it could support at least six remote modules in series and a total bus length of 120 m.

7. Simple low voltage LED power distribution

Using a second Cat5e cable with a different color jacket (or low cost figure-8 power/speaker cable) can provide an attractive means of distributing quite large power to the controlled modules in a system.

As an example, a typical architectural lighting system requires about 1 W per LED and multi-color lighting modules will typically contain between 3 and 36 LEDs.

Conventionally, that power is supplied to each module using power supplies connected to the AC mains. Licensed installers are required for such AC mains wiring and conformance with the regulations both restricts the location of AC outlets and adds greatly to their cost — particularly in outdoor and wet locations.

The use of ‘extra low voltage’ removes many of the safety restrictions and the need for licensed installers.

Regulations vary with country, but generally the use of DC voltages up to 120 V is permitted without strict regulations provided the power supply used to generate that output meets the safety requirements.

While running close to that voltage maximizes the power that could be provided via a Cat5 cable, a more attractive voltage to use is probably 48 V because it is a standard throughout the telecommunication industry meaning a designer has a wide selection of modules at low cost and usually meeting strict standards.

Figure 5 shows an example of a modular system distributing the LED power at 48 V.

The resistance of each Cat5e cable core is less than 10 Ω / 100 m, so using two pairs in parallel for supply and ground gives less than 2.5 Ω /100 m each. The total resistance in supply and return wires is then < 0.5 Ω / 10 m. The allowed voltage drop depends only on the power distribution efficiency limit set by the designer. Given the potential for system cost reduction a designer may accept 5 V to 10 V voltage drop at the furthest module. As an example, a system using 36 W LED modules powered from 48 V and having a total 50 m length, using 4 × 10 m runs in series (for 180 W total lighting), would provide at least 43 V input to the furthest module’s SMPS with total cable losses of 15 W.

If it is practical to site the master control and mains SMPS at the center of the system, then, by using two branches of 3 × 10 m lengths in series each side, it could deliver 252 W of lighting over 60 m. The end modules receive 45 V and total cable losses are about 14 W.

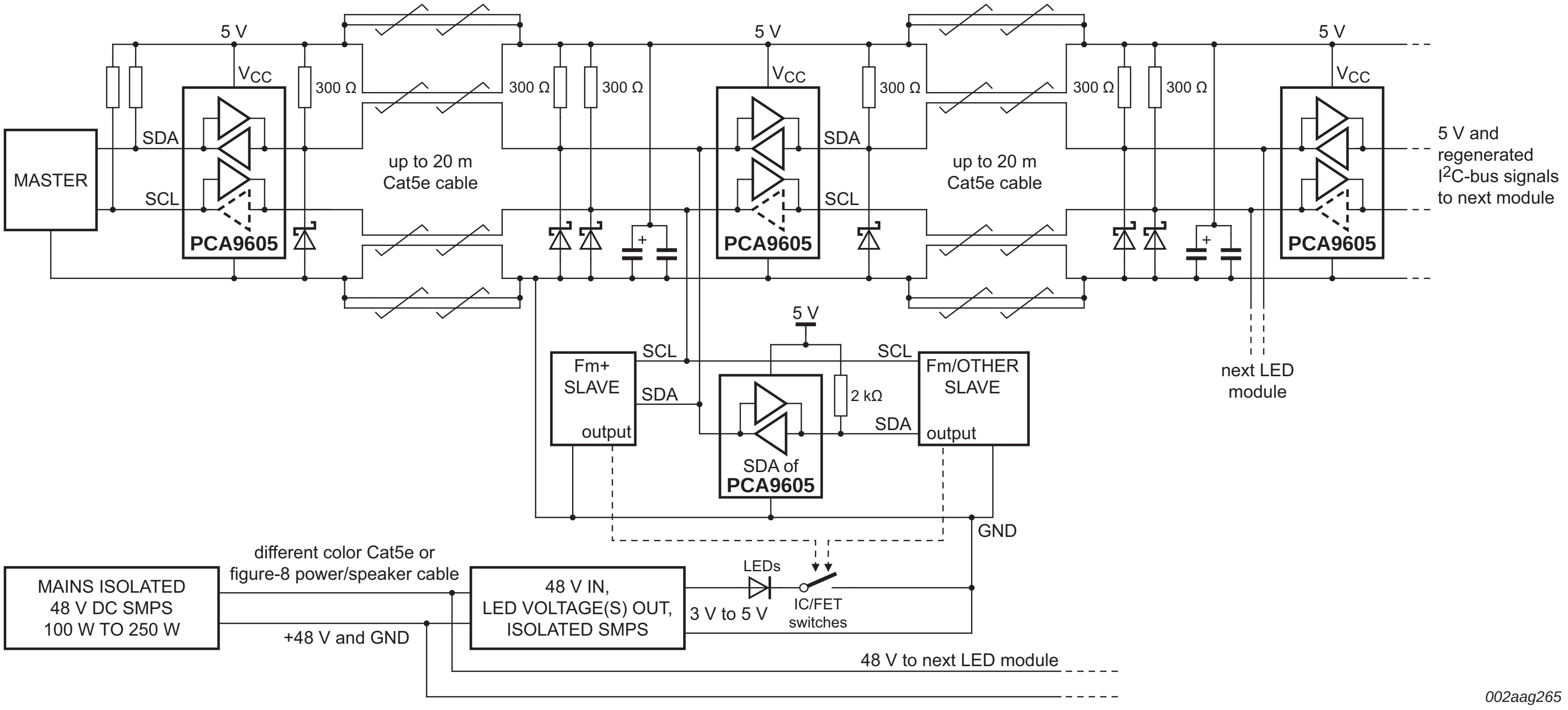
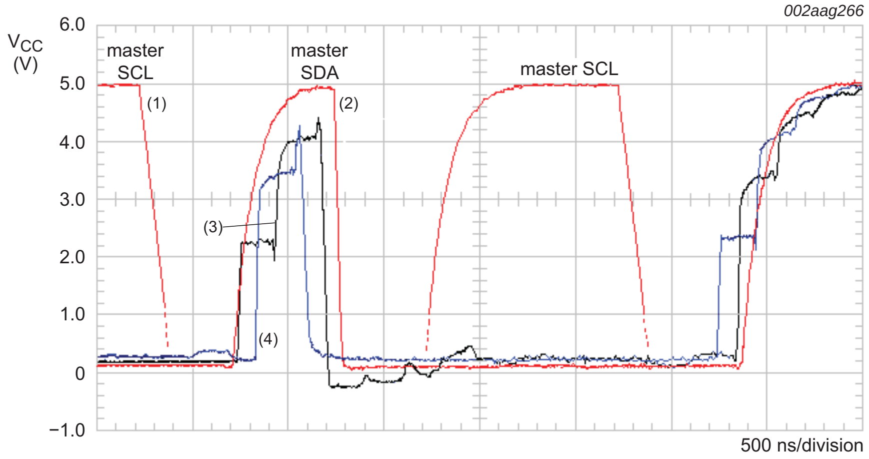


Fig 5. Logic and power distributed using communication cables



(1) Master SCL.
(2) Master SDA.
(3) Buffer output.
(4) I/O signal to slave buffer.

Fig 6. Waveforms from arrangement in Figure 1

Figure 6 shows some important waveforms when running the arrangement of Figure 1 at 400 kHz with a Master controller rated for 400 kHz (89LPC932) and a Slave rated for Fm+ (PCA9633).

The red trace (1) on the left is the Master SCL falling at the start of a 9th clock cycle after the slave has been addressed with a ‘write’. (Bottom of the Master SCL trace has been erased for clarity of the other traces). The master SDA (trace (2)), shown also in red, has been LOW and is released about 400 ns after SCL went LOW.

That LOW input to the SDA buffer at the Master had control of its direction, so as soon as the Master releases the LOW, the buffer output driving the cable and shown by the black trace (trace (3)), starts to rise. The blue trace (4) shows that SDA signal at the other end of the 20 m cable where it is an I/O signal to the Slave buffer.

After one reflection the blue trace reaches the ‘unlock’ level of the Slave buffer and allows the pending ‘Acknowledge’ from the Slave to drive that cable end LOW again. The ACK LOW travels back to the Master buffer where it drives its I/O of the Master SDA buffer LOW (black trace (3)) about 100 ns later. After the LOW propagation delay of the Master buffer (~70 ns) the Master SDA line is driven LOW as shown by the red trace (2). The total ACK delay, by the Master ‘unlocking’ the direction, the buffers and cable, is 940 ns. It is still available some 480 ns before the Master SCL rises. (Requirement is >100 ns). That delay is the sum of the Master release (400 ns) + cable (300 ns) + Slave buffer (70 ns) + cable (100 ns) + Master buffer (70 ns).

After the next SCL fall, the Slave ACK is released and that SDA HIGH is available at the Master about 650 ns after the Master clock went LOW (red trace, right hand side). It is required to be available within 1200 ns.

Section 9 “Appendix 1: Calculating bus delays and using a graphical method to predict transmission line signals” contains details of the system timing requirements and calculation. As it explains, it is important when building these simple systems, even with a small number of series buffers, to ensure the data hold time as generated by the master is long enough to exceed the bus timing ‘skew’ between bus rising and falling edge that is created by the buffers. With just a few buffers in series and when using dedicated master devices this will not be a problem, but if the bus waveforms are generated using ‘bit-bashing’ then due care must be taken to generate a sufficient data hold time.

It is also possible to build very large-scale systems, with a very large number of series buffers, but the system speeds will be much slower. Application Note *AN11084, “Very large I^{2}C-bus systems and long buses”* gives details of simple delay modules to handle the very large skew caused in such systems.

8. Summary

PCA9605 buffers provide a simple interface for driving I^{2}C-bus signals over communication cables at least 20 meters long at Fast-mode speeds.

Using multiple PCA9605 buffers, or PCA9646 fully buffered bus switches, to ‘regenerate’ clean drive signals allows building large area distributed control systems suitable for controlling I^{2}C-bus LED drivers for signs or architectural lighting. Simpler systems, with just a few buffers, still allow quite large systems that will be capable of speeds up to 400 kHz. Very large systems, with over 100 series buffers and ‘mile long’ branches are also possible, but they require more attention to detail and much lower speeds. In both cases system cost can be reduced by distribution of the buffer and LED power using low-cost wiring operated at relatively low voltages.

9. Appendix 1: Calculating bus delays and using a graphical method to predict transmission line signals

When driving cables at the relatively high frequencies used for I²C-bus signals it is useful to be able to predict the signal delays and any waveform distortions that will modify the effective signal delays or their rise and fall times.

For short cables, just a meter or two, sufficiently accurate predictions are possible by simply treating the cable as a lumped capacitive loading that is added to the other bus load components. Most cables will have a capacitance between 30 pF and 100 pF per meter and 50 pF/m is the most common value found in twisted-pair or flat telephony or LAN cables.

The lumped capacitance method was also sufficiently accurate even for longer cables provided they were driven at relatively low frequencies, say 20 kHz to 30 kHz, and with slower rise and fall times as was typical for the original Standard-mode (100 kHz maximum) I²C-bus systems. Even though drivers such as PCA9605 feature slew control on falling edges, they are capable of driving peak currents over 50 mA with the edge rates around 20 ns/V in order to meet Fast-mode Plus timings.

Much more accurate predictions are needed as I²C-bus data rates approach 1 MB/s. It becomes necessary to apply transmission line theory to predict cable waveforms with reasonable accuracy. Computer modelling is possible, but is only as reliable as the data available for all components. Generally it is difficult to obtain device models that are truly useful. Most available models are unlikely to produce results that are even as reliable as using the simple assumptions and graphical methods as described here.

9.1 Cables as transmission lines

LAN cables such as the 4-twisted pair Cat5e and similar have a characteristic impedance (Z_0) of 100 Ω. That means that if they are driven from, and terminated by, resistive impedances of 100 Ω, then they will produce minimal distortions of the data signals and introduce only the simple propagation delays due to the effective ‘speed of light’ delays. For these cables that delay is approximately 5 ns per meter of length. When using those cables to carry I²C signals, it is not practical (or possible) to achieve those required source impedances or terminations.

In practice, the source impedance driving the cable will be an I²C-bus device and parts like PCA9605/P82B96/PCA9600 when driving LOW will drive to ground with impedance less than 5 Ω, and typically under half that value. When they release the LOW they are essentially an open circuit and the local pull-up resistor (if any) becomes the effective driving impedance. At the cable end remote from the driving IC, the cable termination is just the bus pull-up resistor that is fitted at this end and maybe some lumped device capacitance when significant.

Normally, when a long cable is used to provide the data link between two existing I²C-buses, buffers will be added to isolate the cable loading and the effects of paralleling two buses that may already be heavily loaded. That means that, in practice, there will not be any significant capacitive loading component at the cable ends, there will only be a few ICs and any pull-up resistors. With essentially simple resistive terminations, graphical analysis provides a quick and reasonably accurate way to predict, and control, even high clock frequency bus waveforms.

Figure 7 shows one cable pair represented as a 100 Ω transmission line with source and load terminations. The transmission of the clock (SCL) in single-master PCA9605 systems is unidirectional but the data (SDA) is always bidirectional. There is usually no reason to make the SDA transmission asymmetrical, so the allowable pull-up resistance will be simply split and half will be placed at each end of the cable. That means the cable termination at the load end will be twice the allowable minimum pull-up resistance value. For most 5 V Fm+ systems or buffered Fast-mode systems the static device (buffer) drive capability is only 30 mA, so the lowest possible pull-up loading for a 5 V bus and 0.4 V LOW is 153 Ω. If that is split then the pull-up at each end of a cable cannot be lower than 300 Ω — and a 300 Ω termination is well above the cable's characteristic impedance and is therefore going to cause important distortions of the bus signals.

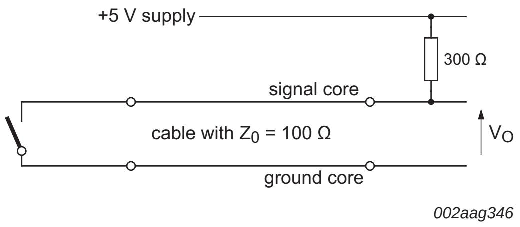


Fig 7. 100 Ω cable terminated at one end by 300 Ω, as used for SCL

Note that the +5 V supply is assumed bypassed to the cable 'ground' core. That means the pull-up resistors become the cable terminations before the switch is closed. The switch will be closed (it is actually an I^2C device) to send a bus LOW. The signal at V_O can be estimated using a Bergeron diagram.

The Bergeron method starts with the initial conditions and then graphically represents the state changes that occur as the signal propagates and is reflected at the cable terminations.

Figure 8 shows a Bergeron diagram for the arrangement essentially as in Figure 7, but for completeness also includes a finite switch resistance (Z_S or source impedance) of 5 Ω for the condition after the switch closes.

The diagram plots the line's source (Z_S) and load (Z_L) impedances starting from the initial conditions, so for the load resistance or cable termination the starting point (before the switch closes) is +5 V and zero current. For the source impedance, before the switch closes, the starting point is zero volts and zero current. To derive the output voltage a line is drawn with the impedance of the transmission line (Z_0) starting also from the initial line input voltage (5 V) until it intersects the cable source impedance. (This point represents the initial input voltage to the line.) A line is then drawn with the inverted line impedance until it intersects the load impedance.

The intersection represents the first output voltage at V_O after a delay equal to the propagation time along the cable. In the diagram this is shown to be about −2.4 V. That represents a new 'initial condition' point for the cable and the start of a reflected wave that travels back to the source impedance where it is again reflected and, after two more cable propagation delay periods, appears at V_O. That is predicted by again constructing lines with the slope of the line impedance until reaching the source impedance and with inverse cable slope until reaching the load again. V_O has the value around +1.2 V this time.

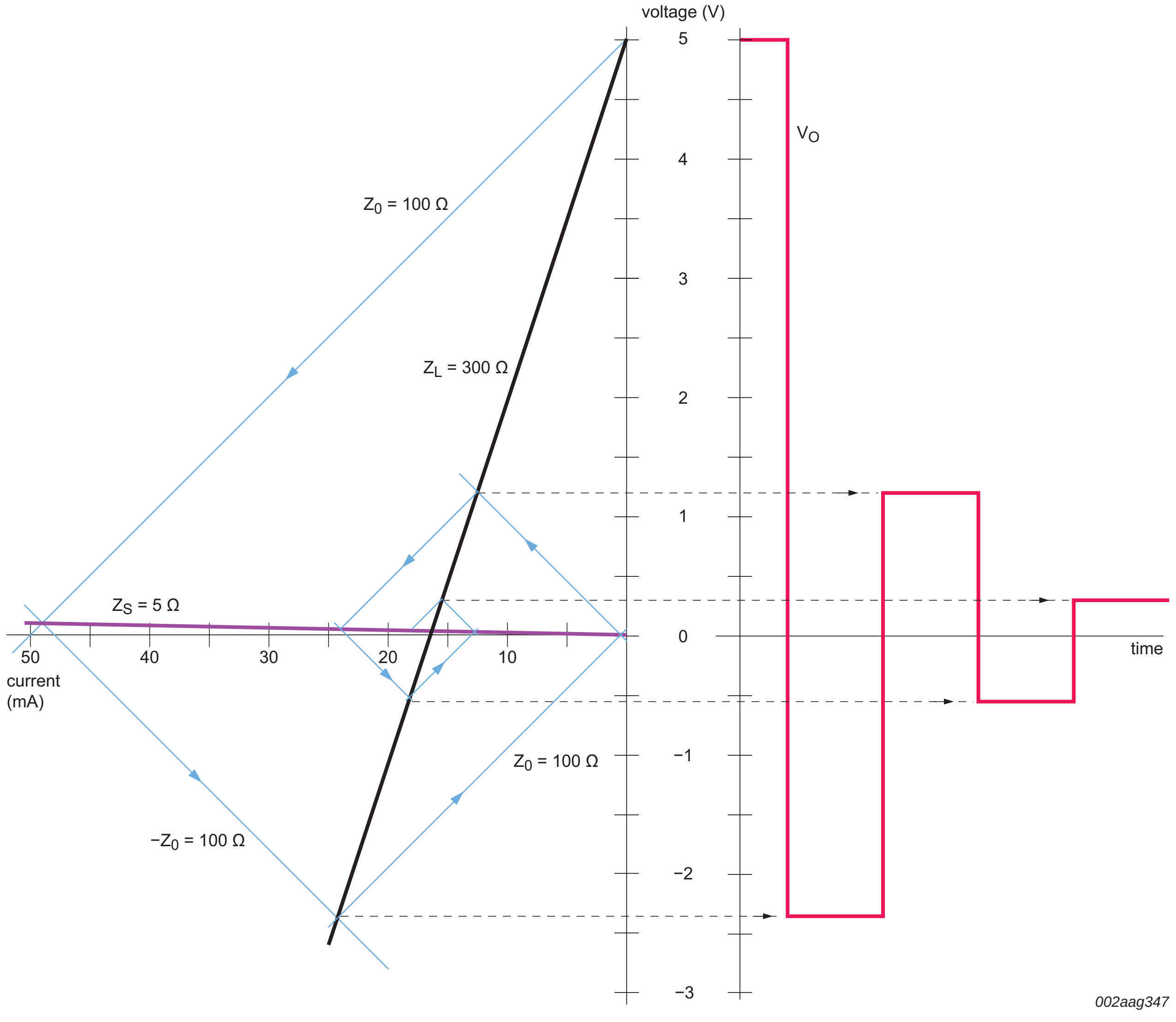


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Fig 8. Bergeron diagram graphically calculates V_O after switch closes

The procedure is repeated and the construction lines will spiral until they reach the final settling voltage for the cable with its source and termination. That will be 5 V / (300 + 5) Ω = 16.4 mA flowing, and V_O will be 82 mV. When there is a second pull-up at the ‘sending’ end it will raise the current in the source impedance and slightly increase the initial voltage drive to the cable after the switch closes but the effect, for drivers with an impedance under 5 Ω, only raises the initial input or settling voltage by less than 80 mV so it can generally be neglected. To include it, the Z_S impedance line could be drawn parallel to the line shown and raised by, say, typically 40 mV.

It is clear that the resulting large negative swing must not be applied to a PCA9605 input rated at –0.5 V maximum and it needs to be clamped by a Schottky diode that will restrict the negative swing to within the IC rating. (While some bipolar buffers are specified to handle these negative transients, clamp diodes may still be needed for protection against severe ESD.)

The Bergeron diagram can include non-linear load lines and Figure 9 shows how the load line is modified at negative voltages by a parallel diode. Because a Schottky's voltage is very small, the diagram is drawn using a 1N4148 switching diode characteristic with a larger voltage so the construction lines will be clearer.

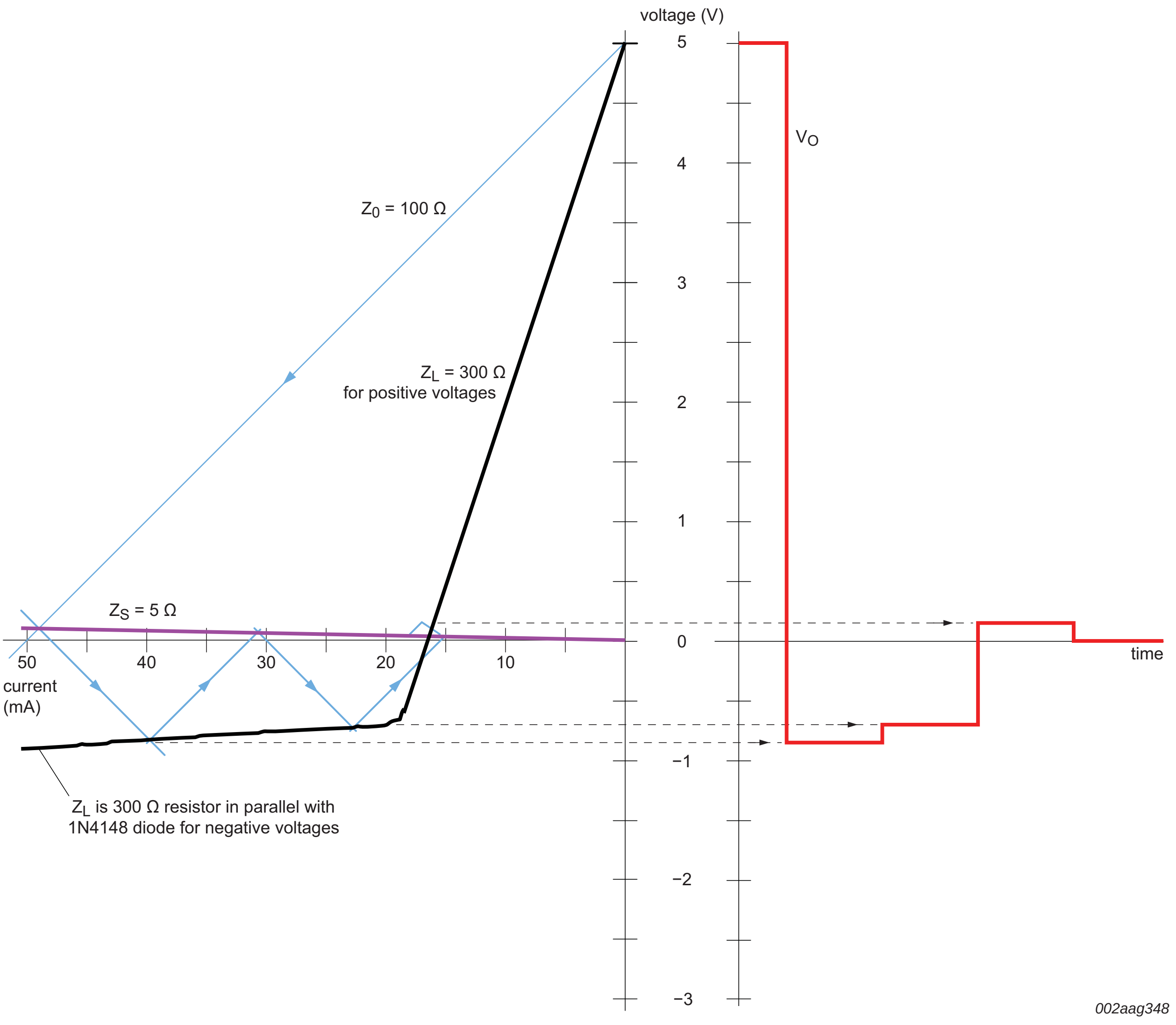
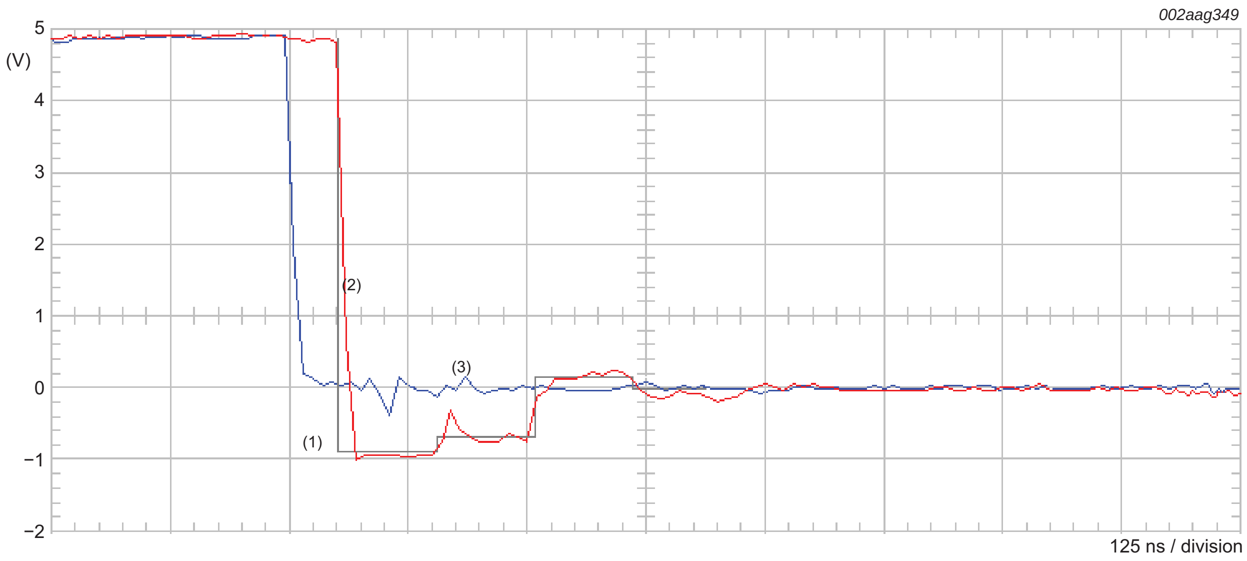


Fig 9. Bergeron diagram including a non-linear load termination

The construction proceeds in the same way, alternately projecting from source to load impedance lines using a slope equal to the transmission line impedance and its inverse. The projected V_O is shown. While the initial negative swing using this standard diode still exceeds the IC rating, the use of Schottky diodes will keep the negative amplitudes to safe levels.

To illustrate the effectiveness of this simple technique, Figure 10 shows the observed cable signals for PCA9605 driving a 10 meter cable terminated by 300 Ω and a 1N4148 diode as used in the construction diagram above (Figure 9). Figure 11 shows the measured and predicted waveforms for 300 Ω termination without any diode.

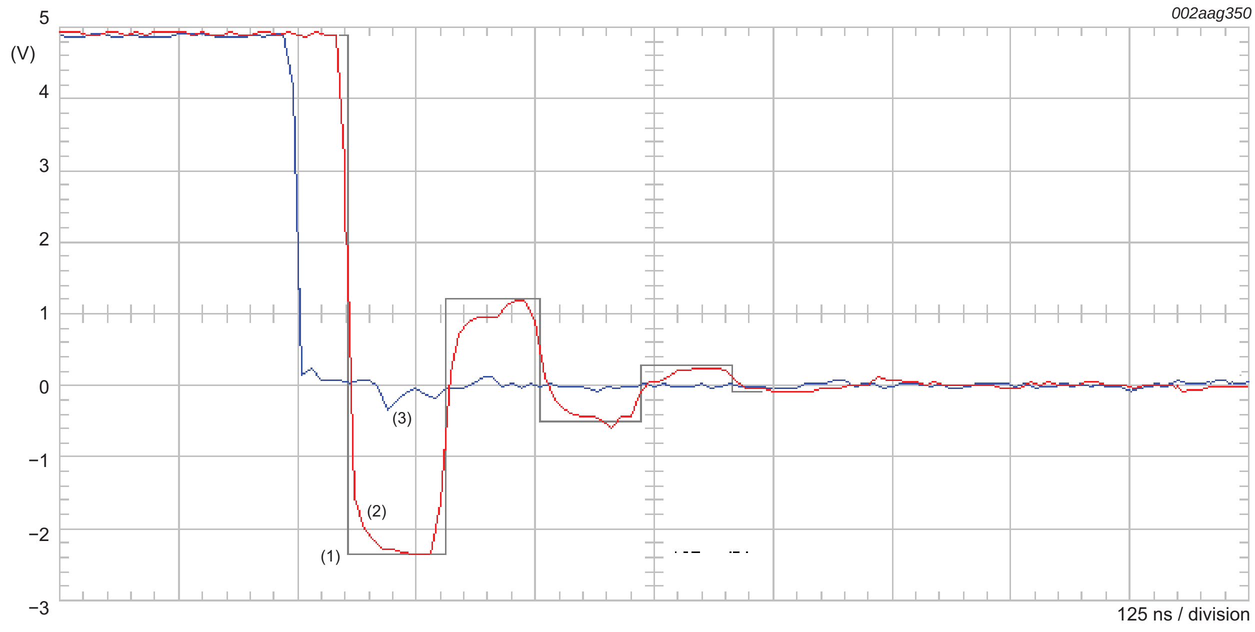


(1) Predicted waveform.

(2) Measured waveform.

(3) Input drive to the cable.

Fig 10. Predicted and measured waveforms for a 10 m cable driven by PCA9605 and terminated by 300 Ω with a 1N4148 clamp diode



(1) Predicted waveform.

(2) Measured waveform.

(3) Input drive to the cable.

Fig 11. Predicted and measured waveforms for a 10 m cable driven by PCA9605 and terminated by 300 Ω without any clamp diode

The same technique can be applied to predict rising bus waveforms, for example of the arrangement in Figure 12 as used for the SDA signals. The resulting rising edge signals are shown in Figure 13.

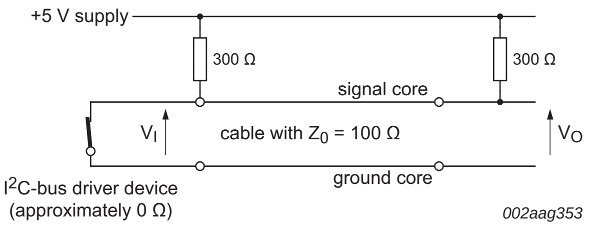


Fig 12. The arrangement of the SDA bus line as used to predict a rising edge in Figure 13

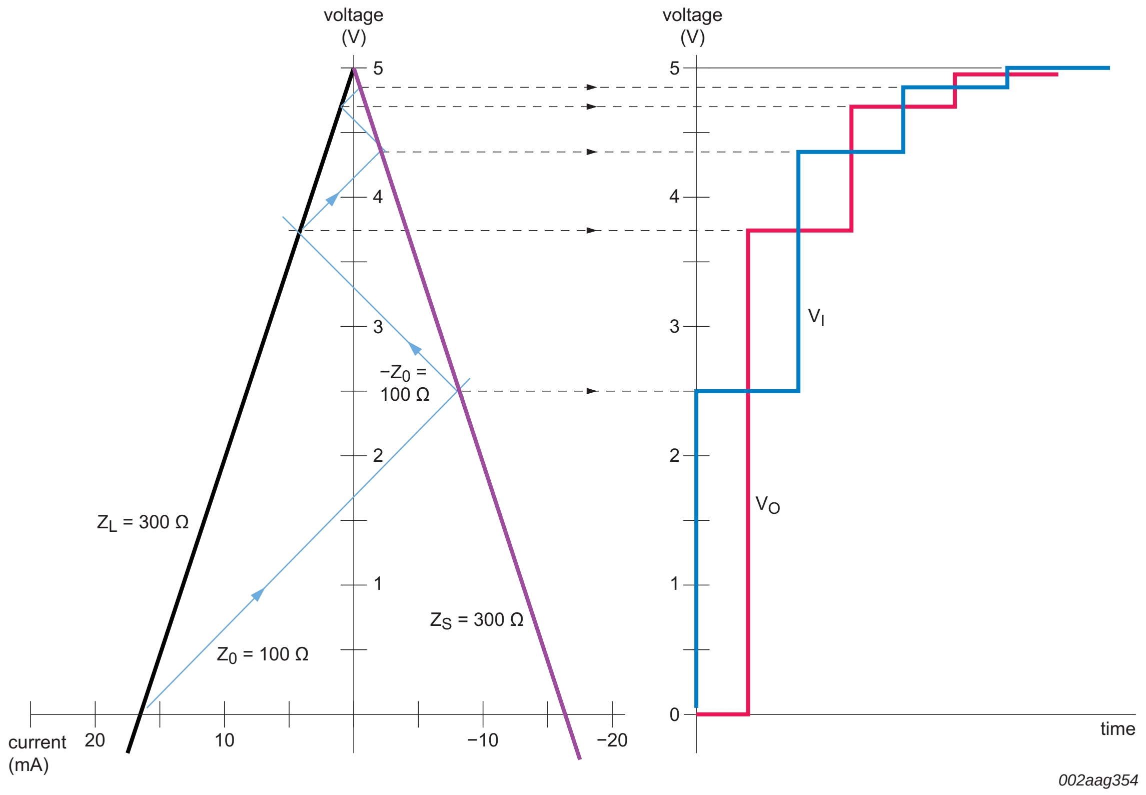


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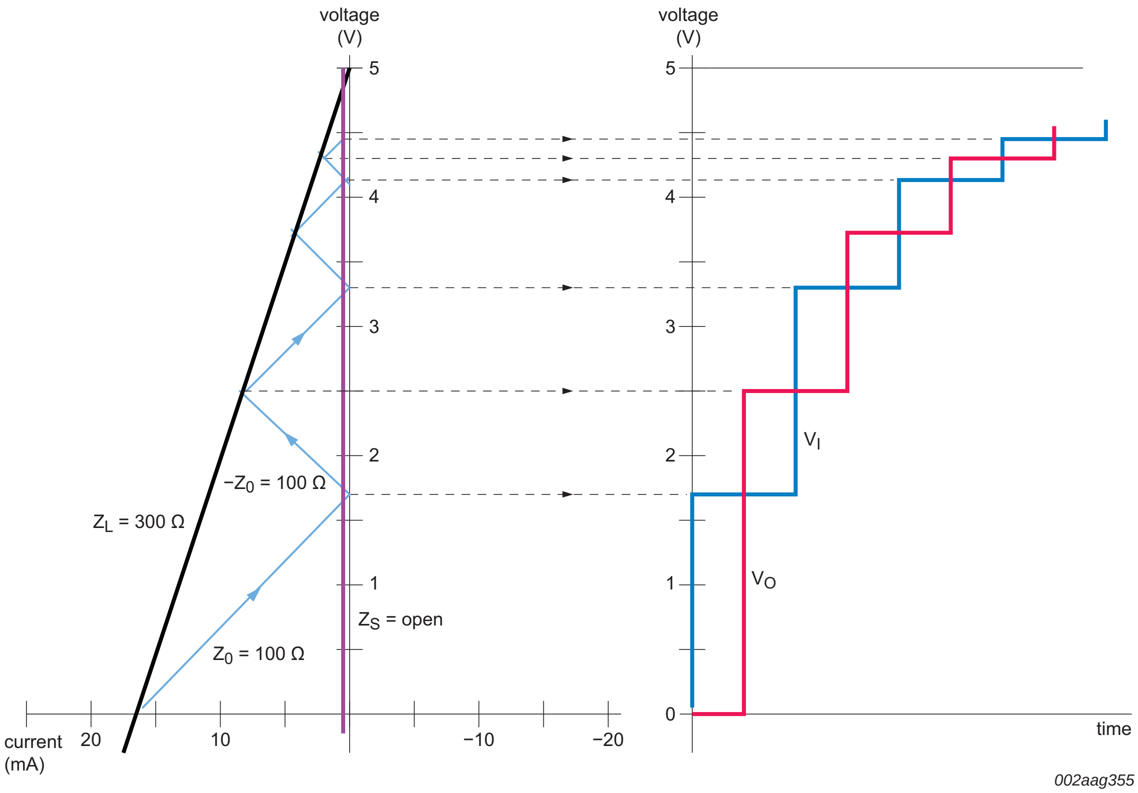
Fig 13. Bergeron diagram for rising SDA bus edges after the I²C device releases the bus

As shown in Figure 13, the first step of the output is at a level of 0.75 × bus supply voltage, guaranteeing a clean logic HIGH level. For the PCA9605 the requirement on 5.5 V supply is that the HIGH level should exceed 2 V.



The arrangement is as shown in Figure 7.

Fig 14. Bergeron diagram for rising SCL bus edges after the I^2C device releases the bus

9.2 Timing of an I^2C transfer through two PCA9605 buffers and 20 m cable

The I^2C-bus specification requires the return of valid Data or an Acknowledge within the Master’s SCL LOW period, including a small allowance for data setup (e.g., 100 ns setup is required for Fast-mode). PCA9605 uses a unidirectional buffer for the clock signal so the Master’s programmed LOW period is not affected (stretched) by the buffer. That means the programmed LOW period must allow the slave’s data to be returned within that period. When calculating the additional delays introduced in cable extensions for a buffer that does not support clock stretching, there are only two delay components to consider:

a) The delay of the falling SCL edge generated by the master, as received by the slave.

b) The delay of the valid SDA data bit generated by the slave as received by the master.

The total delay of the valid SDA data bit signal returning to the master has two possible limit values. One is simply the sum of the delay components a) + b) but there can be another important factor, the time taken to ‘clear’ the master’s LOW data bit in order that the direction of propagation through the PCA9605 can change and allow the slave’s LOW to take control of the bus on the master side.

First consider the delay a).

Because the SCL signal handling through the two PCA9605 buffers is unidirectional, the only important logic signal levels are the V_{IL} and V_{IH}. There is no lock or unlock level associated with the SCL buffer.

The SCL delay components are:

1. The delay through the buffer at the master,
2. The propagation delay of the cable, and
3. The delay through the slave buffer.

There is a falling edge delay at the master, the time taken for the buffer input to fall to a valid LOW level, but the required SCL LOW time is measured from the time SCL reaches the LOW level. The PCA9605 LOW level in a 5 V system is about 0.8 V, so slightly below the usual I^2C LOW level (30 % V_{DD}), but in practice any additional delay caused by the relatively fast edge falling between 1.5 V and 0.8 V is likely to be negligible and no allowance will be made in these calculations. The falling edge delay through the PCA9605, including the bus fall time is under 100 ns. The propagation delay on 20 m of cable is also 100 ns. Figure 9 shows that the LOW level at the input to the slave end PCA9605 is crossed on the received (fast) falling edge. The delay of the falling edge through the slave end PCA9605 is also under 100 ns so the total delay of the SCL falling edge from master to slave, including the fall time of the slave bus, is under 300 ns.

The slave will then respond, when required, by providing data or ACK after it receives the falling edge of SCL. The slave has a t_{VD} specification. That specifies the time required to output valid SDA data (including any rise or fall time) after the SCL is LOW. If the slave data sheet has no t_{VD} specification, then it is necessary to use the ‘worst case’ value required by the I^2C-bus specifications. Often that will mean the extended bus must be run below the slave’s published maximum speed rating.

For these calculations, assume the slave has a t_{VD} of 900 ns, the maximum allowed for Fast-mode parts.

The master has a specification, $t_{HD;DAT}$, that specifies the time it holds its output data bit. This has a maximum value implied in the I^2C-bus specifications. It must be less, by the bus rise/fall time, than the time that is allowed to provide the correct new data bit. For Fast-mode, $t_{HD;DAT}$ is a maximum 600 ns.

Now consider the delay b).

If the master's address byte has specified that it will next 'read' a data byte, then the last data bit it provides in the address byte is a HIGH (the read bit). The slave's address ACK bit will be a LOW. The ACK LOW delay returning to the master will be the same as the master's SCL falling edge, namely 300 ns.

If the slave was delivering bits of a data byte and the data supplied by a slave needs to change from a LOW to a HIGH then the delay of the slave's input HIGH level through the slave buffer is only around 10 ns so can be neglected. The cable HIGH reaches the master end buffer V_{IH} level after 100 ns propagation delay (Figure 13). The master side buffer delay is also only 10 ns, so the total delay b) for a data HIGH is 100 ns. This is faster than the ACK delay of 300 ns so is not a limiting factor.

That delay is still not necessarily the 'worst case' delay for an SDA data bit. The 'worst case' delay might happen after the master's address byte specifies the next byte will be a 'write'. In this case the last bit sent by the master before it requires the slave's ACK is a LOW, the write bit. While the PCA9605 can handle bidirectional signals on SDA, only one device (one side of the buffer) can be in control at any one time. It is therefore necessary for the master to remove its LOW before the LOW from the slave can pass through the buffers. That means the release of the SDA line to HIGH by the master needs to reach the slave's PCA9605 buffer, releasing control of that buffer, before the slave's LOW can start to be returned.

The timing follows this sequence:

1. The master releases the SDA line and it is HIGH by the time $t_{HD;DAT}$, maximum 600 ns.
2. The PCA9605 at the master end releases the cable and a HIGH propagates on the cable to the PCA9605 at the slave end.
3. When the SDA HIGH at the slave PCA9605 exceeds the 'unlock' level that allows any LOW, waiting on SDA on the slave side of the buffer, to pass back to the cable side, pulling it LOW. That LOW propagates on the cable to the master PCA9605 then through the buffer to the master side where it provides the required ACK (LOW) to the master.

The propagation delay for a HIGH at the input to a PCA9605 to its output is around 10 ns and can be neglected. The SDA cable signals now rise as shown in Figure 13. The SDA level crosses the typical 'unlock' level (3.5 V) at the slave end after just one cable propagation delay, 100 ns. A 'worst case' design, based on reaching the maximum 'unlock' level of 4.5 V would need to allow for a cable reflection, i.e., an additional 200 ns for a total of 300 ns.

Typically, a slave ACK LOW may be blocked by the master for a total time (1 + 2 + 3) = 600 + 0 + 100 = 700 ns and worst case it could be 900 ns. This becomes the limiting delay factor b) that may need to be considered.

This delay, due to the master having control of the buffer direction, only becomes relevant if the slave ACK has become available by the instant the slave's buffer is released, that is 700 ns (maximum 900 ns) after the master SCL is LOW.

Because the SCL falling edge reaches the slave 300 ns after the master SCL is LOW, the ACK is not available on the slave's side of the slave buffer until after a maximum of (300 + 900 ns) = 1200 ns after SCL is LOW.

It takes 300 ns to propagate back to the master (two buffer delays and the cable delay) and is available 1500 ns after SCL is LOW.

The master's blocking delay, using these 'worst case' Fast-mode timings, is therefore not actually relevant — in this example it is the availability of the slave ACK that is the real limiting factor.

The SCL LOW period must be long enough to accommodate the return of the slave ACK (1500 ns) and the data set-up time (100 ns), so the master SCL LOW must be programmed for (worst case) 1600 ns, an increase of 300 ns over the minimum 1300 ns, causing the total period to become (2500 + 300) = 2800 ns or a maximum speed of 357 kHz.

If only Fm+ slaves (with a t_{VD} of 450 ns maximum) were used, then their ACK time is reduced by 450 ns and Fast-mode master becomes the limitation. It is blocking for 900 ns, worst case, and that means the ACK is not available until 1200 ns after the SCL is LOW but that still guarantees the full 400 kHz.

9.3 Buffers can 'skew' the SCL/SDA timing

In the examples above, the falling edge signal delays through a buffer were around 70 ns while the rising edge delays were less than 10 ns. The I^{2}C-bus specification does not mandate any data hold time, it simply suggests that a system designer must make provision to cover the maximum bus fall time. That is allowed to be 300 ns in a Fast-mode system. An Fm+ master can change the data line just 120 ns after the fall of SCL. If the data change is LOW-to-HIGH, then after clock and data pass through, say, five series buffers, the SCL fall will be delayed about 350 ns while the SDA rise delay will be less than 50 ns. That means the rising SDA edge coming after five series buffers rises 300 ns before the SCL falls and that represents the special sequence for a bus START condition. A START is not allowed during data bit transfers.

Slaves can also generate data bits quite quickly after the falling SCL edge. A slave adjacent to the master will provide data changes after their t_{VD} time. That data change will propagate, just like master data, to more remote slaves. The t_{VD} of even Fm+ parts is unlikely to be shorter than 200 ns, so at least three series buffers between two slaves will generally present no problems. If in doubt, check the bus timings with an oscilloscope.

10. Abbreviations

Table 1. Abbreviations

Acronym	Description
CAN	Controller Area Network
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
Fm+	Fast-mode Plus (I^{2}C-bus)
I^{2}C-bus	Inter-Integrated Circuit-bus
I/O	Input/Output
IC	Integrated Circuit
LAN	Local Area Network
LED	Light-Emitting Diode
RAM	Random Access Memory

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Date of release: 19 August 2011
Document identifier: AN11075