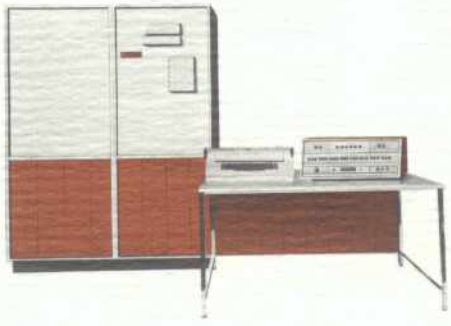
DDP-124

MICROCIRCUIT

General Purpose
Digital Computer



COMPUTER CONTROL COMPANY, INC.

FEATURES

- silicon monolithic integrated circuitry
- 1.75 μsec memory cycle
- 24-bit word, sign magnitude arithmetic
- fast multiply-divide hardware
- 3 hardware index registers
  (one standard, two optional)
- indirect addressing
- modular memory expansion to 32,768 words directly addressable
- program compatibility with DDP-24 and DDP-224
- powerful instruction repertoire; simple command format
- complete, real-time oriented programming package including FORTRAN IV

DDP-124 is a fast general purpose digital computer featuring μ-PAC™ monolithic integrated circuit construction — a parallel, 24-bit word, binary, core memory, single address, stored program machine with indexing and indirect addressing. Standard main-frame includes 4K memory with 1.75 μsec cycle, hardware index register, fast multiply-divide hardware, electric input-output typewriter, 300 cps paper tape reader, and 110 cps paper tape punch. Comprehensive software supplied; fully program compatible with DDP-24 and DDP-224. Modular design and broad I/O options enable DDP-124 to be tailored to a variety of applications, on or off line. DDP-124 is competitively priced.

INTRODUCTION

μ-PAC CONSTRUCTION

Logic in the DDP-124 is 5 mc μ-PAC™ digital modules. μ-PACS are silicon monolithic integrated circuits mounted on etched glass-impregnated epoxy cards. With all circuit inputs and outputs available at connector pins, they make possible traditional computer design and permit design modification and simplified procedures for check out and maintenance.

Twenty months of in-house funded research and design went into 3C development of standard μ-PAC integrated logic packages which have the flexibility of long established 3C discrete package lines used in DDP-24, DDP-224 and DDP-116 computers. This flexibility was achieved while retaining price, size, and reliability (see DDP-124 Reliability section) advantages inherent in integrated circuitry.

SPEED

DDP-124 is capable of 285,000 computations per second. Basic memory cycle is 1.75 microseconds. Input and output can occur asynchronously and be interleaved with processing at transfer rates up to 285,000 words per second. Most instructions which do not access memory are executed in 1.75 microseconds.

PROGRAMMING/USER SERVICES

Sign magnitude machine code is used for maximum convenience to operator and programmer. The DDP-124 communicates with peripheral equipment with a minimum of external coding. DDP-124 command structure is flexible and straightforward.

A complete programming package, including a FORTRAN IV compiler, an assembler, a scientific programming system for the minimally experienced user, and comprehensive utility, service, and executive routines come with the DDP-124. Programmer and maintenance training, user information service and installation services are all part of the DDP-124 user support program.

EXPANSION/OPTIONS

The standard 24-bit 4096 word core memory is optionally expandable to 32,768 words.

DDP-124 I/O options include interrupt lines and a multi-level priority system. Buffered input-output channels for parallel and character transfer can be added as required. Ready and interrupt modes enable the computer to be used in primary or sub-system applications.

Peripherals are easily added, including magnetic tape units, card punch and reader, high speed line printers, digital plotters, cathode ray tubes, paper tape punch, and reader.

RELIABILITY

DDP-124 parallel machine organization permits use of moderate-speed circuitry and wide reliability performance margins.

3C has drawn on 10 years' reliability experience with digital modules to develop microcircuit DDP-124. Computer design engineers participated heavily in defining logical capability and configuration parameters for μ-PAC monolithic integrated circuit modules. To achieve optimum system reliability, extensive consideration was given to circuit design approaches, component values, component tolerances, margins, heat transfer and performance specifications.

Inherent advantages contributing to μ-PAC reliability are:

1. Greatly reduced number of thermal compression bonds required on a typical digital integrated circuit.
2. Fewer component interconnections.
3. Fewer sealed packages per circuit.
4. Less variability between individual integrated circuits.
5. Easier traceability of defective circuits.

Hybrid circuits used in DDP-124 employ high quality, high stability discrete components. All semi-conductor components are silicon.

Rigid inspection, testing and over all quality assurance programs are an integral part of both the μ-PAC and DDP-124 manufacturing processes.

SPECIFICATIONS

TYPE
Binary, core memory, parallel, single address with indexing, and indirect addressing.

WORD LENGTH
24 bits; sign/magnitude code.

SPEED (Including Instruction and Operand Access)

Add	3.5 μsecs
Multiply	14 μsecs (avg.)
Divide	22 μsecs (fixed)
Add double precision fixed point	26 μsecs
I/O word transfer	1.75 μsecs

MEMORY
4,096 words, expandable to 32,768 words; all words directly addressable; coincident current ferrite core; non-volatile storage. 1.75 μsec cycle time, 0.8 μsec access time.

INPUT-OUTPUT
Electric typewriter, 300 cps paper tape reader, 110 cps paper tape punch with character buffer and channel. A large number of additional I/O channels can be added. Program controlled input-output, or automatic interrupt for any input-output channels; up to 64 control pulses to peripheral equipment; up to 64 sense inputs from external sources.

SIGNAL LEVELS
Zero volts for logical ZERO; + 6 volts for logical ONE. All inputs are diode coupled/isolated.

MANUAL CONTROLS
Manual data entry and display of main registers, operational controls, maintenance lights and controls for detection of system malfunction.

SOFTWARE

FORTRAN	— Fortran IV compiler with Boolean statements, capable of operating with basic DDP system.
DAP	— Symbolic Assembly Program, relocatable or absolute object output; subroutine linkage, allowing Fortran compatibility.
DIP	— Scientific Interpretive Programming System.
DEBUG	— Program Debugging Aid.

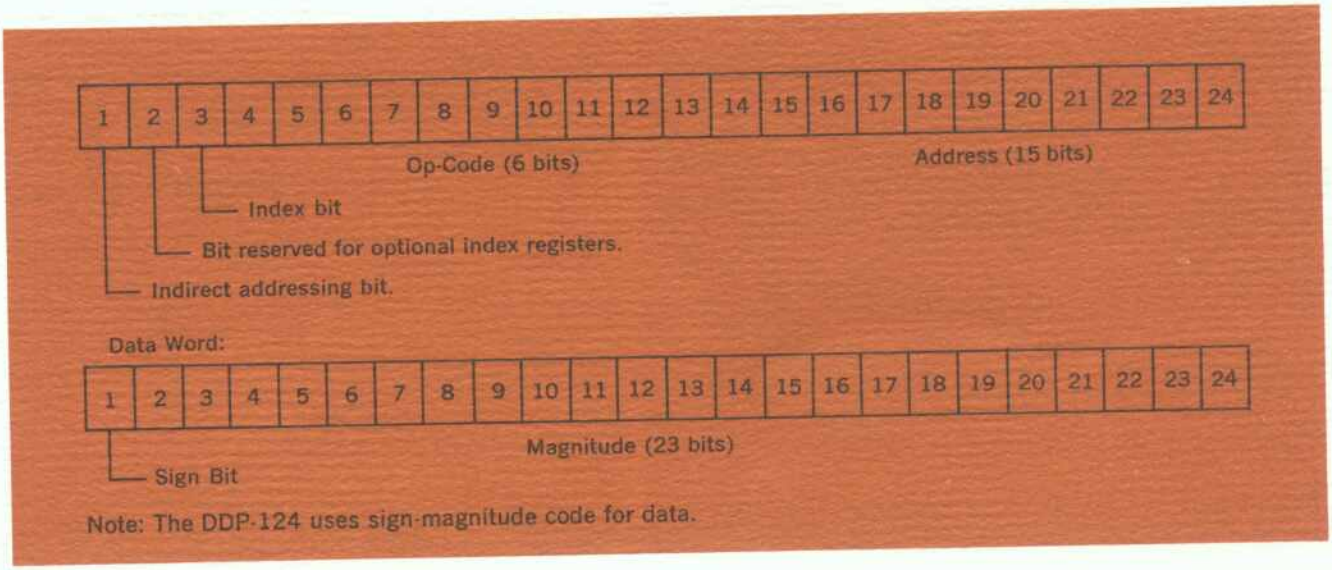
Complete set of utility and service routines.
Software compatible with DDP-24 and DDP-224.

INSTALLATION

Power	single phase, 115 ± 10 volts 60 cps single phase
Operating temperature range:	10°C to +40°C.
Humidity range:	to 90%

Requires no air conditioning, wiring, subflooring or other special installation preparation.

POWER
Regulated power supplies are included in the DDP-124; no additional regulation is required if input power is within the stated specifications. Overall supply voltage variations due to worst case combinations, input line voltage changes, dc load regulation, dynamic load regulation, ripple, long term drift, etc., are less than 2% (well within the ±10% circuit tolerances).



Note: The DDP-124 uses sign-magnitude code for data.

INTERNAL COMPUTER ORGANIZATION

Functionally, the computer consists of four units:

- Arithmetic unit
- Control unit
- Input-output unit
- Memory unit

Computer operations take place in parallel.

ARITHMETIC UNIT

Consists of the A-register, B- register and Adder. The Z-register may also be considered part of the arithmetic unit at certain times.

A Register — Main arithmetic register of the computer.

B Register — Auxiliary arithmetic register.

Z Register — A 24 bit register receiving its information from the memory. After a command fetch the 15 least significant bits contain the address of the instruction, or the 15 bit operand in some cases. After an operand fetch the Z-register contains the operand and then is to be considered part of the arithmetic unit.

Adder — The logic structure providing for sums or differences during computations.

CONTROL UNIT

Consists of the program counter (P-register), op-code register (O-register), index register (X-register), shift counter (S-register), transfer bus, and control unit clock. The Z-register can sometimes be considered part of the control unit.

Program Counter — (P) Contains the memory location of the next instruction to be performed. Normally its contents are incremented with a ONE each time a new command of the computer is fetched out of memory. In case of a transfer in the program the program counter will be filled with the memory location to which the program shall transfer.

Op-Code Register — (O) Contains the 6 bit op-code for the instruction being performed, the index bit and the indirect address bit.

Index Register — (I) If the index register is specified by an instruction, its contents are added to the address of the instruction and the result becomes the effective address.

Shift Counter — (S) Used with the shift instructions to indicate the number of shift steps.

Transfer Bus — A gating structure to which computer registers are connected both as source and destination. In this way, transfer of information of any one register to another can take place by simultaneously opening the proper paths from one register to the transfer bus and from the transfer bus to the other register. The transfer bus allows simple inter-connections between the many different computer registers and the adder.

Control Unit Clock — This timing pulse generator is needed for the different operation sequences of the command executions.

INPUT-OUTPUT

This section corresponds to the input-output bus structures, character-buffer, the decoding of the incoming sense signals for test by the SKS instruction (Skip for Sense Line Not Set), and the outgoing control signals of the OCP command (Output Control Pulse), and the interface with the I/O typewriter, paper tape reader and punch.

Data transfer of input-output information into or out of the DDP-124 takes place with a separate input-output transfer bus connected to the computer transfer bus. This allows a maximum flexibility and expandability of input-output capabilities, and provides direct communication between the input-output and arithmetic sections.

MEMORY

Standard DDP-124 memory is a magnetic core unit of 4,096 words of 24 bits each. It contains information register (MIR) and address register (MAR). The memory transfers data to and from the DDP processor via the memory bus. The memory of the DDP-124 can be optionally expanded to 32,768 words by adding modules.

TIMING

Parallel operation of the DDP-124 is synchronous and controlled by a 2.86 mc clock. Memory has a 1.75 microsecond cycle time and 0.8 microsecond access time. DDP-124 has a computation rate of 285,000 additions per second. Most instructions which do not access memory are executed in 1.75 microseconds. Input and output can occur asynchronously and be interleaved with processing at transfer rates up to 285,000 (24 bit) words per second in the standard system.

OPERATION AND MAINTENANCE

CONTROL PANEL

A convenient operator control panel with displays and controls is included with the 124 cabinet. Binary displays are grouped for octal representation. (Remote control console optionally available.)

MAINTENANCE PROVISIONS

Maintenance displays, toggles, and control buttons are provided for computer maintenance and diagnostics.

Facilities include such features as:

Content Display of:

- CONTROL CLOCK
- SHIFT COUNTER
- CONTROL FLIP FLOPS

Control Switches for:

- SINGLE STEP
- EXECUTE
- FETCH
- INTERRUPT ON/OFF
- CLOCK
- ON/OFF

Convenient access is provided to all circuits. The design is oriented to isolate and repair failures in minimum time.

COMMAND STRUCTURE

The flexible DDP-124 command structure includes a multiply command, and a multiple precision step command for very simple and fast double, triple and other multiple precision routines. The jump-store command allows for subroutine linkage and easy nesting of subroutines. For status check or alarm-limit comparisons the DDP offers powerful conditional program transfer commands, comparing the contents of the arithmetic A-register and a specified memory cell.

INSTRUCTION REPERTOIRE

(Execution times include instruction and operand access)

TYPE	CODE		TIME	DESCRIPTION
	OCTAL	MNEMONIC	(μsec)	
LOAD AND STORE	03	STB	3.5	Store B
	05	STA	3.5	Store A
	06	STD	3.5	Store Address portion of A
	23	LDB	3.5	Load B
	24	LDA	3.5	Load A
	55	TAB	1.75	Transfer A to B
	57	IAB	1.75	Interchange A and B
	60	CRA	1.75	Clear A
ARITHMETIC	10	ADD	3.5	Add
	11	SUB	3.5	Subtract
	30	SMP	3.5	Step Multiple Precision
	34	MPY	14.0*	Multiply
	35	DIV	22.0**	Divide
	62	RND	1.9	Round A
SHIFT	40	ARS	2.8 + x	A Right Shift
	41	ALS	2.8 + x	A Left Shift
	42	LRR	2.8 + x	Long Right Rotate
	43	LLR	2.8 + x	Long Left Rotate
	44	LRS	2.8 + x	Long Right Shift
	45	LLS	2.8 + x	Long Left Shift
	47	LGL	2.8 + x	Logical Left Shift
JUMP	12	SKG	4.2	Skip if A Greater
	13	SKN	4.2	Skip if A Not Equal
	25	JRT	3.5	Jump Return
	27	JST	3.5	Jump and Store Location
	70	JPL	2.1	Jump if A Positive
	71	JZE	2.1	Jump if A Zero
	73	JOF	2.1	Jump on Overflow
	74	JMP	2.1	Unconditional Jump
LOGICAL	15	ANA	3.5	AND to A
	16	ORA	3.5	OR to A
	17	ERA	3.5	Exclusive OR to A
INDEX	54	ADX	1.75	Add to Index
	56	LDX	1.75	Load Index
	63	TAX	1.75	Transfer A to Index
	66	STX	3.5	Store Index
	67	IRX	5.25	Increment, Replace, Load Index
	72	JIX	2.1	Jump on Index
	75	JXI	2.8	Jump on Index Incremented
INPUT/ OUTPUT	07	INM	3.5 min.	Input to Memory
	22	OTM	3.5 min.	Output from Memory
	50	OTA	2.1 min.	Output from A
	52	INA	1.75	Input to A
	53	OCP	2.1	Output Control Pulse
	61	SKS	4.3	Skip if Sense Line Not Set
CONTROL	00	HLT	1.75	Halt
	02	XEC	1.75	Execute
	77	NOP	1.75	No Operation

* average ** Fixed $x = (n-4)\,0.35$

INPUT-OUTPUT

DDP-124 offers a unique combination of input-output capabilities, specifically adapted to on-line, real-time system applications. These require a fast input-output data transfer and easy adaptation of the computer to allow its efficient operation in many different system configurations. For this DDP-124 provides a variety of input-output channels, four different input-output modes of operation; easy, modular expansion of its I/O capabilities and high data transfer rates.

DDP-124 allows direct data transfer into or out of either the main arithmetic register or any memory location with a single command. Transfer of character inputs or outputs into or out of the arithmetic register can be controlled by a mask included with the instruction. Any combination up to 6 bits of the character data can be read or generated. This allows flexible formatting.

I/O rates of up to 285,000 24-bit parallel words per second can be handled with the DDP-124.

Internal organization of the input-output system of the DDP-124 is modular and allows flexibility and expandability. The Option Interface Unit (OIU) facilitates interconnection of the central processor with DDP-124 optional peripheral devices and I/O expansion options. The OIU also simplifies field expansion.

INPUT-OUTPUT MODES

1. **Ready Mode** — Computer program tests periodically for channel-ready signals. If the test is successful the program will transfer to the proper subroutine; if not, the program carries on with the current routine. Simultaneous testing of up to 12 I/O channel-ready signals is possible.

2. **Interrupt Mode** — Computer program is automatically interrupted and a program jump takes place to memory location directly related to the interrupt concerned. On completion of the interrupt subroutine the main program resumes at the interrupted point. Any I/O channel can be operated either in ready-mode or interrupt mode. Up to 16 interrupt lines may be provided, each with unique memory destinations.

Multi-level interrupt functions are performed when a remote signal (interrupt line) causes a particular computer routine in memory to be executed. This routine may, in turn, be interrupted by a higher priority line which automatically starts a new computer routine. The completion of the higher priority interrupt routine will return the computer operation to the point where the lower priority routine was interrupted. This mode of operation is called interrupt of interrupt.

3. **Single Line Data Transfer** — Single bit input from sense lines or output for control signals are handled by properly coded DDP commands.

4. **Direct Memory Access** — Optional input-ouput mode for direct access into or out of successive memory locations independent of the computer program, after being initially set up. Direct Memory Access (DMA) channels have priority over the control unit of

DDP

PERIPHERAL EQUIPMENT OPTIONS	INPUT/OUTPUT OPTIONS	STANDARDS	OPTIONAL
• Magnetic tape unit tape transport 45 ips • Magnetic tape unit transport 75 ips • Card reader • High speed line printer • Digital plotter • Card punch	• Direct memory access (DMA) channel • Word forming buffer • 16 priority level interrupt lines • Up to 64 input sense lines • Up to 64 output control pulse lines • Character buffer registers • Parallel I/O channels	• 4096-word memory • Index register • Indirect addressing • Operator's console & maintenance panel • Complete programming package • Support services • Electric typewriter • Paper tape reader, 300 cps • Paper tape punch, 110 cps	• Memory expansion to 32,768 words • Additional index registers • Remote console

the computer for memory access. Data rates up to 285,000 words per second (24 bits) are possible. The main computer program cannot obtain access to memory while the DMA channel injects into or reads out of memory.

INTERNAL EXPANSION

Core Memory — Standard 24-bit, 4,096-word core memory is expandable to 32,768 words. All words are directly addressable. Memory operates under control of DDP-124 control unit or direct memory access input/output control unit (DMA).

Index Registers — Two additional 15-bit flip-flop index registers can be added.

INPUT/OUTPUT EXPANSION

Direct Memory Access (DMA) — Input/output control unit, which includes a parallel information buffer register and input/output channel and address selection register, injects into or reads out of memory independently of the control unit, after initial setup by the computer. Transfers up to 285,000 24-bit words a second. The DMA has priority over the control unit for memory access. If addressing occurs simultaneously, the DMA obtains access to memory for a cycle to inject or read a word.

Word Forming Buffer — Automatically builds a computer word from input characters and checks parity. Generates output characters with parity from computer words. Special control specifies number of 6-bit characters to be transferred (1, 2, 3 or 4 characters per word transfer).

Interrupt Lines — Up to 16 interrupt lines can be provided, each with unique memory destinations and priority assignments of interrupt levels. A higher level will interrupt execution of a lower level routine. A lower level will not interrupt a higher level routine. Multi-level interrupt option is available in 2 groups of 8 lines.

The option includes capability for individually enabling or inhibiting the sixteen interrupt lines.

Sense Lines — Single-bit input lines (sense lines) are available in 8 groups of 8 which enable the computer to determine the status of external devices. The sense lines may be tested under program control. Also available are 6 sense switches on the control panel with associated sense lines for manual input of control data. Any or all of the sense switches may be tested simultaneously. The presence of dc signals on any of the 64 sense lines indicates the busy status of external devices, and this is sensed by means of the SKS command.

Output Control Pulses (OCP) — Up to 64 output control pulses can be addressed and generated by the DDP-124. The pulses may be used by themselves to perform programmed control functions. An OCP is a 0.5 microsecond output pulse, available in groups of 8. The OCP pulse is initiated by the execution of a properly coded OCP instruction.

Character Input/Output Buffer Registers — A large number of character buffer registers can be added to the DDP-124. These 6-bit flip-flop registers check and assign parity, and operate in ready mode or with interrupt lines. Options include:

1. 6-bit character buffer register and channel for either input or output with parity checking or assignment.
2. Time shared 6-bit character input/output buffer register and channels with parity checking and assignment.

Parallel Input/Output Channels — A large number and variety of parallel 24-bit input and/or output channels are available as options. Options include:

1. Parallel input channel operable in ready or interrupt mode.
2. Parallel output channels operable in ready or interrupt mode.
3. Parallel input/output buffer register and channels operable in ready or interrupt mode.
4. Time shared parallel input and output buffer register and channels operable in ready or interrupt mode.

COMPREHENSIVE PROGRAMMING AND SERVICES

SOFTWARE

A comprehensive software package which will satisfy the needs of the experienced programmer or the occasional user is supplied with the DDP-124 at no extra cost. The programming languages and utility routines have been designed to conform with the most widely used programmer's standards and conventions. The same high degree of quality that is in the DDP-124 hardware is provided to the user in software — programming facility has been the criterion. All software is compatible with 3C's DDP-24 and DDP-224.

Fortran IV with Boolean Capabilities. FORTRAN is the best known, most widely used programming language. FORTRAN IV compiler has been designed to accept statements and translate them into the machine language of the DDP-124, and will also translate Boolean statements that provide capabilities for logical operations with full words or any part of a word all in the same FORTRAN program. These capabilities are provided for the basic system (4K memory, paper tape reader and punch and typewriter).

DAP — Symbolic Assembly Program. This two-pass assembly program will translate a language that is more closely oriented to the machine language of the DDP-124. The language format conforms with SHARE standards and DAP accepts all of the basic instruction mnemonics plus extended machine and pseudo-operations. The following are some of the operations that are included in the language and are familiar to most programmers: ABS, BCI, BES, BSS, DEC, EQU, OCT, ORG. Object output may be either relocatable or absolute; symbolic output is in the form of a side-by-side listing on the typewriter (unless the programmer specifies that he doesn't want a listing). Of course subroutine linkage is provided that will allow FORTRAN IV compatibility.

DIP — Scientific Interpretive Programming System. DIP is a programming aid especially designed for the occasional user. With only half a day's training, personnel with minimal programming experience can use the DDP-124 for scientific computation with ease. As a training tool, DIP's simplified structure, which eliminates number system conversions, scaling and other rules unfamiliar to the novice, makes it helpful as an introduction to the fundamentals of digital programming.

Debug — Program Debugging Aid. This is a self-loading program that interprets commands entered through the typewriter. This program would typically remain in memory most of the time and would perform functions such as the following upon demand: dump specified memory locations; load a program; load consecutive memory locations; punch out memory; clear selected memory location; etc.

Utility Routines. Includes paper tape I/O routines, typewriter I/O routines, program load routines, formatted memory dumps, data conversion routines, card I/O routines, magnetic tape routines, etc.

Service Routines. Includes double precision floating point routines, double-precision fixed-point routines, transcendental functions, program diagnostic routines, hardware diagnostic routines, etc.

USER SERVICES

Support services, included with purchase of the standard DDP-124, are designed to provide the user with continuing service and flow of information after delivery.

Programmer Training Course. Includes instructions for programming in machine language, an introduction to DDP-124 programming systems, and instructions in DDP-124 operation. One-week course, provided quarterly at no cost.

Maintenance Training Course. Includes operation, logic design, diagnostic procedures, diagnostic routines, preventive maintenance procedures and a logistic support program for personnel with previous digital logic design knowledge. Four-week course, provided quarterly at no cost.

Logistic Support Program. Provides after-delivery service and information to DDP-124 users. Statistical compilation of field operating experience based on a failure reporting program, technical notes on system hardware modification, technical notes on programming modification, spare parts provisioning, and stocking of programming forms and paper tapes are provided.

Service. Up to one week installation service is provided with each DDP-124. Programming, maintenance and systems engineering services are available on a contract basis.

DDP-124
SUMMARY OF STANDARD OPTIONS AND PERIPHERAL EQUIPMENT

MODEL NO.	DESCRIPTION
124-00	DDP-124 general purpose digital computer, indirect addressing, hardware index register, hardware multiply and divide, 300 cps paper tape reader, 110 cps paper tape punch, I/O typewriter and integrated console.
124-03	4096 word core memory module.
124-04	8192 word core memory module.
124-06	Remote operator's console (in lieu of integrated console).
124-15	Additional, 15-bit, hardware index register.
124-20	Direct Memory Access (DMA) I/O control unit with 24-bit parallel buffered I/O channel.
124-22	Word Forming Buffer (WFB) with format control for 6-bit character; 1, 2, 3 and 4 characters per word; generates and checks parity.
124-24	Group of 8 priority level interrupt lines with selective enable and disable of interrupt.
124-27	Group of 8 sense lines (maximum of 8 groups of 8 lines).
124-28	Group of 8 output control pulse (OCP) lines (maximum of 8 groups of 8 lines).
124-30	Additional I/O character buffer and channel.
124-32	Parallel input channel (24 bits).
124-33	Parallel output channel (24 bits).
124-34	Parallel I/ O buffer and channels (24 bits).
124-40	Magnetic tape control unit and one transport, 45 ips, 200 and 555 bpi, 25 kc. IBM 729 Mod II compatible.
124-40-1	Magnetic tape control unit and four transports, 45 ips, 200 and 555 bpi, 25 kc.
124-41	Magnetic tape control unit and one tape transport; 75 ips; 200, 555 and 800 bpi; IBM 729 Mod II compatible.
124-60	Card reader, 100 cpm.
124-61	Card reader, 200 cpm.
124-62	Card punch, 100 cpm.
124-64	Medium speed line printer, 120 columns, 300 lines per minute.
124-70	Digital plotter, 300 increments per second.
124-95	Option Interface Unit (OIU).

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