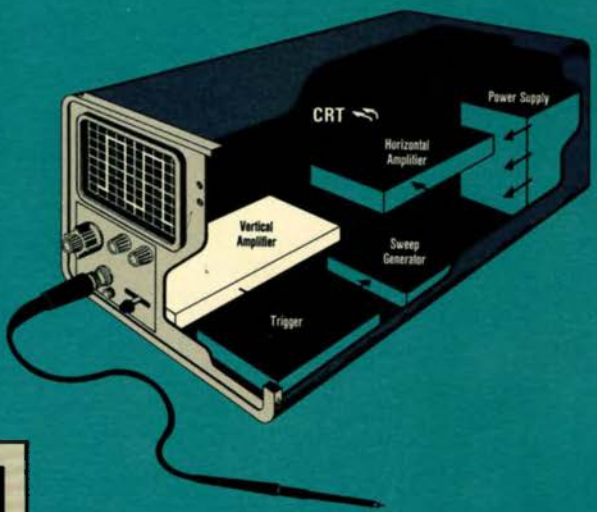
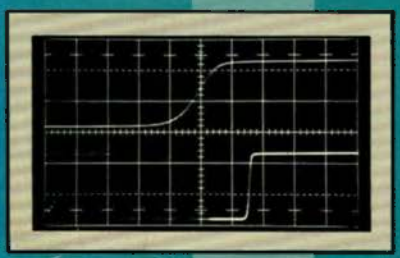
Vertical Amplifier Circuits





Circuit Concepts Series

OSCILLOSCOPE VERTICAL AMPLIFIERS

BY

BOB ORWILER

CIRCUIT CONCEPTS

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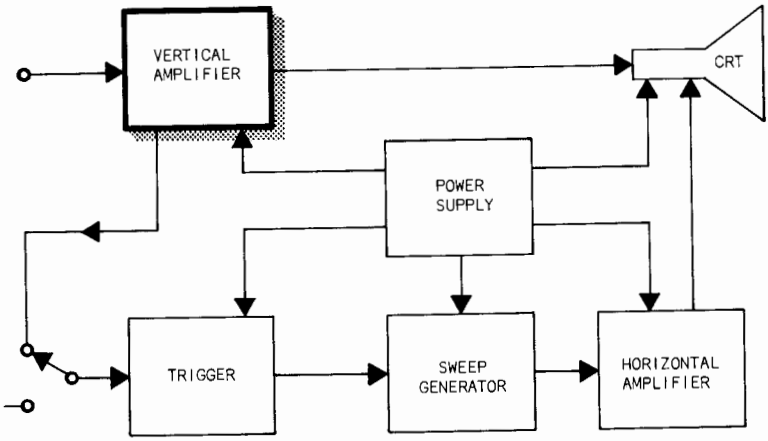

VERTICAL
AMPLIFIER
CRT
POWER
SUPPLY
TRIGGER
SWEEP
GENERATOR
HORIZONTAL
AMPLIFIER

INTRODUCTION

In a study of conventional oscilloscopes, the various circuits of the instrument fall into general groupings: the power supply, cathode-ray tube, trigger circuit, sweep generator, horizontal amplifier and the vertical amplifier.

Each performs an important function. Combinations of individual contributions determine instrument performance.

power supply

The *power supply* converts some form of available power (depending on the type and location of the instrument) to DC operating potentials for all the active circuits of the oscilloscope. Regulation holds most of these potentials to narrow tolerances, guaranteeing precise circuit performance. A power supply might also contain filament power for vacuum-tube circuits, overload protection and facilities for adapting the instrument to various local power conditions.

cathode-ray tube

The *cathode-ray tube* (CRT) displays light on a two-dimensional phosphor screen. It conveys intelligence in the form of alphanumerics, picture images or graphs. Graphical presentations offer an analytical approach: Actual measurements taken with a graticule along the "X" and "Y" screen axis.

The *CRT electron gun* is sealed inside an envelope. A vacuum minimizes collisions between free gas particles and the electron beam. High-voltage power supplies create controllable electrostatic fields which accelerate free electrons from the heated cathode to form an electron beam. The beam of electrons then transit an electron lens which converges or focuses the beam on a phosphor screen. When the high-velocity electrons collide with phosphor atoms at the focal point, photons of light emit towards the viewer.

Varying the electrostatic fields between a set of "X" and "Y" deflection plates positions the light source on the screen. Thus the electron beam creates a display anywhere within the viewing screen area. Since electrons have an extremely small mass, they can be deflected or scanned over the entire screen area millions of times per second. This permits the viewer to observe changing phenomena in real time.

The CRT must not unduly load either the vertical or horizontal amplifier nor require a greater dynamic-deflection range of voltage than the amplifiers can supply. In practice, the CRT and deflection amplifiers are designed together for maximum performance and efficiency.

trigger circuit

Input signals take a wide variety of shapes and amplitudes, many unsuitable as sweep-initiating triggers. For this reason a *trigger circuit* converts these signals to pulses of uniform amplitude and shape. This trigger circuit makes it possible to start the sweep with a pulse that has a constant size, eliminating variations of the sweep-circuit operation caused by changing input signals. The operator now uses either slope of the waveform to start the sweep, selects any voltage level on the rising or falling slope of the waveform, and, in some instances, eliminates selected frequencies of the input signal with ease and repeatability.

sweep generator

The *sweep generator* produces a sawtooth waveform for processing by the horizontal amplifier which then deflects the CRT beam. The sweep generator produces a sawtooth waveform, with the proper rate-of-rise, amplitude and linearity, suitable as a time-measuring reference.

horizontal amplifier

Primarily, the *horizontal amplifier* converts the time-base ramp, developed in the sweep generator, to deflection voltage for the horizontal CRT deflection plates. The resulting trace is the reference for Y-T displays (voltage plotted as a function of time). In those instruments offering X-Y capabilities (where both X and Y inputs are dependent variables) the horizontal amplifier reacts to the external (X) input as a linear amplifier. It exhibits a frequency response comparable to that of the vertical amplifier. Additionally, the horizontal amplifier provides DC-level and amplifier gain controls which permit positioning of the horizontal trace and sweep magnification (expansion) respectively. The latter facility extends instrument sweep speed without imposing additional sweep-rate requirements on the sweep generator.

vertical amplifier

The *vertical amplifier* determines the useful bandwidth and gain of the instrument. Vertical amplifiers take three general forms: a fixed vertical, a complete vertical in a plug-in form or a fixed main vertical amplifier preceded by a plug-in preamplifier.° Selection of plug-ins allows a range of characteristics. An additional type of instrument takes the drive directly to the CRT plates without passing through any type of amplifier.

The general-purpose oscilloscope provides a faithful display of an input voltage. For meaningful results, displayed waveforms contain few aberrations and these but a few percent of the total waveform amplitude.

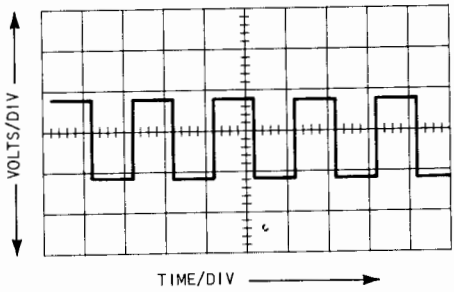


Fig. 1-1. Oscilloscope display.

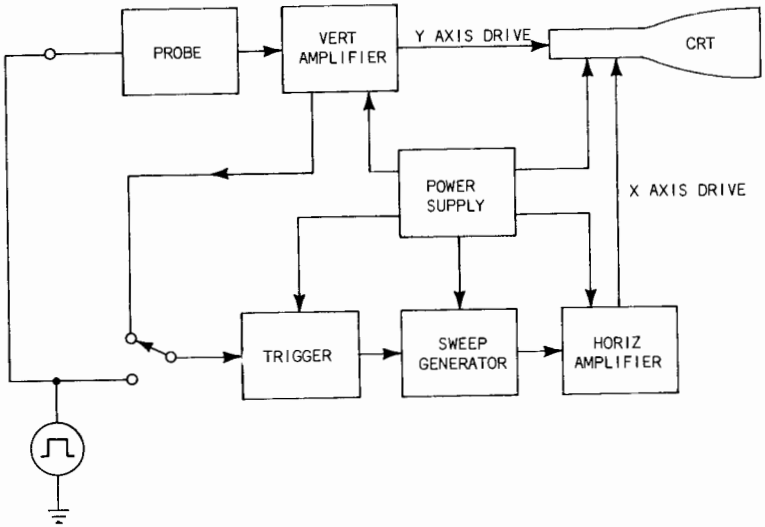


Fig. 1-2. Basic oscilloscope block diagram.

1

VERTICAL AMPLIFIERS

Vertical amplifiers meet requirements briefly summarized below:

1. Buffer the signal source (probe) and the CRT.

2. Provide various modes of operation such as: direct or AC coupling, multiple trace, and, perhaps, selectable differential modes.

3. Finally, the amplifier faithfully reproduces voltage waveforms within specified *risetime-bandwidth-amplitude* limits.

Why these items are important and how they are accomplished by Tektronix is what this book is about.

graticule

An oscilloscope graphically displays signals of interest, as shown in Fig. 1-1. Here periodic rectangular pulses appear superimposed on a grid called the graticule. Equal divisions divide the graticule X and Y axes. Fig. 1-1 shows ten major *horizontal (X)* divisions and six major *vertical (Y)* divisions. Small markings along the center lines describe minor division dimensions at 20% of a major division.

The horizontal base is calibrated in units of time per division; the vertical in units of voltage per division. For example, if each vertical increment is 0.5 volts and horizontal is 0.5 milliseconds per division, then Fig. 1-1 depicts a 1-volt pulse train with pulses recurring each millisecond.

Accurate information from *both* horizontal and vertical circuits creates faithful reproductions of the input waveforms. To accomplish this an oscilloscope generally requires the basic blocks shown in Fig. 1-2.

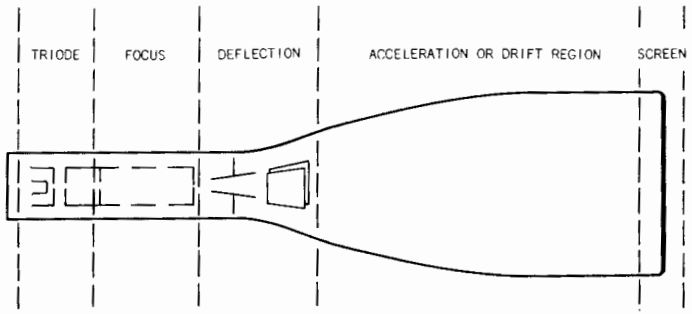


Fig. 1-3. CRT sections.

CRT

Cathode-ray tubes present a reactive load to deflection amplifiers. CRT construction and applied voltages cause a beam of the electrons, emitted by the CRT cathode, to form. The beam forms during electron travel from cathode to phosphor-coated faceplate. Energy contained in this concentrated mass of electrons striking the faceplate or screen is partially converted to light. Deflecting the beam vertically (Y) and horizontally (X) graphically reproduces waveforms. Deflection may be either electrostatic or electromagnetic. Since very few oscilloscopes use magnetic deflection, this book covers electrostatic deflection only.

Two pairs of plates mounted at right angles, as shown in Fig. 1-3, deflect the beam when energized. Leads from each plate penetrate the CRT envelope for connection to external excitation sources. The beam in the CRT shown passes first between the vertical deflection plates, then the horizontal.

A CRT and power supply alone function as a crude oscilloscope. Fig. 1-4 shows such an arrangement.

Horizontal plates connect to D1-D2 and vertical plates to D3-D4. D1, D2 and D4 connect to a common voltage, shown as ground. D3 connects to a signal source represented by the three-position switch. Applying zero volts to D3 centers the beam. Throwing the switch to +V attracts the beam toward D3. Repelling occurs with -V applied to D3.

Connecting either D1 or D2 to a signal source results in horizontal deflection.

A vertical deflection system like this one has one advantage -- simplicity. Unfortunately, there are disadvantages. Some are:

Low sensitivity.

Signal source loading.

Nonlinearity.

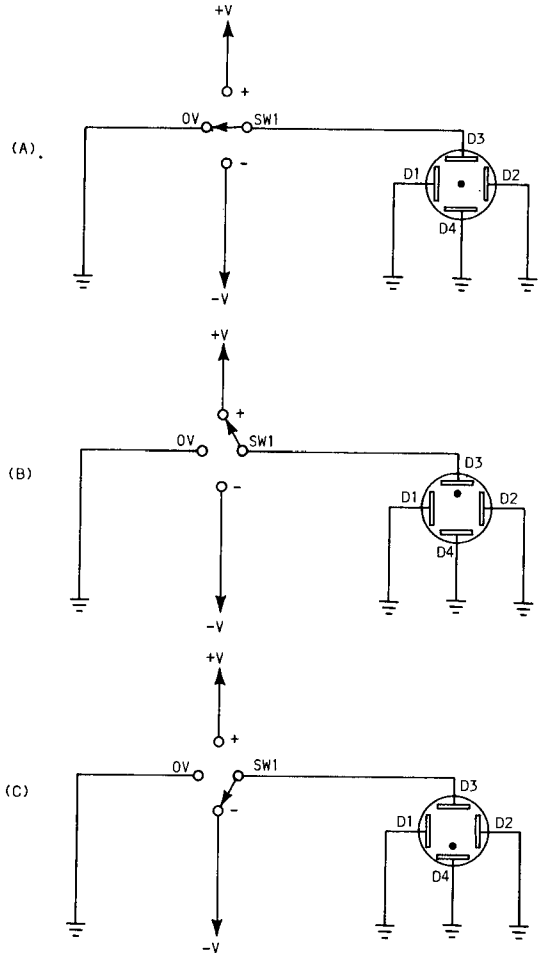


Fig. 1-4. A vertical system utilizing the CRT only.

deflection sensitivity

One needs a means of measuring deflection. Assume a vertical scale inscribed on the CRT faceplate. Scale increments begin at the center extending three divisions up and three divisions down. One needs to know the *deflection sensitivity* to calibrate the scale; i.e., how many scale divisions each volt deflects the electron beam. If divisions were scaled one centimeter apart (a representative dimension) the ratio cm/V expresses deflection sensitivity. 0.1 cm-per-volt represents a general deflection sensitivity. This restricts practical direct measurements to one volt minimum signal. Deflection sensitivity and screen diameter fix the maximum measurable level.

signal source isolated

Inserting a probe and an amplifier increases deflection sensitivity and isolates signal source and CRT. The deflection plates appear as capacitive circuit components. Connected directly this reactance might drastically change monitored circuit characteristics. The probe - vertical amplifier - CRT combination presents a high impedance to the circuit under test, allowing measurements to represent nominal circuit conditions. This vertical deflection system by including an amplifier implies voltage gain. Vertical amplifiers can increase deflection sensitivity. Further, the amplifiers contain calibrated step control of gain and attenuation extending input deflection sensitivity from, perhaps, 0.04 div/V to 100 div/V in several steps.

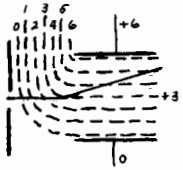
sensitivity improved

deflection factor

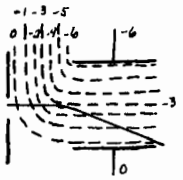
Division-per-volt terminology usually requires calculation for meaningful observations. Tektronix, therefore, uses *deflection factor* to conveniently express sensitivity. Deflection factor is the inverse of deflection sensitivity and is listed as volts-per-division (V/div): The CRT was earlier assigned a deflection sensitivity of 0.1 div/V. This is a deflection factor of 10 V/div. Including an amplifier increased vertical-deflection sensitivity to 100 div/V -- in terms of deflection factor, 10 mV/div. Rather than say the input sensitivity is selectable in eight steps from 0.04 div/V to 100 div/V, one states the steps, in terms of deflection factor, as from 25 V/div to 10 mV/div. Each observed division of CRT deflection now reads directly.

linearity improved

Almost all oscilloscopes use push-pull vertical and horizontal amplifiers. Push-pull CRT drive combats deflection nonlinearity. This is because single-ended drive develops a zero-volt equipotential surface near the grounded plate, while push-pull deflection centers the zero-volt equipotential surface between plates.

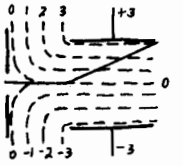


Consider a single-ended system with a positive signal voltage applied. An electron approaching the plates encounters positive equipotential surfaces; axial velocity therefore increases. Assume this results in two divisions of deflection above center.



Nonlinearity shows upon application of an equal-amplitude opposite-polarity signal. An electron now decelerates as it approaches the deflection plates due to negative equipotential surfaces encountered. The beam then deflects further below center, perhaps by one division, than in the case above. Nonlinearity to this degree is unacceptable.

Push-pull voltages applied to both D1-D2 and D3-D4 eliminate nonlinearity of single-plate drive. Equal signal voltages of opposite polarity appear on the plates. Deflection voltage develops across the plates but the zero-volt equipotential surface remains centered between plates. An electron approaching the deflection plates encounters a surface approximating anode voltage. It then experiences neither acceleration nor deceleration. Deflection signals cause equal radial velocity either side of center.



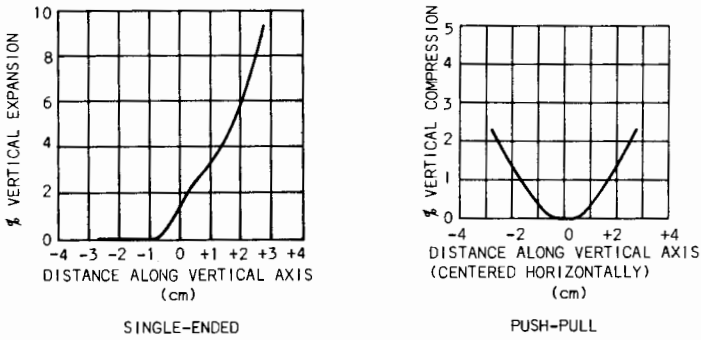


Fig. 1-5. Linearity comparison.

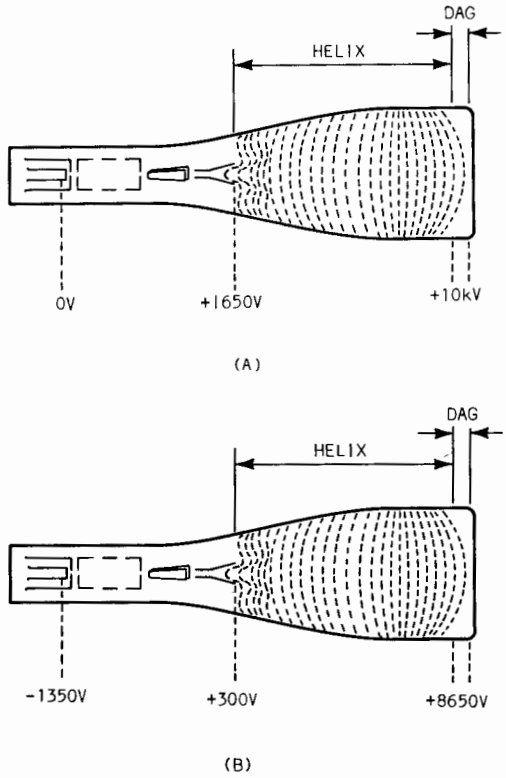


Fig. 1-6. Locating the deflection-plate voltage gradient (not to scale).

push-pull and single-ended linearity contrasted

Each type of CRT does exhibit characteristic nonlinearity. However, dramatic improvement results from push-pull drive. Compare the graphs of Fig. 1-5 to contrast the linearity between push-pull and single-ended deflection. These graphs are of the same tube type under nearly identical conditions. Even the linearity characteristics vary between drives. Push-pull suffers a low percentage of compression; single-ended creates unacceptable expansion.

CRT design holds deflection-plate rest potential to specific limits. This calls for deflection amplifiers designed to operate around these levels.

The voltage gradient between CRT cathode and aquadag (dag) creates the restrictive deflection-plate operating levels. Fig. 1-6A is a cut-away CRT which includes the equipotential surfaces in the post-deflection-acceleration (PDA) region. Gradients develop between the cathode and the low-voltage end of the helix. The deflection plates set in an area bisected by the 1600-to-1700-volt equipotential surface. To prevent severe distortion of surfaces in the PDA region, external deflection-plate leads should connect to a voltage source equal to the internal voltage environment -- in this case between 1600 and 1700 volts. Deflection amplifiers driving these deflection plates maintain quiescent deflection-plate voltage 1600 to 1700 volts above the CRT cathode.

Operating amplifiers above 1.5 kV is a bit unreasonable. This among other reasons, is why operating voltages are as shown in Fig. 1-6B. Operating with the cathode below ground reduces the positive operating level, required by the deflection plates, to a reasonable value.

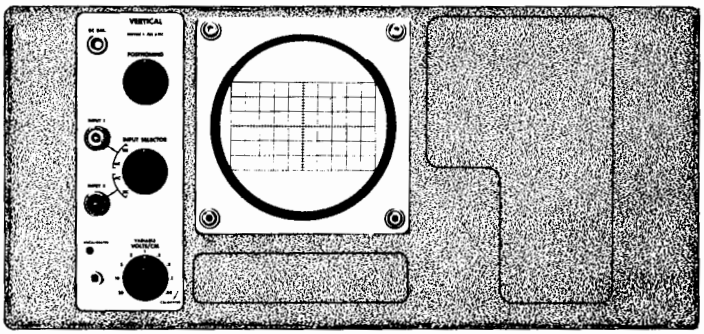
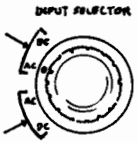


Fig. 1-7. Oscilloscope vertical controls.

operating controls

Fig. 1-7 is a representative oscilloscope with all controls, other than vertical, blanked out. The instrument illustrated includes basic front-panel vertical-amplifier controls: Vertical POSITION, INPUT SELECTOR, VOLTS/CM selector and the VARIABLE control.

Adjusting the vertical-POSITION control moves the CRT display up and down along Y axis. Centering the vertical POSITION and restricting the input to zero volts centers the vertical CRT display.



The INPUT SELECTOR allows the operator to choose either of two input connectors. It further extends his choice to a direct connection (DC) or capacitive coupling (AC) from input connector to vertical amplifier.

VOLTS/CM and VARIABLE mount on concentric shafts. The VOLTS/CM selector is shown as an input deflection-factor selector. One selects, in nine calibrated steps, input deflection factors between 0.05 V/cm and 20 V/cm. This is the deflection factor at the input connectors. The continuously adjustable VARIABLE provides between-step, uncalibrated, deflection-factor control: With the VOLTS/CM set to 1, the VARIABLE may set input deflection factor at any point between 1 V/cm and approximately 2 V/cm. This control slips into a detent at the extreme clockwise position allowing calibrated input deflection factor. Placing the VARIABLE in detent, one reads deflection factor as indicated by the VOLTS/CM selector. These controls and connectors are a part of circuits generally located in the *vertical preamplifier*.

vertical preamplifier

Subdividing vertical amplifiers into preamplifiers and main amplifiers helps simplify concept development. Two tests separate vertical preamplifiers and main vertical amplifiers: (1) Circuits which contain front-panel controls most commonly occur in preamplifiers, and (2) a vertical circuit into which a connector could be inserted to allow preamplifier plug-in capability is a main amplifier.

main vertical amplifier

The *main-vertical-amplifier* tag evolved from main-frame vertical amplifier. The advent of plug-in capability required a vertical-amplifier separation -- one portion removable and the other a permanent part of the oscilloscope *main frame*, thus the tag: *main frame* vertical. Common usage shortened the name by dropping "frame."

The vertical preamplifier acts upon signals appearing at the input connector. It then converts the signal to push-pull. Vertical preamps also provide gain as selected with the volts-per-division selector. Preamplifier gain is that necessary to provide a constant deflection factor at the preamplifier output. A push-pull signal of 100 millivolts-per-division is representative. The main vertical amplifier then is a push-pull amplifier of fixed gain. Amplification is as needed to match the constant input deflection factor to that of the CRT. An internal gain calibration frequently constitutes a part of the main vertical amplifier.

gain

$$A_v = \frac{V_o}{V_{in}}$$

$$A_v = \frac{DF_o}{DF_{in}}$$

Gain in this book refers to voltage gain. Since oscilloscope vertical amplifiers are basically voltage-actuated devices, gain in terms other than voltage has little direct meaning. A simple expression, output voltage divided by input voltage, defines voltage gain. Substitute deflection factors for voltages in the gain ratio to determine required amplifier gain. As an example, assume the CRT deflection factor is 20 V/div and the VOLTS/DIV selector sets at 1 V/div. Ratio $\frac{20\ V/div}{1\ V/div}$ expresses the required vertical-amplifier gain. Overall vertical-amplifier gain may be unity, less than unity or greater than unity.

One seldom refers to gain directly when describing the characteristics of a vertical amplifier. He does describe input deflection factor such as: the VOLTS/DIV selector of Fig. 1-7 allows selection of input deflection factors between 0.05 VOLTS/DIV and 20 VOLTS/DIV or, as used earlier, as an expression of amplifier sensitivity. This partially describes the limits or capabilities of the instrument.

bandwidth

Bandwidth expands oscilloscope descriptions. Bandwidth, applied to a specific vertical amplifier, defines the frequency limits of calibrated input deflection factors. That is, a one-volt input signal, to a vertical amplifier set at one volt-per-division input deflection factor, deflects the CRT one division *only* if the signal frequency is within the capabilities of the vertical amplifier. Oscilloscope bandwidth specifications express frequency capabilities of the vertical amplifiers.

One type of Tektronix instrument is advertised as a DC-to-10 MHz oscilloscope. In the same advertisement, under vertical characteristic summary: bandwidth DC-coupled, DC to 10 MHz. AC-coupled, 2 Hz to 10 MHz. This specification should have the same meaning to everyone.

However, an oscilloscope vertical amplifier must also be capable of faithfully reproducing complex waveshapes, and this requires good transient response characteristics. Stated another way, we need to have a linear phase-versus-frequency response.

bandwidth plot

Fig. 1-8 graphically shows the described bandwidth. One constructs a graph of this type by applying, to the vertical amplifier input, signals of varying frequency but constant amplitude. He then plots displayed amplitude versus input frequency. The solid line of Fig. 1-8 represents a bandwidth of DC-to-10 MHz. Displayed signal voltage remains essentially the same between 0 Hz (DC) and 1 MHz.

Refer to this as 0-dB attenuation. As the input frequency increases (input voltage held constant) the displayed signal amplitude decreases, reaching 70.7% of zero-hertz (DC) voltage at 10 MHz.

upper-frequency limit

Refer to this point as 3-dB attenuation. The upper- and lower-frequency 3-dB-down points define bandwidth. No lower-frequency 3-dB point appears

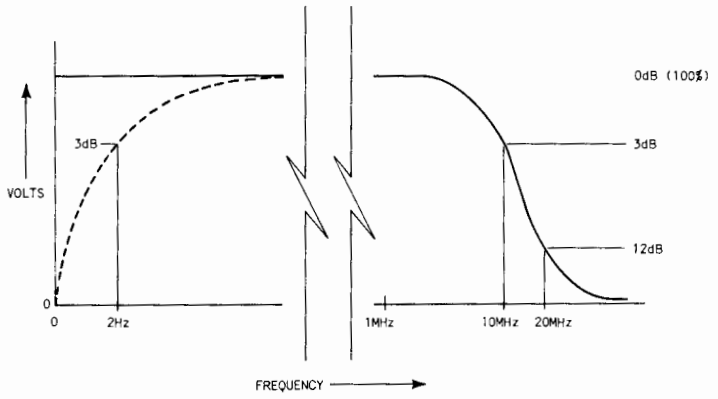


Fig. 1-8. Bandwidth curve.

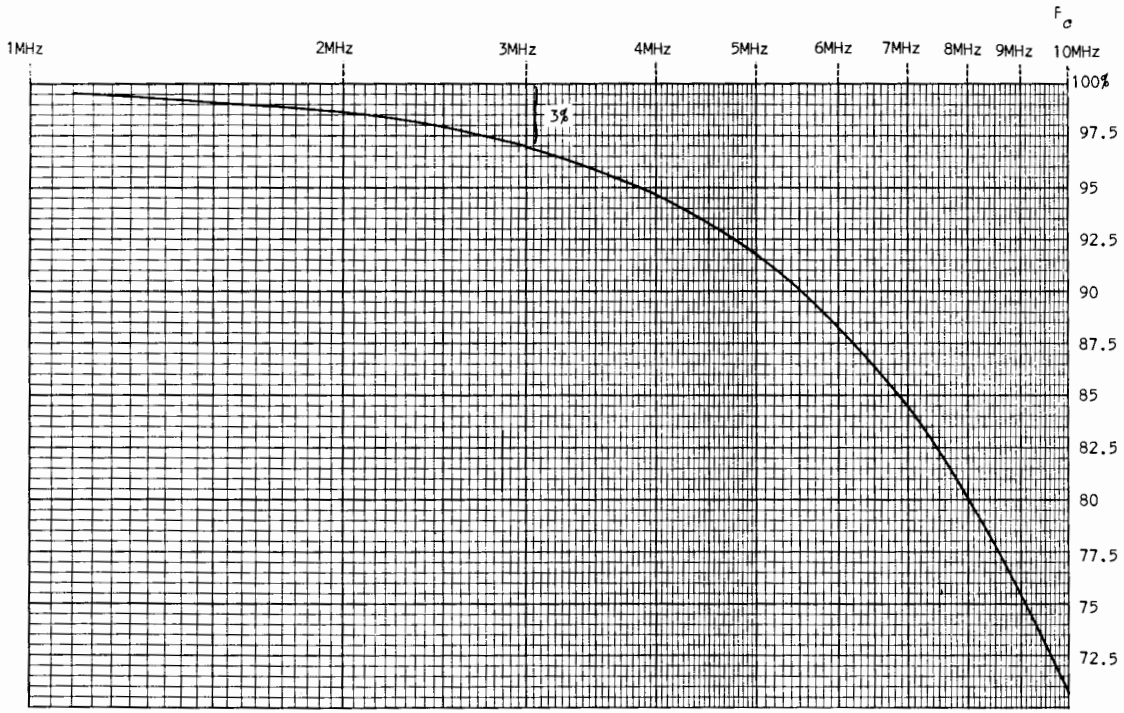


Fig. 1-9. Expanded frequency curve.

on the solid line graph. This is characteristic of direct-coupled instruments. Thus, one frequently refers only to the upper-frequency limitation: "This is a ten-megahertz scope."

lower-frequency limit

A precise description of an AC-coupled instrument must include the lower-frequency 3-dB point. The dotted line on Fig. 1-8 follows the slope of low-frequency response. 3-dB attenuation occurs at 2 Hz. Midfrequency and high frequency remain as for direct-coupling. 2 Hz is a low frequency and the majority of general-purpose oscilloscopes must respond to DC. Therefore, the upper 3-dB-down frequency (F_c) receives greatest attention.

The bandwidth curve of Fig. 1-8 has neither square corners, nor does it actually achieve a flat top. Beginning at the lower (2 Hz) 3-dB point, the curve ascends from 70% of maximum to exceed 99% at 20 Hz. Response continues to ascend until reaching maximum, then descends again dropping to 99.5% at 1 MHz.

measurement errors

Fig. 1-9 expands the upper frequency portion of the curve between 1 MHz and 10 MHz. This curve indicates that one experiences voltage *display* errors of discrete frequencies above 1 MHz: 0.5% at 1 MHz, 1.5% at 2 MHz, 5.5% at 4 MHz, 12% at 6 MHz, 20% at 8 MHz and 30% at 10 MHz (F_c). This is why some use the "thumb rule of 5:" That the scope bandwidth should exceed the highest frequency to be measured by five. The error at 20% of cutoff (F_c) is less than 2%. If one were satisfied with a 3% display error he could economize by using a scope whose F_c exceeded maximum measurement needs by 3.

Incidentally, the curve of Fig. 1-9 applies to most oscilloscopes. One need only apply F_c to the upper 3-dB point of his instrument and assign percentage values to the listed frequencies: 8 MHz is 80% of F_c, 6 MHz is 60% of F_c. . . .and 1 MHz is 10% of F_c. Using the chart to correct for display errors gives an accurate amplitude measurement of sinewaves.

One might wonder why he pays for frequency response he is not using. Why not provide him with a scope with a flat response between frequencies which then drops abruptly to zero? This would give him accurate displays within the specified frequencies and reject all frequencies above and below these limits.

Actually he uses all of the bandwidth he buys. The proposed abrupt response considers only frequency not time delay or phase shift. Phase relationships come into play during reproduction of nonsinusoidal waveforms. Even persons concentrating exclusively on frequency domain areas seldom, if ever, encounter a pure sinewave. An aberration of interest or a circuit distortion, such as clipping, creates complex waveforms. Accurate display of these waveforms depends upon vertical-amplifier phase-gain characteristics.

squarewave evaluation

One method of performance evaluation applies periodic rectangular waveshapes (squarewaves) to the vertical-amplifier input. This allows one to demonstrate frequency and phase response of a vertical system.

transient voltage

Fig. 1-10 shows three cycles of a periodic rectangular wave. There are two theoretical methods of constructing a squarewave: the transient-voltage and sinewave method. In terms of transient-voltage method, the voltage of Fig. 1-10 remains set from T_0 to T_1 at -2 volts; changes abruptly at T_1 to +2 volts; remains at +2 volts until T_2 suddenly changes to -2 volts; the level remains at -2 volts until T_3, and so on.

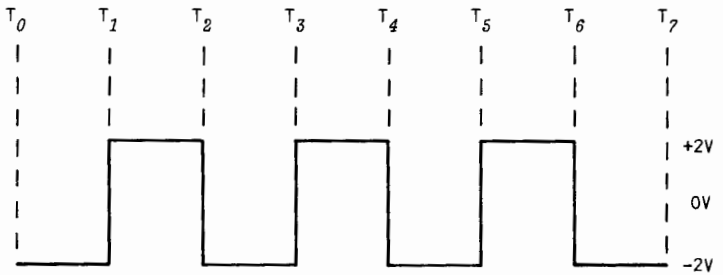


Fig. 1-10. Squarewaves.

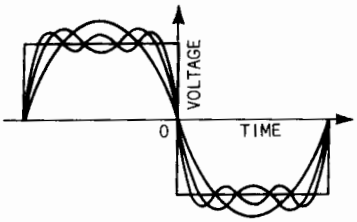
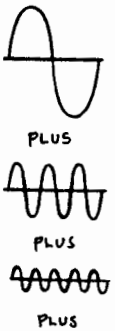


Fig. 1-11. The addition of successively higher-order harmonics to a fundamental sinewave to produce a close approximation of a squarewave.

frequency components

The sinewave method follows the assumption that a squarewave contains a number of frequencies. Fig. 1-11 shows the reproduction of a symmetrical squarewave. It shows three frequency summations superimposed on an "ideal" squarewave. First the fundamental sinewave establishes the basic rate. Next the third harmonic algebraically adds to the fundamental. Finally, the fifth harmonic adds to the waveform resulting from the first and third. This waveform only begins to resemble a squarewave. The corners are rounded and the top is not flat. Each additional harmonic sharpens the corners and flattens the top.



These harmonics bear both proper phase and amplitude relationship. As the fundamental frequency begins in a positive direction, all harmonics must also ascend. And at the completion of one fundamental cycle, as the fundamental intercepts zero amplitude from the negative, so must all harmonics. The fundamental completed 360°; the 3rd harmonic, 1080°; the 5th, 1800°; and so on through the odd-order harmonics.

Amplitude relationships must also be maintained. The 3rd harmonic is 1/3 of fundamental amplitude, the 5th is 1/5 and so on . . . .

A squarewave allows one to evaluate vertical amplifiers. For example, assume a "perfect" squarewave input appears on the CRT with rounded corners. Fourier analysis predicts higher harmonics sharpen the corners, therefore, the vertical amplifier suffers high-frequency attenuation.

waveform contains frequency information

Fig. 1-12 locates frequency information on one pulse. Notice that both the corners and vertical pulse excursions contain high-frequency information. Notice also the rounded pulse corners and vertical slopes. Properly extending an amplifier's frequency response preserves pulse corners, vertical slopes and "flat" tops.

time domain

Time-domain studies are concerned with the transit time from one voltage level to another. When discussing time-domain methods one encounters the term *step function*. This waveform results when a voltage "steps" from one level to another. Fig. 1-13 illustrates the two forms of the step function. In Fig. 1-13A the voltage sets at a level then abruptly changes to and remains at a more positive level. Fig. 1-13B illustrates a transit to a more negative voltage. Both figures imply a single change in voltage.

step function

pulses as step functions

Repetitive signals are generally more practical than single events. Thus, one finds periodic rectangular pulses used as step functions. Fig. 1-14 shows such a pulse. To consider pulses as step functions, pulse duration must be long compared to voltage level transit time.

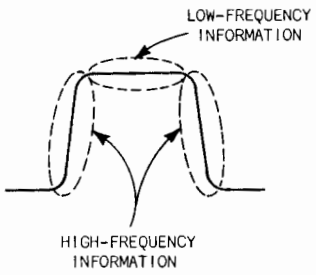


Fig. 1-12. A summary of the low- and high-frequency information found in a squarewave.

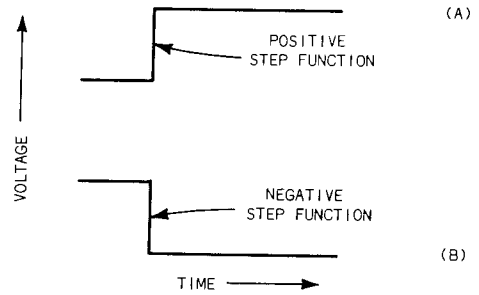


Fig. 1-13. Positive-going and negative-going step functions.

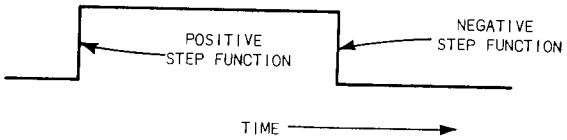


Fig. 1-14. Positive and negative step functions.

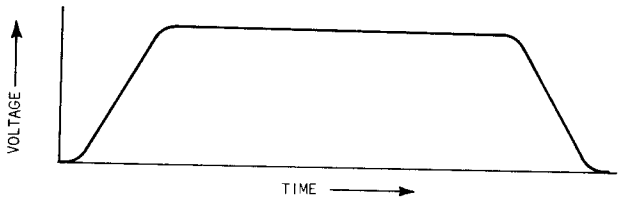


Fig. 1-15. Pulse shape.

How well vertical amplifiers reproduce ideal step functions is a measure of performance. Step functions of Fig. 1-14 are ideal, voltage transition occurs in zero time. Applying the "ideal" step to a vertical amplifier results in a display having rounded corners and a slope to voltage excursions. Fig. 1-15 shows such a response.

risetime

The term *risetime* refers to voltage-level transition time. Risetime applies to either positive or negative step response. However, a displayed

falltime

negative excursion is popularly termed *falltime*.

One measures risetime along a portion of the slope only. Initial and final portions of an excursion make close measurement arbitrary, at best. Risetime refers to only the middle 80% of a step function. Fig. 1-16 illustrates proper oscilloscope risetime measurement. This figure indicates risetime as the transit time between 10% of maximum voltage and 90% of maximum voltage.

Applying a step function to an RC network results in risetime dependent upon network time constant. The leading edge follows an RC curve, such as shown in

2.2 RC

Fig. 1-17. Risetime resolves to 2.2 RC: 10% of maximum occurs in 0.1 RC and 90% in 2.3 RC, the difference is 2.2 RC.

$$\text{Risetime } (t_r) = 2.2 \text{ RC.}$$

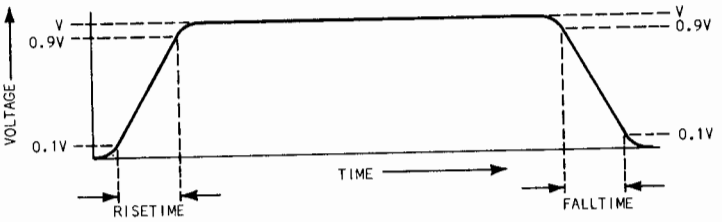


Fig. 1-16. Pulse measurement.

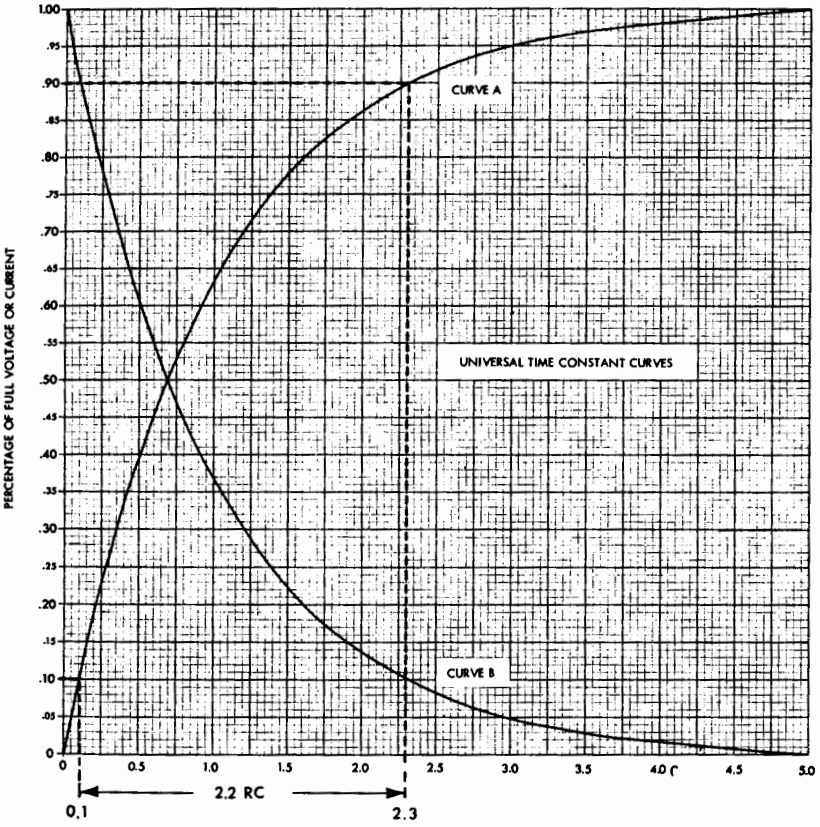

PERCENTAGE OF FULL VOLTAGE OR CURRENT
1.00
.95
.90
.85
.80
.75
.70
.65
.60
.55
.50
.45
.40
.35
.30
.25
.20
.15
.10
.05
0
CURVE A
UNIVERSAL TIME CONSTANT CURVES
CURVE B
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
2.2 RC
0.1
2.3

Fig. 1-17.

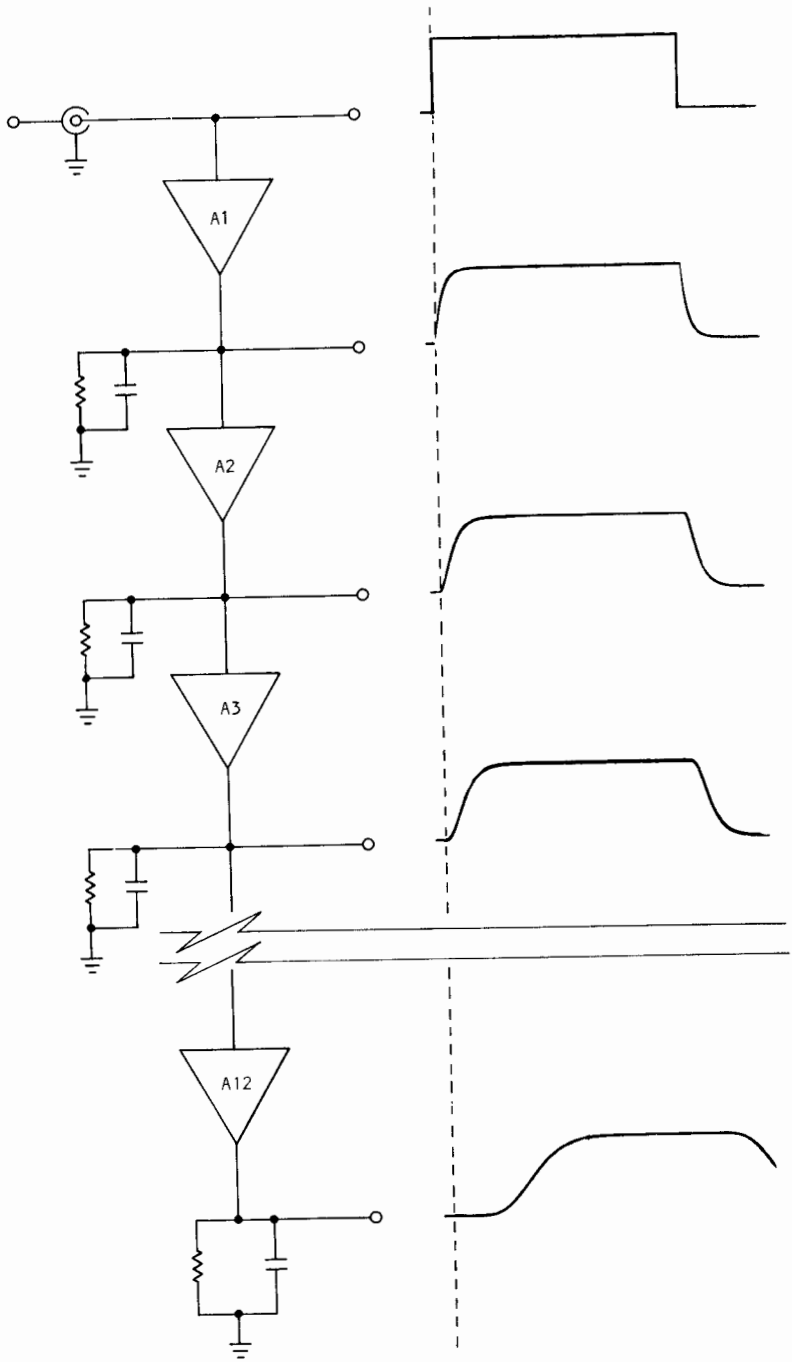


Fig. 1-18. Cascaded RC amplifier response to an ideal step.

A solitary RC circuit response is fairly easy to visualize. But, how does a cascade of RC amplifiers react to an approximation of the ideal step?

Ultimate risetime occurs later, rises slower and assumes a new shape. Fig. 1-18 shows these effects. Consider each amplifier increment:

Input -- The amplifier input step has zero risetime, both 10% and 90% points occur at T_0.

A1 -- Output risetime follows the curve of a universal time constant. Risetime increases and a small delay occurs. The step reaches 10% at 0.1 RC ascending to 90% 2.2 RC later. This is the input to A2.

A2 -- A2 receives an input with a varying change-of-voltage-per-unit-time. The output, developing across an RC network, ascends to 10% at a different slope rate. A greater time also lapses between 10% and 90%.

A3 -- The 10% point here occurs still later and risetime (t_r) again increases. At this output the curve between minimum amplitude and 10% begins to resemble the curve between 90% and maximum amplitude. This condition continues with each stage contributing an increase in time delay and risetime. And with each stage the upper and lower step halves approach mirror-image shapes. After an infinite number of stages the step in fact assumes a mirror-image shape.

A12 -- Here there is a considerable delay between T_0 and the 10% point. Risetime has noticeably increased and response appears to be symmetrical about the 50% point. The curve between minimum and 10% approximates the curve between 90% and maximum. This approximates a gaussian step response.

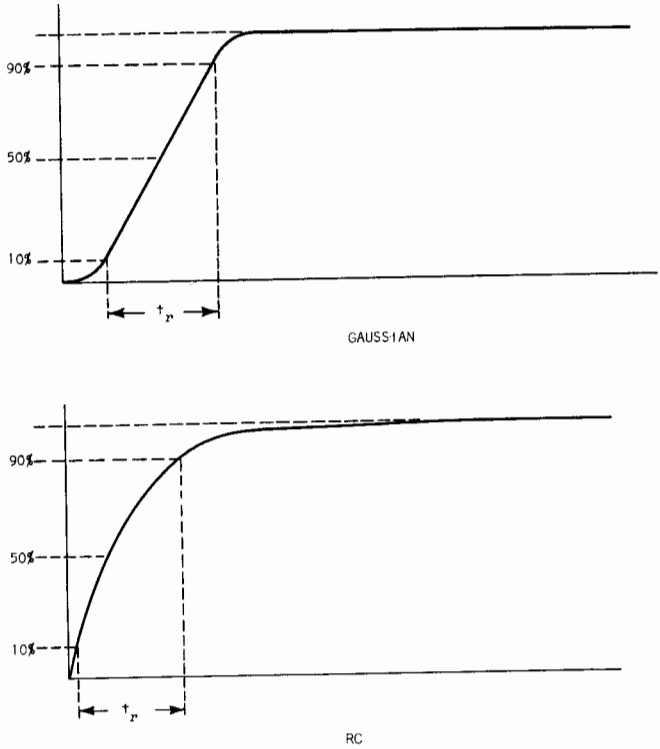


Fig. 1-19. Step response.

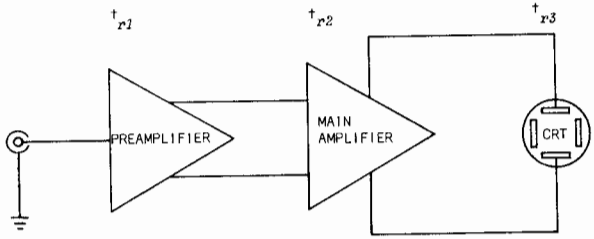


Fig. 1-20. System risetime results from individual amplifier risetimes: $t_r^2 = t_{r1}^2 + t_{r2}^2 + t_{r3}^2$

Fig. 1-19 compares a gaussian and an RC step response of equal risetime. The RC step rises abruptly, at an almost linear rate, from zero to 10%. Rate of rise then changes, requiring as much time from 90% to 99% as from zero to 90%.

On the other hand, gaussian responses rise from zero to 10% more slowly, assuming an almost linear slope between 10% and 90%, then ascend the last 10% in a curve equal to the first 10%.

Oscilloscope vertical-amplifier step response, except for a few specialized types, falls between the RC and the gaussian. Gaussian responses receive more detailed treatment later. For now, realize that a *true* gaussian amplifier is impossible. Vertical amplifiers do, however, very closely approach a gaussian response.

When an ideal step function passes through amplifiers in cascade, each amplifier contributes to risetime deterioration in a predictable manner. Fig. 1-18 showed this pictorially but failed in indicating predictability. Refer to Fig. 1-20 and assume the following conditions: An ideal step-function applied to a vertical input passes through two cascaded amplifiers and is displayed on a CRT. One predicts displayed risetime by applying the formula:

$$t_r = \sqrt{t_{r1}^2 + t_{r2}^2 + t_{r3}^2}$$

where:

t_r = displayed risetime of the amplifiers and CRT.

t_{r1} = risetime of the preamplifier operating alone.

t_{r2} = risetime of the main amplifier alone.

t_{r3} = CRT risetime.

For example, assign values:

t_{r1} = 3 microseconds

t_{r2} = 4 microseconds

t_{r3} = 10 nanoseconds

$$t_r^2 = (3 \times 10^{-6})^2 + (4 \times 10^{-6})^2 + (10 \times 10^{-9})^2$$

$$\approx (9 + 16)10^{-12}$$

$$t_r = \sqrt{25 \times 10^{-12}} = 5 \times 10^{-6} \text{ seconds}$$

Displayed risetime resulting from an ideal step function is about 5.0 microseconds.

vertical risetime must be less than test device

One now might ask, how can an oscilloscope user measure risetime? To do so the oscilloscope vertical amplifier must have a risetime much less than the device being measured. Suppose one wishes to display a given waveform. He also requires the displayed waveform to be within 2% of the input waveform. Fig. 1-21 indicates oscilloscope performance for the required result. For example, 2% (Y axis) intercepts the graph slope at the ratio of 5 (X axis). This tells an operator that to observe a 50-nanosecond risetime waveform, with 2% accuracy, his oscilloscope must have 10-nanoseconds risetime or less.

Fig. 1-21 was calculated from the square root of the sum of the squares equation. A modification of this formula allows one to determine true risetime of a circuit under test:

$$t_{rA}^2 = t_{rg}^2 - t_{rd}^2 - t_{rO}^2$$

where:

t_{rA} = Amplifier risetime (amplifier under test).

t_{rd} = Displayed risetime.

t_{rg} = Risetime of the squarewave generator (or other source).

t_{rO} = Oscilloscope vertical-amplifier risetime.

Using these calculations one moves from "ideal" restrictions to reality. Fig. 1-22 shows a possible condition. A squarewave generator develops the step function with risetime, t_{rg}. The amplifier under test increases risetime as does the vertical-amplifier system. All devices contribute to risetime displayed, t_{rd}. Thus an operator must know the risetime of the step-function source and his oscilloscope *from the probe tip*. He then substitutes the known and measured values into the formula for true risetime of the amplifier under test.

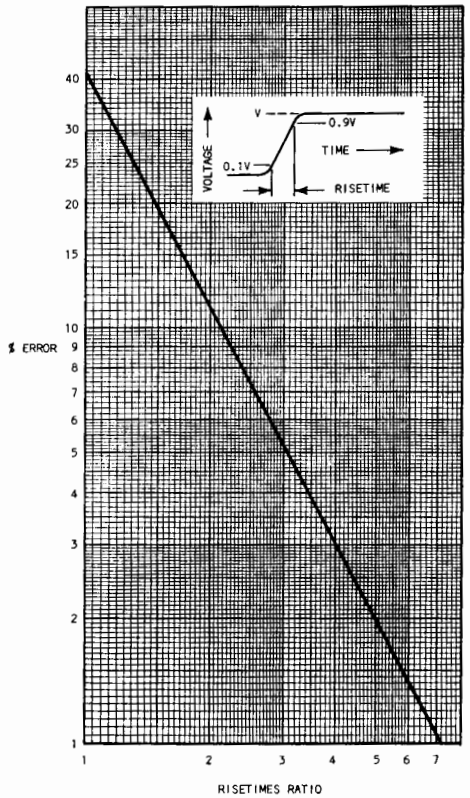


Fig. 1-21. Percent error in risetime measurement (Y axis) plotted against ratio of input waveform risetime to oscilloscope risetime (X axis).

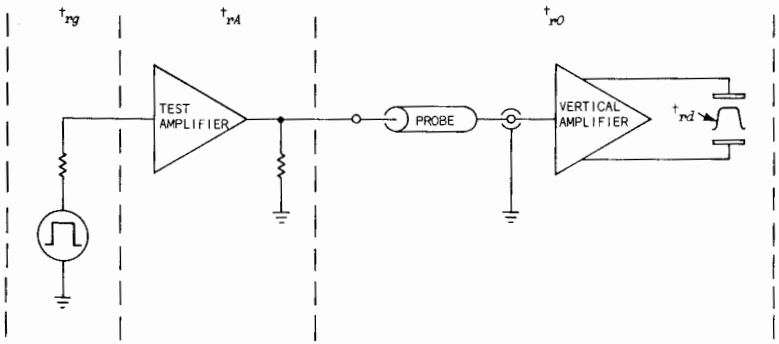


Fig. 1-22. Factors determining actual risetime of a circuit under test.

One note of caution about oscilloscope risetime. One Tektronix oscilloscope type, specified at 7 ns, actually meets a performance of 6 ns or better when it leaves the factory. On the other hand, instrument risetime can be considerably degraded without user awareness. Whether due to conservative specifications or eroded performance, the calculations may be in error. Measure your instrument performance.

risetime-bandwidth product

Vertical amplifiers have so far been considered from two standpoints, risetime and bandwidth. A definite relationship exists between risetime and bandwidth. This is expressed as a constant, K, equal to the risetime-bandwidth product: $t_r \cdot \text{bw} = K$. $K = 0.35$ in the case of RC amplifiers. K results from a combination of the risetime formula and the -3 dB frequency formula:

$$t_r = 2.2\ RC$$

and

$$F_c = \frac{1}{2\pi RC} \quad \text{or} \quad RC = \frac{1}{2\pi F_c}$$

substituting,

$$t_r = 2.2 \left(\frac{1}{2\pi F_c}\right) = \frac{2.2}{2\pi F_c} = \frac{0.35}{F_c}$$

$$t_r F_c = 0.35$$

If one considers F_c as bandwidth then:

$$t_r \cdot \text{bw} = 0.35$$

gaussian circuits

The above derivations apply only to an amplifier whose bandwidth is RC limited. Cascading a number of such amplifiers or proper compensation in a single-stage amplifier results in an essentially gaussian response. In this case the risetime-bandwidth product also partially describes the amplifier.

A *true* gaussian response resolves to $t_r \cdot \text{bw} = 0.32$. Because of several factors oscilloscope amplifiers don't meet the requirement for *true* gaussian response. "Gaussian" circuits are thus essentially gaussian. Empirical products, arrived at through years of research, define these "gaussian" circuits. For a gaussian response, $t_r \cdot \text{bw} = 0.35$ to 0.45. Higher products indicate least risetime. However, overshoot

accompanies the risetime reduction. A product of 0.45 results in about 5% overshoot and when $t_r \cdot bw = 0.35$ there is little, if any, overshoot in the step response. Tektronix usually establishes the product at $K = 0.35$, sacrificing risetime for minimum overshoot.

Fig. 1-23 compares *relative* bandwidth rolloff to step response. The bandwidth rolloff of Fig. 1-23A approximates gaussian. Step response, symmetrical about the 50% point, exhibits fastest rise *without* overshoot.

overshoot

Overshoot appears in Fig. 1-23B. In this figure upper frequency response falls off too steeply to be gaussian. Step response rises above then returns to 100% voltage level. This is called overshoot. Frequently associated with overshoot, a damped

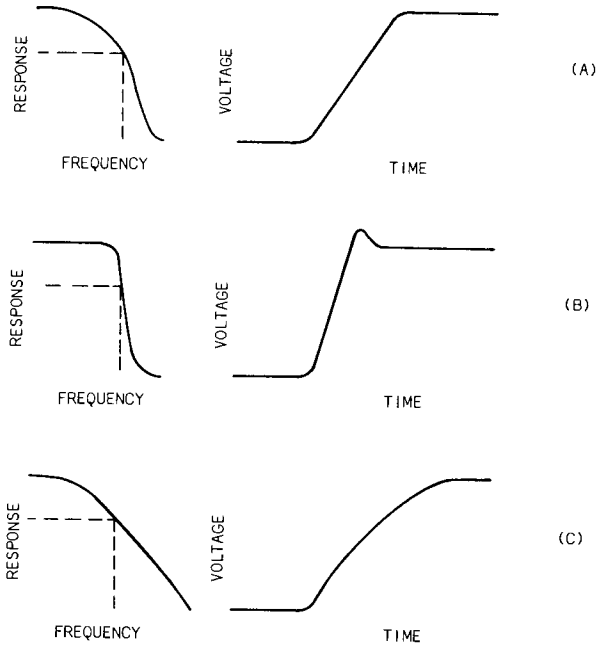


Fig. 1-23. Bandwidth versus frequency.

oscillation may appear along the top of the wave. A few percent overshoot can represent an acceptable level when optimizing a system for least risetime.

slow rise

In Fig. 1-23C, the frequency-response curve falls off too slowly. The corresponding step response takes undue transit time.

phase shift linear

The gaussian rolloff expresses step-function response because of frequency-phase relationships. A circuit must impose two related phase characteristics for optimum step response: A linear shift with frequency or all frequencies equally delayed. Reactive components which attenuate also affect a phase shift. Impedances with gaussian attenuation shift phases linearly with frequency.

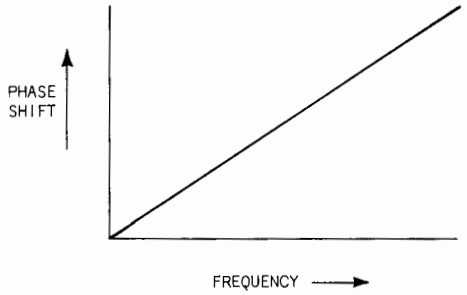


Fig. 1-24. Phase shift linear with frequency.

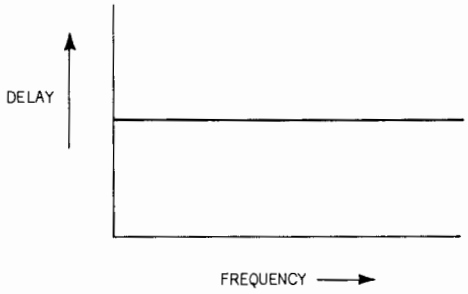


Fig. 1-25. Delay constant with frequency.

group delay

Fig. 1-24 shows phase shift-frequency relationship necessary for gaussian response. For optimum step response all frequency components must be equally delayed (Fig. 1-25). In other words, the frequency components of a pulse transiting a gaussian network experience phase shift increasing linearly with frequency. Also, all pulse-forming frequencies arrive at the termination simultaneously.

Now that a vocabulary has been established, a much more compact statement will summarize the amplifier description. Completely describing a linear amplifier by means of steady-state sinewave testing requires two plots:

1. Amplitude versus frequency, and,

2. Phase versus frequency.

Theoretically, given the amplitude and phase characteristics, one can calculate step response.

The most common input for amplifier testing is the step signal. This describes a linear amplifier by means of the time response to any input signal. Complete step response contains all of the information that amplitude and phase plots contain.

Theoretically, given a complete step response one can calculate the amplitude and phase characteristic. The tool used to deduce one information set from the other is the Fourier transform. Frequency response (amplitude and phase versus frequency) is the Fourier transform of an impulse response. The impulse response is basically the time derivative of the step response.

The step response of an amplifier with abrupt upper-frequency rolloff contains both preshoot and overshoot. Fig. 1-26A.

Nonlinearity of the phase characteristic adds distortion. Fig. 1-26B shows three types of phase characteristics. These are plotted in terms of phase and delay:

a. Ideal,

b. Insufficient delay of high frequencies,

c. Peaks, or excessive delay at high frequencies.

Fig. 1-26C approximates the step response resulting from nonideal phase characteristics.

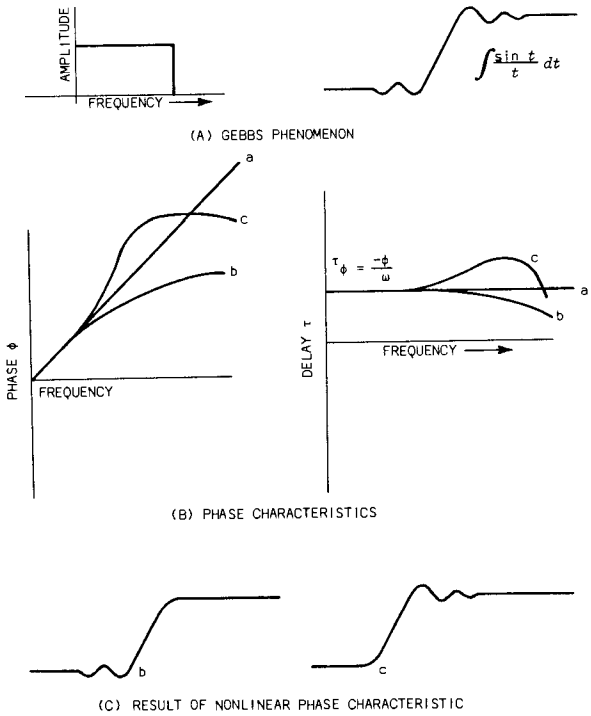


Fig. 1-26. Frequency response -- step-response interdependence.

These interrelationships can also be demonstrated by shifting and attenuating the harmonic content of a squarewave.

Fig. 1-27 shows three of many frequency components contained in a squarewave. The fundamental completes one cycle between T_0 and T_4; during the same interval the 3rd harmonic completes three cycles; the 5th completes five and so on through all odd harmonics. This relationship must be maintained for squarewave reproduction. Should the fundamental be shifted 90° (T_1) the third harmonic must shift 270° and the 5th 450°. 3 x 90 = 270, 5 x 90 = 450. Further, to maintain this phase relationship all frequency components must be delayed equally: If the fundamental is delayed 5 µs, then all harmonics must also be delayed 5 µs.

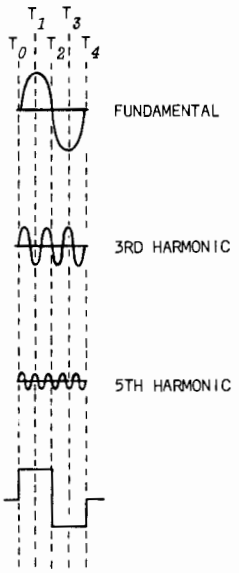


Fig. 1-27. Equal group delay.

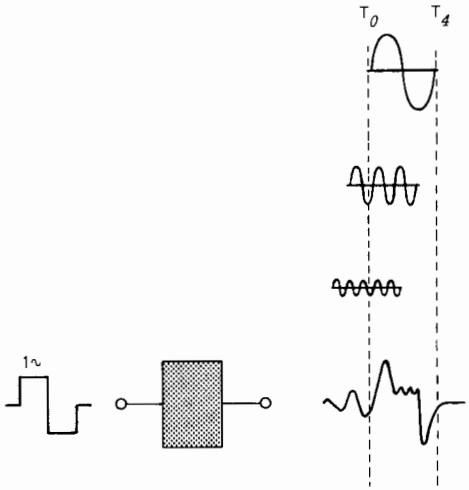


Fig. 1-28. Unequal group delay.

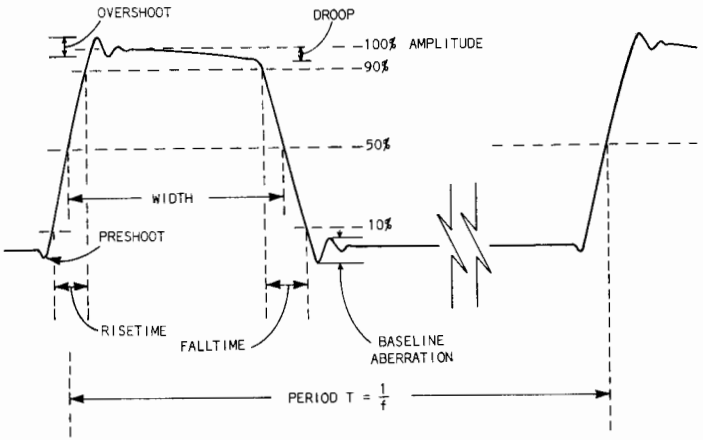


Fig. 1-29. Pulse nomenclature.

unequal group delay

Fig. 1-28 represents the results of unequal delay. High frequencies transit the network faster than low frequencies. High-frequency energy *appears* to arrive at the output before T_0. A distorted output waveform results. In this figure the output waveform was approximated using only a few odd harmonics to show aberrations preceding the main output pulse.

These requirements for linear phase shift or flat delay apply to all waveshape reproduction.

risetime

falltime

pulse width

Apply the nomenclature covered to the simulated display of Fig. 1-29. Risetime measurements occur along the leading edge of the pulse, falltime at the trailing edge. The terms risetime and falltime become ambiguous on an inverted pulse. Therefore, risetime is always measured along the leading edge. Pulse width and pulse-recurrence time are both measured at the 50% amplitude points.

aberrations

baseline shift

preshoot

overshoot

droop

This illustration includes fast and slow deviations. Fast deviations appear as baseline and top aberrations. Droop (tilt) indicates slow deviations. In this case the vertical amplifier apparently imposes unequal frequency delay: High frequencies transit faster than low, creating preshoot. Overshoot also results since unequal group delay makes linear phase shift impossible. Droop is also an unequal group delay indicator. Droop shows excessive low-frequency delay. The baseline ringing, like overshoot, occurs during nonlinear phase shift/frequency relationships.

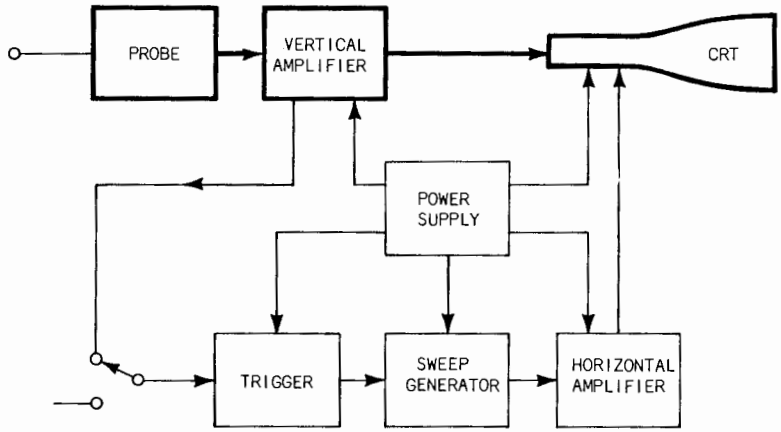


Fig. 2-1. Vertical amplifier.

2

INPUT CIRCUITS AND COMPENSATED ATTENUATORS

The first vertical circuits to affect an input signal are the input selector and input attenuator. Fig. 2-2 shows an input selector, attenuator and input amplifier block.

The INPUT SELECTOR determines lower-frequency bandwidth. Placing the input selector to AC capacitively couples signals, appearing at input connector J1, to the input attenuator. Switching to GND *opens* J1 and grounds the attenuator input. DC, the position shown, directly connects the attenuator to J1.

switching logic

Fig. 2-3 shows improved switching logic. As an operator switches from DC to AC he grounds the input attenuator temporarily. This action discharges

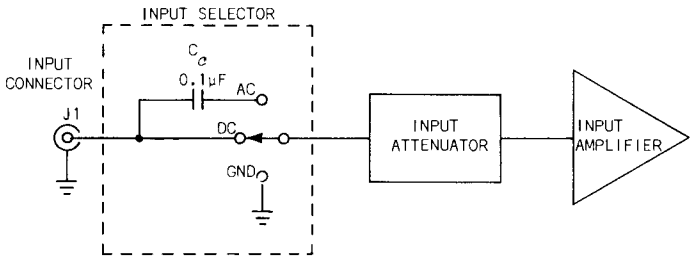


Fig. 2-2. Input-selector switching.

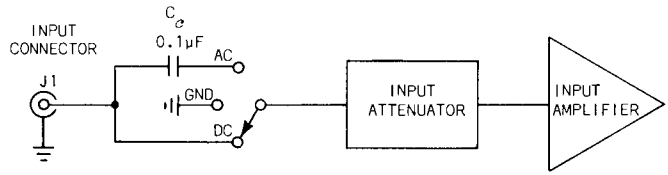


Fig. 2-3. Improved input-selector switching.

input attenuator capacitance, reducing the quantity of C_c charge current which must flow through the attenuator networks.

input charge current

Some consider the input circuit charge current negligible -- not so! There have been instances of switch contact destruction. Consider the effects of the following sequence: An oscilloscope user checks or sets the level of the -150 volt supply. The input selector is set to DC. He then decides to measure ripple content of the +150 volt supply. To do this he removes the probe from the -150 volt supply, switches to AC and connects the probe to the +150 supply.

C_c in Fig. 2-2 initially charges toward 300 volts. The input attenuator contains -150 volts charge and +150 appears at input connector J1.

In Fig. 2-3, charge current is reduced by half. When the input selector moves from DC to AC it contacts GND, removing stored charge in the input attenuator. C_c charges to the *applied* voltage.

The user certainly can reduce charge current by placing the input selector to GND between measurements. The circuit in Fig. 2-3 removes this memory burden.

C_c charge current flows through the attenuator in both cases. The vertical amplifier reacts during charge time as though a signal were applied. At best, this causes a measurement delay while the display follows the changing input charge signal. Further, C_c could have retained an additive charge from some previous measurement. This is because C_c is an open circuit in input selector positions other than AC. Adding a resistor to the circuit in Fig. 2-3 from the AC contact to the attenuator would close the loop in any input selector position.

Fig. 2-4 includes resistance R_c which closes the C_c charge path. C_c charges to the input voltage through R_c with DC or GND selected. Selecting AC shorts R_c to prevent unnecessary attenuation of input signals. This accomplishes two purposes: First, it reduces the charge current through the attenuator and the switch contacts; second, C_c cannot contain an unknown captive charge.

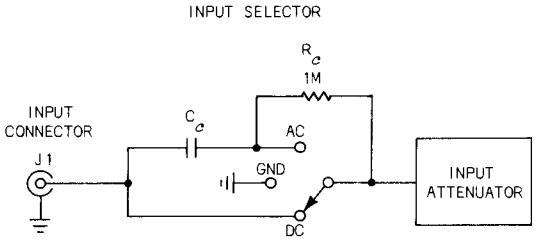


Fig. 2-4. Providing C_c an additional charge path.

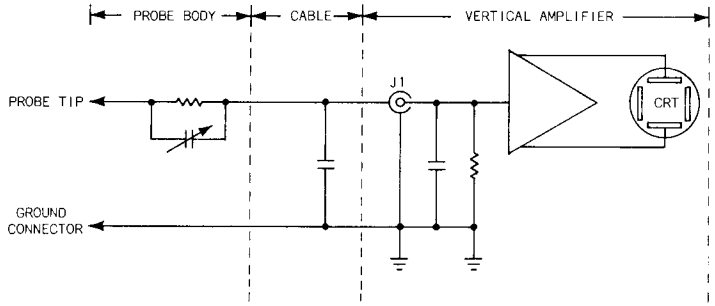


Fig. 2-5. Input circuit of a vertical system.

fixed input RC

Oscilloscopes have a fixed input RC. The attenuator changes the input deflection factor (volts per division) but not the input RC. Maintaining a constant RC eliminates probe recompensation with attenuation changes.

probe

One must couple the signal of interest to the vertical-amplifier input. Simple test leads work for some low-frequency applications. Generally, use of an oscilloscope probe results in greater convenience and accuracy. Assume the probe is connected to J1 of Fig. 2-4 and the selector switch positioned to DC.

Fig. 2-5 represents circuit equivalents of the probe and vertical-amplifier input. The probe body consists of a resistor shunted by a variable

capacitor. A single capacitor represents distributed cable capacitance. An RC network appears to the right of J1. This parallel circuit is the fixed-input time constant of the vertical amplifier.

V_{in}

Lumping fixed cable and vertical-amplifier input capacitance evolves the circuit of Fig. 2-6. In this figure V_{in} represents the signal of interest; V_o the vertical-amplifier signal; R_p, probe resistance; C_p, probe capacitance; R_i, vertical-amplifier input resistance; C_i, vertical-amplifier input and cable capacitance.

Fig. 2-6 is a compensated voltage divider as long as time constant R_iC_i equals time constant R_pC_p. C_p and C_i form a capacitive divider creating voltage division across the capacitors equal to the division across R_p and R_i. Ratio $\frac{R_p + R_i}{R_i}$ defines basic DC attenuation. C_p and C_i form a capacitive divider of the same ratio so that the resultant time constants equal, $R_pC_p = R_iC_i$.

attenuation ratio

An adjustable C_p allows one to adjust the probe time constant to match a specific vertical-amplifier-input time constant. This probe compensation must take place each time one connects the probe to an oscilloscope since input capacitance varies between instruments. Examples of input-time-constant specifications are listed below:

compensation

1 MΩ x 15 pF
1 MΩ x 20 pF
1 MΩ x 24 pF
1 MΩ x 33 pF
1 MΩ x 47 pF.

The listing shows a wide variation of input RC between different type oscilloscopes. Oscilloscopes of one type also vary, but to a much lesser degree. For a specific vertical amplifier one need compensate the probe once only. An input attenuator must be designed and calibrated to meet this criteria.

Compensated voltage dividers create a number of misunderstandings. Therefore, one needs to imbed the concepts of compensated voltage dividers in his mind. Fig. 2-6, the equivalent probe-scope input

circuit, contains the basic compensated voltage-divider components. And probe compensation offers an oscilloscope user a vehicle for demonstrating the effects of voltage-divider compensation.

Some say that a compensated voltage divider presents a constant impedance. No! Impedance *ratio* remains constant, but total impedance changes with frequency. Compensating a voltage divider sets up an impedance *ratio* independent of frequency.

Input voltage (V_{in}), Fig. 2-6, develops across an impedance (Z_T) which changes with frequency. The impedance of the probe (Z_p) and of the input (Z_i) also changes but when compensated, the ratio remains constant. This occurs when the RC time of one network matches the RC time of the other network: $R_pC_p = R_iC_i$.

If R_p = 9 MΩ, R_i = 1 MΩ, C_p = 2.2 pF and C_i = 20 pF, then $R_pC_p = R_iC_i$.

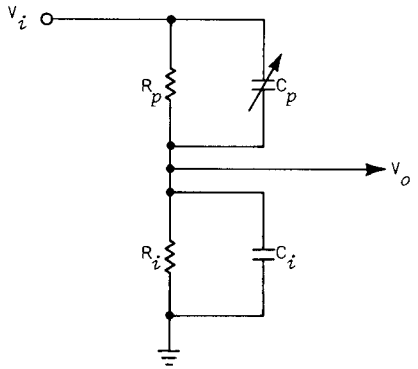


Fig. 2-6. Equivalent input circuit of a vertical system.

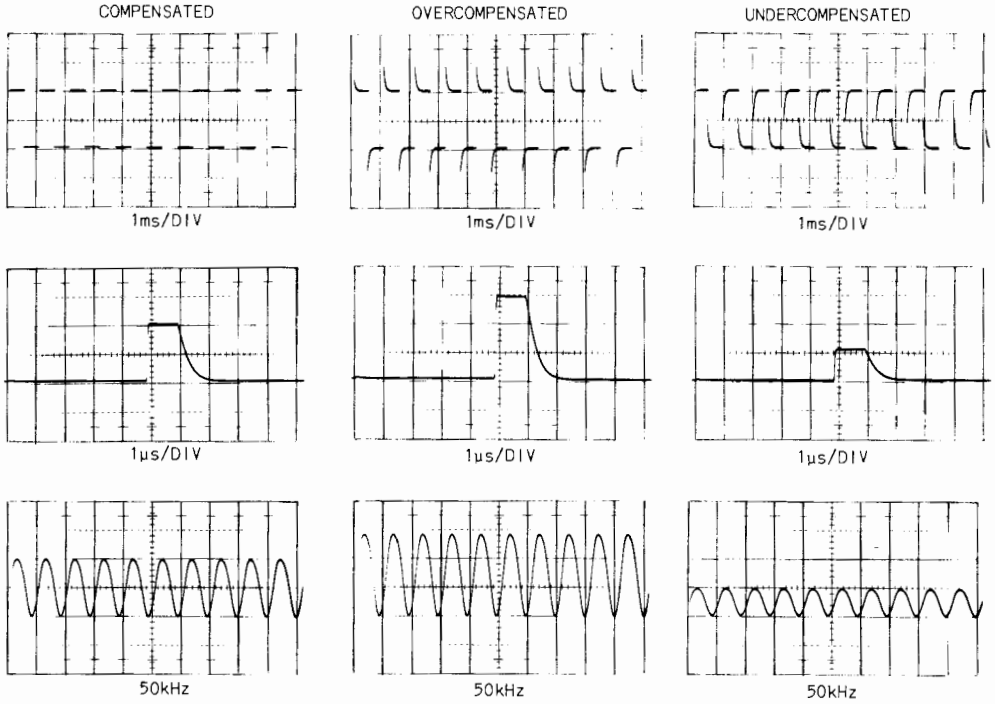


Fig. 2-7. Effects of probe compensation.

Fig. 2-7 demonstrates the effects of probe compensation. To compensate his probe one connects to a squarewave source, such as the calibrator output on most oscilloscopes. These pulses may be much slower than the vertical amplifier system.

correctly compensate

Compensate the probe by adjusting for fastest risetime without overshoot. Accurate measurements are now possible whether they be pulses or high-frequency sinewaves -- within the instrument risetime-bandwidth limits.

overcompensated

Overcompensation shows as overshoot in the calibrator waveform. Both narrow pulses and discrete high frequencies appear larger than life.

undercompensated

Rounded calibrator waveforms indicate undercompensation. Narrow pulses and high-frequency sinewaves suffer excessive attenuation.

Notice that neither the sinewaves nor *narrow* pulses change shape. This is one of the dangers. Overall waveshape does not necessarily indicate proper probe compensation.

The probe offered a logical circuit point to describe compensated voltage dividers. Mentally disconnect the probe and consider input attenuators alone. The input attenuator consists of selected voltage dividers controlled at the front panel by the VOLTS/DIVISION selector. The VOLTS/DIVISION selector is calibrated in terms of deflection factor at the input connector. To expand the discussion of input attenuator functions, assume the following vertical-amplifier conditions:

1. 33 pF x 1 MΩ specifies the fixed time constant at the input connector.
2. DC selected by the INPUT SELECTOR.
3. 10 millivolts per division is the basic input deflection factor.
4. The VOLTS/DIVISION selector steps in a 1-2-5 sequence; 0.01, 0.02, 0.05, 0.1, 0.2, 0.5, 1, 2, 5, 10 and 20 V/div.

The above assumptions relate to Fig. 2-8. To the right of the attenuator block is the grid RC of input amplifier, V1. R1 and C1 remain in the circuit at all times. They always form a part of the attenuator network. All network switching, however, takes place in the attenuator block.

X1

Placing the VOLTS/DIV selector to 0.01 switches the attenuator to X1. Selecting X1 attenuation directly connects the top of R1 to the input. Distributed capacitance (C_d) forms an appreciable portion of the input RC, and specified at the input: 1 MΩ must shunt 33 pF. R1 meets the resistive requirement, but C1 contributes only 3.3 pF. C_d then must appear as 31.7 pF:

distributed capacitance

RC_i = 1 MΩ x 33 pF; R1 = 1 MΩ; C1 = 3.3 pF;
33.0 - 3.3 = 29.7 pF.

Consider distributed capacitance a component in all vertical-amplifier input circuits.

X2

Selecting 0.02 VOLTS/DIV switches the attenuator to X2 voltage attenuation. Fig. 2-9 shows the X2 attenuator schematic. Signal voltage applied to J1 appears at the top of C20, R21 and C21. 50% of the input voltage develops at the grid of V1.

Basic attenuation consists of R21, R22 and R1. 500 k, total resistance of parallel network R22-R1, matches the resistance of R21. Resistance, thus voltage, division is equal. 1 MΩ appears from J1 to ground.

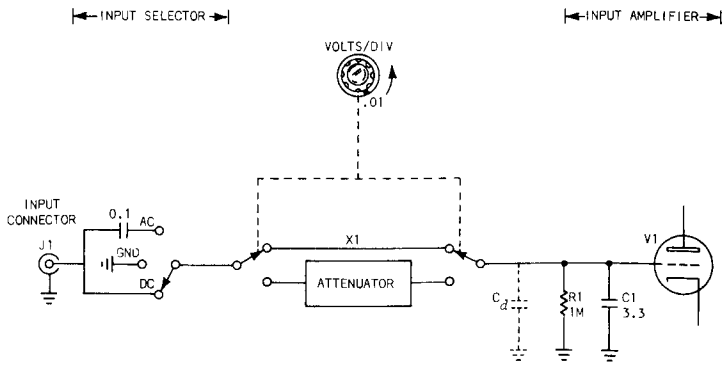


Fig. 2-8. X1 input attenuation.

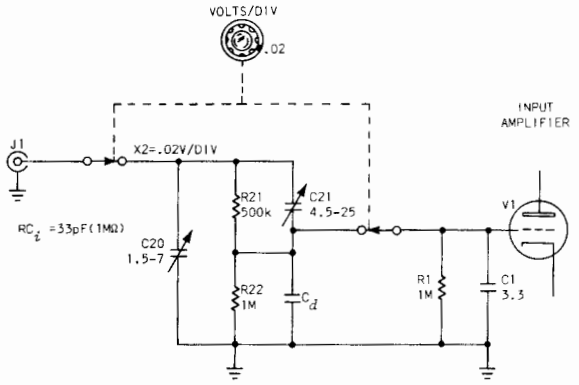


Fig. 2-9. X2 input-voltage division.

voltage divider compensation

C1 and parallel distributed capacitance (C_d) shunt the lower divider leg. One adjusts C21, across R21, to match the upper leg RC to the lower leg RC.

input compensation

Input RC = 33 pF x 1 MΩ. Switching to X2 maintained input resistance but altered capacitance. C20 shunts this network providing adjustment for 33-pF total input capacitance. Although C_d changed due to stray capacitance at the input lead, the input C altered mainly from the series effect of C21 with C_d and C1:

$$C_i = \frac{C21(C_d + C1)}{C21 + C_d + C1} .$$

C20 shunting the attenuator thus raises total input shunt capacitance to the standardized value: C_i + C20 = 33 pF.

Moving the VOLTS/DIV selector through its range step-selects additional attenuator networks of appropriate ratios. All of the attenuator networks use the same concept: Simple RC voltage dividers which maintain a set ratio to one another and present to the input a resistance of 1 MΩ and a capacitance of 33 pF.

X100

Fig. 2-10 contains circuitry resulting from a VOLTS/DIV selection of 1.0. The operator switched in the X100 attenuator. The basic divider consists of: R202, paralleled by R1, in series with R201. C202, C_d and C1 shunt the lower resistive leg forming a capacitive voltage divider with C201. Adjusting C201 compensates the voltage divider. Adjusting C200 matches total input capacitance to other attenuator positions.

component quality

Input attenuator parts must be of high quality. They are not only close tolerance resistive or capacitive values, but also must contribute small and predictable amounts of alien components. Resistors contain capacitance or inductance or both. Capacitors also contain resistance or inductance or both. These components should be as pure as possible for use in the input attenuator. Quantity production requires physical repeatability and predictability which usually calls for purity compromises. Therefore, capacitors add L and R, and resistors add L and C.

Interconnecting and component leads are inductors. Long leads or those with a bend impose more inductance than short straight leads. Leads also contribute capacitance, dependent upon conductor spacing.

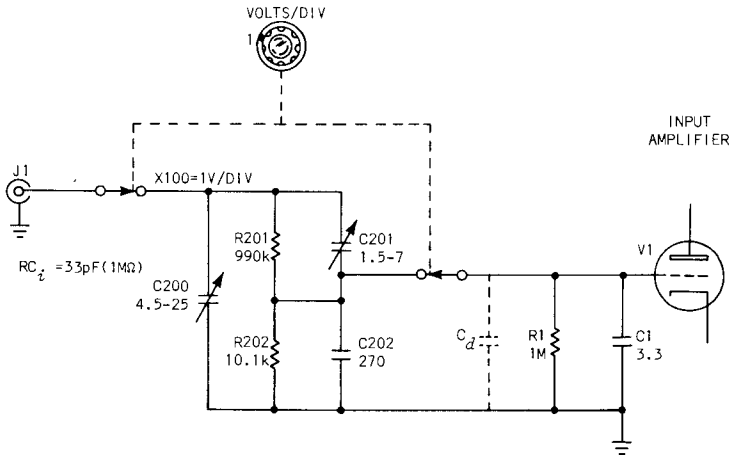


Fig. 2-10. X100 input-voltage division.

Capacitance develops between switch terminals and contacts, between circuit-board strips and so on. Any connection, in fact, is a potential capacitor. The relatively slow effect is hook. *Hook* is a small dip, of short duration, on the flat top of a displayed step, immediately following the leading edge. The capacitance variation that causes hook usually results from dielectric alterations during transit time. Dielectrics involved can be attenuator capacitors, active device input capacitance, terminal stand-off insulation, or that of a circuit board. Terminals or circuit boards are the most common offenders. This dielectric modification occurs during the step-transit time. Following pulse or step transition, the dielectric returns to normal, creating a discharge current with a time constant much slower than the input-step risetime. The discharge current develops a voltage across the output, which subtracts from the input level. Tektronix corrects for hook at the attenuator by component selection, circuit layout and circuit-board construction.

hook correction

Selected components, careful layout and quality assembly reduces stray reactances to a practical tolerance for instruments of medium risetime. As a rule-of-thumb, which will have several exceptions, assume instruments with risetimes of 10 ns or longer contain simple attenuators as shown in Figs. 2-9 and 2-10. Verticals in the 7-10 ns range may contain input attenuators as in Figs. 2-9 and 2-10, or the attenuators may reflect the techniques of the "faster" instruments.

stray components

"Fast" instruments react to stray components of sometimes obscure origins, such as the paint on components. Vertical amplifiers capable of reproducing steps of 7 ns or less have extra parts which counter component-induced distortion. This distortion takes two forms: Rolloff, due to *changing* input capacitance, and overshoot (ringing), caused by adding inductance.

Varying input capacitance is the input amplifier's response to a fast step. This "negative-input-resistance characteristic" receives treatment in the next chapter. At the input attenuator the change takes the form of additional capacitive current. Series-peaking networks provide one solution.

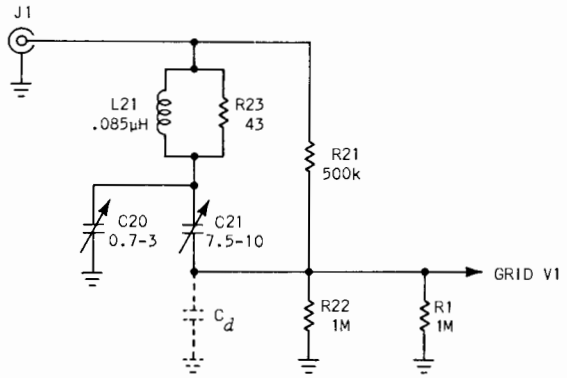


Fig. 2-11. X2 attenuator with series peaking.

series peaking

Fig. 2-11 shows series-peaking network L21 and R23 added to a X2 attenuator. This circuit is taken from a preamplifier with an overall risetime of about 2 ns. L21 and R23 maintain a delicate balance between signal and regenerative currents.

Input voltages which change levels in a few nanoseconds demand maximum capacitive current from the attenuator. The grid of V1 also draws additional capacitive current. However, during signal transit, L21 presents maximum opposition to signal-current flow. R23 then establishes total attenuator signal-current flow. If R23 signal-current reduction equals the current drawn by V1, the attenuator achieves a voltage division of 2. This only results from delicate part selection and placement. Components involved are L21, R23, C20, C21, C_d and the capacitive *change* in the V1 grid circuit. Should the components be improperly proportioned the input either rings or degrades risetime.

Precise RLC responses are very complex. For this reason only basic ideas explain peaking-network action here. R23 shunts the peaking coil. For explanatory purposes a small resistor shunting the coil has the same effect as a large series resistor. A series RLC circuit responds to a step function in one of two basic ways: It develops a

overdamped

underdamped

pulse of current, or it rings. Overdamped response (a current pulse) occurs when the L-to-C ratio is small and the series resistance is correspondingly large. Underdamped response (ringing) results from a large L-to-C ratio and a small series resistance. Curves of Fig. 2-12 show circuit current relative to L, C and R values.

Since damping is the same, a small resistance shunts L21 rather than a large series component. Keeping R23 small negates effects on all but the "fast" signals.

The overdamped response current only occurs in attenuator reactances. 1 MΩ resistance shunts the reactive leg, so when the reactive current drops to zero, total signal current flows through the 1 MΩ resistance.

In the case of Fig. 2-13, L21 and R23 separate C_i from C_d during signal transitions. C_i consists of quiescent input capacitance modified by V1 negative

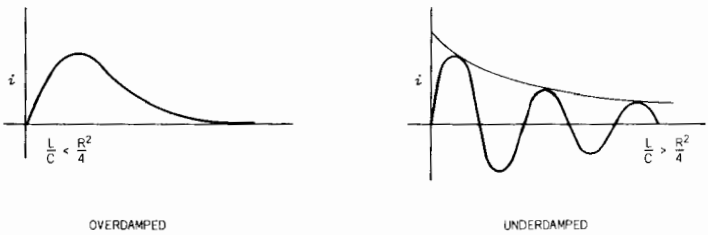


Fig. 2-12. Comparison of overdamped and underdamped response.

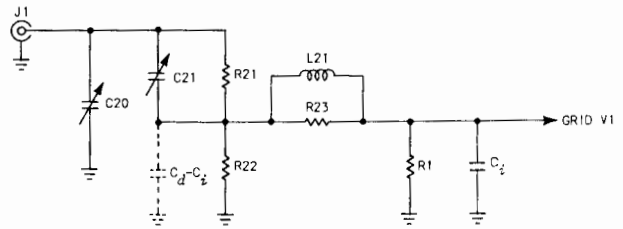


Fig. 2-13. Alternate location of X2-attenuator series peaking.

input characteristics and, possibly, circuit-board dielectric loss. L21 and R23 probably do not retain the values listed in Fig. 2-11. L and R values must combine with circuit capacitance to form an underdamped response.

RLC appear as part of the input attenuator only when the changing capacitance is an appreciable percentage of the capacitive divider. Increasing attenuation reduces the need for peaking. This is because component capacitance shunting the grid line becomes larger. The preamplifier from which Fig. 2-11 was taken has an RLC network in the X2, X5, X10, X20 and X50 voltage dividers. The X100, X200 and X500 have none, neither of course does the X1.

high-value dividers

Fig. 2-14, the X100 divider, includes no LR network. Two capacitances, C200 and C202 are much larger values than counterparts, C20 and C_d, in the X2 attenuator. The smaller value of C201 makes this necessary. Series capacitance C201 establishes total divider capacitance. Therefore, C200 must be large enough to set the input RC equal to the X1 RC at J1. C202 added to C_d should approximately compensate the divider at the midrange setting of C201: R1C1 = R2C2.

Changing capacitance at the grid line, or due to C201 dielectric deviations, represents too small a percentage of the total capacitance to consider a peaking network necessary.

ringing

R203 loads the circuit to damp oscillations. This ringing results from stray inductances, inherently a part of the capacitors, resistors and attenuator wiring. R203 adds but 1/2% error to the voltage divider.

eliminating input networks

Eliminating attenuator components reduces production costs and stray reactances. There are two major techniques used to eliminate networks: Stacking and amplifier-gain switching.

stacking

Stacking reduces only production cost. Stacking input attenuators reduces the total number of parts required for a given range of input deflection factors. The representative VOLTS/DIV selector (shown in Fig. 2-15A) and information so far presented, leads one to believe each switch position

is a separate attenuator circuit. This 11-position selector indicates 10 RC voltage dividers. (X1 is not considered a voltage divider.) There are not necessarily 10 networks. Five networks, eliminating a number of parts but adding a slightly more complex switching system, provide the same result as 10.

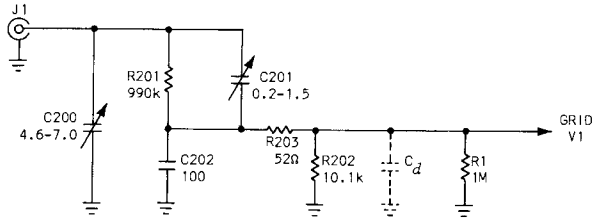
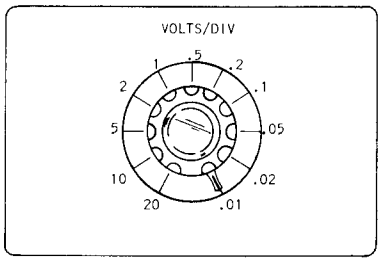


Fig. 2-14. The X100 attenuator of a "fast" preamplifier.



(A)

VOLTS/DIV	NETWORK	STACKED WITH
0.01		
0.02	(÷) X2	
0.05	(÷) X5	
0.1	(÷) X10	
0.2	(÷) X10	(÷) X2
0.5	(÷) X10	(÷) X5
1.0	(÷) X100	
2.0	(÷) X100	(÷) X2
5.0	(÷) X100	(÷) X5
10.0	(÷) X1000	
20.0	(÷) X1000	(÷) X2

(B)

Fig. 2-15. Stacked-attenuator switching logic.

stacking program

Stacking cascades, by switch selection, voltage dividers to multiply attenuation ratios. Fig. 2-15B lists a stacking program. The first column lists selected input deflection factors; the second, primary attenuators selected; and the last column, the selected cascaded attenuator. For input deflection factors 0.01 VOLTS/DIV through 0.1 VOLTS/DIV only primary attenuators appear. Selections 0.2 VOLTS/DIV through 20 VOLTS/DIV utilize X2 and X5 attenuators in cascade; of this group 1 VOLTS/DIV and 10 VOLTS/DIV utilize primary attenuator selections alone.

÷ and X interchangeable

Symbols (÷) and (X) both appear in Fig. 2-15B. These symbols are interchangeable and either may appear on a schematic diagram. Read X2 as an attenuation of 2; and ÷2 as a voltage division of 2.

Compare Fig. 2-15B and Fig. 2-16. Fig. 2-16 illustrates a stacked X20 or ÷20 input attenuator. Fig. 2-15B indicates attenuation results from selection of 0.2-VOLTS/DIV input deflection factor. Each attenuator network presents 1-MΩ input impedance. Therefore, connecting the X2 network across R102 shunts the same as R102 connected to the grid of V1. R1 does parallel R22. Both X10 and X2 attenuators then load as though connected in the circuit alone. Proper voltage division occurs:

1. 200 millivolts at J1 develop 20 millivolts at junction R101-R102.

2. 20 millivolts across the X2 attenuator develop 10 millivolts at the grid of V1.

Stated in terms of deflection factor:

1. 200 millivolts/division at J1.

2. 20 millivolts/division input to the X2 attenuator.

3. 10 millivolts/division at the grid of V1.

Selecting 0.5 VOLTS/DIV substitutes a X5 attenuator. Input voltages now receive an attenuation of 50. Concepts remain the same for all stacked configurations.

compensation

One compensates these dividers in switch positions that place single networks in the circuit. From Fig. 2-15B, these positions of the VOLTS/DIV selector would be: 0.02, 0.05, 0.1, 1.0 and 10. Selecting stacked positions creates the need for compromise adjustment. Unfortunately, stacking limits minimum input capacitance. The electro-mechanical effects of each stack adds capacitance.

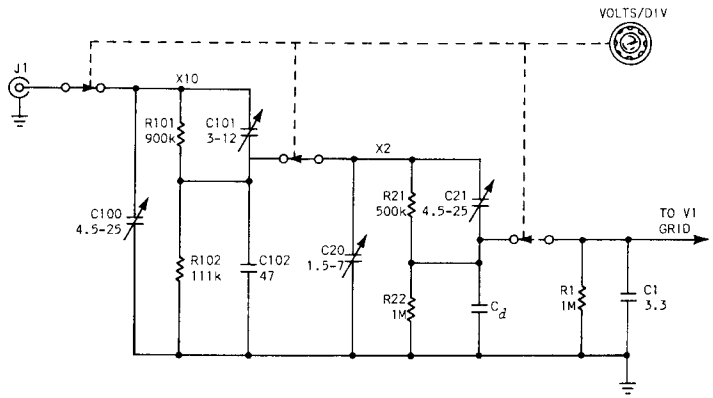


Fig. 2-16. X20 or ÷20 stacked attenuator.

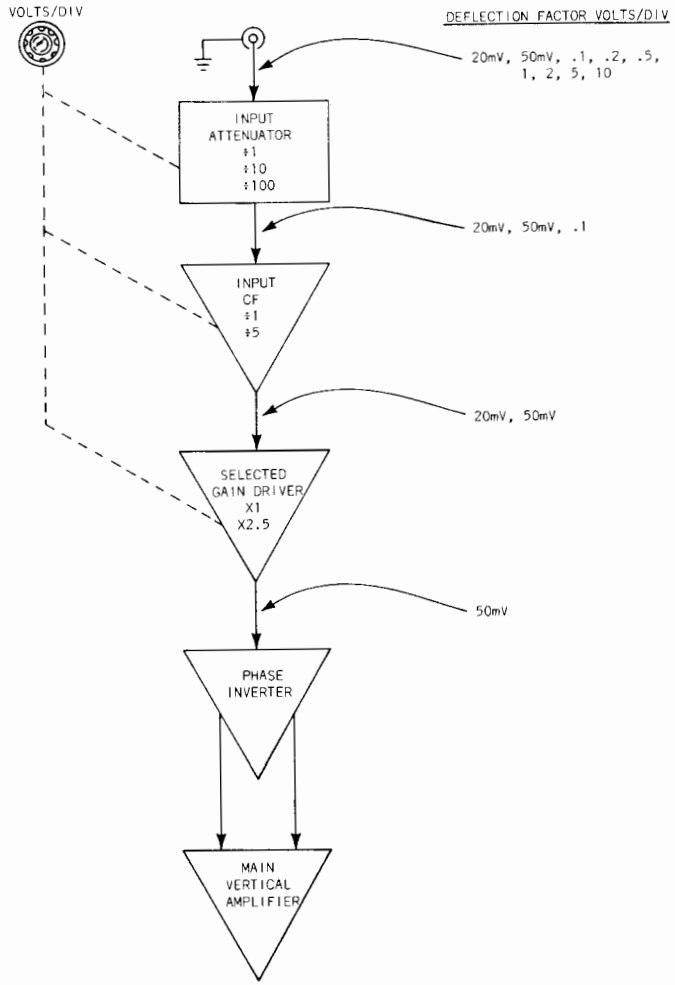


Fig. 2-17. Preamplifier switching logic.

gain switching

Amplifier-gain switching, mechanically ganged to the input attenuator, provides the present solution for numerically reducing input attenuator networks. Fig. 2-17 shows in block form the switching logic necessary to drive a phase inverter at a constant deflection factor. Blocks labeled Input Attenuator, Input Cathode-Follower and Selected-Gain Driver mechanically gang to the VOLTS/DIV selector. Deflection factor at the input jack is from 20

input attenuator

input CF

millivolts to 10 volts per division, step-selected in a 1-2-5 sequence. The three input dividers reduce the nine input deflection factors to three: 20 millivolts, 50 millivolts and 100 millivolts.

selected-gain driver

Selecting cathode-follower gain of 1 or 1/5 gives an input deflection factor to the selected-gain driver of 20 and 50 millivolts per division. The selected-gain driver can now have a constant output deflection factor.

Wafer switches contribute significantly to total capacitance, even to the simplest input attenuators. Stacking compounds the difficulty. Stray inductance increases due to wiring complexity as well as stray capacitance.

turret attenuator

The device which reduces stray reactances the most is the seldom used turret attenuator. Fig. 2-18 is a photograph of one type of Tektronix turret attenuator. The body of the turret holds voltage-divider components. These parts need have very short leads thereby reducing inductance. Rotating the turret body moves voltage-divider parts and associated connectors to the single set of switch contacts. No method yet devised contributes as few reactances as the turret attenuator.

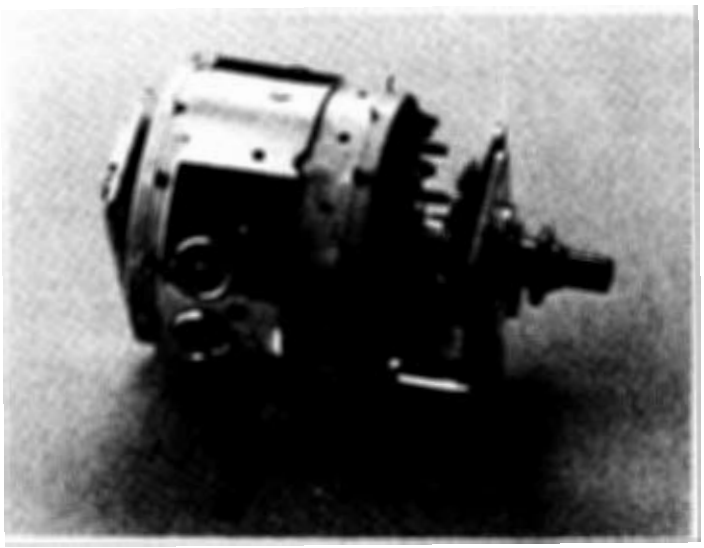


Fig. 2-18. Turret attenuator.

Turret attenuators at present just don't lend themselves to quantity production. For this reason only a few Tektronix instrument types contain turret attenuators.

Modern oscilloscopes have a constant input RC. The input attenuator consists of compensated voltage dividers. Deflection factors change in one of three basic methods:

1. Selecting one of a group of compensated voltage dividers.

2. Program selecting stacked compensated voltage dividers.

3. Amplifier-gain switching combined with one of the above techniques.

3

FOLLOWERS

three basic configurations

Followers consist of three basic circuit configurations: Cathode followers, source followers and emitter followers. Follower circuits might appear in any stage of oscilloscope circuitry. Basic follower characteristics justify such wide usage. Characteristics necessary to achieve uniform frequency response over a wide range of input frequencies and amplitudes are indigenous to followers:

1. Low input capacitance (high input impedance).
2. Low output impedance.
3. Linear amplification.
4. Gain stability.
5. Can handle large input voltage swings.

Additionally, there are peculiar characteristics of followers that are made use of:

6. Gain is less than one but can be made to approximate unity.
7. No signal inversion.
8. Quiescent level is easily set.
9. Supply voltage fluctuations are greatly attenuated at the output.

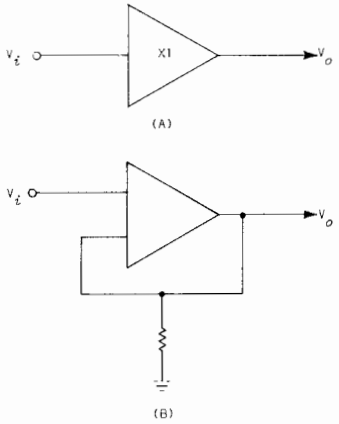


Fig. 3-1. Follower symbols.

circuit symbols

Circuit symbols, as shown in Fig. 3-1, apply to followers. (A) symbolizes a unity gain amplifier. However, one might interpret (A) to indicate phase inversion unless the initials CF, SF, or EF appear within the triangle. CF abbreviates cathode follower; SF, source follower; and EF, emitter follower. On the other hand, symbol (B) is exclusive to followers. This symbol indicates noninverted unity gain. Both symbols appear in block diagrams through this book.

CF, SF and EF abbreviations

low input capacitance

Any discussion of follower circuitry in wideband amplifiers utilizes the terms impedance transfer or isolation. These terms generally apply to all characteristics but specifically consider the first two: low input capacitance (another term for high input impedance) and low output resistance.

low output R

risetime improvement

Fig. 3-2 illustrates the principle of placing a follower between a large resistive output and a large capacitive input to improve risetime. Risetime (bandpass) of an amplifier is a function of the product of resistance and capacitance. 2.2 RC defines circuit risetime. Follower amplifier A2 shunts the large output resistance of A1 with a small capacitance. A2 also presents to A3 a small R_O to shunt the large input capacitance of A3. The resultant risetime is less than connecting A1 directly to A3.

input amplifier

Followers are not restricted to interstage isolation. They also function as output amplifiers or, as shown in Fig. 3-3, input amplifiers. The followers' high input impedance shunts the attenuator very little, allowing passive device values to set input impedance at J1. Of the three basic follower configurations, cathode followers currently appear most frequently as input amplifiers.

cathode follower

Fig. 3-4 shows a cathode follower. In this figure, a pulse applied to the grid develops at the cathode with corners rounded and attenuated. Consider first the signal attenuation. Attenuation implies

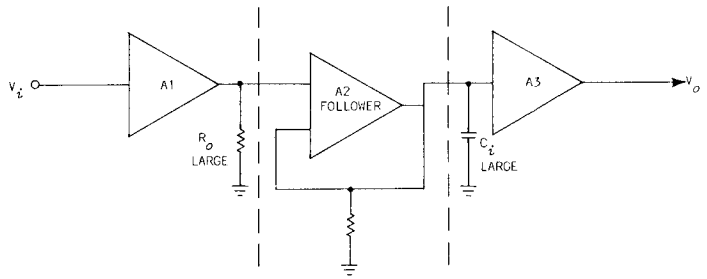


Fig. 3-2. Isolation block diagram.

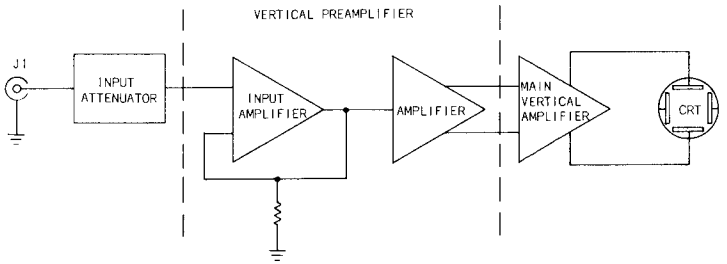


Fig. 3-3. Vertical-amplifier block diagram.

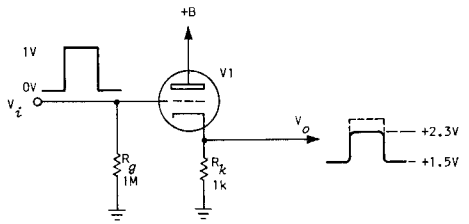


Fig. 3-4. Cathode follower.

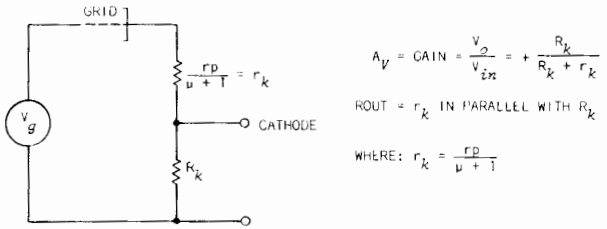


Fig. 3-5. Equivalent CF circuit (1).

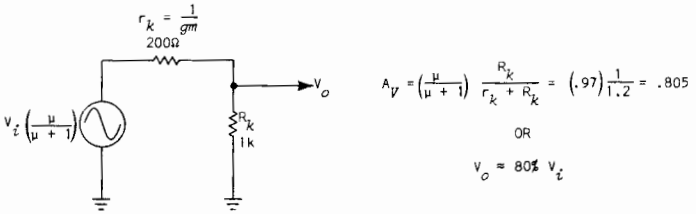


Fig. 3-6. Equivalent CF circuit (2).

voltage-divider action and that is just what happens. The voltage applied to the grid develops across R_k and the internal impedance of V1.

Fig. 3-5 depicts a cathode-follower model. A theoretical voltage generator, or source, drives the control grid. Grid voltage (V_g) develops across a voltage divider consisting of external cathode load (R_k) and internal tube impedance (r_k). Formulas included in Fig. 3-5 define gain as a voltage-divider ratio. They also show that output impedance at the cathode terminal results from R_k paralleling r_k.

Active device parameters such as amplification factor (μ) and plate resistance (rp) must be considered. Because transconductance (gm) applies to any active device, it appears more often in this book than any other dynamic parameter.

Using parameters μ and gm, one builds the cathode-follower model shown in Fig. 3-6. This figure assumes $\mu = 30$ and $gm = 5000$ µmho. The voltage source applies grid voltage, modified by μ, across voltage divider r_k and R_k. Both models (Figs. 3-5 and 3-6) develop gain of 0.8, indicating active parameter interdependence.

gain approximations ignore μ

Usually satisfactory approximations result from using transconductance alone. Discarding μ in the gain formula of Fig. 3-6 leaves the resistance ratio only. Gain now resolves to 0.83, sufficiently accurate for most circuit analysis.

transconductance determines output impedance

Parameter *gm* establishes output impedance as shown in Fig. 3-7. Output circuits connect to the junction of R_k and r_k. Therefore, output impedance (R_O) cannot exceed the value of $r_k\left(\frac{1}{gm}\right)$. High *gm* devices present a smaller R_O to output circuits than low *gm* devices.

plate current affects *gm*

Plate current affects *gm*, causing questionable gain stability of the circuit shown in Fig. 3-8. For small signals this circuit might be satisfactory. But large signal gain stability does not exist because of the large change in plate current. The circuit as shown experiences 65% plate current change. Plate current and *gm* relate directly and gain is a function of *gm*:

$$r_k = \frac{1}{gm}.$$

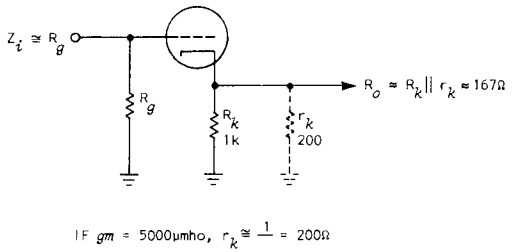


Fig. 3-7. CF output impedance.

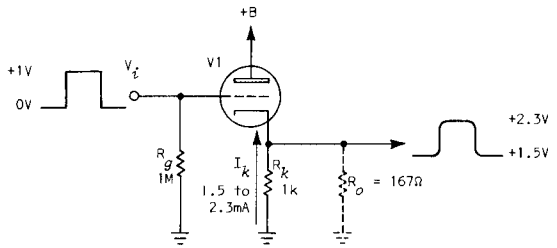


Fig. 3-8. CF signal current.

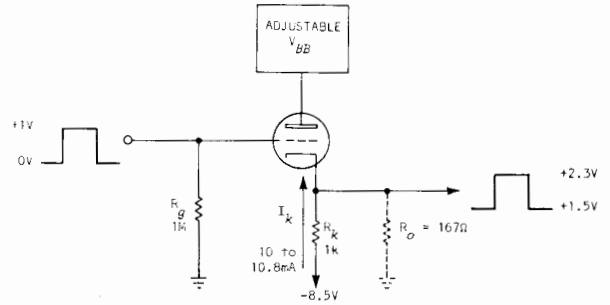


Fig. 3-9. Plate voltage determines output level.

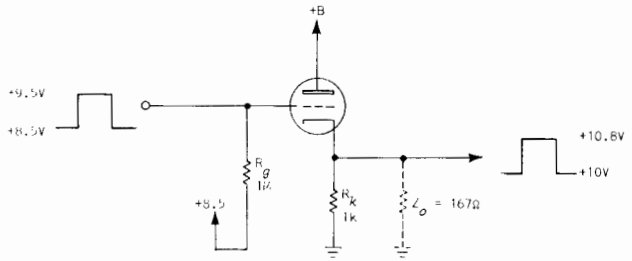


Fig. 3-10. Positive grid return equivalent to negative cathode return.

gain stability results from constant plate current

Fig. 3-9 represents an improvement. Notice that output DC levels, output impedance and gain are the same as in Fig. 3-8. An adjustable plate return sets the quiescent output DC level. Plate current is determined by self-bias, R_k and the negative cathode supply voltage. The positive signal excursion now causes only 8% change in plate current. This percentage reduces further when both R_k and the negative return increase. For example, if R_k were 2 kΩ returned to a -18.5 V supply, an input signal of 1 V would cause 4% plate-current change. The external components free the circuit to act as a constant-current device. Fig. 3-10 functions the same as the circuit in Fig. 3-9 except the cathode resistor returns to ground.

longtailing

constant I_p stabilizes *gm*

A method of current driving an active device, so popular it has a name, is shown in Fig. 3-11. This is a *longtail* circuit. The name derives from the large cathode resistor. Ratio of r_k to R_k is such that output impedance is $\frac{1}{gm}$ and gain is $\frac{\mu}{\mu + 1}$. One volt signal causes less than 3/4% change in plate current, stabilizing transconductance.

The cathode returns to -150 volts through 30 kΩ. Operating characteristics demand cathode potential of +1.5 volts at quiescence. 5.05 mA then flows under no signal conditions. Increasing grid voltage 1 volt increases cathode current by 0.03 mA or a total of 5.08-mA plate current.

This small change hardly affects *gm*. Notice that gain approaches unity. The longtailed cathode follower meets most of the follower requirements.

Fig. 3-12 shows a longtail configuration returning R_k to ground. Concepts remain as explained.

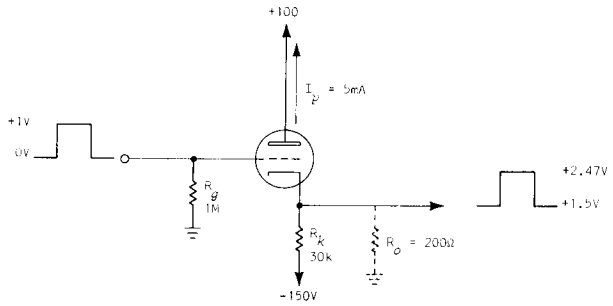


Fig. 3-11. Longtail cathode follower.

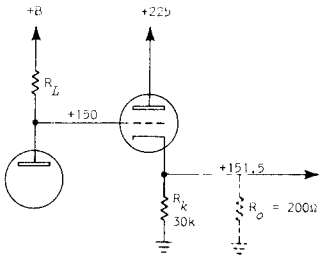


Fig. 3-12. Longtail CF with cathode returned to ground potential.

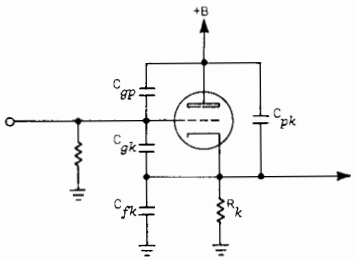


Fig. 3-13. Interelectrode capacitance.

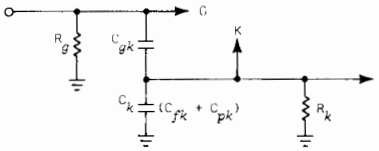


Fig. 3-14. Input capacitance.

triode capacitances

The presentation assumed only resistive components acted upon signals, yet reactive elements exist in *any* circuit. Reactive components within the tube, grid-to-plate and grid-to-cathode capacitance, are of greatest concern. The effect of these capacitors depends upon circuit design. Fig. 3-13 identifies triode capacitances.

How much a capacitor affects a signal is determined by the signal voltage across the capacitor. C_{gp} and V1 plate return to a low-impedance voltage supply. Cathode follower design then innately reduces the effect of C_{gp}, although still a circuit component.

gain and grid-to-cathode capacitance establish input capacitance

If unity gain could be realized, capacitance from grid to cathode could be ignored. With no voltage difference across the capacitor, equivalent capacitance is zero. Equivalent grid capacitance then is C_{gk} multiplied by one minus voltage gain: [$C_g = C_{gk} (1 - A_V)$]. Another reduction is illustrated in Fig. 3-14. Capacitance, filament-to-cathode and plate-to-cathode, appears in series with

C_{gk}. Assume cathode follower input capacitance falls between less than one picofarad and two picofarads.

output impedance provides charge path for output capacitance

Capacitance, associated with cathode-follower output, rapidly charges through the low-output impedance. This capacitance affects the performance of "fast-rise" amplifiers and as such receives attention later in the chapter. Ignore, for now, cathode-follower output capacitance.

typical circuits

Vertical amplifiers having a frequency response of DC to ten megahertz or so contain cathode followers as developed. Fig. 3-15 through 3-20 are examples of typical oscilloscope circuits using concepts presented.

Fig. 3-15 shows a pair of cathode followers driven push-pull. These longtailed circuits function to breakup parallel capacitive networks.

V6 and V7 operate independently to act as a kind of coupling circuit. R6 and R7, in conjunction with the positive grid potentials, longtail V6 and V7. DC levels and signal amplitudes applied to the output amplifier approximate values applied to V6 and V7 grids.

Both the preamplifier and main vertical output amplifiers are plate loaded. A longtailed cathode follower presents much less input capacitance and

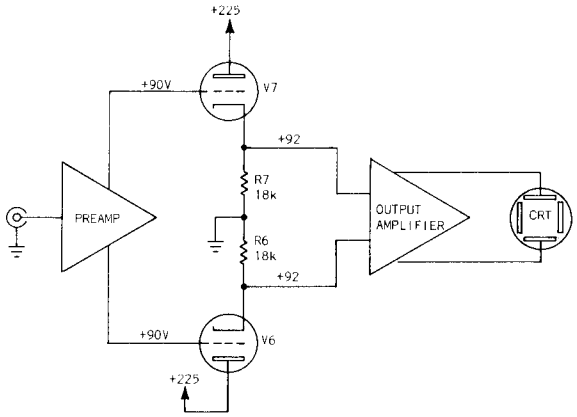


Fig. 3-15. Main vertical input amplifier.

output impedance than a plate-loaded amplifier.

risetime improvement

Placing the cathode followers between the plate-loaded amplifiers then improves risetime. The small input capacitance of V6 and V7 shunts the preamplifier output, while the relatively large input capacitance of the output amplifier rapidly charges and discharges through the small R_o of V6 and V7.

Series peaking coils may appear in the output leads of V6 and V7.

Fig. 3-16 depicts a cathode-follower circuit, used to improve bandwidth (risetime), which includes a balance control within the longtail network.

coupling devices

Driven push-pull, V1 and V2 operate independently. Grid DC and signal levels originate within the preamplifier. The cathode followers merely couple preamplifier voltages to the driver amplifier, elevated by a DC level representing self bias.

R4 serves to reduce the positive supply voltage to the correct operating level at V1 and V2 plates. R4 is common to V1 and V2 plate current. Push-pull signal currents flow in V1 and V2 and these equal-amplitude opposite-phase currents maintain a constant drop across R4. A capacitor bypassing R4 is thus superfluous.

centering control

One sets R3 for a vertically centered CRT display. Most main vertical amplifiers consist of cascaded direct-coupled push-pull stages. Any imbalance at the input, amplified, deflects the CRT as a signal. This is the correct action for DC measurements.

centering empirical

Quiescently however, the CRT display must center. Placing a ground at input connector J1, one adjusts R3 to compensate for: An unbalanced preamplifier, small differences between V1 and V2, and unbalanced conditions of following stages.

Changing R3 changes V1 and V2 plate currents in opposite quantities. Plate current and *gm* track. Therefore, adjusting R3 affects small changes in cathode-follower gain in opposite quantities.

Breaking up capacitive networks to improve high-frequency response or risetime sums up the purpose of the circuit in Fig. 3-17.

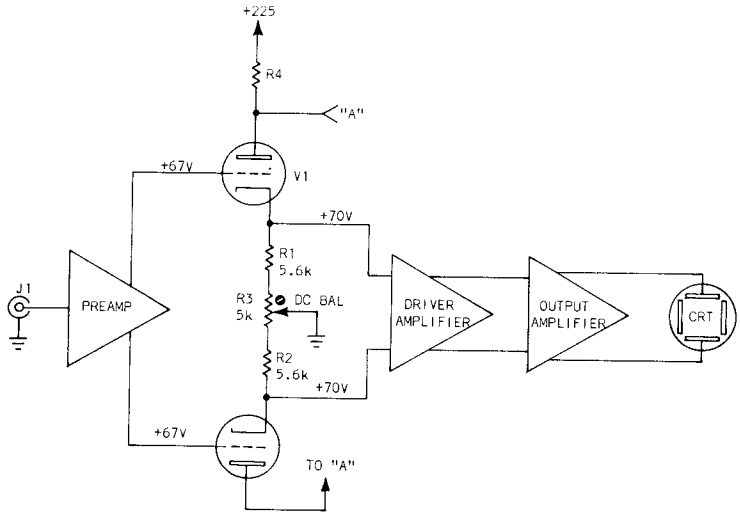


Fig. 3-16. Main vertical input amplifier.

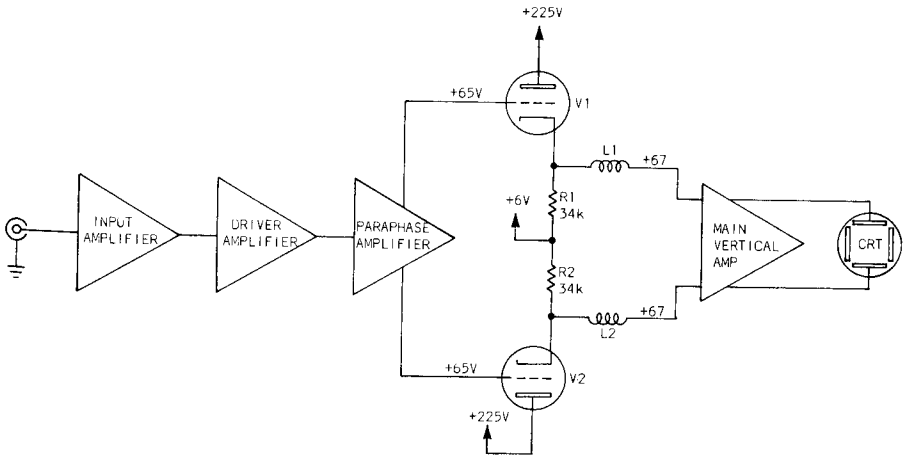


Fig. 3-17. Preamplifier output amplifier.

V1 and V2 drive, both signal and DC level, originates in the phase inverter; this is a direct-coupled push-pull cathode-follower stage. The circuit is longtailed by R1 and R2 grid levels and cathode return supply. Amplitude of drive is also a factor in longtailing, and this circuit is a case in point.

Voltage drop across R1 and R2 is much less than circuits thus far presented but consider the signal magnitude. A typical deflection factor is 100 mV (push-pull) per division. Translated to one grid, 50-mV signal drive to V1 results in one-division vertical deflection at the CRT. 500 mV deflects 10 divisions, but causes less than 1% change in V1 or V2 cathode current.

connector capacitance increases risetime

Preamplifiers are frequently plug-in units. Interconnecting plugs have an appreciable capacitance. High-impedance drive, such as the output of the phase inverter, charges and discharges this capacitance slowly enough to cause risetime or high-frequency deterioration. Placing a cathode follower between the two improves conditions. Capacitance of the interchassis connector is driven by a small output impedance, and the high impedance of the phase inverter drives a very small capacitance. L1 and L2 series-peak to improve high-frequency response.

The push-pull longtailed cathode follower shown in Fig. 3-18 drives a capacitive load. This circuit includes beam-position indicators as an operator aid.

Cathode followers V1 and V2 provide a low-impedance charge path for the capacitance presented by the vertical deflection plates. R1 and R2, cathode return supply, and grid voltages longtail V1 and V2. Network R3, B1, B2, R4 and R5, shunts longtailing but this network imposes negligible loading.

beam-position indicators

Located on the front panel, neon lamps B1 and B2 indicate relative vertical displacement:

Both lamps off, display centered.

Up lamp (B1) on, display deflected above center.

Down lamp (B2) on, display deflected below center.

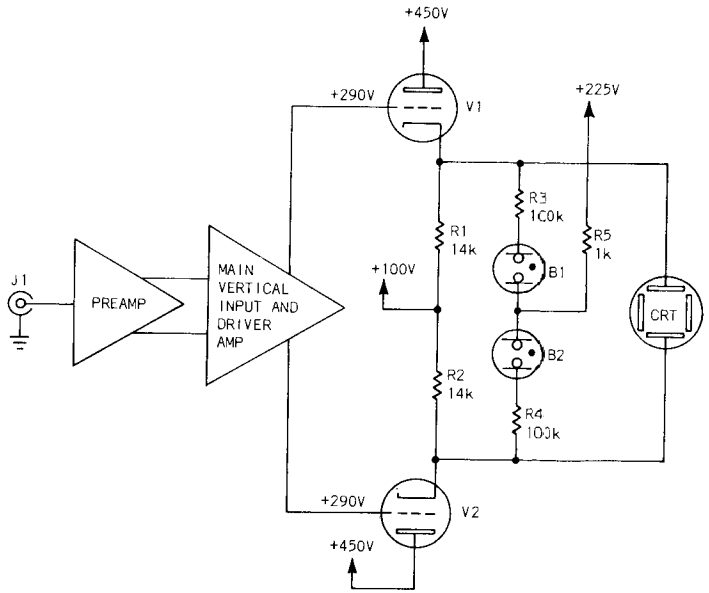


Fig. 3-18. Output amplifier.

Under no signal conditions, with the trace centered, neither neon fires. Cathodes of V1 and V2 are not quite positive enough for firing potential across the glow tubes. Positioning the trace upward raises V1 cathode and B1 fires. Positioning the trace below center raises the cathode of V2 and B2 fires.

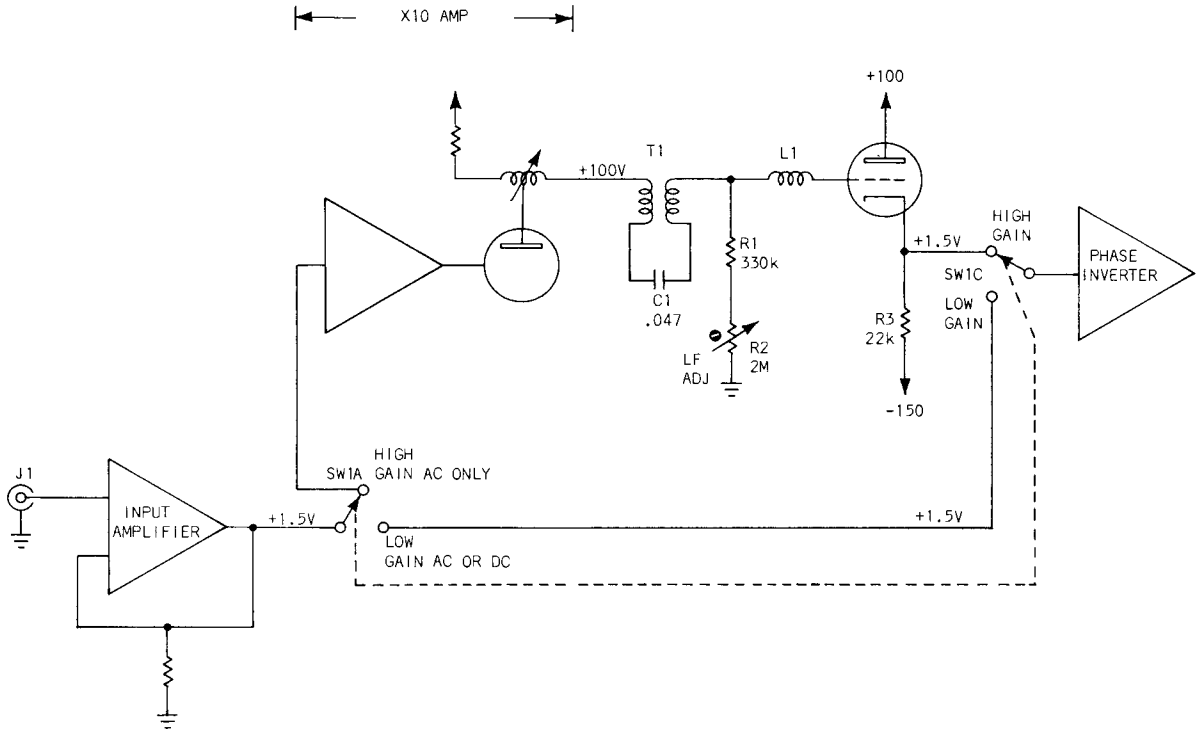


Fig. 3-19. AC coupled follower.

small signals AC only

Frequently one needs to observe small AC voltages superimposed on a relatively high DC level. An AC-coupled vertical amplifier allows one to monitor only the small AC component at low input deflection factors. Fig. 3-19 represents a preamplifier capable of amplifying small AC signals.

high gain

low gain

Positioning SW1 to HIGH GAIN AC ONLY, as shown, routes input amplifier signals to the X10 amplifier; then via cathode follower V4 to the phase inverter. Throwing SW1 to LOW GAIN AC OR DC directly connects the input amplifier and phase inverter.

The X10 amplifier increases small signal voltages to amplitudes appropriate to the phase-inverter input deflection factor. But, these signals suffer a frequency-dependent phase shift; and the quiescent DC level at both contacts of SW1C should equal.

X10 amplifier compensation appears in longtailed cathode-follower V4 circuitry. This circuit has several functions:

1. Isolates the high-impedance X10 amplifier and phase inverter.
2. Matches the input-amplifier output DC level.
3. Broadband input coupling.
4. High-frequency compensation.
5. Low-frequency phase compensation.

quiescent output of X10 and input amplifiers match

Switching from high gain to low gain one should observe very little vertical trace movement. To accomplish this the quiescent output of the X10 amplifier and input amplifier must closely match. AC coupling (C1) allows a ground return for the grid of V4. Stabilized by longtailing the self-biased operating point for V4 equals the output DC level of the input amplifier.

T1 couples signals around C1

C1 couples low frequencies and T1 couples high frequencies around C1. C1 is both hero and villain. It must have a voltage rating high enough to prevent breakdown and enough capacitance to pass low frequencies. These requirements determine physical construction of C1. Shunt capacitance to the chassis, due to physical properties and placement of C1, deteriorates high-frequency response. The primary of

T1 is in series with C1 and as shunt capacitive current increases, transformer action increases. The circuit suffers very little high-frequency signal loss.

L1 series peaks

Both amplitude and phase compensation are shown. L1 and the input capacitance of V4 develop series peaking for high-frequency amplitude compensation. Low-

C1, R1 and R2 phase compensate

frequency phase compensation depends on the time constant of RC network, C1, R1 and R2. One adjusts R2 for optimum presentation, such as pulse train symmetry.

triode connected

One frequently sees, in equipment designed a few years earlier than this writing, triode-connected pentodes as cathode followers. Consider these devices as high-*gm* triodes.

pentodes as cathode followers

The active device in Fig. 3-20 is a pentode. Cathode-follower-connected pentodes function as described for triodes, keeping in mind the difference in tube characteristics. For example: $r_k = \frac{1}{gm}$, but μ in a pentode is so large that formula $\frac{\mu}{\mu + 1}$ is meaningless. Therefore, assume the signal voltage across divider r_k and R_k equal to control-grid signal voltage.

The circuitry of Fig. 3-20 makes use of the screen-grid to improve signal-to-noise ratio at low signal levels.

screen grid decoupled in "AC" only

Ganged switches SW1A and SW1B select high-gain or low-gain amplification. SW1 (positioned as shown) in the LOW GAIN position sets the input deflection factor to 50 millivolts per division. That is, a 50-millivolt control-grid signal results in one division deflection at the CRT. Placing SW1 to HIGH GAIN increases input sensitivity by a factor of ten. The high-gain amplifier has an input deflection factor of 5 millivolts per division *AC only*.

screen decoupling degenerates cathode DC signals

In low-gain operation both AC and DC are amplified. Putting high-impedance decoupling networks in the screen circuit, such as R2-C1, degenerate DC signals at the cathode. Therefore, the screen grid returns to a low-impedance regulated supply. The supply has ripple and transients, which reflect into the cathode as signals. In the low-gain mode these signals are too small to notice.

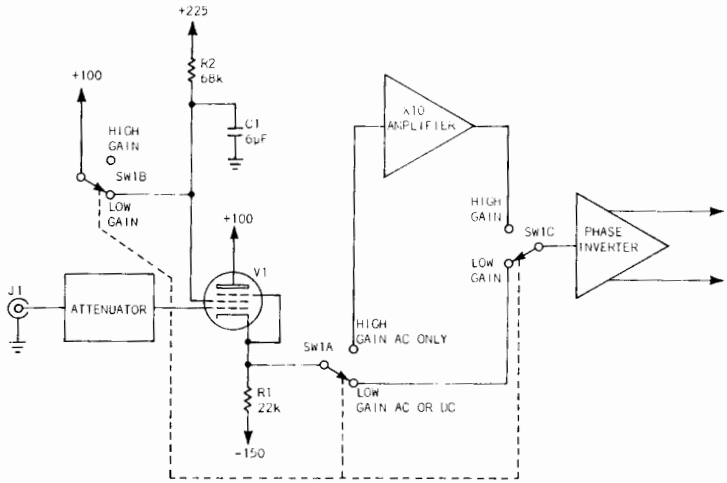


Fig. 3-20. Pentode cathode follower with switched screen grid decoupling.

Increasing the sensitivity (switching to high gain) means a smaller voltage may be monitored, but it also means that the screen grid-induced signals become objectionable. A large decoupling network returned to a higher supply results in a clean signal.

Cathode-follower circuits are a good medium for presenting protective and corrective devices. Protection frequently provides for either operator error or component failure. Corrective devices compensate for unusual or unwanted circuit parameters.

Some circuits correct for undesirable characteristics of active devices that are not apparent or objectionable until very small amplitude signals must be amplified. As an example, control grid current exists in any electron tube. In tubes employing unipotential cathodes, both positive and negative grid currents flow. Positive grid current consists of electrons emitted by the cathode and intercepted by the control grid. Negative grid current results when a heated negative control grid emits electrons to the cathode, adding to the effects of gas molecules and leakage current between the control grid and other tube elements.

positive grid current

negative grid current

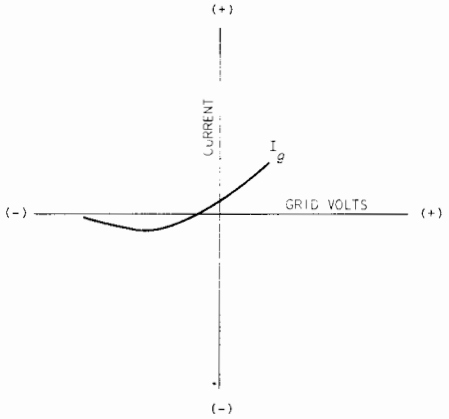


Fig. 3-21. Control grid current versus bias.

Fig. 3-21 graphically illustrates grid current versus grid bias voltage. The horizontal axis extends from a few volts negative through zero to a few volts positive. The vertical current axis extends from a small negative quantity (grid-to-cathode flow) through zero to a small positive quantity (cathode-to-grid flow). At extreme negative bias a small negative grid current flows.

grid current bias intercept

Reducing bias toward zero, negative grid current increases then decreases, intercepting the horizontal at a low negative-bias level. Incremental axis values vary between tube types and to a smaller degree between the same type of different manufacture. Generally, the grid-current grid-bias intercept occurs at less than -1.5 volts.

negative grid current minute

Magnitude of negative control grid current is so small that it is sometimes ignored. When an amplifier must amplify low-level signals (1 to 20 millivolts), this grid current can no longer be neglected. 5 nanoamps of grid current through R1 of Fig. 3-22 raises the grid potential to a level of 5 millivolts. A solution, returning R1 to a negative 5 millivolt supply, results in zero volts from grid to ground.

negative grid return cancellation

Negative grid current continues to flow developing positive grid voltage (Fig. 3-23). When negative grid current develops a voltage across R1 equal to the voltage at the wiper of R4, zero volts appears

between control grid and ground. One checks the setting of R4 by shorting the control grid of V1 to ground. R4 is properly set when the short application and removal causes no displayed vertical deflection.

Positive grid current can be used to advantage. To set up conditions, suppose an operator is measuring ripple on a 500-volt DC power supply. His instrument in X1 attenuation, he inadvertently

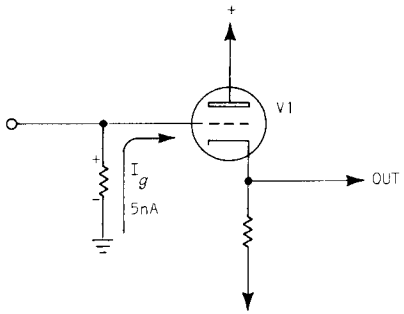


Fig. 3-22. Negative grid current.

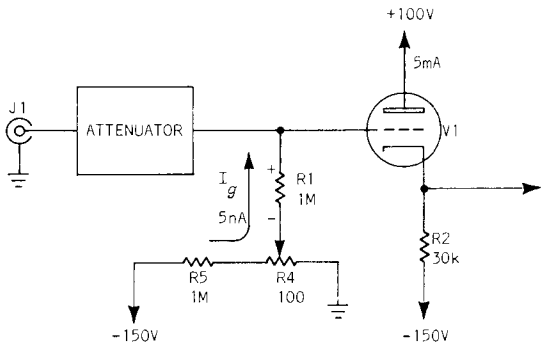


Fig. 3-23. Input-amplifier grid-current adjustment.

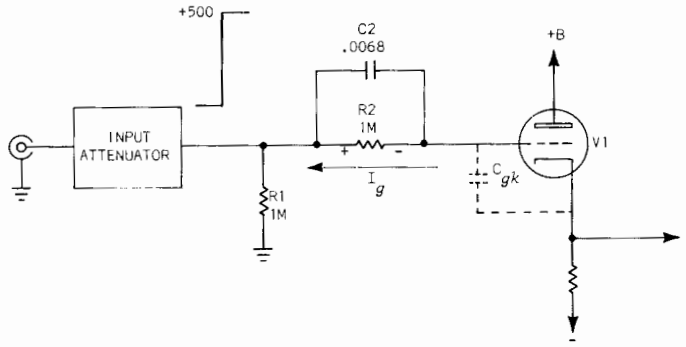


Fig. 3-24. Grid limiting.

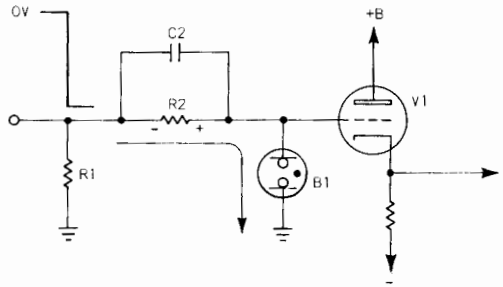


Fig. 3-25. Neon-lamp clamping.

leaves the input selector at DC. Refer to Fig. 3-24. Positive grid current in this circuit prevents a catastrophic failure. 500 volts to an input-amplifier grid requires more power than the tube or associated components safely dissipate. However, grid limiting due to positive grid current and R2 maintains tube current at a safe value.

grid limiting

C2 bypasses R2 so the network does not affect normal signal inputs. C2 provides a current source for discharge of C_{gk} which accumulates a charge during any voltage drop across R2.

C2 charges C_{gk}

Fig. 3-25 shows protection from excessive negative as well as positive excursions at an input-amplifier grid. Excessive potential fires B1. Until this

neon protection

voltage is removed B1 holds the control grid to "on" voltage for B1. B1 extinguishes upon removal of excess input voltage.

Protective circuits incorporated as part of an input amplifier frequently protect following stages (Fig. 3-26). Keep in mind the high probability of direct coupling to following stages. Excessive CF output voltage can result in following stage part damage.

output clamps

D1 and D2 clamp to prevent large output-voltage excursions. Interruption of V1 conduction, such as open filaments, allows the output DC level to seek the -150 volt level to which R_k returns. D1 turns on to clamp as negative output voltages extend below ground potential. Large positive signals turn D2 on. D2 clamps when output-signal excursions exceed +5 volts. D1 and D2 allow a voltage "window" of 5 to 7 volts.

output voltage window

Semiconductor junctions (diodes) require a "turn-on" or forward bias dependent upon chemical make-up. Once turned on these devices maintain a voltage drop across the junction approximating turn-on potential. Assume that turn-on and diode voltage drop are equal. The list below includes semiconductor type and junction voltage drop:

1. Gallium Arsenide (GaAs) 1-V turn-on.
2. Germanium (Ge) 0.2-V turn-on.
3. Silicon (Si) 0.6-V turn-on.

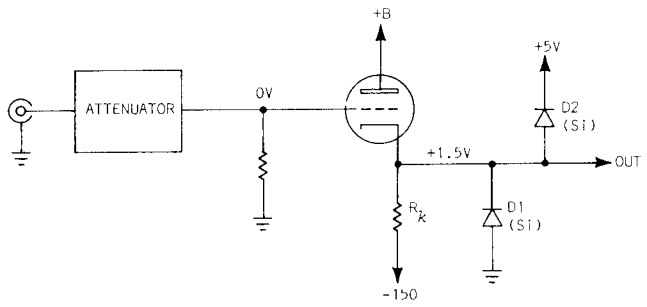


Fig. 3-26. Diode protection.

Although these values are not precise, they suffice for the purpose of this book. All following discussions consider the above as true conditions. Further, all semiconductors in this book are identified as: GaAs, Ge, or Si, when applicable.

2.1-volts negative voltage swing

Diode D1, of Fig. 3-26, conducts when cathode voltage reaches -0.6 V; then clamps at -0.6 V; and turns off when cathode voltage becomes more positive than -0.6 V. Negative signals may vary from quiescence, +1.5 V to -0.6 V -- a maximum negative voltage change of 2.1 V.

4.1-volts positive voltage swing

Clamping circuitry allows 4.1-volts positive-voltage changes. The cathode of D2 returns to +5 V. Therefore, when V1 output rises to +5.6 V, D2 turns on. This represents 4.1 volts more positive than quiescence. Output voltage then extends from -0.6 V to +5.6 V, or a "voltage window" of 6.2 V.

positive clamp endangers tube

A positive clamp (D2) in the circuit creates the need to protect V1. Assume a positive 10 volts appears at V1 grid. D2 clamps as V1 cathode passes +5.6 volts and, since a positive bias condition exists, tube current increases sharply. Positive tube elements must dissipate excessive power.

Fig. 3-27 includes a protective circuit which reduces electrode power-dissipation requirements. Components D3, C8 and R8 function to reduce plate voltage during overload conditions.

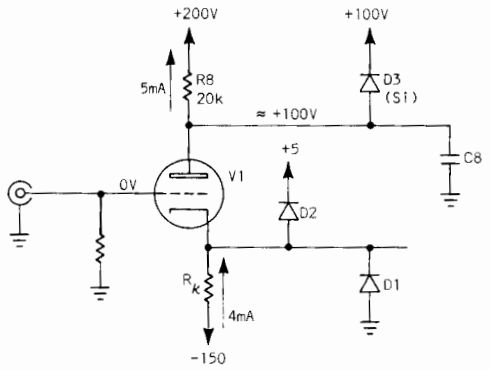


Fig. 3-27. Diode protection.

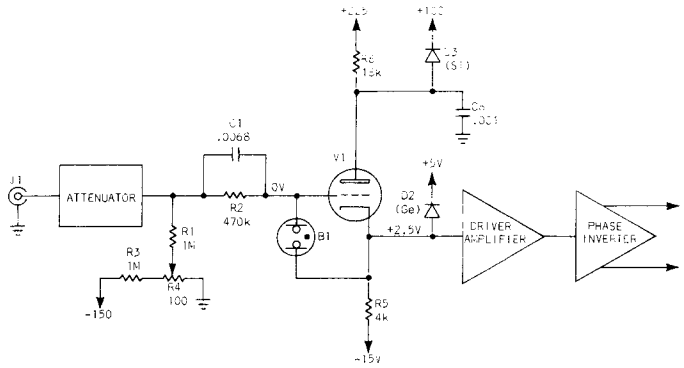


Fig. 3-28. Input amplifier.

At quiescence both V1 plate current and D3 current flows through R8 developing about +100 V plate voltage. C8 filters diode noise. Protective action begins when D3 disconnects. Assume again +10 volts at the control grid: D2 clamps causing a large plate current increase. This increased tube current drops more than 100 volts across R8, disconnecting D3. For each mA increase in plate current, plate voltage drops 20 volts. Tube parameters change drastically, but tube power (EI) remains at a safe level.

protection and correction

The longtailed input amplifier of Fig. 3-28 incorporates most of the protective and corrective concepts covered.

negative grid current

Grid resistor R1 returns to a negative voltage source. With R4 properly adjusted, negative grid current develops zero volts from V1 control grid to ground.

positive grid current

Positive grid current through R2 limits during large positive input excursions. Bypass capacitor C1 acts as a current source to discharge input capacitance.

glow lamp

Neon glow lamp B1 fires to maintain grid-to-cathode difference at a maximum of 50 to 60 volts.

output clamp

Diode D2 protects the driver amplifier by clamping when positive signal excursions reach +5.2 volts. The driver amplifier includes a negative clamp.

Longtailed cathode followers, as described, have two major disadvantages:

1. They do not follow negative-going signals with the same fidelity as positive-going signals.

2. High voltage is required.

positive risetime "faster" than negative

Output capacitance charge time is restricted only by internal impedance (r_k) for positive signal swings. Therefore, positive signal swings are at a *gm* determined rate. On the other hand, charge time for negative signal swings is determined by external cathode resistance. RC time for negative and positive signal swings can differ by hundreds of units. There is no cure for single-ended longtailed amplifiers. The negative slope always exceeds positive risetime. However, the negative slope should be linear for a wide range of signal amplitudes. To do this the longtail must provide a constant current over the range of signal amplitudes.

active device longtailing

pentode longtail

One solution makes R_k dynamic. (Fig. 3-29). A pentode substitutes for R_k. Pentodes operate with a very high plate resistance. This extends the negative supply many hundreds of volts and makes the constant-current characteristics extremely flat. 5-mA longtail current flows during both positive and negative input excursions. During positive excursions output capacitance charges through r_k of the cathode follower. Negative signals reduce follower conduction, but 5-mA longtail current continues to flow. The quantity of longtail current now flowing as cathode current is available to charge C_O. The circuit is very successful but requires rather high voltage supplies.

transistor longtail

Transistors have characteristics very similar to pentodes (Fig. 3-30). Q1 determines total circuit current and adjusting base voltage sets the output DC level to near zero volts. Supply voltages are low and constant-current characteristics are excellent.

feedback

Another solution is possible when driving a cathode-follower stage push-pull. The longtail is passive but an additional current source charges output capacitances (Fig. 3-31).

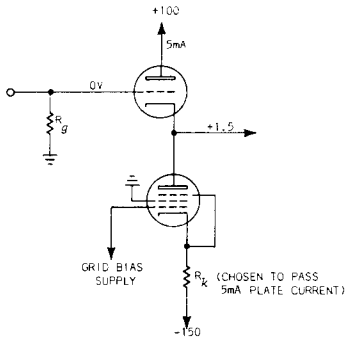


Fig. 3-29. Dynamic longtail using an electron tube.

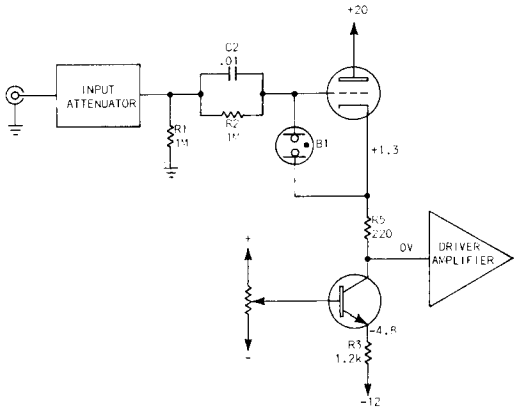


Fig. 3-30. Dynamic longtail using a transistor.

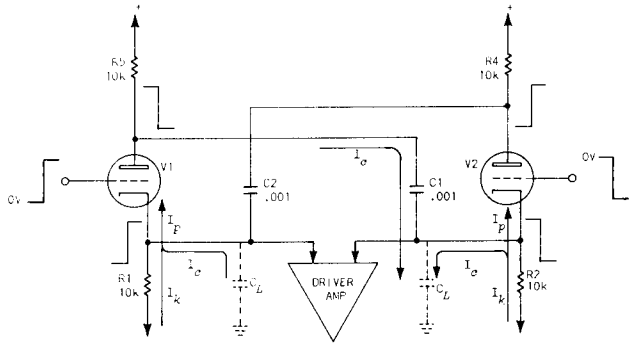


Fig. 3-31. Cathode followers with feedback.

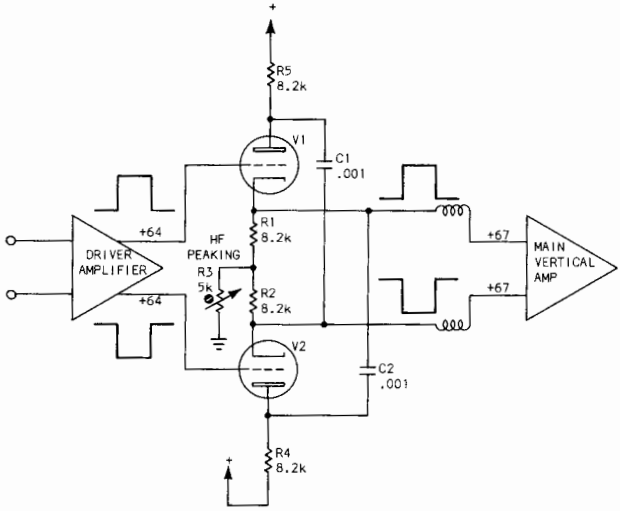


Fig. 3-32. Output amplifier with feedback.

V1 and V2 are push-pull driven cathode followers. Assume a positive step waveform applied to the grid of V1. A step of opposite phase but equal amplitude drives V2. Full cathode current and load capacitance determine V1 following rate. Time constant $R2C_L$ normally controls V2 following rate. However, V1 plate goes negative at V1 cathode rate and this signal couples to V2 cathode. Coupling capacitor C1 is large compared to C_L so load capacitance quickly charges, allowing V2 cathode to swing negative at the signal rate. C2 develops no charge since the stage has unity gain viewed from cathode or plate and the in-phase signals change at the same rate. Action is the same with phase reversal except the negative-going current source (plate of V2) assists V1 cathode.

unity gain at plate or cathode

In Fig. 3-32 the concept just discussed is shown as a preamplifier output stage, essentially a push-pull cathode follower with high-frequency balancing networks.

gm adjust termed HF PEAKING

Full cathode current and load capacitance determine the rate at which a cathode follower follows a positive-going signal; so adjusting R3 controls high-frequency response, thus the name HF PEAKING.

Miller-effect

A small Miller-effect, due to plate loading is present. For this reason cathode followers frequently drive this stage.

negative-input characteristics

Miller-effect, a degenerative signal fed to the grid from the plate by the grid-to-plate interelectrode capacitance, increases the input capacitance to an amplifier. Usually considered a disadvantage, Miller-effect can be utilized to improve overall response of an amplifier. It is one method of combating "negative-input resistance characteristics." These negative" properties, to which a longtailed follower is especially prone, distort input waveforms.

Input waveforms distorted

ringing

Under some conditions, a follower (cathode, emitter, or source) rings when a high-amplitude "fast" step is applied. This explains the name "negative-input resistance characteristic." The major effect upon vertical amplifiers occurs at the input amplifier. Capacitance at the grid changes during signal transit, upsetting the input attenuator compensation. Input capacitance is greater during "fast" signal changes than "slow." The cure increases quiescent capacitance so that input capacitance remains the same for all input waveforms.

Earlier the point was made that CF gain reduced C_{gk} because of the reduced voltage across the capacitance: $C_g = C_{gk}(1 - A_V)$, if $A_V = 0.95$, then only 5% of the input voltage develops across C_{gk}. C_{gk} is only 5% of listed value.

Fig. 3-33 and 34 show an initial A_V of 0.5. C_{gk} then is 50% of listed value. This is the *change* of input capacitance that affects compensation of the input attenuator. Total circuit reaction is rolloff.

From the standpoint of "negative-input resistance" the explanation takes a different tack but states the same thing.

charging input capacitances

Understanding properties of a "negative-input" requires, initially, application of current-voltage relation for a charging capacitor (Fig. 3-33). Capacitances involved are those making up input-capacitance of a cathode follower. Assume a "perfect" step applied. The input rises from a quiescent level to its peak voltage (V_{pk}) in zero seconds (T_0). Output cathode voltage rises from quiescence to V_1 at the input rate. Amplitude of voltage V_1 depends on the values of the capacitive voltage divider, C_{gk} and C_k.

I_p increases

Full-step amplitude appears at the grid while a portion develops across C_k. The initial voltage difference, positive bias, creates an increased plate-current demand (Fig. 3-34). This increased current charges C_k toward grid potential but also flows through C_{gk}.

regeneration

Input capacitance charging current (I_x) originates in the signal source flowing through internal source impedance R_i. This reactive current develops a voltage across R_i which adds to the grid voltage, which increases I_p, which increases I_x, which increases the drop across R_i, which . . . . Even if grid clamping occurs, initial regeneration distorts the input waveform.

Since the current flows through C_{gk}, label it reactive: I_x, and since the effect of I_x reduces input impedance, give it a negative sign.

negative resistance

The initial exponential rise from V_1 toward peak, across C_k, indicates a resistive component. This resistance has a relationship to R_k and r_k which decreases with I_p increases. Give this resistive element a negative value also.

-RC effect

If both a negative reactive current and a negative resistance are indicated, then an RC equivalent represents the effect.

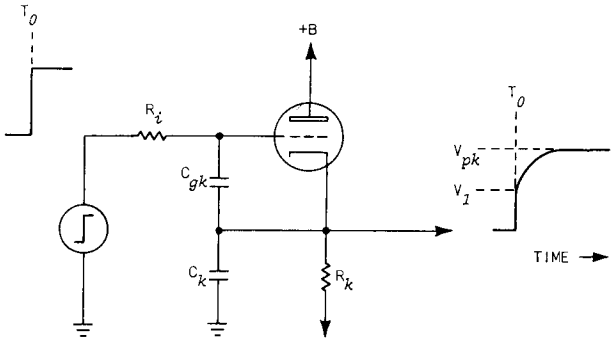


Fig. 3-33. Cathode-follower input capacitance.

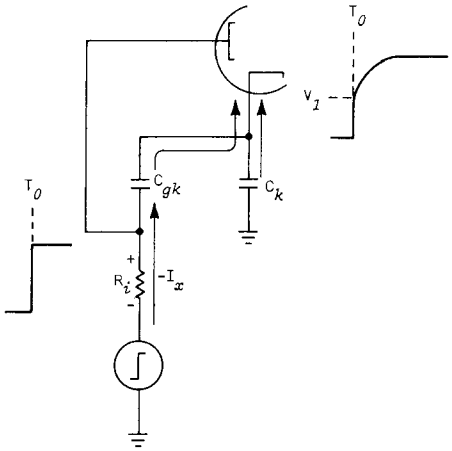


Fig. 3-34. Negative input characteristic current.

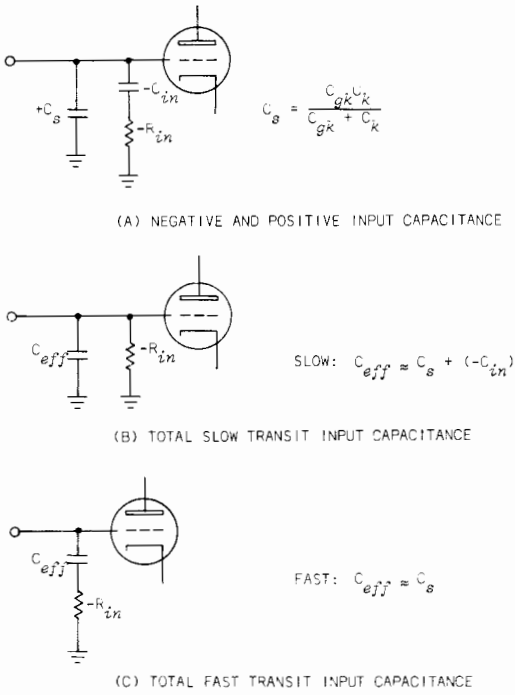


Fig. 3-35. Input capacitance.

equivalent circuits

Refer to Fig. 3-35, a schematic of equivalent input circuits. These three equivalent circuits are the basis for illustrating compensation concepts. (A) shows input capacitance lumped into one component, C_s. (B) and (C) illustrate the change in effective input capacitance (C_{eff}) with signal transit time.

input C lowest at low frequencies

At low frequencies, where $-I_x$ flows and exhibits capacitive phase shift, C_s and $-C_{in}$ add:

$$C_{eff} \approx -C_{in} = 1.9 \text{ pF},$$

Higher frequencies cause less $-I_x$ phase shift until the current appears resistive. At this point C_s defines total input capacitance:

If $C_s = 2.4$ pF and $-C_{in} = 1.9$ pF,

then:

$$C_{eff} \approx -C_{in} + C_s \approx -1.9 + 2.4$$

$$C_{eff} \approx 0.5 \text{ pF at low frequencies,}$$

and:

$$C_{eff} \approx C_s \approx 2.4 \text{ pF at high frequencies.}$$

The information given leads one to think that a designer should either increase grid-signal losses or make input capacitance flat over the input bandwidth. This is a fair approximation of compensation techniques: Grid-signal losses are introduced, or C_{eff} is made to appear constant at all frequencies, or the techniques are combined.

Two methods, shunt RC compensation and Miller-effect degeneration, prevent $-I_x$ flow in R_i. These methods thus maintain input capacitance constant.

R_cC_c the source for $-I_x$

Shunt RC compensation appears in the grid circuit. Fig. 3-36 includes compensation components shown as C_c and R_c. R_cC_c equal the predicted value of $-(R_{in}C_{in})$. When the "negative" components demand current, the compensating components demand equal-amplitude "positive" current. $-I_x$ then flows in a "positive" direction through R_cC_c to charge $-C_{in}$. None of the reactive current flows in R_i, therefore capacitive source loading, C_s, is flat.

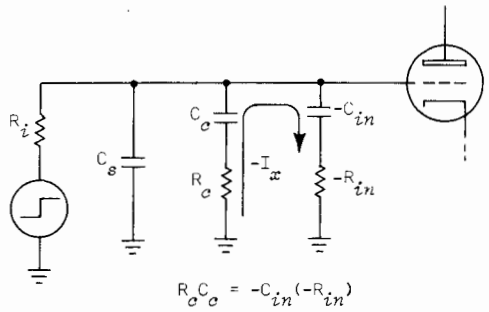


Fig. 3-36. Shunt RC compensation.

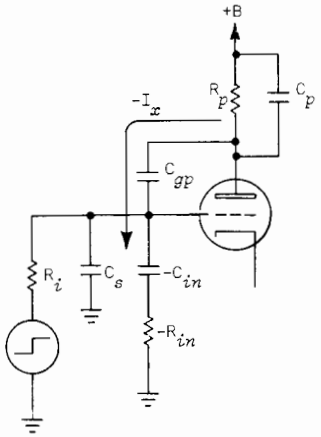


Fig. 3-37. Compensation using Miller effect.

Miller capacitance, the source for $-I_x$

Plate-compensation (Miller-effect) also contains $-I_x$ within the grid circuit, causing a constant input capacitance. Fig. 3-37 shows the plate circuit functioning as the source for $-I_x$. Here a signal, out-of-phase with the input, develops across R_p. A portion of this signal energy couples back through the Miller capacitance as $-I_x$. Again, no current flows in R_i so C_s can represent input capacitance to all signals.

Miller capacitance increases with A_V

C_{gp} is interelement capacitance which is supplemented in a few cases by an additional shunt capacitance. C_{gp} has a component value which changes with plate gain: If the plate were to do the impossible and follow input signals 1:1, no voltage difference would appear across C_{gp} and no current would flow. C_{gp} would be some infinitely small value. In earlier descriptions C_{gp} returned to signal ground, +B. Input signals across C_{gp} caused reactive current flow. Current quantity depended upon the component value of C_{gp} and the voltage across it. Imposing plate gain, as in Fig. 3-37, increases the voltage across C_{gp}, therefore the current quantity. To input circuitry, capacitance appears to increase with gain. One expresses shunt Miller capacitance by the formula: $C_m = C_{gp}\ (1 + A_V)$; if C_{gp} were 3 pF, and A_V were 10, then C_m would be 11. This is the concept used to compensate for "negative input characteristics."

plate gain creates feedback current

A change in cathode current causes a voltage change across R_p, which in turn creates feedback current from plate to grid. Plate risetime determines plate signal amplitude or A_V. For slow rise signals R_p sets gain. However, C_p shunts R_p during fast rise signals reducing gain toward zero. Feedback current and input capacitance decrease with risetime. This is in keeping with $-I_x$ demand.

feedback exponential

Initially the cathode waveform follows the input step. During this rapid change, C_p shunts R_p preventing plate gain thus feedback current. When the cathode begins to ascend exponentially, plate-current rate-of-change reduces, developing a plate signal across R_p. Plate-to-grid feedback now becomes $-I_x$. R_pC_p gain characteristics are exponential, as the cathode, providing feedback current that satisfies $-I_x$ demand. Here also, no reactive current flows in R_i so C_s represents a fixed input capacitance.

From a frequency standpoint C_p shunts R_p more at high frequencies than low. Gain decreases exponentially with frequency. C_m then increases low-frequency input capacitance, decreasing with frequency so that effective input capacitance will be flat at all frequencies.

suppressor resistors

Stray inductive components can resonate with changing input capacitance causing overshoot (ringing). A small suppressor resistor in series with the grid signal imposes losses. These resistors in values of 10 to 50 ohms damp the regenerative power.

None of the methods function perfectly and individual characteristics overlap. Therefore, one may expect to find individual or combined methods.

Generally one finds in slowest rise circuits a suppressor resistor, then in decreasing risetime order: plate compensation, plate compensation combined with a suppressor, shunt RC compensation and shunt RC combined with plate compensation.

"Negative-input-characteristics" compensation appears in many amplifier configurations whether the active device be electron tube or semiconductor Fast-rise input amplifiers always use compensation.

plate compensation

The circuit of Fig. 3-38 uses Miller-effect to compensate negative-input characteristics. A small voltage out-of-phase with the input signal develops across R5 at low frequencies. Capacitance, plate-to-grid, couples this degenerative signal to the control grid preventing oscillations. Shunting of R5 by C5 increases with frequency, reducing plate-signal amplitude. Quantity of feedback increases with plate-signal amplitude. Degeneration, thus, capacitance due to Miller-effect develops most at low frequencies, decreasing with an increase in frequency. The result is equal input capacitance at all frequencies. Or, negative current flows from plate to grid rather than through input circuit components.

suppressor resistor

Suppressor resistors, as R3 in Fig. 3-39, oppose current flow, minimizing the quantity of negative current. Suppressor resistors, used alone at the input amplifier, generally indicate narrower bandwidth than instruments employing plate compensation.

shunt RC compensation

Currently popular shunt RC compensation is shown in Fig. 3-40. C3 and R3 act as a current source for negative input components. The positive-current demand of R3C3 equals the negative-current demand of $-(R_{in}C_{in})$.

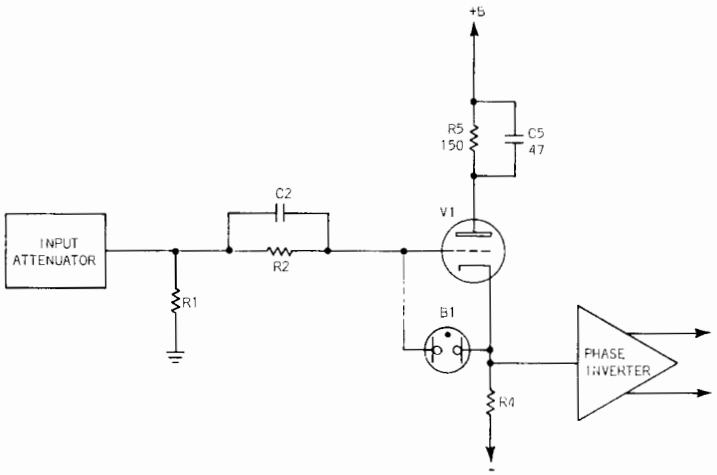


Fig. 3-38. Plate compensated input amplifier.

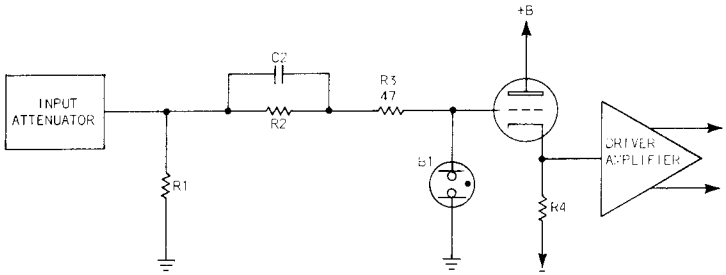


Fig. 3-39. Input amplifier with suppressor.

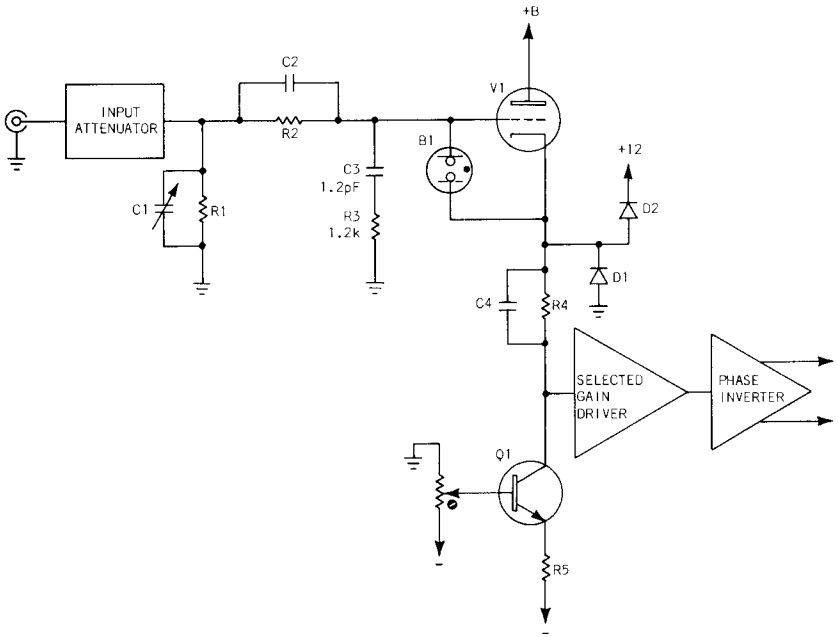


Fig. 3-40. Input-amplifier shunt RC compensated.

Fig. 3-40 incorporates many of the cathode-follower concepts presented:

C1 shunts grid resistor R1, providing input-voltage-divider compensation.

C2 bypasses grid-limiting resistor R2.

C3 and R3 compensate for negative-input characteristics.

Neon lamp B1 protects against grid-to-cathode overload.

Diodes D1 and D2 clamp to protect the input circuit of the selected-gain driver.

R4 is a dropping resistor. V1 self biases about 1.5-volts positive. Cathode current through R4 allows one to adjust the voltage at the collector of Q1.

Q1 dynamically longtails V1. One adjusts base bias for near zero volts to the selected-gain driver.

Fig. 3-40 is the basic circuit of a switched-gain input amplifier. Chapter 2 pointed out how input deflection factor was extended by two methods: "Stacking" attenuators or, to reduce input capacitance, gain switching amplifiers in calibrated steps.

switched-gain block

Fig. 3-41 is a block diagram of switching logic necessary to drive a phase inverter at a constant deflection factor. Blocks labeled Input Attenuator, Input CF and Selected-Gain Driver mechanically gang to the VOLTS/DIV selector. Deflection factor, at the input jack, is from 20 millivolts to 10 volts per division selected in a 1-2-5 sequence. The input dividers reduce the nine input-deflection factors to three: 20 millivolts, 50 millivolts and 100 millivolts. Selecting cathode-follower gain of 1 or 1/5 gives an input-deflection factor to the selected-gain driver of 20 or 50 millivolts per division. The selected-gain driver can now have a constant output-deflection factor. The circuit concepts of interest are those of the input cathode follower.

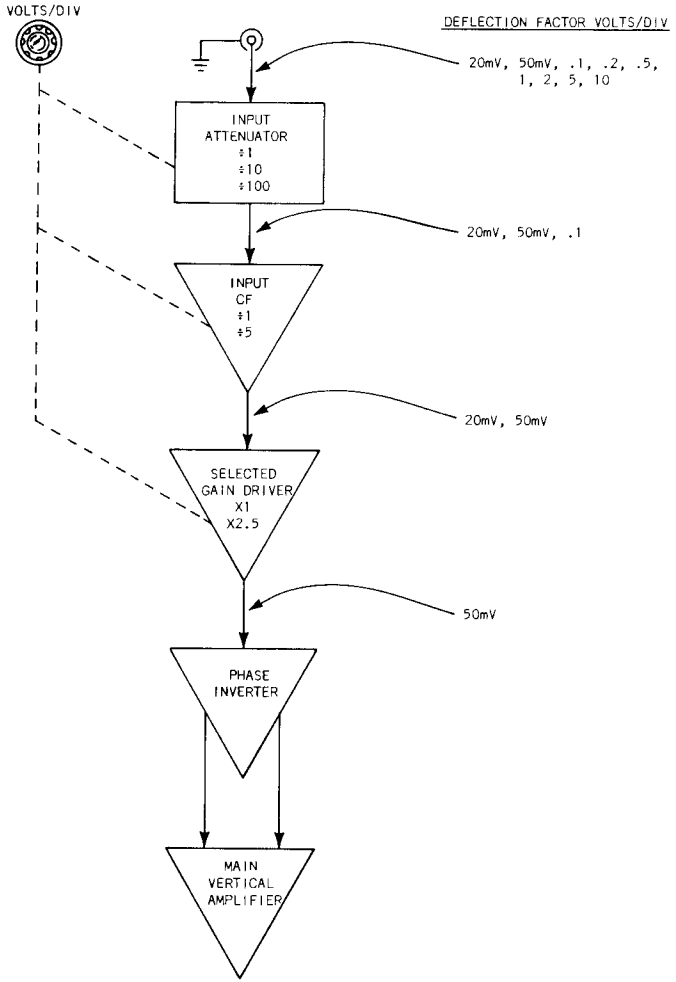


Fig. 3-41. Switched-gain amplifier.

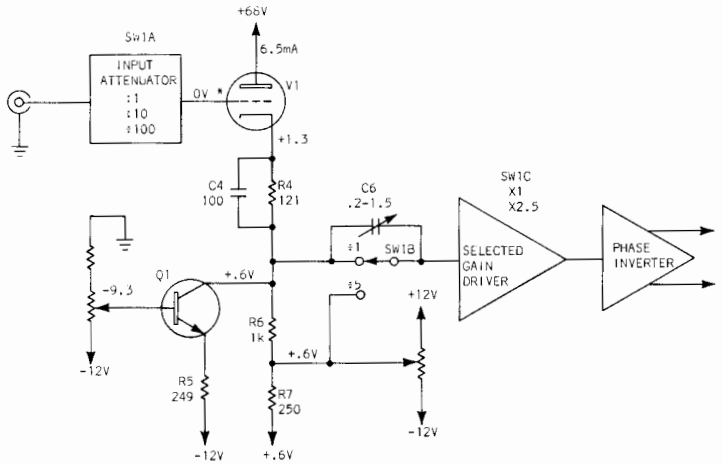


Fig. 3-42. ÷1, ÷5 input-amplifier cathode circuitry.

Assuming unity gain, deflection factor at Q1's collector equals the factor at V1's grid.* (Fig. 3-42).

CF output either 20 or 50 mV/div

Signal voltage at the top of R6 or R7 drives the selected-gain driver. With SW1B positioned as shown, a deflection factor of 20 mV or 50 mV exists at the collector of Q1. Selecting 100 mV/div at Q1's collector places SW1B in the down or ÷5 position. Since R6 and R7 is a 5:1 divider, drive to the selected-gain driver is 20 mV/div. Deflection factor out of the input cathode follower is either 20 or 50 millivolts.

*Unity gain provides convenient figures. A more realistic figure, considering actual CF gain and drop across R4, is 80% of V1 grid signal (A_V = 0.8 at collector Q1).

compensated voltage divider

C6 makes R6-R7 a compensated voltage divider. Distributed capacity shunts Q1 and R7. With SW1B positioned as shown, no additional capacitor is necessary -- C6 is shorted. With SW1B in the down or ÷5 position, C6 shunts R6 requiring an adjustment for proper capacitive voltage division.

setting quiescent voltages

No quiescent voltage difference should exist between the ÷1 and ÷5 positions of SW1B. With the input jack grounded, one switches the VOLTS/DIV selector through its range and should observe no vertical CRT deflection. If a quiescent voltage appears across R6, switching from ÷1 to ÷5 appears as a signal to the following stages. Amplified, it vertically deflects the CRT trace.

The quiescent levels result from V1 self-bias resistive values, and adjustable longtailing. V1 self-bias determines the voltage at the top of R4. Q1, controlling total cathode current, sets the voltage drop across R4. Q1 base-voltage adjustment sets the collector level to the proper operating point for following direct-coupled stages. Returning the junction of R6-R7 to a variable voltage allows one to adjust for no-voltage difference across R6. voltage return for R7 approximates Q1 nominal collector level. At quiescence, with voltage levels adjusted, no discernible deflection results from actuating SW1B.

compensated voltage divider

C4 compensates R4. One must consider R4 as part of the resistive network across which an input signal develops. The capacitance across R4 compensates as in the other voltage-divider networks already discussed.

For a complete input amplifier, combine the components of Fig. 3-40 and 3-42.

Fig. 3-43 depicts the input stage of a broadband vertical preamplifier. A low-resistance network shunts the cathode resistor which reduces gain to 50%.

grid circuit

Begin circuit analysis with the grid circuit. Grid resistors R1 returns to an adjustable negative-voltage supply, consisting of R8, R9, R10 and the -15 volt supply. One adjusts R10 for a voltage equal to the drop across R1 which results from negative grid current (current created when the heated control grid emits electrons).

Grid limiting develops across R2. C2 bypasses R2, rapidly charging input tube capacitance.

negative R

R11, R12 and C12 compensate for negative-resistance input characteristics. R11 is a suppressor. Plate signals across R12 develop Miller-effect. C12 bypasses R12 to reduce degenerative feedback at high frequencies.

protection

B1 and D1 are protective devices. B1 ignites during signal overloads and D1 clamps negative excursions at about 0.2 volts below ground.

controls

Location of controls VARIABLE VOLTS/DIV (R6) and Gain (R5) in the cathode circuit of V1 complicates

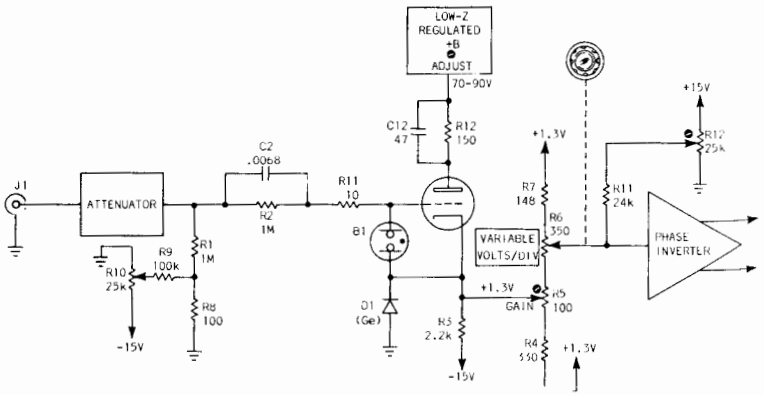


Fig. 3-43. Constant output impedance CF.

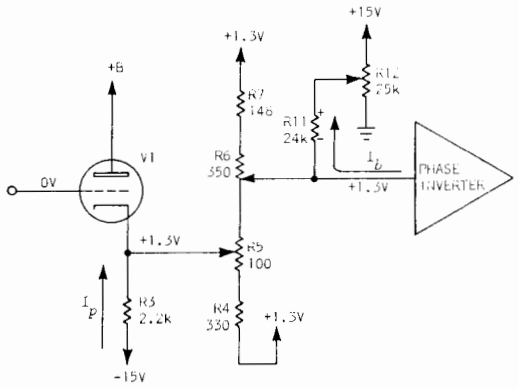


Fig. 3-44. Constant output Z CF, simplified.

this amplifier. These controls usually appear in one or more later amplifier stages, frequently the phase inverter. In this case, placing Gain and VARIABLE controls at the input amplifier improves overall vertical response.

R6 extends to the front panel providing the operator a continuously variable uncalibrated between-step deflection-factor control. Adjusting R5 Gain calibrates. One adjusts R5 with R6 set to the least resistance between the wiper of R6 and the connection with R5. (The lower extreme as shown in Fig. 3-43). For the variable (R6) to be most useful, no vertical deflection should occur when one moves R6 through its range.

no quiescent current flows in VARIABLE or Gain

Preventing quiescent current flow through resistive network R4, R5, R6 and R7 allows one to use the VARIABLE without deflecting the vertical display. When a current flows through R6, moving the wiper of R6 creates a voltage change at the phase-inverter input. Following stages amplify this voltage change, vertically deflecting the CRT. V1 plate supply, R4 return, R7 return and adjustment R12 set circuit conditions for zero current through network R4, R5, R6 and R7. Under no signal condition, one then varies R5 or R6 without causing vertical deflection.

Refer to Fig. 3-44, a simplification of Fig. 3-43. Applying equal voltage to the four terminals prevents

quiescent current flow through R4, R5, R6 and R7: Both R4 and R7 return to +1.3 volts. Wipers of R5 and R6 rest at 1.3 volts. Zero current is then demanded.

R4 and R7 return to a fixed supply. Self-bias of V1 sets R5 wiper potential. By adjusting V1 plate return, one changes V1 tube parameters forcing a self-bias equal to the return voltage for R4 and R7.

Current originating in the phase inverter develops a voltage across R11 and R12. This causes the same potential to appear at the wiper of R6 as at other terminals. Setting the wiper of R12 more than 1.3-volts positive demands all phase-inverter current flow through R11 and R12 rather than R4, R5, R6 and R7. R11 and R12 are high resistances to prevent signal shunting.

External cathode resistance remains constant at all settings of R5 and R6. Total plate current flows through R3 under no-signal conditions. R3 functions as a longtail. However, signal voltages cause currents to flow through all cathode-circuit resistors.

$R_k \approx 200\ \Omega$

These shunt currents create a total R_k of approximately 200 ohms. Signal voltages develop across a divider consisting of r_k and R_k. Wideband stability depends upon this ratio remaining constant. The circuit configuration shown maintains R_k constant at all settings of Gain and VARIABLE controls.

100% of the CF signal develops at the wiper of R5. R5 setting establishes signal percentage across R6 and R7. Because of resistors R11 and R12, varying R6 affects no shunting. R5 is not so obvious. Set for maximum gain, the wiper of R5 rests at the R5 to R6 connection: R4 and R5, paralleled by R6 and R7, shunt R3. At nominal gain R5 is centered: One-half R5 appears in each parallel leg shunting R3. Minimum-gain setting causes R5, R6 and R7, paralleled by R4, to shunt R3. Total R_k does approximate 200 ohms over the total range of R5.

Fig. 3-45 develops equivalent circuit cathode resistance. Assume r_k is 200 ohms. Fig. 3-45A shows the desired equivalent circuit: Input signals, modified by μ, develop across divider R_k and r_k.

R_k 208 Ω at maximum gain

Fig. 3-45B solves for maximum gain R_k: Resistive network R4, R5, R6 and R7 is an equivalent shunt resistance of 230 ohms which parallels R3. R_k

R_k 204 Ω at mid gain — resolves to 208 ohms. Nominal gain results in 204 ohms R_k (Fig. 3-45C). Lowest resistance R_k occurs at minimum gain: R_k = 196 ohms (Fig. 3-45D).

R_k 196 Ω at low gain — Referred to nominal gain, R_k varies from 2% at maximum gain to 4% set at minimum.

small input R to the phase inverter varies — This CF circuit presents a low resistance to the phase inverter, as is required. The phase-inverter input resistance does, however, change with Gain and VARIABLE adjustments.

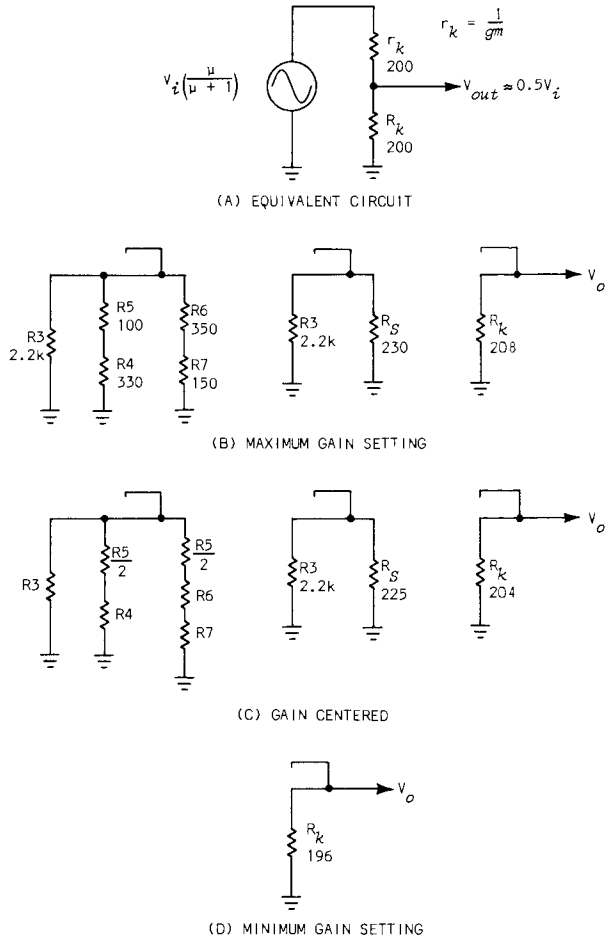


Fig. 3-45. Equivalizing cathode resistance.

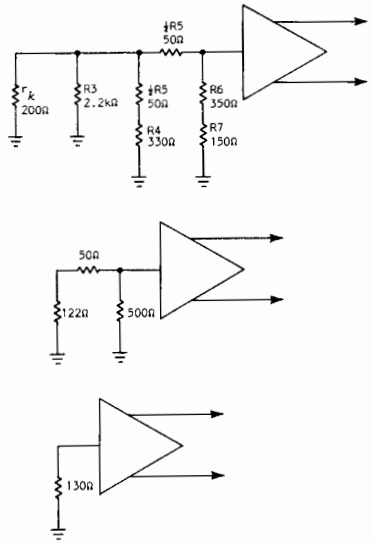


Fig. 3-46. Nominal-gain phase-inverter input resistance.

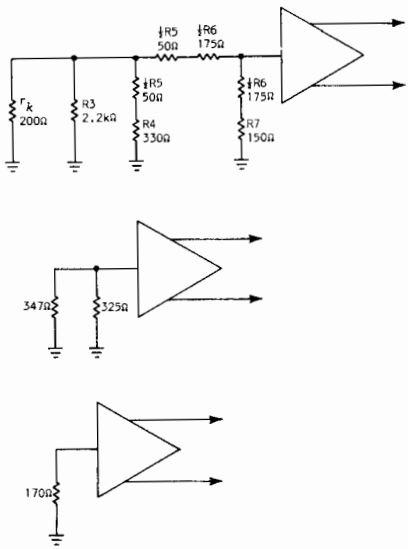


Fig. 3-47. Phase-inverter input resistance, variable centered.

gain changes input R

Fig. 3-46 shows input resistance as 130 ohms, with R6 in calibrated position and R5 centered. Input resistance changes with gain settings from a minimum of 100 ohms to a maximum of 150 ohms. 100 ohms represents high gain; 150 low gain.

VARIABLE changes input R

Assume nominal gain. Actuating the VARIABLE increases then decreases phase-inverter input resistance. Input resistance varies from 130 ohms through 170 ohms to 120 ohms. 170 ohms occurs with the VARIABLE centered (Fig. 3-47).

Many of the cathode-follower concepts are not peculiar to tube-type circuitry. Source or emitter followers exhibit similar characteristics modified by active-device peculiarities.

Emitter follower (EF) symbols and terms are those common to all followers: high input impedance, low output impedance, minimized Miller-effect capacitance, and longtailing to stabilize and emphasize all characteristics. Differences, however, exist.

Input Z lower than CF or SF

Terms such as *low* and *high* can be misleading when they refer to impedance values. Impedances of an emitter follower when compared to source followers or cathode followers are of a different magnitude, much lower. For example, the input impedance of an EF is high compared only to other transistor configurations. Input impedance is neither high enough nor stable enough to meet input-amplifier requirements. The loading on an input-attenuator network would be too great. Cathode followers and source followers are for this reason the only followers used as preamplifier input amplifiers. Emitter followers may be used in all other circuits of a vertical amplifier.

EF never used as input amplifier

the tube and FET are *on* devices

transistor is an *off* device

Another difference appears during basic operating considerations. The electron tube and some field-effect transistors (FET) are normally *on* devices while a transistor is normally *off*. That is, with zero bias, plate or drain current flows. However, a transistor turns *off* with zero bias applied.

	FORWARD-BIASED JUNCTION			V_{CE} (SAT)
	ACTIVE	CUT-IN/CUT-OFF	SAT	
Si	0.6	0.5	0.6	0.2
Ge	0.2	0.1	0.2	0.1

Fig. 3-48. Semiconductor operating voltages.

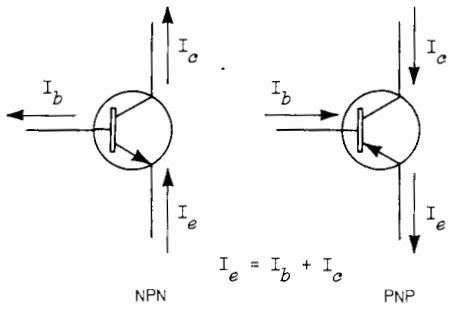


Fig. 3-49. Transistor current (electron) flow.

Consider the transistor as a device in one of three states: on, off, or saturated. Fig. 3-48 lists the active bias conditions assumed in this book for either silicon or germanium transistors. These are not absolute values but satisfy circuit analysis approximations.

forward bias

Applying forward bias to a transistor, 0.6 V for silicon (Si) or 0.2 V for germanium (Ge), causes emitter current flow. Fig. 3-49 indicates current distribution. Emitter current (I_e) flows into the NPN transistor and divides, forming base current (I_b) and collector current (I_c), which flow in the external circuits. I_b and I_c flow into the PNP transistor and combine to form I_e. In either type transistor a percentage of I_e flows in the base circuit, establishing the input impedance of an emitter follower: I_b increases with I_e.

alpha
beta

The percentage of I_e flowing in the base and collector circuits sets two transistor parameters, alpha (α) and beta (β). $\alpha \approx \frac{I_c}{I_e}$ and $\beta \approx \frac{I_c}{I_b}$. Since

terms are common, $\alpha = \frac{\beta}{1 + \beta}$ and $\beta = \frac{\alpha}{1 - \alpha}$. One sometimes sees α represented by h parameter, h_{fb}, and β by h_{fe}. This book will not use h parameters.

β indicates relative input Z

α and β tell a great deal about a transistor. A low β indicates a relatively large quantity of base-current flow. Stated differently, a low β indicates a relatively low input impedance. Since I_b is a percentage of I_e then the I_b quantity depends upon I_e quantity. This implies emitter impedance affects base input impedance. It does. $R_{in} = \beta R_E$ where R_E is total emitter impedance. Conversely, external circuits which impede I_b reflect into the emitter circuit $\frac{1}{\beta}$ times: 100-ohm base circuit load appears in the emitter as $\frac{100}{\beta}$ ohms.

α fairly constant

α remains a fairly constant parameter while β may change significantly. A large dynamic emitter current can cause α to change a few percent, but if α changes slightly β varies drastically: Assume 10-mA emitter-current change causes α to drop from 0.98 to 0.96. The difference between 9.8-mA and 9.6-mA I_c might go unnoticed. However, β changed from 49 to 28!

Initially: $\beta = \frac{\alpha}{1 - \alpha}$

$\beta = \frac{0.98}{1 - 0.98} = \frac{0.98}{0.02}$

$\beta = 49$

Changed to: $\beta = \frac{\alpha}{1 - \alpha}$

$\beta = \frac{0.96}{1 - 0.96} = \frac{0.96}{0.04}$

$\beta = 28$

β is only one factor determining output impedance (R_o) of an emitter follower. Additional terms used are:

R_b, base spreading resistance;

R_r, reflected base resistance;

r_e, dynamic emitter resistance;

R_t, transresistance resistance; and

R_E, external emitter resistance.

base spreading resistance

Base spreading resistance (R_b) exists in the transistor as a result of the manufacturing process. This resistance is a physical component which opposes the flow of base current. It takes a value between 1 Ω and 1 kΩ depending upon transistor type. Assuming 250 Ω gives a fair low-frequency approximation. I_b flows through R_b as a series component.

reflected resistance

I_b represents only a portion of I_e, therefore only a portion of R_b opposes emitter current. The value of reflected resistance (R_r) is the quotient of R_b and β: $R_r = \frac{R_b}{\beta}$. If β were 50 and R_b were 250 Ω, $R_r = \frac{R_b}{\beta} = \frac{250}{50} = 5$.

estimated R_r

One seldom knows the value of R_b. For purposes of circuit analysis, assume between zero Ω and 10 Ω as the value of $\frac{R_b}{\beta}$

dynamic emitter resistance

Fig. 3-50 shows base spreading resistance as viewed from the base level. Viewed from the emitter this resistance appears as R_r as shown in Fig. 3-51. Dynamic emitter resistance (r_e) also appears as the remaining series portion of transresistance resistance (R_t).

Dynamic emitter resistance is *gm*-determined, as internal cathode impedance. However, a formula one should commit to memory makes r_e approximations simple: $r_e = \frac{26 \times 10^{-3}}{I_e}$, where I_e is emitter current. This formula, which applies to all transistors used as linear amplifiers, is derived from the general equation for current through a PN diode junction:

$$I = I_s \left(e^{\frac{V}{kT/q}} - 1 \right).$$

Where:

I = Quiescent or net diode current

I_s = Saturation current

e = Natural log base

V = Applied forward voltage

k = Bolzmann's constant = 1.38×10^{-16} erg/K

T = Absolute temperature, K

q = Electron charge = 1.602×10^{-19} coulomb

If V exceeds kT/q by 5, the equation simplifies to:

$$I \approx I_s \frac{V}{e^{kT/q}}$$

(kT/q at room temperature is 26 mV).

Substituting the simplified formula into the forward-conductance formula yields r_e. Differentiating the original current equation for small increments of dynamic conductance results in conductance gm.

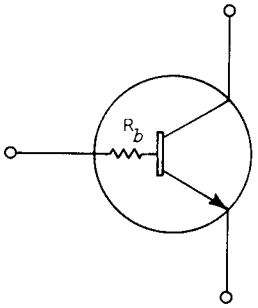


Fig. 3-50. Base spreading resistance.

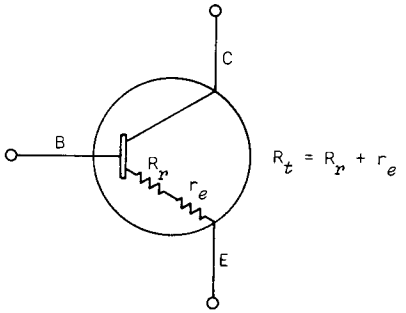


Fig. 3-51. Transresistance (R_t) components.

$$\frac{\Delta I}{\Delta V} \approx \frac{dI}{dV} = \frac{I_s \frac{V}{kT/q}}{e^{kT/q}} = gm = \frac{1}{r_e}$$

Now substituting:

$$gm = \frac{I}{kT/q}$$

$$r_e = \frac{kT/q}{I}$$

Since kT/q at room temperature is 26 mV,

$$r_e \approx \frac{26 \times 10^{-3}}{I_e}$$

All of which shows that R_t is predictable and small, developing for emitter followers high gain and low output impedance. To demonstrate this, assume $\beta = 50$, $R_b = 250\ \Omega$, and $I_e = 1$ mA.

$$R_t = R_r + r_e = \frac{R_b}{\beta} + \frac{26 \times 10^{-3}}{I_e}$$

$$R_t = \frac{250}{50} + \frac{26}{1} = 5 + 26 \approx 30\ \Omega.$$

R_t appears in series with external emitter resistance (R_E) for signal development, and in parallel with R_E to present output impedance. Fig. 3-52 shows the emitter-follower basic circuit, equivalent circuit, and formulas. Gain times the base signal develops across R_E. Gain depends upon the resistance of R_E and R_t. When R_E exceeds R_t by 10 or more, gain approaches unity and R_t expresses output impedance. Further, R_t decreases with an increase in emitter current, indicating an advantage to longtailing.

longtailed emitter follower

Fig. 3-53 shows an NPN silicon transistor connected as a longtailed emitter follower. The collector returns to positive 10 volts and the base to ground. The emitter circuit contains turn-on voltage for the device. 39.4 volts across R_E demands approximately 4-mA emitter current. This is all the information needed for analysis:

$$A_V = \frac{V_{in}}{V_o} = \frac{R_E}{R_E + R_t}$$

$$R_O = \frac{R_E R_t}{R_E + R_t}$$

$$R_t = R_r + r_e$$

$$r_e = \frac{26 \times 10^{-3}}{4 \times 10^{-3}} = 6.5\ \Omega$$

Arbitrarily add 3.5 Ω for R_r to round R_t to 10 Ω.

In this case $A_V \approx 1$ and $R_O \approx R_t = 10\ \Omega$. I_e is high enough and R_E large enough for unity gain and low output impedance. Assuming R_r low is justified since the base driving circuits are unknown.

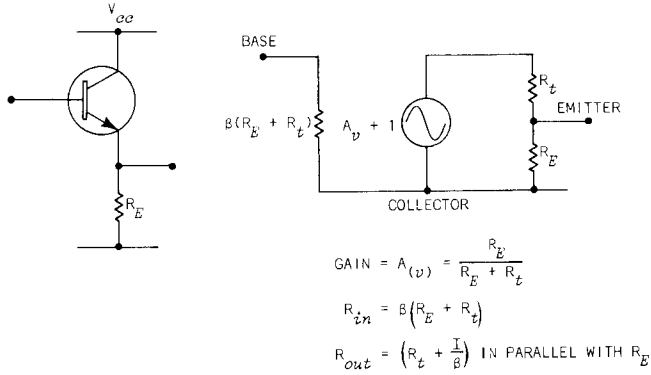


Fig. 3-52. Common collector.

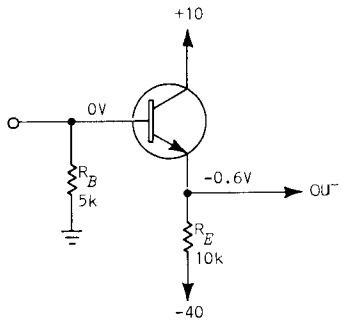


Fig. 3-53. Longtailed EF.

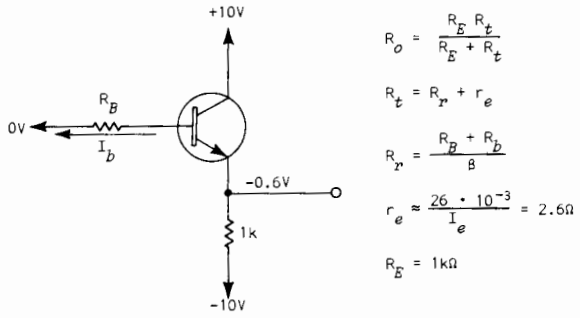


Fig. 3-54. Input components appear in the emitter output.

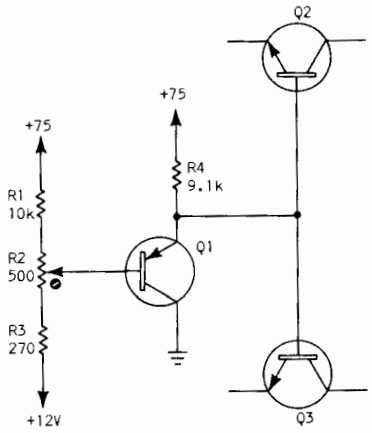


Fig. 3-55. Emitter follower providing low-impedance base supply.

input source impedance affects output impedance

Source impedance of base driving circuits can be important since this opposition to base current appears in series with R_b. Therefore, source impedance added to R_b and divided by β constitutes R_r at the emitter. Should this raise R_t appreciably, both gain and output impedance are affected.

Fig. 3-54 shows an emitter follower with equivalent source impedance included in the base lead. About 9-mA I_e flows, resulting in less than 3-Ω r_e. R_t

now depends upon β and R_B. R_o and possibly gain will be a result of these factors. Assign β a value of 50. If R_B were 100 Ω, then R_r would increase by 2 Ω. This is hardly enough to worry about. One could safely assume an R_t between 5 and 10 Ω. However, were R_B 1 kΩ, R_t then appears as about 25 Ω. Gain is about 0.98 and R_o has increased appreciably.

determining emitter-follower action

To show how one determines emitter-follower action in an operating circuit, consider Fig. 3-55. Emitter follower Q1 functions as low-impedance voltage source, providing base voltage for grounded-base amplifiers Q2 and Q3. This circuit also provides thermal compensation.

impedance transformer

Q2 and Q3 as grounded-base amplifiers require a low-impedance base supply voltage. In this case they also require an adjustable return. Q1 reduces the value of voltage divider R1, R2 and R3 by β, keeping the initial R_B of Q2 and Q3 low and preventing large R_B variations during adjustment of base voltage.

temperature compensation

Temperature compensation results from all transistors being silicon and mounted near one another. Since the transistors share thermal environment, they experience equal base-emitter voltage changes. However, Q1 is a PNP transistor. Should I_e increase due to temperature, Q1 emitter voltage drops, decreasing the forward bias on Q2 and Q3 which counteracts temperature-induced current demand in Q1 and Q3.

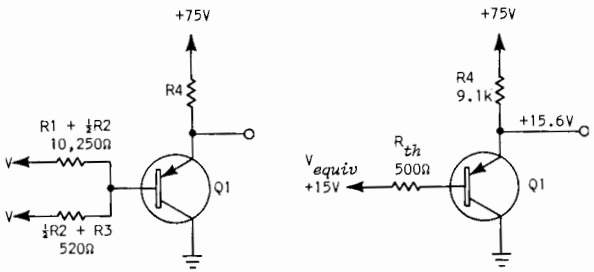
Q1 base circuit

One analyzes the circuit of Fig. 3-55 by first "Thevenizing" the base circuit of Q1. This gives an equivalent resistance returned to an equivalent voltage. The equivalent voltage is base voltage which, raised one diode junction (0.6 V for silicon), is Q1 emitter voltage. Q2 and Q3 base voltage is Q1 emitter voltage. And dropping this voltage one junction resolves Q2-Q3 emitter voltage. In other words, Q1 base voltage and Q2 or Q3 emitter voltage are equal.

Assuming R2 set to midrange, one breaks voltage divider R1, R2 and R3 as shown in Fig. 3-56: The base connects to the junction of a 10.25 kΩ and a 520 Ω resistor. Voltage at the resistive junction and the shunt value of the resistances give the Thevenin equivalent circuit. R_{th} is 500 Ω returned to +15 equivalent volts. Add 0.6 V to assign emitter voltage.

Now that the drop across R4 is known, solve for I_e and r_e. R_r consists of R_B and R_b divided by β. In this case R_{th} is R_B. Use a conservative β, say 50, and R_r is 16. The value R_b/β is arbitrary. Any value between 1 Ω and 10 Ω may be used. 6 is chosen merely to give an even power of ten to the sum: $R_r + r_e$.

R_o is R_t. One might think the shunting of R4 should be considered. Don't waste the time! R4, 470 times larger than R_t, changes output resistance less than the R_r approximation error.



$$I_e = \frac{59.4V}{9.1 \cdot 10^3} = 6.65mA$$

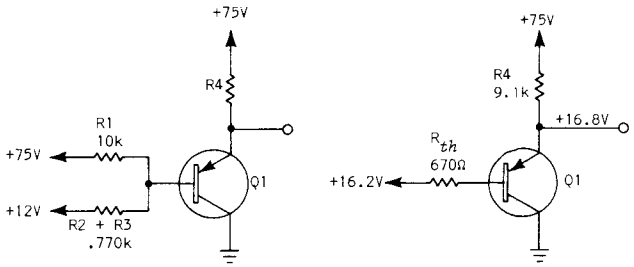
$$r_e = \frac{26 \cdot 10^{-3}}{6.65 \cdot 10^{-3}} \approx 4\Omega$$

$$\frac{R_{th}}{\beta} \approx 10\Omega$$

$$\frac{R_b}{\beta} \approx 6\Omega$$

$$R_t = 4 + 6 + 10 = 20\Omega = R_o$$

Fig. 3-56. Circuit equivalent with R2 centered.



$$I_e = \frac{59.2}{9.1 \cdot 10^3} = 6.65\text{mA}$$

$$r_e = \frac{26 \cdot 10^{-3}}{6.65 \cdot 10^{-3}} \approx 4\Omega$$

$$\frac{R_{th}}{\beta} = 13.4\Omega$$

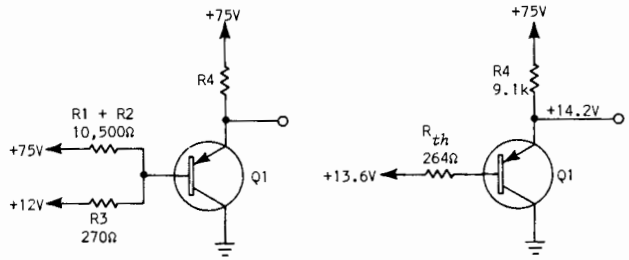
$$\frac{R_b}{\beta} = 6\Omega$$

$$R_t = 6\Omega + 13.4\Omega + 4\Omega = 23.4\Omega = R_o$$

Fig. 3-57. Circuit equivalent with R2 set to maximum.

maximum positive

For consistency, hold reflected base spreading resistance at 6 Ω for all settings of R2, and β at 50. Fig. 3-57 represents the equivalent circuit for maximum positive V_{BB}. R_{th} and the equivalent voltage to which it returns are larger values. Longtailing holds I_e and, therefore, r_e fairly constant. R_{th} (R_B) reflects a few additional ohms into the emitter, representing the increase in R_o over the midsetting of R2.



$$I_e = \frac{60.8}{9.1 \cdot 10^3} = 6.7\text{mA}$$

$$r_e = \frac{26 \cdot 10^{-3}}{6.7 \cdot 10^{-3}} \approx 4\Omega$$

$$\frac{R_{th}}{\beta} = 5.3\Omega$$

$$\frac{R_b}{\beta} = 6\Omega$$

$$R_t = 6\Omega + 5.3\Omega + 4\Omega = 15.3\Omega = R_o$$

Fig. 3-58. Circuit equivalent with R2 set to minimum.

minimum positive

Continuing the reasoning, Fig. 3-58 shows the circuit with R2 set to minimum. Here again, because of longtailing, R_B determines the change in R_o.

R_o also represents R_B for Q2 and Q3. Keeping R_B small is a basic requirement for grounded-base amplifiers. Fig. 3-59 includes a formula which indicates R_B should be large. This is true if one ignores wanted signal degeneration. Temperature increases cause a decrease in emitter-to-base voltage -- an increase in forward bias. I_e, thus I_b, increases until the drop across R_B raises V_{EB} to the nominal bias level. Unfortunately, wanted signals suffer the same degeneration as thermal noise. This is the reason for the PNP-to-NPN configuration shown in Fig. 3-60.

Temperature increases cause V_{EB} of Q2 and Q3 to decrease, perhaps 2.5 mV/°C, which increases emitter-current demand. A signal is born! But, Q1 V_{EB} also decreases and the increased emitter current through R4 develops a more negative base voltage for Q2 and

Q3. Q2 and Q3 emitter currents return to quiescence. Desirable signals are not coupled into the feedback loop, therefore suffer no degeneration.

signal amplifier

Emitter followers also perform as impedance transformers in signal paths. This occurs in oscilloscope preamplifiers where the input amplifier is a cathode follower. Cathode followers have the required high input impedance and a relatively low

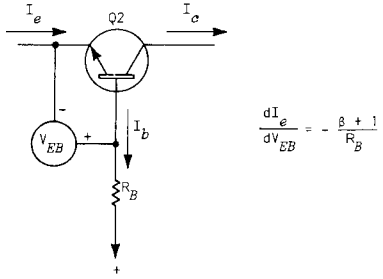


Fig. 3-59. A large R_B minimizes I_e changes, due to V_{EB} variations.

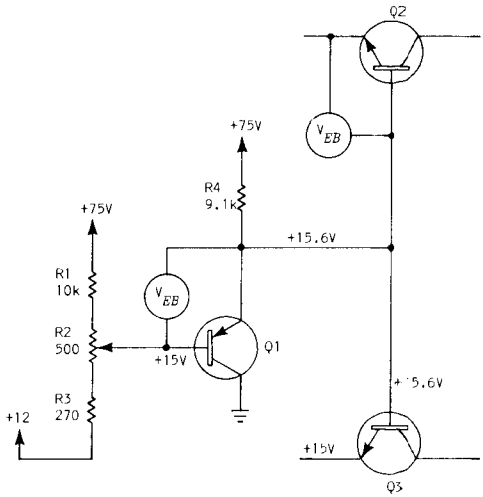


Fig. 3-60. Providing the thermal compensating effects with an emitter follower.

vacuum tube *gm* decreases with age

output impedance. Unfortunately a vacuum tube changes parameters during aging. Transconductance decreases at an unpredictable rate, increasing cathode follower output impedance. The increase in r_k could negligibly decrease CF gain and yet seriously decrease overall gain of a following transistor amplifier.

changing r_k changes R_t

In Fig. 3-61A the common-emitter amplifier receives V_{in} via the CF. $\frac{V_o}{V_{in}}$ defines stage gain. With certain values a selected collector load resistance gives the gain desired. CF longtailed, gm = 5000 μmho, β = 50, and $\frac{R_b}{\beta} + r_e = 6\ \Omega$. Low-frequency gain remains at the desired level only so long as gm (r_k) remains constant. This is because r_k reflects into the emitter circuit, imposing degeneration as an unbypassed emitter resistor.

Refer to Fig. 3-61B. The CF voltage source applies base voltages through its internal impedance. R_B ($1/gm$) reflects into the emitter as a portion of R_t. R_t in this case constitutes total emitter degeneration of 10 Ω. During the operating life of the tube transconductance decreases. The longtailed CF appears a fairly constant voltage source whose internal impedance increases with age. After many operating hours, perhaps 1000 to 2000, r_k increases 5 or so times. The circuit then changes to that shown in Fig. 3-61C. R_t increases 2-1/2 times, reducing gain accordingly.

Using emitter-follower coupling (Fig. 3-62) affects β multiplication: Cathode follower r_k changes 500%, R_o of the emitter follower changes 300%, however, R_t of the common-emitter amplifier changes but 1 Ω. And R_t values before and after aging are less than without the EF.

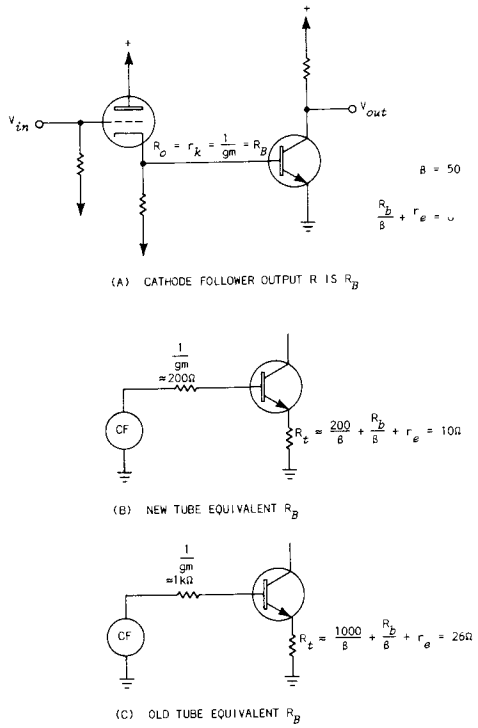


Fig. 3-61. Tube parameters increase R_B after many operating hours.

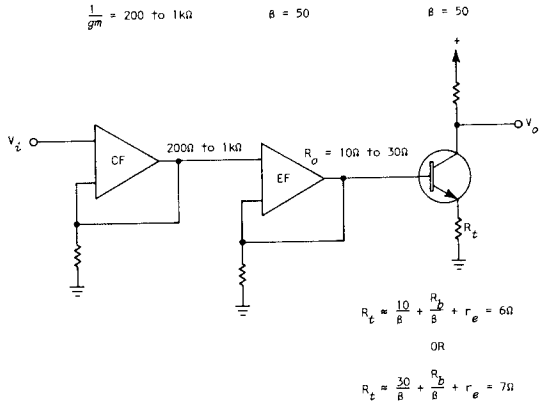


Fig. 3-62. EF coupling reduces common-emitter input impedance.

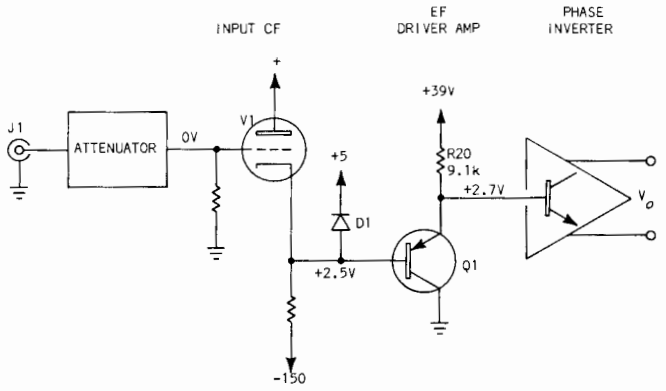


Fig. 3-63. An emitter follower used to reduce impedance and as a negative clamp.

Fig. 3-63 depicts an emitter follower used as described. Q1 also functions as a negative clamp.

V1, a longtailed cathode follower, applies input signals slightly attenuated to the base of Q1. Longtailed emitter follower Q1 functions as a very low-impedance signal source driving the phase inverter.

V1 self-bias, 2.5 volts, appears at the anode of D1 and base of Q1. Both are germanium. D1 clamps to prevent excessive positive excursions and Q1 clamps during excessive negative excursions. Cathode excursions which exceed +5 V turn D1 on. D1 then clamps the output at +5.2 volts to prevent reverse breakdown of Q1.

Reverse breakdown is not necessarily harmful. Drawing small current just puts the device in another mode of operation. However, most vertical circuits like the input cathode follower draw large current quantities. This increases the power dissipated by the junction beyond tolerable limits. Thus the clamp, which prevents reverse-breakdown.

Q1 conducts, collector-to-base, as a diode when base voltage drops 0.2 volts below ground. This most often happens during tube substitution. Removing V1 causes -150 volts to appear at the base of Q1. Q1 base-collector diode turns on, dropping

the voltage across the CF longtail resistance.

Q1 clamping — The Q1 clamp protects the phase inverter, an NPN, from reverse breakdown.

Interchassis connections create capacitance. Emitter followers are therefore frequently used as preamplifier output amplifiers. The push-pull amplifier of Fig. 3-64 drives the main vertical amplifier as a low-impedance source. Emitter current through R1 and R2 longtail Q1 and Q2.

balance — R3 and C1 carry the name High-Frequency Balance. Without R3 and C1, Q1 and Q2 operate as independent amplifiers. This is fine if both the input and output signals are truly push-pull. An unequal reactive load on either base or emitter lead, or for that matter in any stage from the phase-inverter to the CRT, causes an unequal phase shift. Cross coupling R3 and C1 balances the phase shift. One adjusts R3-C1 for minimum necessary phase shift -- for best CRT step-function display.

negative input resistance characteristics — Emitter followers experience "negative-input-resistance characteristics." The conceptual effects of capacitances, impedances and transconductance are as explained for cathode followers. The same compensation concepts apply: suppressor resistor, shunt RC, and "Miller-effect" -- degenerative feedback from collector to base in a transistor.

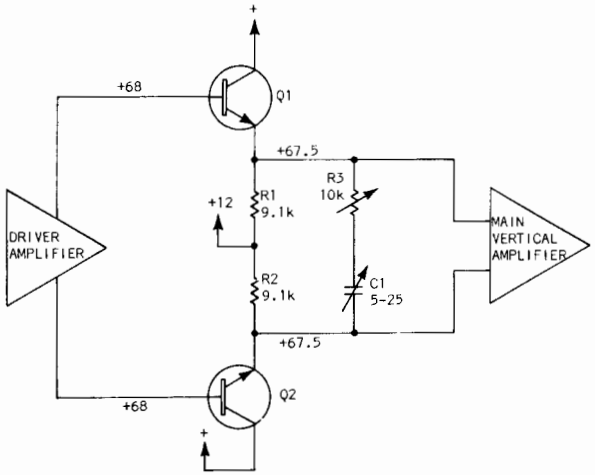


Fig. 3-64. Push-pull emitter followers.

step response

Longtailed emitter followers follow positive and negative steps at different rates. Cathode followers react more faithfully to positive voltage transitions than negative transitions. And this becomes more pronounced with longtailing. Emitter followers have similar reactions except the direction of current flow, thus reaction to positive and negative steps, depends upon transistor type.

NPN emitter followers, like cathode followers, follow positive step functions more faithfully than negative. PNP emitter followers react in opposite manner, reproducing negative step functions more faithfully than the positive step.

Capacitance charge time generally restricts the step response of any amplifier. Fig. 3-65 includes a simplified NPN emitter follower. The input signal consists of a positive step function followed sometime later by a negative step function. Refer to the positive transition as risetime (t_r) and the negative transition as falltime (t_f). Output t_r appears equal to the input. Output t_f, however, considerably exceeds input t_f. The output waveform effectively graphs C_O charge rate. This is determined by components C_O, R_E and R_t.

C_O represents total output capacitance which includes EF open-circuit output C, lead C, connector C and following-stage input C. R_E is the total external emitter-load resistance. R_t remains the active device transresistance.

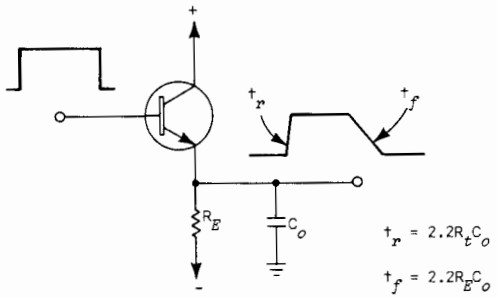


Fig. 3-65. NPN emitter followers react faster to rising steps than to falling steps.

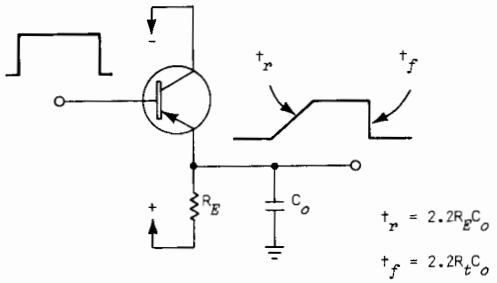


Fig. 3-66. PNP emitter followers react faster to falling steps than rising.

t_r = 2.2 RC defines response. C in the formula is C_O for positive or negative step response. R changes: For positive steps put the value of R_t in the formula while R_E is the value for negative step response.

C_O is not large, probably between 8 and 20 pF. During t_r charging current flows as emitter current. Only R_t limits charging current quantity. NPN emitter followers then increase risetime very little.

Current flows *into* the emitter of NPN transistors. Emitter current cannot contribute to the charge of C_O during t_f. C_O charges by drawing current from the negative supply through R_E. R_E, always a much larger resistance than R_t, accounts for the difference between t_r and t_f.

Longtailing establishes t_f. The total current available sets the charge rate of C_O. During t_f (NPN) the maximum current is that provided by the longtail. Circuit falltime will probably be linear (ramp-like) but longer than risetime.

C_O charging rate also determines PNP step response (Fig. 3-66). However, emitter current flows *out* of the PNP causing opposite polarity response compared to NPN devices.

Positive step functions reduce emitter current forcing C_O to charge toward the positive supply through R_E. This of course increases t_r.

t_f input and output appear equal. Emitter current charges C_O negative, again only R_t opposes C_O charge current.

push-pull

This unequal response is one reason that a vertical signal is converted to push-pull one or two stages after the input amplifier. If one views the single-ended output from an impedance standpoint, the difference in transit time indicates output impedance changes with step polarity. Push-pull amplifiers tend to maintain output impedance constant between terminals. However, push-pull circuits can create design problems for the inclusion of controls, particularly those that should return to the chassis.

An example of this is the switched-gain amplifier mechanically coupled to the input attenuator. Fig. 3-67 is the input amplifier driving the switched-gain amplifier. Q1B operates with zero emitter volts at quiescence, or center-screen. Therefore each attenuator position can return to chassis ground and switching causes no vertical CRT displacement. V1 and Q1A function as a longtailed input follower which sets and maintains Q1B emitter voltage at zero volts quiescent operation.

Analyze the voltage setting and temperature compensating of Q1A by first examining other input components.

R1A and R1B return V1 grid to ground and form a constant portion of the input attenuator.

R1A, R3, C3A and C3B oppose the negative input characteristics of CF V1. R1A restricts the quantity of current drawn by the negative resistance of V1. C3A and B form with R3 shunt compensation causing flat input capacitance to all frequencies and pulses. C3 results from circuit-board construction. R2 connects to conductor strips each of which is one capacitor plate. Circuit-board base material is the dielectric. Dielectric variations with frequency add to the input capacitance change. Including a connector near both

ends of R2 creates the second capacitor plate. Returning C3A and B to ground through R3 stabilizes the capacitance, and selecting resistance correctly, the network performs as shunt RC compensation for negative-resistance characteristics.

C2 bypasses grid-limiting resistor R2 to rapidly charge or discharge V1 input capacitance.

R4-C4 in the plate of V1 develop Miller-effect even though gain is low:

t_r (2.2 RC) is 66 microseconds or F_c, $\frac{1}{2\pi Rc}$, is 5.3 kHz.

protective devices

B1, D1 and D2 are protective devices: B1 protects V1 against input voltage overloads. Should grid-to-cathode voltage exceed ignition for neon tube B1, it fires. B1 regulates grid voltage until removal of the excessive input voltage. Assume B1 protects against grid-to-cathode arc due to negative voltage -- reasonable grid current through R2 limits positive grid voltage.

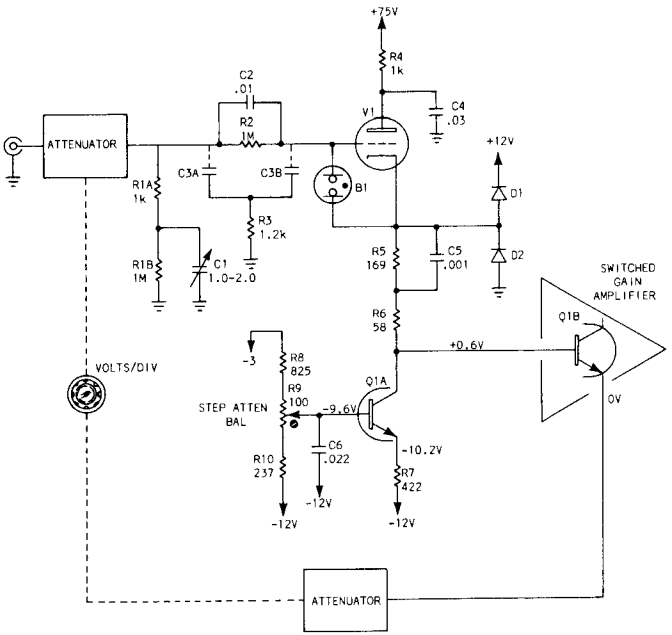


Fig. 3-67. Cathode follower with longtail providing temperature compensation to the following stage.

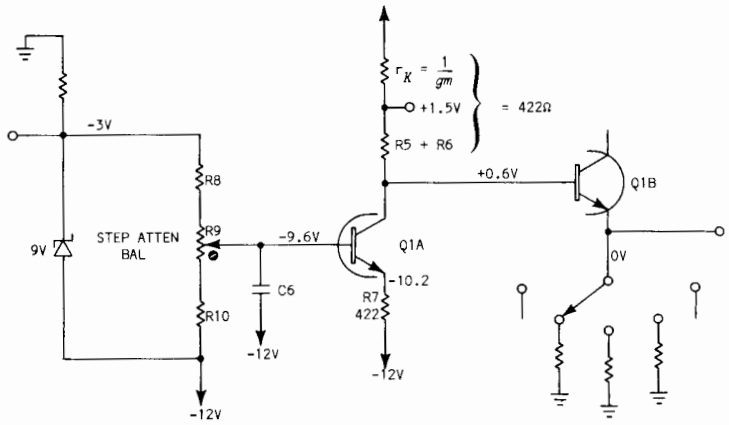


Fig. 3-68. Longtail temperature compensation.

D1 protects Q1A. Should cathode voltage exceed +12 volts D1 clamps. This prevents base-to-collector breakdown of Q1A.

D2 functions during warmup of V1. V1 cathode must heat before V1 consumption equals the current delivered by Q1A. Q1A thus charges C5 toward the -12 volt supply. This causes the grid to appear more and more positive, demanding current from a cold cathode. D2 prevents this by turning on and clamping one diode junction below ground, holding positive bias at about 0.6 volts.

speedup capacitor

C5 bypasses R5 to "speedup" the development of fast-rise signals at the base of Q1B.

V1 self-bias, V1 *gm*, R5, R6 and the conduction of Q1A set the base, thus emitter, operating level of Q1B. Further, due to the high impedance at the collector of Q1A compared to R5 and R6, almost the entire cathode voltage develops across Q1A. These truths permit the circuit simplification of Fig. 3-68. This figure includes partial Q1B emitter circuitry. The emitter connects to a switch which may be positioned to any one of several resistors. Each

resistor returns to ground and the emitter sets at zero volts. This is the desired quiescent condition: An operator actuating the switch causes no vertical deflection. A voltage at the emitter appears as a signal whose amplitude depends upon the emitter resistance selected. Following vertical circuits amplify this signal to deflect the CRT. Grounding the preamplifier input jack and vertically centering the CRT trace should develop zero volts at the emitter of Q1B.

Q1A collector current, through R5 and R6, sets Q1B operating point. The voltage at the top of R5-R6 results from the self-bias of V1. Q1A collector current drops a voltage across R5-R6 setting Q1B base voltage. One adjusts R9 in the base circuit of Q1A for proper base voltage. Since self-bias varies between tubes and with tube aging, this is an empirical adjustment. To check this adjustment switch through the range of the VOLTS/DIV selector. No vertical deflection should occur with the vertical input grounded and the CRT trace vertically centered.

Small power-supply variations do not change Q1A base voltage. This is because Q1A base and emitter components return to the same power supply and the drop across R8, R9 and R10 is regulated. Should the -12 volt supply change, the change occurs at the bottom of R7 and R10, and at the top of R8 due to the zener diode. Equal-voltage changes at both ends of the voltage divider demand an equal change at the base. Forward bias remains constant, thus collector current, thus the drop across R5-R6.

Capacitor C6 returns to -12 volts to prevent power supply fluctuations from appearing as signals at base of Q1A. Any -12 volt change also develops at the wiper of R9. C6, therefore, need not charge to a new level. If C6 returned to ground any voltage change at the wiper of R9 would depend upon C6 charging to the new level. This would develop a signal at Q1A collector, deflecting the CRT accordingly.

temperature compensation

The longtail-configuration temperature compensates Q1B. Q1A and Q1B share temperature environment -- the same case. Equal temperature-induced bias changes occur in Q1A and B. Q1A amplifies the temperature signal by -1, returning Q1B to the correct operating point.

Temperature compensation is necessary to maintain a stable display. A temperature-induced voltage, with Q1B uncompensated, develops at the emitter of Q1B causing a slow CRT display drift, up or down. In this case, an upward drift indicates a temperature increase and downward drift, a decrease.

In-phase equal-amplitude thermal signals appear at the base-emitter of Q1A and B. An out-of-phase thermal signal develops at the collector of Q1A. For this signal to cancel the thermally induced signal, Q1A must amplify by 1. This is the reason for equal Q1A collector and emitter loads.

Assume temperature increases to develop one-mV forward-bias increase. Center-screen voltage at Q1B emitter ascends from 0 to +1 mV. The same change develops at Q1A. To increase Q1A emitter voltage 1 mV, emitter current through R7 must increase 2.4 μA ($I = \frac{E}{R}$). If $\beta = 50$, 2.35-μA collector current flows. Collector current through R5, R6 and r_k drops an additional 1 mV; making Q1B base 1 mV more negative; which returns Q1B emitter to 0 V. One need not consider β to determine collector current. Part tolerances impose sufficient error that one can consider emitter current and collector current equal.

R7 sets total emitter current, therefore determines the collector resistance needed for desired voltage gain. 2.4 μA through R7 develops 1 mV. The collector-voltage drop resulting from this current depends upon collector resistance. 422-ohms collector load gives the desired unity gain. R5, R6 and r_k sum to 422 ohms. Include r_k ($\frac{1}{gm}$) since total collector current flows as CF plate current. Don't consider the cathode as signal ground. A portion of the collector signal appears at the cathode whose amplitude is represented by r_k returned to virtual ground.

Single-ended control circuits, represented by the partial circuitry of Q1B, have been proven in thousands of Tektronix scopes. Q1A compensates for the major disadvantage, thermal drift. Keep this in mind while considering a seemingly unrelated development -- the FET.

field-effect transistors

Semiconductor manufacturers in the recent past developed field-effect transistors (FET) suitable for use in Tektronix instruments. Generally one considers these devices as direct substitutes for triodes. Numerous economies result: Initial cost, reliability, size, weight and heat. Heat savings here refer to elimination of tube filaments. FET displacement of tubes is very attractive for new design.

The FET source follower replaces the CF as an input amplifier. However, FET thermal reactions come into play. Current through the FET decreases as temperature increases. This is opposite to transistor temperature reaction.

A model of a source-follower input amplifier appears in Fig. 3-69. Q1 is the source follower longtailed by Q2. Q1 and Q2 are encapsulated in the same case so that Q2 temperature compensates the circuit. Setting R4 establishes total current initially through R2, Q2, R1 and Q1. Q1 self-bias develops the voltage at the top of R1.

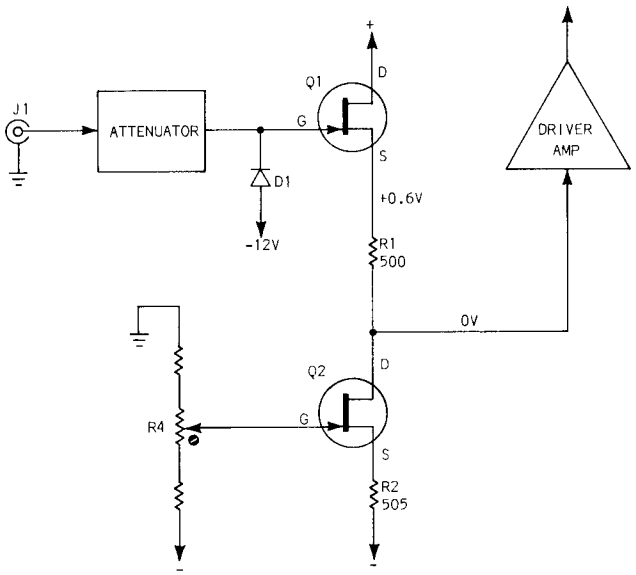


Fig. 3-69. Source-follower input amplifier.

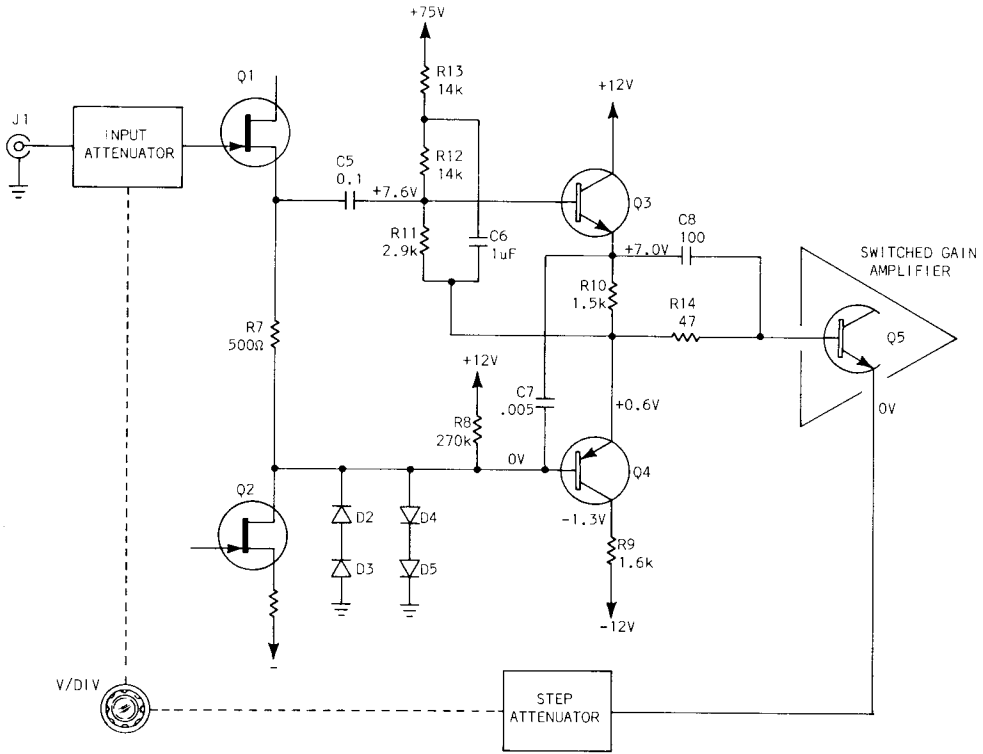


Fig. 3-70. Switched-gain driver amplifier.

Longtail current through R1 sets the output level, shown as zero volts. During temperature increases Q1 conduction decreases, decreasing self-bias. When the voltage at the top of R1 moves negative so should the output voltage. But, Q2 decreases conductivity with Q1, current through R1 decreases maintaining zero volts output.

Preventing output-voltage changes with temperature is good. It does not, however, allow direct connection of the single-ended transistor control amplifier, as the preceding example, since there is no temperature compensation of the control amplifier. Coupling the source follower to the advantageous single-ended control amplifier poses a problem. Fig. 3-70 illustrates one solution.

Emitter followers, Q3 and Q4, couple voltages to, and temperature compensate, the input transistor (Q5) of the switched-gain amplifier. Q3 and Q4 appear to have a complementary connection. They don't function as the classic complementary emitter follower and, therefore, will not carry the name.

Q4 performs several functions: Sets Q5 operating level, temperature compensates Q5, couples signals from DC to several Hz, and provides Q3 emitter current.

Q3 is a broadband emitter follower whose bandwidth exceeds 100 MHz.

Q2 sets the base voltage of Q4. Q4 elevates this voltage one silicon junction to establish the operating point for Q5. Fig. 3-70 shows center-screen nominal-temperature voltages. Q4 and Q5 share a heat sink. Q4 experiences the same temperature changes suffered by Q5. Thermal bias changes also equal. However, Q4 is a PNP device whose base voltage does not vary with temperature. Q4 emitter voltage then becomes more negative as temperature increases and more positive as temperature decreases. This action cancels Q5 thermal-bias reaction, holding the emitter to correct operating levels.

The selection of Q4 depends upon a PNP transistor whose temperature characteristics match those of NPN Q5. Everything has a price. The cost here

was frequency response. Emitter follower Q3 provides the circuit bandwidth. Cross coupling extends the low-frequency response of Q3 and stabilizes input capacitance at the base of Q4.

low-frequency considerations

First consider circuit reaction to signals from DC to 5 Hz, eliminating components of little consequence in this frequency range: D4, D5 and R8 protect Q4 against collector-to-base breakdown, maintains Q3-Q4 emitter current, and holds Q5 base and Q2 drain voltages at reasonable levels. Should Q1 and Q2 be removed from the circuit, R8 functions as the base return for Q4. Silicon diodes D4 and D5 clamp at +1.2 V thus preventing reverse breakdown of Q4. The clamping also prevents drastic circuit changes by containing Q3 and Q4 current changes to about 6% and holding Q5 emitter voltage at about +1.2 V. Effects upon temperature compensation and active-device power dissipation are negligible with Q2 in or out of the circuit. Further, the voltage across D4 and D5 represents a reasonable drain voltage for Q2 when it is replaced.

D2 and D3 clamp when signals exceed -1.2 volts to protect Q5 against reverse breakdown.

Diodes, connected as D2-D3 at the base of a PNP transistor, protect preceding or following devices but not the PNP. Imagine D2 and D3 open: Negative base signals cause positive collector signals moving the base-collector junction toward forward bias. An input signal of about -2.5 volts forward biases this junction and current flows from base-to-collector. This is merely normal forward biased diode action. Negative signals of this magnitude do represent reverse breakdown for the following NPN directly coupled to the emitter of Q4.

C5, C6, C7, C8 and R14 react at frequencies higher than those now considered. Using only the remaining components simplifies the initial circuit analysis. Refer to Fig. 3-71.

First determine quiescent conditions: Q3 and Q4 both have turn-on potential. Q4 elevates the zero-volts input one junction setting the voltage across R11, R12 and R13. 10% of the voltage develops across R11. One silicon junction below this base voltage is Q3 emitter voltage. These voltages create Q4-emitter-current demand. 2.4 mA must flow

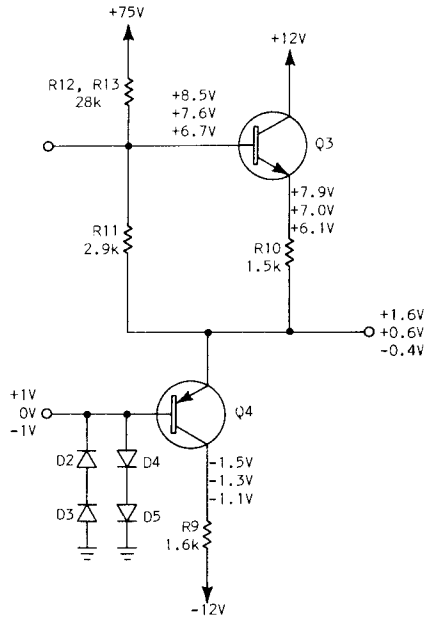


Fig. 3-71. Operating bias circuitry.

through R11 and 4.3 mA through R10. The current sum flows as Q4 emitter, thus collector current. 6.7 mA establishes Q4 collector voltage at -1.3 V. This current stabilizes Q3 and Q4 as longtail current by changing little during maximum signal-voltage variations.

The effects of voltage divider R11-R12-R13 cause Q4 collector-voltage change. A positive 1-volt signal reduces the voltage across R11-R12-R13, reducing current demand. This current change of about 0.03 mA per volt adds to Q3 emitter-current change. The voltage divider develops 90% of Q4 emitter voltage at the base, therefore, emitter of Q3. Decreasing the voltage across R10 decreases Q3 emitter current 0.0667 mA. Summing Q3 and voltage-divider current changes, indicates Q4 collector current changes about 0.1 mA.

Negative signals increase Q4 collector current. The voltage divider draws more current and Q3 emitter current increases to drop an additional 0.1 volt across R10 for a -1 volt input.

Consider now the effects of the circuit configuration upon bandpass. Q4 alone couples signals from DC to a few Hz as a longtailed emitter follower, with R11, R12, R13, R10 and Q3 functioning as the longtail. Setting quiescent conditions establishes circuit reaction at the very low end of the bandpass. Due mostly to input capacitance, Q4 frequency response deteriorates at fairly low frequencies. Emitter follower Q3 functions at low frequencies to stabilize Q4 input capacitance.

capacitance stabilization

Fig. 3-72 includes circuit components necessary for capacitance stabilization at the base of Q4. The voltage source and its internal resistance (R_g) represent input circuitry. Signals above a few Hz couple through C5 to the base of Q3. Signal driving Q3 has two effects: Emitter current becomes constant, eliminating Q4 Miller-effect, and Q4 input capacitance discharges through C7.

Miller-effect results from Q4 collector-voltage changes. This adds to input capacitance. C5 couples a portion of the input signal to the base of Q3. Each signal increment reduces emitter-current *change*. As frequency increases, greater percentages

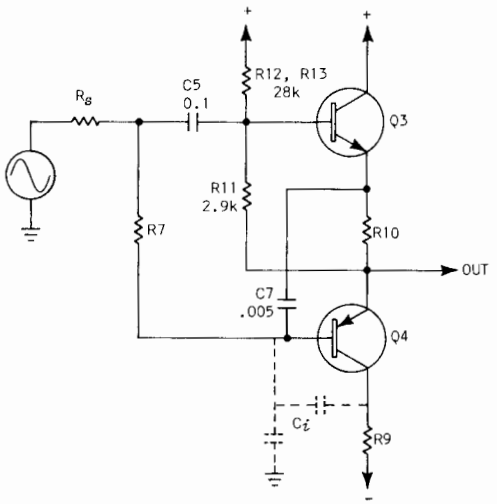


Fig. 3-72. Low-frequency signal circuit stabilizes input capacitance.

of the input voltage appear at Q3 until Q3 and Q4 emitters change equal amounts. When this occurs, emitter, thus collector, current is constant regardless of signal amplitude. Input capacitance is therefore no longer increased by Miller-effect.

Input capacitance yet exists at the base of Q4. This capacitance, however, quickly charges or discharges through C7 and the low emitter impedance of Q3. Cross coupling fails to eliminate input capacitance but does stabilize it to a constant value. C7, empirically selected, is listed at a nominal value.

Selection of C7 depends to a degree upon coupling-circuit time constant at the base of Q3. This time constant should be long to couple low frequencies. There is a problem: Physically or electrically large components contribute reactive shunts.

Returning R11 to the emitters increases the time constant by effectively increasing input R. Signals coupled through C5 develop across R12 and R13 paralleled by R11; an equivalent resistance of 2.8 kΩ. If R11 were returned to ground, the coupling RC time constant would be $C5(2.8\ k\Omega) = 0.28 \times 10^{-3}$ seconds.

$$F_c = \frac{1}{2\pi\ 0.28 \times 10^{-3}} = 0.57 \times 10^{3} = 570\ Hz.$$

Returning R11 to the emitter increases R, thereby F_c, by 10. At low frequencies, 100% of input voltage develops at the base of Q4 and 90% at the base of Q3. C5 still drives 2.8-kΩ equivalent resistance but this resistance returns not to ground but to 90% of signal voltage. For one-volt signals C5 need couple but 0.1 volt -- or only 36-μA signal current need flow through C5: $\frac{0.1\ V}{2.8\ k\Omega} = 36\ \mu A$. Since 36 μA develops

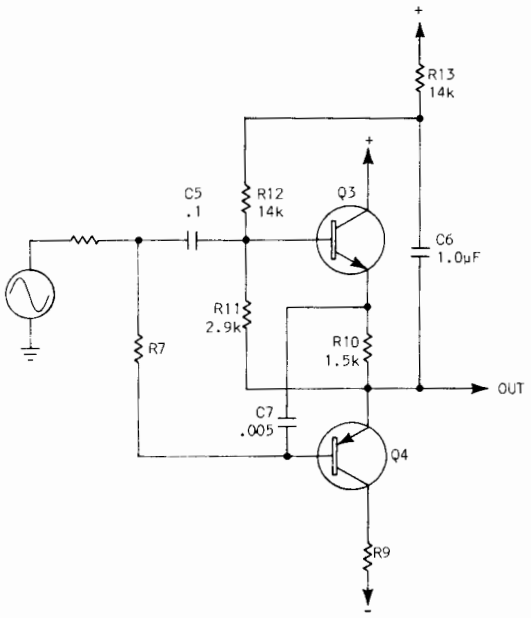


Fig. 3-73. C6 extends Q3 input time constant.

full signal voltage at the base of Q3, apparent input R is 28 kΩ:

$$R = \frac{E}{I} = \frac{1}{36 \times 10^{-6}} = 28 \times 10^{3}\ \Omega.$$

$$T = C5\ (28 \times 10^{-3})\ (2.8 \times 10^{-3})\ \text{seconds.}$$

$$F_c = \frac{1}{2\pi(2.8 \times 10^{-3})} = 0.57 \times 10^{2} = 57\ \text{Hz.}$$

To prevent low-frequency phasing problems Q3 should react to even lower frequencies. Extending low-frequency response must not include increasing the physical or electrical size of C5. This is the purpose of C6.

See Fig. 3-73. C6 shunts R11 and R12 of voltage divider R11-R12-R13. Q4-emitter signal voltages develop across the series circuit C6-R13. Therefore, C6 charge current adds to that demanded by R11-R12; and both currents are in phase with signal voltages. Signal voltages which develop across R13 via C6 increase apparent input resistance at the base of Q3.

The -3 dB point for C6-R13 is 11.4 Hz. 70% of this input-signal voltage develops across R13, boosting the signal amplitude at the base of Q3. More of Q4 emitter voltage now develops at the base of Q3. Since Q3 equivalent base resistance returns to 97.2% of signal voltage, C5 need provide 10-μA signal current to develop 1-volt signals at the base of Q3: $I = \frac{0.028}{2.8\ k\Omega} = 10 \times 10^{-6}$ A

$$R_i \approx \frac{1}{10 \times 10^{-6}} \approx 100\ k\Omega$$

$$F_c = \frac{1}{2\pi\ C5\ R_{in}} \approx 16\ Hz.$$

All of which indicates that C5 couples signal energy to the base of Q3 at less than 20 Hz. Q3 then functions as signal-driven emitter follower maintaining Q4 input capacitance at a low value.

To this point Q4 coupled all signals to the switched-gain amplifier. When one increased input signal frequency and Q4 faltered, Q3 forced proper emitter-follower action. This "bootstrapping" by Q3 works for a portion of the bandpass until, at higher frequencies, Q4 becomes just another passive device.

Consider Q4 a passive device at frequencies above 1.5 MHz. At this frequency C5 couples full signal voltage, C6 is a short circuit and C7 continues to fix Q4 base capacitance. The last two components now come into play.

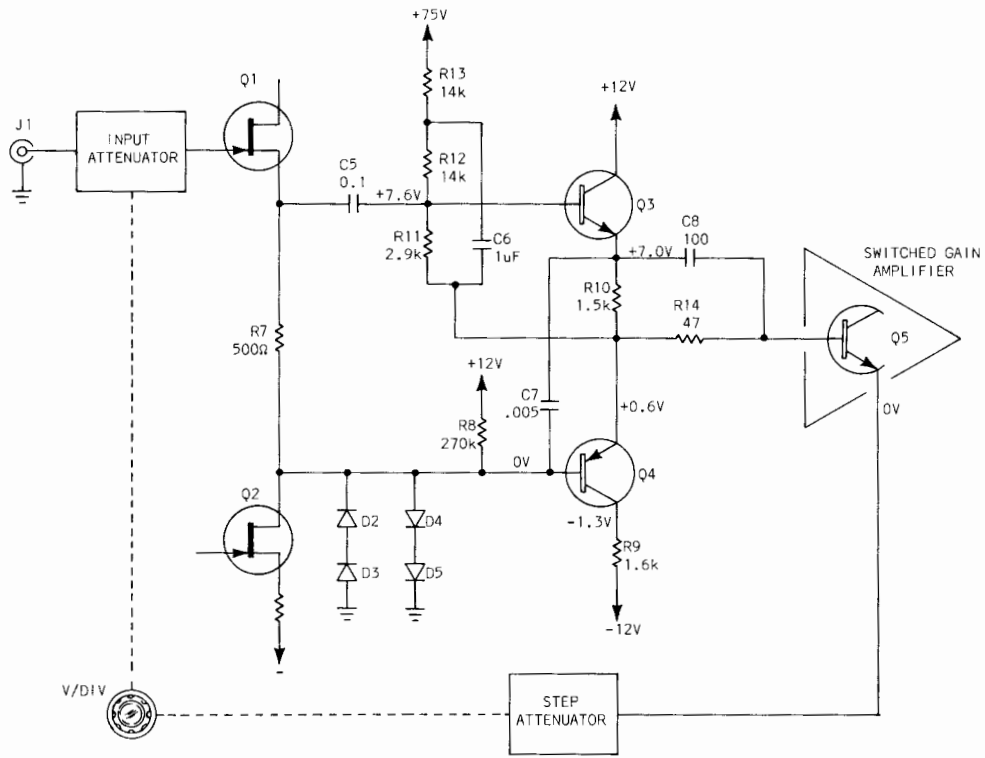


Fig. 3-74. Switched-gain driver amplifier.

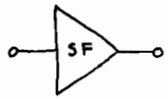
Fig. 3-74 is the complete schematic including C8 and R14.

C8 bypasses R10 providing a coupling path from Q3 emitter to the base of Q5. R14 attenuates signals little if any.

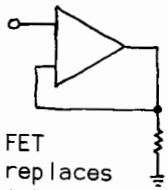
R14 emitter-loads to damp oscillations. As with conventional complementary emitter followers, high-amplitude fast-rise signals develop negative-input resistance characteristics of Q3-Q4. Since C8 bypasses R10, R14 represents total emitter-to-emitter impedance. R14 resistance is sufficient to damp oscillations yet small enough to have negligible effect upon desired signal amplitude.

Although of a different magnitude than cathode followers, emitter followers are high-input impedance, low-output impedance devices. They are found in any circuit of an oscilloscope vertical amplifier except the front end or preamplifier input stage.

source follower



A source-follower general description uses the old familiar phrases: High-input impedance and low-output impedance. These words describe any follower. Comparatively, source-follower (SF) input impedance exceeds that of the cathode follower or emitter follower. SF output impedance also exceeds that of the other followers.



FET replaces tube

Source-follower characteristics result from field-effect transistor parameters. These describe a high-input-impedance semiconductor. Oscilloscopes for years have been solid state except for those circuit points requiring high-input impedance. The FET then becomes attractive as a tube replacement. Some of the advantages are:

High-input impedance
Solid-state reliability
No microphonics
Excellent aging characteristics
Small size
Power-supply demand reduced.

Field-effect transistors fall into two general categories, junction (FET) and insulated gate (IGFET or MOSFET).

CHARACTERISTICS	TUBE	JUNCTION FET	INSULATED GATE FET
INPUT IMPEDANCE	HIGH	HIGH	VERY HIGH
NOISE	LOW	LOW	UNPREDICTABLE
WARM-UP TIME	LONG	SHORT	SHORT
SIZE	LARGE	SMALL	SMALL
POWER CONSUMPTION	LARGE	SMALL	SMALL
AGING	NOTICEABLE	NOT NOTICEABLE	NOTICEABLE
BIAS VOLTAGE TEMP COEFFICIENT	LOW, NOT PREDICTABLE	LOW, PREDICTABLE	HIGH, NOT PREDICTABLE
TYPICAL GATE/GRID CURRENT	≈1nA	≈.1nA	≈10pA
GATE/GRID CURRENT CHANGE WITH TEMP	HIGH, UNPREDICTABLE	MEDIUM, PREDICTABLE	LOW, UNPREDICTABLE
RELIABILITY	LOW	HIGH	HIGH
SENSITIVITY TO OVERLOAD	VERY GOOD	GOOD	POOR

Fig. 3-75. Electron tube vs field-effect transistor.

Only junction field-effect transistors, at this writing, appear in Tektronix vertical amplifiers.

Fig. 3-75 compares tube, FET and IGFET, characteristics. The FET matches or exceeds the tube in every category except one, overload sensitivity. Under IGFET the word *unpredictable* expresses today's FET preference.

conductivity voltage controlled

A FET is a resistance whose conductivity is voltage controlled. Majority carriers travel the *channel* which consists of "n" or "p" material. The majority carriers enter the channel at the *source* and exit at the *drain*.

n channel

source

drain

Fig. 3-76 is an "n" channel. Electrons, "n"-material majority carriers, flow from the negative voltage at the source through the channel to the positive voltage at the drain. Only voltage polarity determines which is the drain and which is the source end of the channel. Drain current (I_D) always flows from source to drain in "n" channels.

p channel

Majority carriers are holes in "p" channels. Therefore "p" channels function as described for "n"

channels. Just remember to reverse polarity: I_D always flows from drain to source in a "p" channel.

channel voltage gradient

Fig. 3-77 illustrates a very simple but important point: A voltage gradient develops along the channel. The channel is nothing more than a resistance without polarity. But if one could reach into the device he would measure voltage differences along the channel, becoming more positive as he neared the drain ("n" channel). If drain current flows a voltage gradient must develop: E = IR.

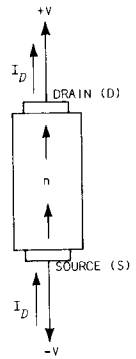


Fig. 3-76. FET channel.

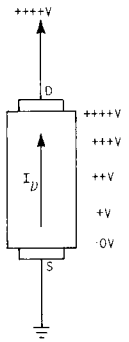


Fig. 3-77. Drain current develops voltage gradient across the channel.

Keep the voltage gradient in mind while completing the FET model. A *gate* is the final terminal needed.

Picture the channel as a bar of "n" material with connectors at either end. Now join two smaller pieces of "p" material at either side of the bar, centered along its length. Add connectors and label the terminal *gate*. Fig. 3-78 is such a model.

gate

This figure shows an intrusion into the channel called a depleted region. When the "p" and "n" material join a change occurs at the junction. Free electrons in the channel fill "p"-region holes. Right at the junction a barrier forms preventing further combination of holes and electrons. Around the junction is a small area almost devoid of free carriers. Increasing the depleted area is the operating principle of an FET. This also explains why a junction FET is called a *depletion-mode* device.

depleted region

Returning gate and source leads to ground and the drain lead to a low-impedance supply allows zero-bias analysis (Fig. 3-79). The emitter follower functions as a low-impedance drain-voltage supply. Setting emitter voltage slightly positive causes drain current to flow. Since the gate and source leads are shorted, gate-to-source voltage (V_{GS}) is zero. I_D indicates drain current under this condition.

Initial drain-voltage (V_D) application caused "p"-material holes to move toward the gate terminals, but channel holes cannot cross the junction. Current flows only when carriers flow continuously through the entire circuit. This also applies to electrons. Channel electrons move away from the junction, but the gate (p) provides no free electrons to cross the junction.

Channel electrons pulled from the area near the gate leave this region completely free of carriers. The original small depleted area enlarges as shown. A depletion region conducts poorly. Enlarging this region then reduces the effective channel cross section, increasing channel resistance.

channel resistance increased

Notice that the depletion region skews toward the drain. Drain current develops a channel-voltage gradient creating this shape. I_D flows through a

length of "n" material, between the source connection and the nearest gate-junction edge. The resultant voltage drop, representing reverse bias, pulls the depletion region toward channel center. Reverse bias increases along the channel, pulling the depletion region further into the channel. Gate-to-drain voltage (V_{GD}) of course represents maximum reverse bias.

Increasing drain voltage (V_D) increases I_D and the depleted area up to a point. Raising V_D above this point affects no I_D increase. This point carries the name *pinch-off* (V_p). The depletion region appears to reach into the channel and "pinch-off" any change in drain current.

pinch-off

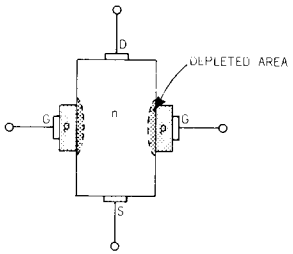


Fig. 3-78. Field-effect transistor model, n channel.

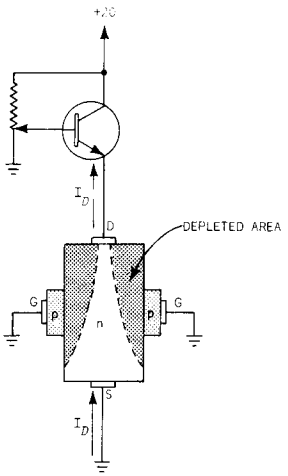


Fig. 3-79. Voltage gradient increases area depleted.

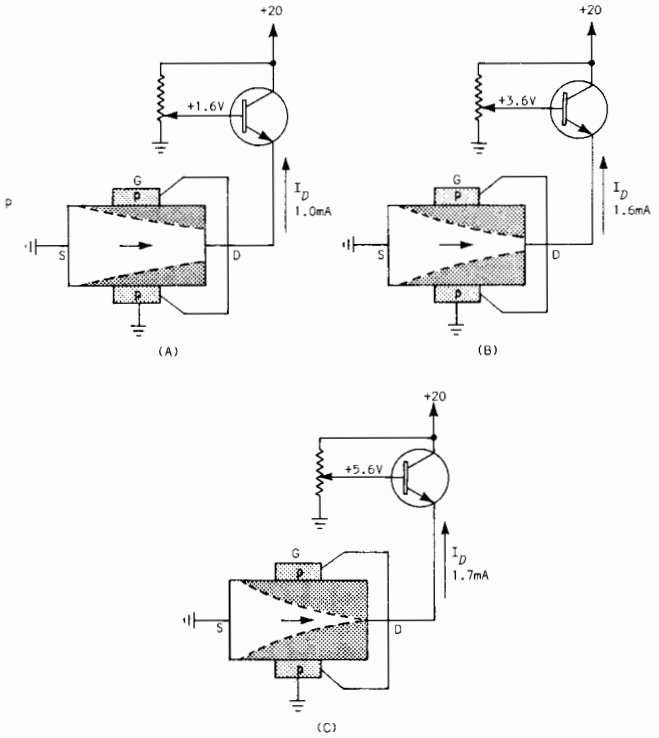


Fig. 3-80. I_D increasing with V_D.

V_p

The FET models in Fig. 3-80 show the effects of increasing V_D. In (A) 1 volt at the drain draws 1-mA drain current, creating a depletion region enlarged at the drain end. Increasing V_D 2 volts (B) increases I_D by 0.6 mA and the depletion area extends further into the channel. Raising V_D another 2 volts to 5 increases I_D only 0.1 mA. The depletion regions almost touch. V_D increases, above 5 volts, draw no more than 1.7 mA through the channel. This then is pinch-off voltage (V_p).

Pinch-off occurs when the bias from *drain* to *gate* causes maximum depletion-region growth. Remember, V_p is a value of drain-to-gate voltage (V_{DG}).

A curve of this action appears as Fig. 3-81A. V_D increases, between 0 and 5 volts, increase I_D. Above 5 V_D, I_D changes little. When a voltage change across a device causes a current change in the device, the device has a predictable ohmic value. For this reason, call that portion of the curve below V_p the *ohmic region*. Above V_p, I_D remains constant with changes in V_D indicating infinite dynamic resistance.

ohmic region

Drain-current nomenclature also changes above V_p. With gate and source shorted, I_D above V_p is considered saturated channel current: I_{DSS}.

I_{DSS}

drain-to-source resistance

Resistance in question appears as the FET drain-to-source resistance (r_{ds}). The r_{ds} curve, related to Fig. 3-81A, is plotted in Fig. 3-81B. Large r_{ds} values result from self-bias created by the voltage gradient between source and gate. FET curves thus resemble those of a triode with a large unbypassed cathode resistor.

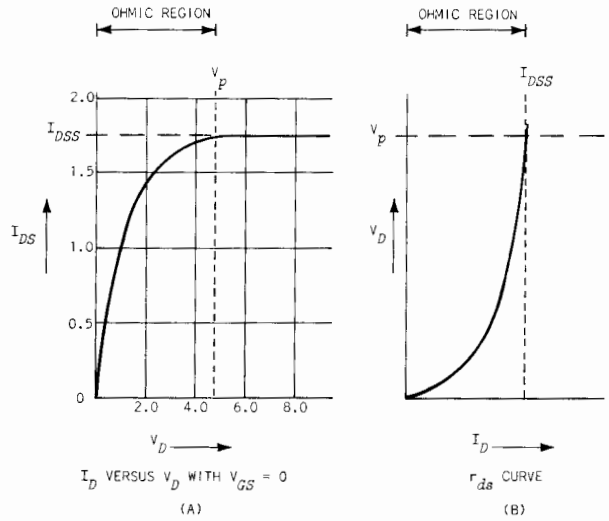


Fig. 3-81. Ohmic and pinch-off regions.

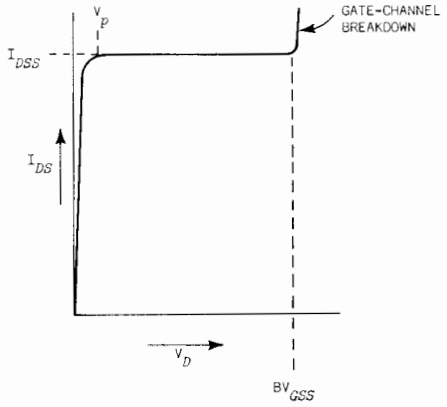


Fig. 3-82. Gate-to-channel breakdown, V_{GS} = 0.

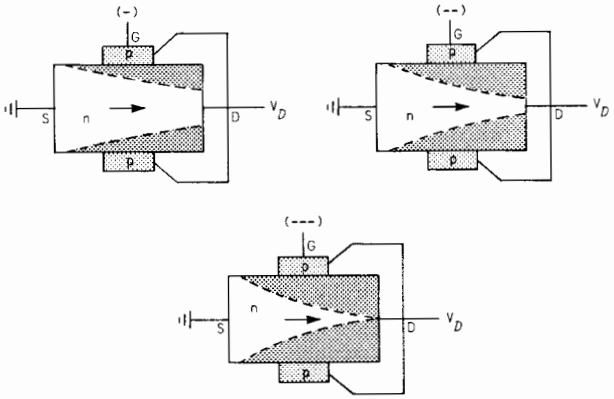


Fig. 3-83. Back-bias controlling-current flow in an n-channel FET.

gate-to-channel breakdown

Do not dismiss an FET as analogous to a tube, whether triode or pentode. This is a semiconductor. For example, increasing V_D far above V_p causes gate-to-channel breakdown. I_{DSS} of Fig. 3-82 remains constant as V_{DD} increases until reaching gate-to-channel breakdown voltage (BV_{GSS}). The I_D curve now ascends toward infinity. Operating an FET into BV_{GSS} usually destroys the device.

Drain-to-gate bias (V_{DG}) controls channel cross-section area at the drain end of the channel. Gate-to-source bias (V_{GS}) sets channel-current demand for a given V_D. Therefore small voltage changes at the gate cause relatively large I_D changes.

controlling conduction with V_{GS}

The model of Fig. 3-83 controls I_D with V_{GS}. Here the source returns to ground, the drain to a set low-impedance voltage supply and gate voltage varies. Initial V_{GS} restricts I_D little. Applying greater negative voltage increases the depletion area, subtracts from channel area, thereby opposing I_D. This continues until the device reaches pinch-off voltage. V_p occurs when *drain-to-gate* bias reaches the same value as with the 0-V_{GS} drain curve.

Since one most often measures voltage to ground or the source, V_p specifications list V_D and V_{GS} voltages at some small I_D flow. Many consider that driving the gate to V_p achieves cutoff. This for most practical measurements is true. A junction FET cannot be cut off or a voltage gradient across the channel would not develop. However, only nanoamperes or microamperes of I_D flow at V_p (cutoff).

Displacement current establishes basic input capacitance at the gate. Assume gate voltage, in the model of Fig. 3-83, swings from minimum negative to maximum negative then back to minimum negative. The depleted area swells then shrinks with gate-voltage changes. Depletion region carriers move with the region. This is displacement current. The name and effect are those of a capacitor dielectric.

drain characteristic curves

Plotting drain current versus drain voltage at various gate-voltage steps develops drain-characteristic curves. Fig. 3-84 drain characteristics resulted from a photograph of a Tektronix curve-tracer display. Pinch-off occurs at 6 volts. Only when $V_{GS} = 0$, do V_p and V_{DS} equal. However, V_p is always 6 V_{GD} for this particular device. Consider V_D values for V_{GS} settings other than zero:

At V_p, when $V_{GS} = 0$, $V_D = +6$
$V_{GS} = -0.5$, $V_D = +5.5$
$V_{GS} = -1.0$, $V_D = +5.0$
$V_{GS} = -1.5$, $V_D = +4.5$
$V_{GS} = -2.0$, $V_D = +4.0$.

Experimenters have difficulty pinpointing V_p and circuit analysts sometimes need to know *gm* of a given device. A transfer curve provides information for both.

Fig. 3-85 is such a curve. Determining I_{DSS} is simple and plotting other I_D points are easy enough until V_{GS} approaches V_p. I_D changes little near V_p, destroying confidence in the final V_p point. However, lay a straight edge at the I_{DSS} intercept

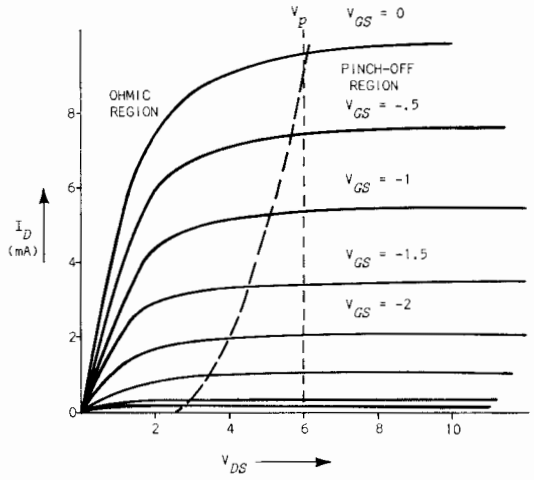


Fig. 3-84. Drain characteristics of FET.

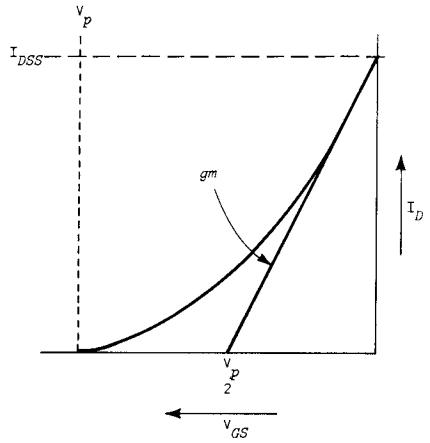


Fig. 3-85. Drawing a tangent to the transfer curve establishes *gm* and V_p.

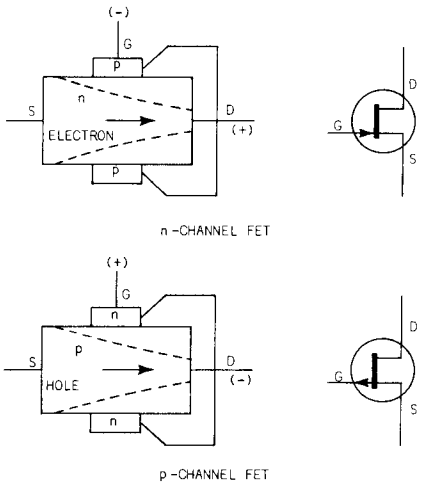


Fig. 3-86. Comparison of an n-channel FET and a p-channel FET.

plotting *gm* and V_p

and draw a line, tangent to the curve, to intercept V_{GS}. The tangent intercepts at one-half V_p. The slope of the line is *gm*.

Fig. 3-86 compares "n"- and "p"-channel FET's. These FET's operate alike. They are "on" devices operated

toward cutoff. Stated differently: An FET, either "p" or "n" channel, performs when reverse-biased.

A forward-biased junction FET essentially ceases to be an FET. Input impedance falls and drain current bears no useful relation to input signals. This might well raise a question: Since the gate normally draws no current, and gate voltages control channel depletion electrostatically, what happens if an insulator be placed between gate and channel?

depletion mode IGFET

The answer: The device becomes an Insulated Gate FET (IGFET). Gate voltages deplete the channel as before with far lower gate leakage current (I_{GSS}). Now, however, ordinary metal serves as well as semiconductor for gate material. Call this device a *depletion-mode IGFET*.

MOSFET

The model of Fig. 3-87 is named MOSFET. This stands for Metal-Oxide-Silicon FET, one of several advertising names for IGFET's. MOSFET does describe IGFET construction. The silicon channel lays in substrate covered by insulation, a thin oxide layer thermally formed on the semiconductor surface. A layer of metal deposited on the oxide forms the gate. Holes in the oxide provide source and drain lead access to the channel.

surface effects

IGFET gate voltages create effects which take place near the semiconductor surface. The channel surface, oxide insulator and metal gate form a capacitor.

enhancement mode

Forward-biasing a properly designed IGFET enhances channel conductivity. Fig. 3-88 illustrates an IGFET which operates in the depletion *and* enhancement mode. The lightly doped channel, a moderate conductor, terminates in heavily doped regions at the drain and source. Negative gate voltages deplete the channel. Positive voltages enhance conductivity by inducing charges into the channel. Since the input is a capacitor, positive gate voltages cause equal negative charges on the surface of the channel. A concentration of electrons forms this negative charge *enhancing* the channel.

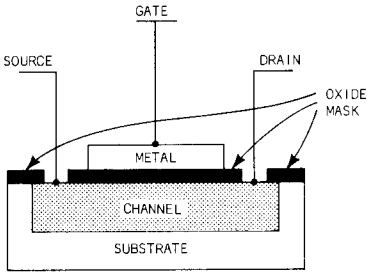


Fig. 3-87. Depletion-mode-only MOSFET construction.

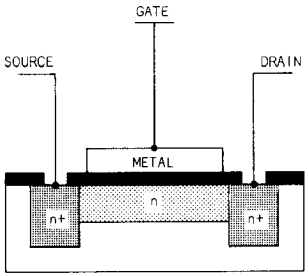


Fig. 3-88. Construction of an IGFET which operates in enhancement and depletion modes.

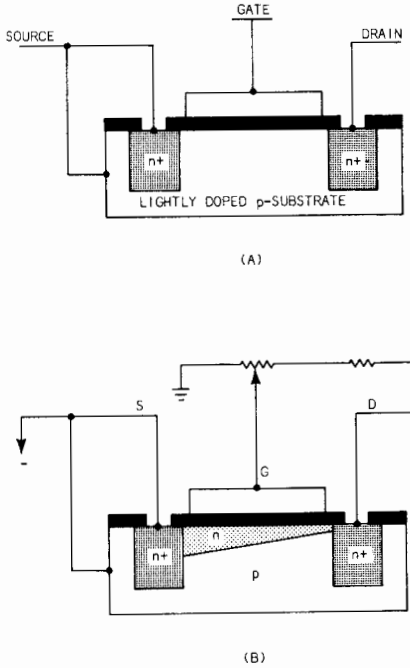


Fig. 3-89. Enhancement-mode-only IGFET.

The third type of IGFET works in the enhancement mode only. Fig. 3-89A is a model of this type IGFET. Channel "p" material prevents current flow between the heavily doped "n" source and drain. In the absence of forward gate voltage no drain current flows. One of the channel "pn" junctions, with the gate open, is always reverse-biased regardless of voltage polarity across the channel.

Forward bias, as shown in Fig. 3-89B, causes channel conduction. Sufficient forward bias induces charges into the channel, bridging source and drain. This actually changes the "p"-channel surface into an "n" semiconductor.

transfer characteristics

IGFET transfer characteristics follow as the FET. Fig. 3-90 shows relative characteristics. Notice I_{DSS} relationships: I_{DSS} is maximum I_D for depletion only devices and zero for enhancement-mode only IGFET's.

IGFET's do not at present appear in Tektronix vertical amplifiers. Whether IGFET's will appear in the future is pure conjecture. A number of companies devote considerable developmental activity to all types. Today junction FET's are cheaper and more predictable.

Schematic IGFET symbols appear in Fig. 3-91.

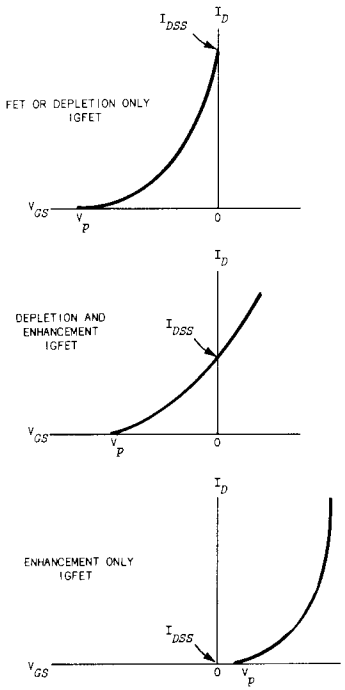


Fig. 3-90. Transfer characteristic comparison.

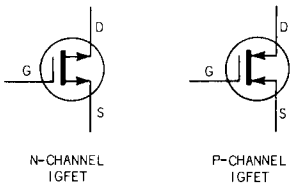


Fig. 3-91.

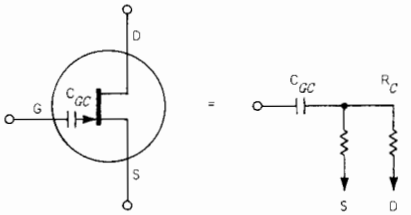


Fig. 3-92. The field-effect capacitance forms part of SF input capacitance.

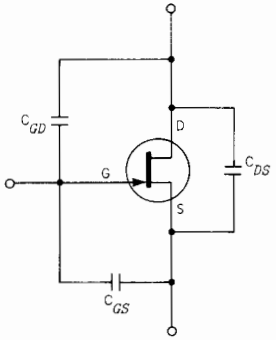


Fig. 3-93. Designating inter-element capacitance.

C_{GC}

Source follower terms differ but effects parallel those of the other followers. Input impedance, Miller-effect, output impedance and voltage gain receive similar treatment. One component, however, differs from other three terminal devices, "gate-to-channel capacitance (C_{GC})." (Fig. 3-92.)

Field-effect is C_{GC}. Gate voltages cause displacement current within the semiconductor material which defines C_{GC}. Signals applied to the gate develop across C_{GC} in series with a small resistance. This resistance is the parallel value of drain-to-gate and source-to-gate channel resistance. C_{GC} must then be small to prevent signal-source loading. Incidentally, this presents an FET design problem: High transconductance requires a large gate, but low input capacitance requires a small gate.

input capacitance

C_{GC} constitutes a portion of input capacitance (C_{iss}). Interelement capacitances combine to appear as C_{iss}. Fig. 3-93 labels these capacitances. C_{DS}, drain-to-source capacitance, adds to output capacitance rather than input. Gate-to-drain (C_{GD}) and gate-to-source (C_{GS}) capacitances shunt C_{GC}. The sum C_{GD}, C_{GS} and C_{GC} is C_{iss} with drain and source shorted.

Source-follower configuration changes C_{iss} somewhat. Returning the source to ground through a resistor and the drain to V_{DD} (apparent ground) slightly modifies C_{iss}. Stray capacitance and C_{DS} shunt the source resistor, thereby appearing in series with C_{GS}. This reduces C_{GS} apparent value from gate to ground, reducing input capacitance. C_{GD} remains constant since it returns to apparent ground at the drain.

reverse capacitance

C_{GD} is the Miller-effect coupling capacitor. Adding a resistance between drain and V_{DD} causes C_{GD} to increase $(1 + A_V)$ times. The effect carries the name reverse capacitance (C_{rss}). Listing C_{rss} with a specific value "*ss*" indicates source and gate shorted.

Fig. 3-94A shows the equivalent input circuit of a source follower whose drain returns to apparent ground. The signal generator works into a capacitive load equal to C_{iss}. On the other hand, loading the drain changes input C as indicated in

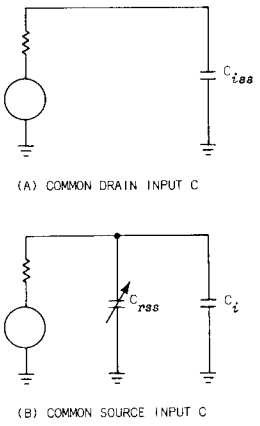


Fig. 3-94.

Fig. 3-94B. C_i consists of C_{iss} less C_{GD}. C_{rss}, which is C_{GD} varied by gain, shunts C_i as the generator load. Miller-effect occurs as in electron tubes and transistors. An FET merely has less capacitance to be affected.

follower gain similarities

Voltage gain is also similar. See Fig. 3-95. The source-follower reaction to an input step reproduces an output with slightly rounded corners and some signal loss. Rounded corners result from reactive components first presented. Signal loss indicates some form of voltage division.

voltage gain less than unity

The input step develops across external resistance R_S and internal channel resistance r_s in series. Voltage gain can never be more than the ratio of R_S to total resistance. However, a large R_S and a small r_s result in small signal losses. Assume 0.8 or better as longtailed-source-follower gain.

longtailing

Longtailing has the obvious advantage of providing large R_S values but there is another. An FET is a square-law device. Operating in the ohmic region causes r_s to vary according to square-law. Current driving an FET by longtailing maintains operation in the pinch-off region which may not reduce but holds r_s constant.

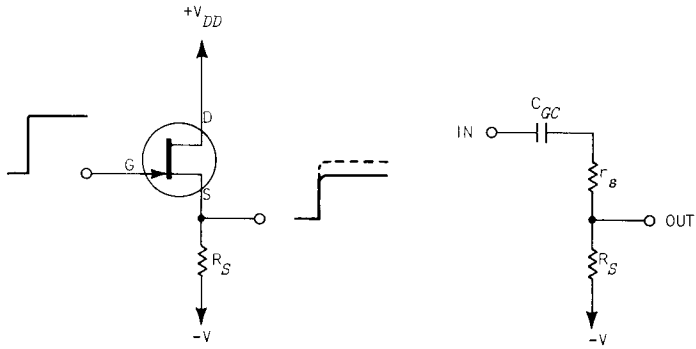


Fig. 3-95. $A_V \approx \dfrac{R_S}{r_s + R_S}$

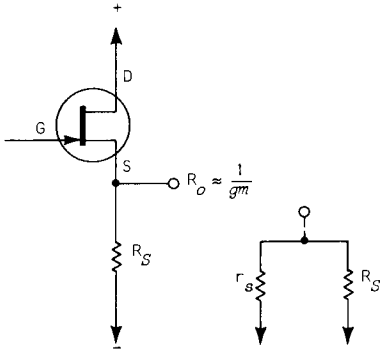


Fig. 3-96.

output impedance

R_S and r_s also determine output impedance. Like r_k inverting transconductance approximates r_s. And if R_S be large, $R_O \approx r_s \approx \frac{1}{gm}$. Fig. 3-96 indicates this. However, if R_S fails to exceed r_s by ten, R_O must be considered the parallel value of R_S and r_s. An FET has fairly low *gm* (somewhere between 500 and 3000 μmhos). Higher-*gm* devices occur as design and manufacturing techniques improve. While considering FET circuit description in this book, assume 2000 μmhos, an r_s of 500 Ω.

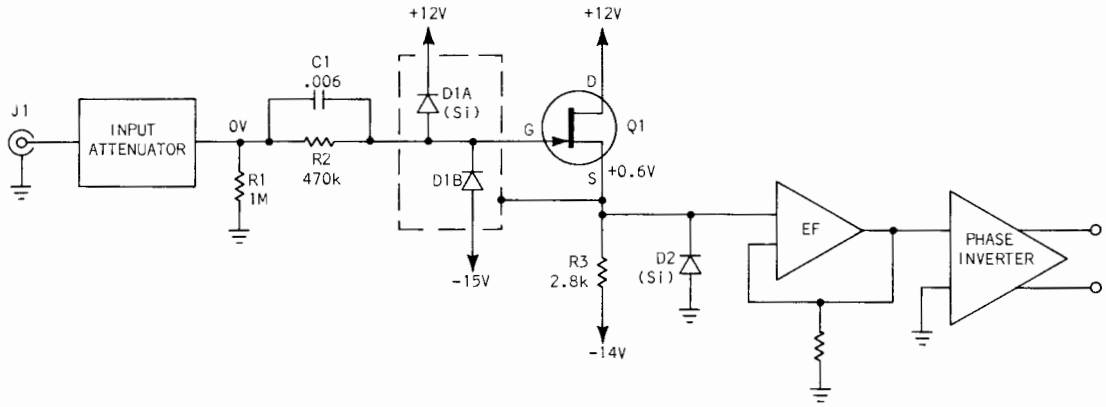


Fig. 3-97. Source-follower input amplifier.

input amplifier

Passive components of the SF input amplifier appear at first identical to those of a CF. As a case in point refer to the input amplifier of Fig. 3-97. R1, R2, R3, D2 and C2 appear in the same configuration here as in a CF input amplifier. R1, R3, D2 and C1 react in a similar fashion. R2, however, limits when D1A or D1B is on, rather than utilizing leakage current (I_{gss}).

R1 returns the gate to ground. And it forms a part of the input-attenuator voltage divider.

C1 serves as a current source which rapidly charges and discharges input capacitance. Input capacitance would otherwise charge through R2 slowing SF reaction to "fast" signals.

R2 prevents a low-resistance shunt of the circuit under test during conduction of D1A or B.

limiting

D1A serves as a current source which reduces Q1-gate-current demand. Applying a signal, +12.6 volts or more, to the gate of Q1 forward biases the gate-drain junction. This is not necessarily harmful to Q1. Current flows from drain to gate as in any semiconductor diode and is limited by R2. However, heavy current from drain-to-gate slows the recovery time of Q1. D1 has much less forward resistance than Q1 therefore excess positive inputs draw most of the current through D1A and very little through Q1. In the X1 attenuator position D1 in series with R2 shunts the circuit under test.

protection

D1B protects Q1. Positive voltages at the gate of Q1 can draw current from the drain or source or both. This does no damage, Q1 merely becomes a forward-biased "pn" junction. However, moderate current flow into the channel from the gate destroys an "n"-channel FET! D1B turns on when input voltages exceed -15.6 volts, clamping V_G so that V_{DG} fails to reach BV_{gs}. The voltage "window" between clamps is as large as Q1 can handle since V_{DD} = +12 V and V_{ss} = -14 V.

reducing input capacitance

Tying the case of D1 to the source of Q1 reduces input capacitance. Stray capacitance associated with D1 must return to some reference for its effect to be predictable. Returning this capacitance to the source reduces the voltage across the capacitance, reducing effective gate capacitance.

clamping

R3 longtails and D2 clamps to protect the emitter follower. D2 prevents the voltage at the EF input from exceeding -0.6 V, resulting from signals or the removal of Q1.

reducing output impedance

The emitter follower functions as an impedance transformer. In this case the transistor phase inverter receives drive from 5 or 10 Ω rather than 500 Ω or more at the output of Q1.

balanced phase-inverter input impedance

Equal impedance at each phase-inverter input terminal is often as important as low-impedance drive at the active terminal. One terminal of the phase inverter is shown at ground. This is apparent ground. Both terminals return to an equal quiescent bias and, ideally, to equal input impedance. One method to accomplish this is to bias the undriven terminal of the phase inverter with circuits identical to the signal-drive chain. Fig. 3-98 is appropriate.

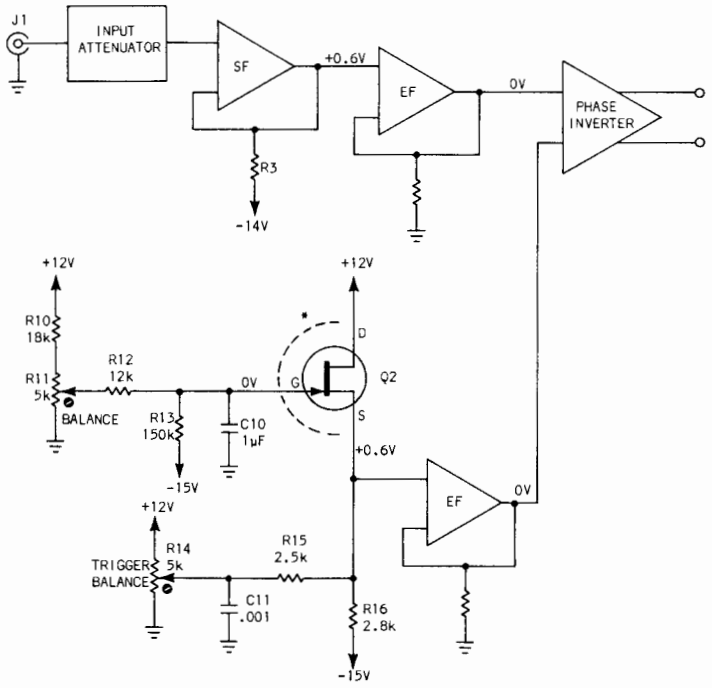


Fig. 3-98. Balancing the phase-inverter input terminals.

balanced phase-inverter bias

Of the same FET type, Q1 and Q2 share temperature environment. Identical emitter followers drive the phase inverter, therefore one sets Q2 gate voltage for a quiescent null across the phase-inverter input terminals. Now the phase inverter receives not only equal zero-signal voltages but equal low-impedance drive.

balancing adjustments

R10, R11, R12 and R13 in the gate circuit of Q2 allow one to adjust Q2 gate voltage between -1.1 V and +7.0 V. This is sufficient range to compensate for any parameter differences between Q1 and Q2.

C10 filters any transients which might appear at the gate of Q2 and slows power-supply fluctuation effects. All of which holds Q2 output constant so that the undriven terminal of the phase inverter represents apparent ground.

Longtail R16 is shunted by another balancing network. This network balances SF output resistance. Although R16 and R_S for the input SF (R3) equal, R16 returns to -15 V and R3 returns to approximately -14 V. A trigger pickoff circuit, not shown, develops V_{BB} for Q1. Trigger-pickoff part tolerances cause V_{CC} variation between units, and part replacements cause some variation. The result is an off-center zero-signal CRT display. With the signal input grounded, one adjusts R14 for a centered display.

Drain current controls gm; $\frac{1}{gm}$ is r_s; r_s has the greatest control of R_O; and longtailing sets drain current.

To show how R14 adjustments balance R_O, keep the above facts in mind and assume three conditions for Q1 V_{BB}:

1. $V_{BB} = -13$ V
2. $V_{BB} = -14$ V
3. $V_{BB} = -15$ V.

Under condition 1, Q1 draws 4.6-mA I_D. Q2 source voltage, set equal to Q1, establishes the voltage drop across R16 creating a demand for 5.4 mA. Apparently, Q2 draws 0.8 mA more I_D than Q1.

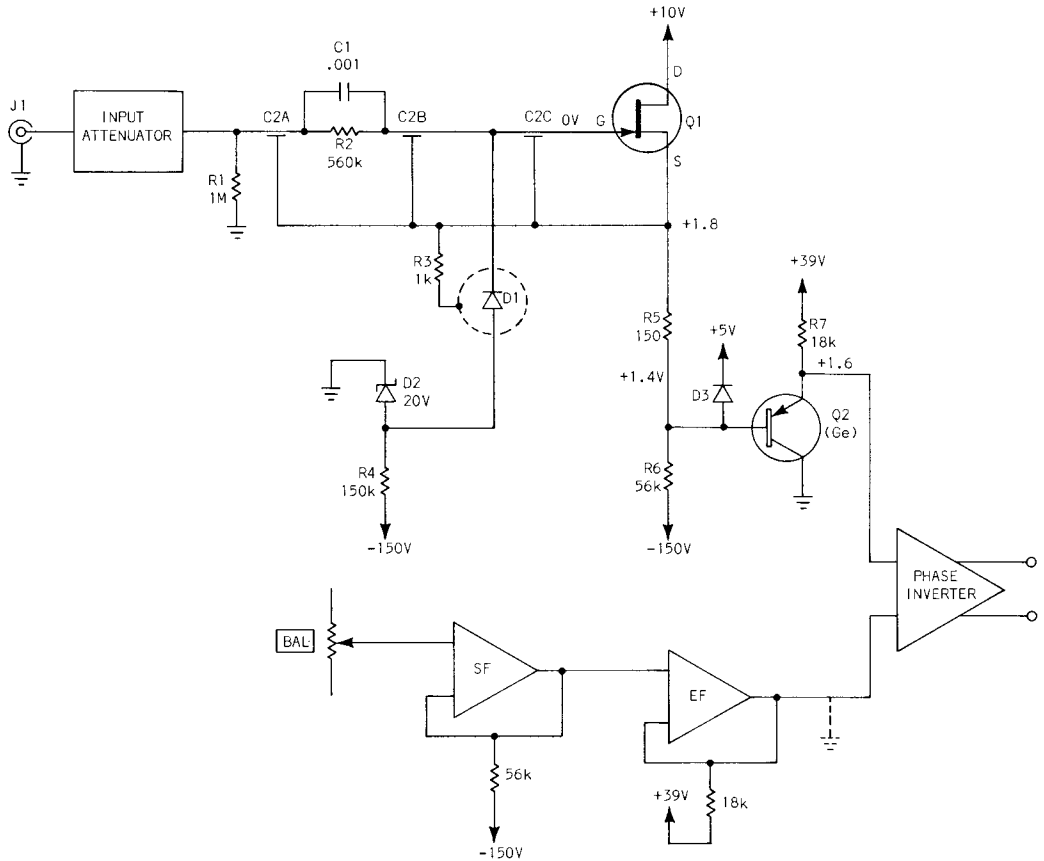


Fig. 3-99. Source follower replaces cathode follower as input amplifier.

Under condition 2, 5 mA flow through R3 and R16 draws 5.4 mA.

Under condition 3, both resistors draw 5.4 mA.

If the current through R16 flowed as Q2 I_D, Q1 and Q2 R_O would differ for conditions 1 and 2, but not 3. However, R14 and R15 shunt part of the longtail current so that Q2 I_D matches Q1 I_D.

4.5 mA is shunted with R14 set to +12 V, leaving about 1 mA to flow as Q2 I_D. Moving the wiper toward ground reduces shunt current which of course increases I_D for Q2. Zero-shunt-current demand occurs at some resistance value slightly above ground.

C11 with R15 decouple to prevent unwanted signals at the emitter-follower input.

input amp changed from CF to SF

Circuit complexity and high voltages usually identify amplifiers modified for source-follower instead of cathode-follower operation. This keeps total amplifier modifications to a minimum. Fig. 3-99 is an example. Q1 and the BALANCE source follower replace cathode followers. Following circuits, including emitter-follower drive to the phase-inverter, remain unchanged.

R1 forms a portion of the input attenuator and returns the gate of Q1 to ground.

R2 is a limiting resistor, bypassed by C1.

input capacitance stabilized and reduced

C2A, B and C are circuit-board strips circling connection terminals. This stabilizes the circuit-board dielectric, and returning C2 to the source, reduces input capacitance.

R3 ties the case of D1 to the source for the same reason -- stabilizes and reduces input capacitance. Capacitance from case to chip of D1 exists. Returning the case to a reference fixes the capacitance. And returning the case to the source reduces signal voltage across the device, thereby reducing capacitance.

protection

Protective circuit D1, D2 and R4 prevent gate-to-channel breakdown in Q1. Applying negative gate voltages which approach gate-to-drain breakdown (BV_{gs}) actuates this protective circuit. Zener diode D2 conducts through R4 to regulate the anode of D1 at -20 V. D1 clamps when gate voltage exceeds -20 V.

Signal voltages develop across r_{ds}, R5 and R6. Because of resistive values most of the input voltage develops across R6 to appear at the base of Q2.

limiting

Positive voltage across R1, exceeding about 4 V, causes both gate-limiting and source-clamping. Clamping and limiting interact. Assume a fairly "slow" positive-going signal develops across R1: The signal appears at the gate and source of Q1. Q1 source follows the input ascension until the R5-R6 connection raises 3.2 volts above quiescence. D3 now turns on because of +5.6 anode volts and +5 cathode volts. D3 clamps the base of Q2 and the source of Q1. As Q1 gate voltage continues to rise, the gate-channel diode becomes forward-biased. Limiting current flows through D3, R5, the source-to-gate channel resistance, and R2. The drop across R2 limits gate current.

test-circuit loading

Notice that during excess voltage application input resistance decreases. The shunt across the circuit under test consists of R1 paralleled by R2, gate-source resistance, R5 and D3. For slow voltage changes R2 approximates the additional load.

balancing phase-inverter drive

The BALANCE source follower and emitter follower are the same type active devices, set to the same operating point as Q1 and Q2. Thus the phase-inverter drive is quiescently balanced. The input voltages and impedances equal at quiescence. Input signals appear at the phase-inverter terminal via Q2. The other phase-inverter terminal remains biased at the quiescent level; therefore is an *apparent* ground. There is an exception: Thermal (source-follower) signals appear at both input terminals. They are of equal amplitude and phase, therefore cancel. This is why active devices and circuit configurations match.

Fig. 3-100 shows the BALANCE circuit. Q4 longtailed by R8 divides Q3 output impedance β times, just as Q2 divides Q1 output impedance. R9 and R10 equal R5 and R6 in the source of Q1. These matched components allow one to adjust Q3 gate voltage for a quiescent center-screen display.

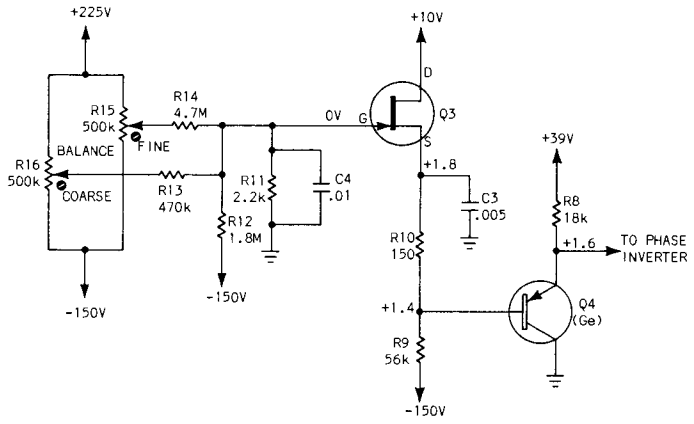


Fig. 3-100. Phase-inverter balance circuit.

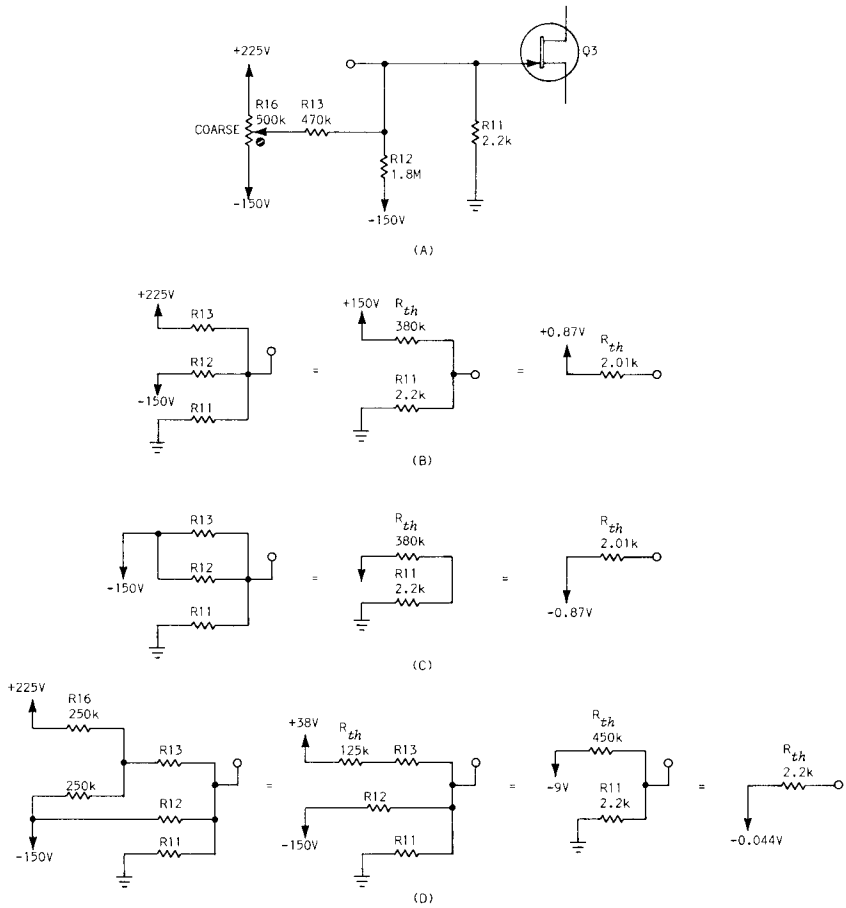


Fig. 3-101. Balance-adjust equivalent circuit.

C3 bypasses R_S to prevent switching transients from developing at the phase-inverter terminal. R11 and C4 filter transients in the gate circuit.

R11 in conjunction with R12, R13, R14, R15 and R16 establishes Q3 gate voltage. One sets this voltage for a "balanced" condition: A centered CRT vertical display at quiescence. To accomplish balancing, ground the vertical input jack, center the vertical POSITION control, and set R15 to mechanical center. Now adjust R16 for an approximately centered display; then set R15 for a display precisely centered.

Although gate supply voltages are quite high, adjusting R16 and R15 changes gate voltage in fairly small increments.

Fig. 3-101 develops the coarse BAL-adjust circuit equivalent including R11:

(A) is the circuit to be "Thevenized."

(B) shows that 2.01 kΩ returns to an equivalent +0.87 V with R16 set to +225 V.

(C) shows that setting R16 to -150 V develops an equivalent of 2.01 kΩ returned to -0.87 V.

(D) evolves the COARSE centered equivalent.

3-101A is the circuit to be "Thevenized."

3-101B shows that 2.01 kΩ returns to an equivalent +0.87 V with R16 set to +225 V.

3-101C shows that setting R16 to -150 V develops an equivalent of 2.01 kΩ returned to -0.87 V.

3-101D evolves the COARSE centered equivalent.

Now substitute the equivalent of Fig. 3-101D for R11, R12, R13 and R16 in the original circuit. This results in the Q3 gate circuit shown in Fig. 3-102A. Fig. 3-102B and C illustrate R15 extremes. Moving R15 from maximum positive to maximum negative changes Q3 gate voltage less than a volt. The fine BAL resistance is centered (Fig. 3-102D).

Centering both R15 and R16 creates the circuit shown in Fig. 3-102E. Gate voltage sets 2.5 millivolts below ground. Assume this is approximately zero volts, accounted for by part tolerances and computation errors. Further, small adjustments of R15 or R16, or both, zero the gate voltage.

input amplifier

The latter part of the emitter-follower section described an unusual emitter-follower configuration which resulted from a cathode follower to source-follower input-amplifier modification. Fig. 3-103 completes that input-amplifier schematic.

compensated voltage divider

Input DC voltages develop across R1, R2 and R3. C1 and C2 compensate this voltage divider for optimum pulse response. 98% of the input voltage develops at the gate of Q1A. R1 has negligible effect upon voltage division. It imposes losses between attenuator inductive components and C4 to prevent ringing.

limiting

C4 discharges stray capacitance, shunting R3, following gate limiting. R4 is the gate-limiting resistor. Because of such small gate current this circuit uses a large limiting resistance, R4.

test-circuit loading

Therefore, circuits under test which develop excessive voltages never work into a load greater than R3 paralleled by R4.

protection

D1 turns on, limiting negative voltages which exceed Q1A reverse-breakdown. When Q1A gate voltage becomes more than -12.6 volts, D1 turns on. D1 draws current through R1, R2, R4 and R6. This current added to that drawn by R3 loads the circuit under test.

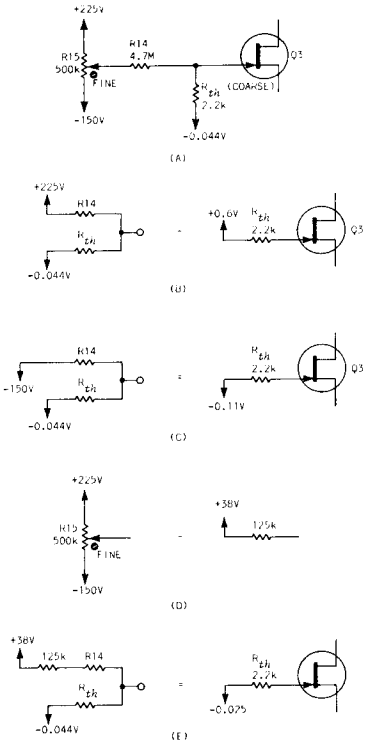


Fig. 3-102. Equivalent BALANCE circuits.

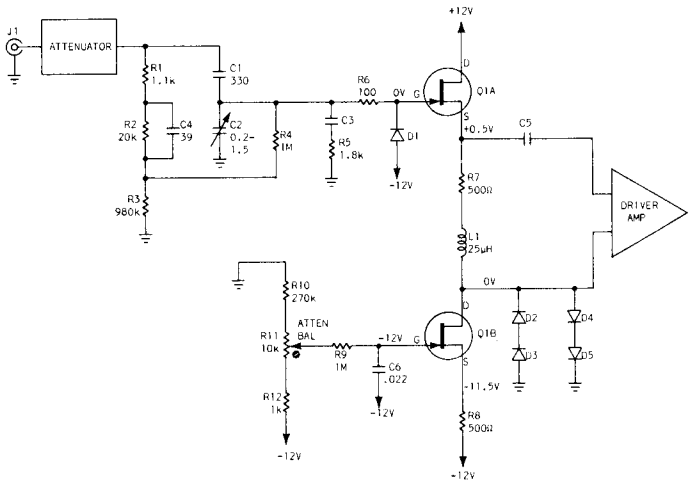


Fig. 3-103. Source-follower input-amplifier modification.

Positive-limiting initiates in the source of Q1A. When source voltage exceeds +1.2 V, D4 and D5 turn on, clamping the driver-amplifier input. Should Q1A gate voltage continue to ascend, the source-to-gate junction becomes forward-biased. Turning this diode on connects the input-limiting circuit to D4-D5 through R7.

L1 slows clamping action, either D4-D5 or D2-D3, during "fast" input voltages.

C1 discharges gate input capacitance upon removal of signal-voltage overloads, just as C4 discharges stray capacitance across R3.

C3 is circuit-board capacitance. Returning C3 to ground through R5 prevents "floating" capacitance. These components then provide negative-input-resistance compensation.

Negative-input-resistance characteristics receive two treatments: *Shunt RC* and a *suppressor*. R5-C3 shunt compensate and R6 is the suppressor.

thermal compensation

Q1 longtail configuration allows quiescent voltage to develop at the driver amplifier and Q1B connection, independent of temperature. One sets Q1B collector to zero quiescent volts. R8, Q1B, R7 and Q1A form a voltage divider between the -12 volt and the +12 volt supplies. If all divider impedances remain constant, Q1B drain voltage remains zero. This is the reason for using identical FET's in a common case: Q1 channel resistance changes with temperature. However, Q1B channel resistance always equals that of Q1A so voltage division remains constant.

Q1B drain voltage, or Q1A longtail current, results from the setting of ATTEN BAL, R11. R11 allows 0.5-volt adjustment at Q1B gate from about -12 to -11.5 volts.

Notice filter capacitor C6 returns to the -12 volt supply. This reduces the amplitude of any -12 volt power-supply fluctuations at the gate of Q1B. C6 also need have a small voltage rating since the source and gate return to the same supply.

Concepts presented in the follower series apply to amplifier concepts yet to be presented, and should be well understood before proceeding.

The following appendage is for those who work with Tektronix instruments and are unfamiliar with FET components.

Fig. 3-104 compares three-terminal active devices.

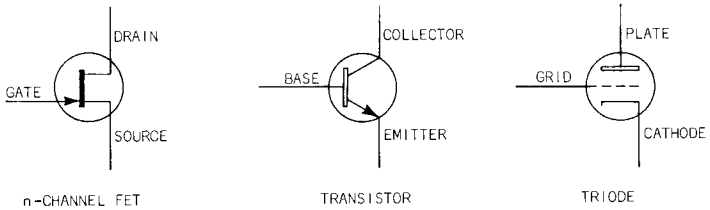


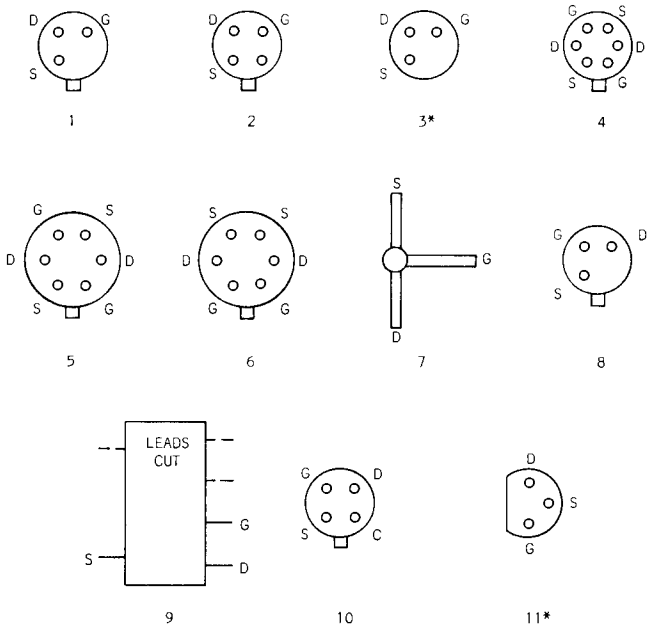
Fig. 3-104. Comparison of basic lead terminology of FET, transistor, and vacuum tube.

GROUP	TYPE	CHARACTERISTICS	HIGH-Z IN	LOW POWER CONSUMPTION	SMALL SIZE	LOW DRIFT	NOISE CHARACTERISTICS	SHORT WARM-UP TIME	SOLID-STATE RELIABILITY
PROBES	282	50Ω-TO-1MΩ ADAPTER	•	•	•	•			•
	P6045	DC-230MHz FET PROBE	•	•	•	•			•
	P6046	DC-100MHz FET DIFFERENTIAL PROBE	•	•	•	•			•
GENERAL PURPOSE PLUG-IN UNITS	1A1	DC-50MHz DUAL TRACE	•			•			•
	1A4	DC-50MHz FOUR TRACE	•			•			•
	1A5	DC-50MHz DIFFERENTIAL COMPARATOR	•			•			•
	1A7A	10μV/cm DIFFERENTIAL	•			•			•
	3A3	100μV/DIV DUAL DIFFERENTIAL	•			•			•
	81A	PLUG-IN ADAPTER	•						•
SPECTRUM ANALYZER PLUG-IN UNITS	1L5	50Hz-1MHz SPECTRUM ANALYZER	•			•			•
	3L5	50Hz-1MHz SPECTRUM ANALYZER	•			•			•
SAMPLING AND DIGITAL READOUT INSTRUMENTS	1S2	90ps TDR	•		•	•	•		•
	3S1	DUAL-TRACE SAMPLING	•		•	•	•		•
	3S2	DUAL-TRACE SAMPLING	•		•	•	•		•
	S1	350ps SAMPLING HEAD	•		•		•		•
	S2	50ps SAMPLING HEAD	•		•		•		•
	3S3	DUAL-TRACE SAMPLING PROBE	•		•	•	•		•
	3T2	RANDOM SAMPLING SWEEP	•		•	•	•		•
	230	DIGITAL READOUT	•						•
	568	READOUT OSCILLOSCOPE	•						•
PORTABLE INSTRUMENTS	323	DC-4MHz	•	•	•	•		•	•
	453	DUAL-TRACE 50MHz-SWEEP DELAY	•	•	•	•		•	•
MONITORS	410	PHYSIOLOGICAL MONITOR	•	•	•			•	•
TV INSTRUMENTS	520	VECTORSCOPE	•		•	•			•
DISPLAY UNITS	601	STORAGE DISPLAY UNIT	•						•
	602	DISPLAY UNIT	•						•
	611	STORAGE DISPLAY UNIT	•						•

Fig. 3-105. Tektronix FET utilization.

Fig. 3-105 lists major reasons for using FET circuits in production instruments.

Finally, Fig. 3-106 gives an FET basing diagram for Tektronix part-numbered FET's.



*PLASTIC
TO-18 -- 1,2,3,4,8,10,11
TO-5 -- 5,6
ALL DRAWINGS ARE BOTTOM VIEWS EXCEPT 9

TEKTRONIX PN	BASING NO	TEKTRONIX PN	BASING NO	TEKTRONIX PN	BASING NO
151-1001-00	9	151-1009-00	4	151-1018-00	10
151-1002-00	8	151-1010-00	4	151-1019-00	4
151-1003-00	4	151-1011-00	4	151-1020-00	4
151-1004-00	3	151-1012-00	2	151-1022-00	1
151-1005-00	3	151-1013-00	4	151-1024-00	10
151-1006-00	3	151-1015-00	2	151-1025-00	11
151-1007-00	4	151-1017-00	7	151-1026-00	3
151-1008-00	6				

Fig. 3-106. FET basing diagram.

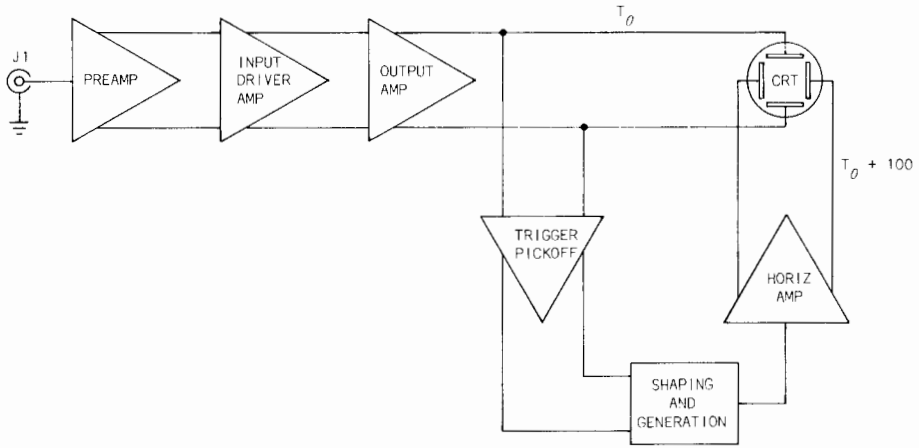


Fig. 4-1. Shaping and generation circuits add delay.

4

TRANSMISSION LINES

When one considers a transmission line as a means of conducting power between points, he may also consider any "black box" as a group of active devices cascaded with short transmission lines. This approach to electronics circuitry usually presents awkward problems for both writer and reader. On the other hand, a transmission-line approach gives the most direct and simple justification for some circuit components. Additionally, advantageous use of the transmission-line propagation velocity recurs again and again in vertical-amplifier design.

Power transits a transmission line at a rate determined by the type of line. This rate can be translated into time-per-unit length. Applying a signal simultaneously to short and long transmission lines of the same type, the signal out of the long line appears delayed in time from the signal out of the short line. Used in this fashion, the long transmission line is called a delay line.

delay line

THE USER MAY OBSERVE THE ENTIRE WAVEFORM THAT TRIGGERS THE HORIZONTAL SWEEP! This is one function of vertical-amplifier delay lines.

delaying factors

A waveform will not travel from input jack to CRT in zero time. Each lead is a transmission line with a velocity factor and each amplifier requires time to act. Circuits that generate, shape or switch add the most delay.

See Fig. 4-1. Assume time zero occurs at the trigger pickoff point. At T_0 the vertical signal appears at the CRT and a portion of the signal feeds the trigger circuits. Switching, shaping, generation and amplification take place before the horizontal sweep begins. The first 80 nanoseconds of the waveform cannot be observed unless the user selects a horizontal sweep slow enough to display at least two waveforms.

Amplification takes time. Fig. 4-2 suggests an improvement by cutting the time differential. But the user still cannot observe the leading edge by selecting a sweep speed which displays only one waveform.

Inserting delay of the vertical signal between the trigger pickoff point and the CRT solves the problem. Fig. 4-3 shows vertical deflection occurring 100 nanoseconds *after* horizontal sweep start. A sweep speed may be selected that expands the presentation to include only the leading edge of the triggering waveform.

NOTE: 80-nanoseconds horizontal delay merely illustrates delay and may or may not be representative.

Delay lines appear most anywhere along the vertical signal path, but the *trigger pickoff* must *precede* the delay line.

Fig. 4-4 shows a line terminated at each end to minimize reflections. Oscilloscopes are voltage activated, so an advantage is sometimes gained by terminating only one end for maximum power transfer as in Fig. 4-5.

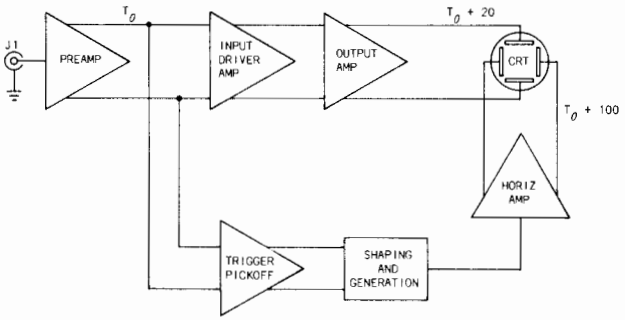


Fig. 4-2. Amplifiers impose less delay than shaping and generating circuits.

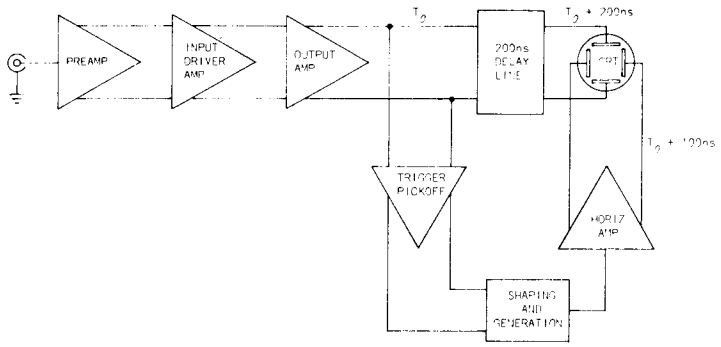


Fig. 4-3. Vertical signal delay allows horizontal sweep to initiate prior to vertical deflection.

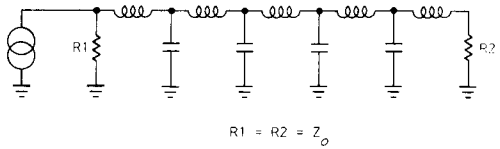


Fig. 4-4. Terminated transmission line.

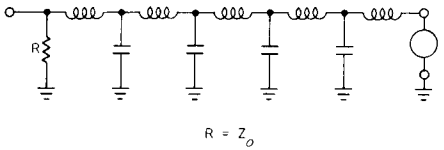


Fig. 4-5. Transmission line with single termination.

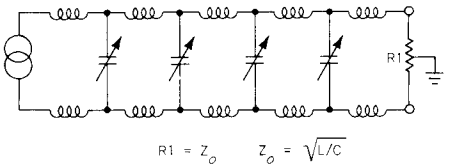


Fig. 4-6. An adjustable push-pull transmission line with single termination.

Lumped-constant transmission lines

Delay lines are driven push-pull and lumped-constant transmission lines must have each section adjustable to be effective (Fig. 4-6). Lumped-constant transmission lines make delay lines of usable bulk which have high impedances (1000-2000 Ω). This refers to the impedance across the line -- not from one side to ground.

There are disadvantages:

1. The time and skill necessary to adjust each section.
2. Lumped-parameter lines exhibit a bandpass which drops abruptly at F_c.

Not much can be done to reduce the adjustment chore. Optimum response requires precise proportioning of L, C and R components in each section. Further, the sections must match one another.

A lumped-parameter transmission line has a delay determined by values of L and C used. Changing either L or C changes line delay. For example: In both the horizontal and vertical amplifier of Fig. 4-7 a short lumped-parameter transmission line couples the driver-amplifier signal to the output amplifier. Capacitive components of both lines, made variable, gang for opposing effects. Maximizing C_V in the vertical, minimizes C_H in the horizontal. This gives a sort of teeter-totter time relationship between horizontal and vertical systems, allowing empirical phase adjustment. PHASING in this case is a front-panel control.

The scope in Fig. 4-7 was designed for X-Y display. Transient response is not considered of primary importance and the line is short. This merely

illustrates the relationship of L and C in a basic lumped-parameter line.

The basic explanation of transmission-line components follows the premise that these networks simulate properly terminated smooth lines. This states that Z_O remains constant over the frequency spectrum with no energy reflected. "Gaussian" response occurs only when velocity remains constant with frequency. Failure to maintain phase shift proportional to frequency ultimately distorts transient response. Transient response also suffers from any amplitude distortion as a function of frequency.

transient response distortion

Design of a lumped-parameter line represents the effort to make each section appear resistive over a broad frequency spectrum. The line-termination impedance should always match the Z_O of the lines.

m-derived filters

Research in this area led to the development of m-derived filters. $\sqrt{\frac{1 - \omega_c^2}{\omega_\infty^2}}$ establishes m where:

$\omega_c = 2\pi F_c = 1/\sqrt{LC}$

$\omega_\infty = 2\pi F_\infty$

F_∞ = angular frequency of peak attenuation.

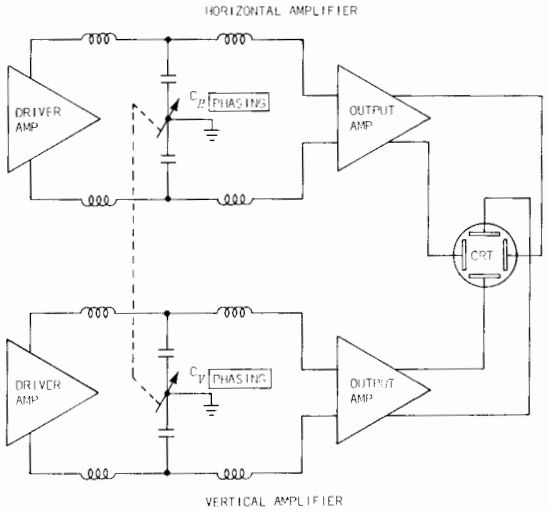


Fig. 4-7. X-Y phase adjustments.

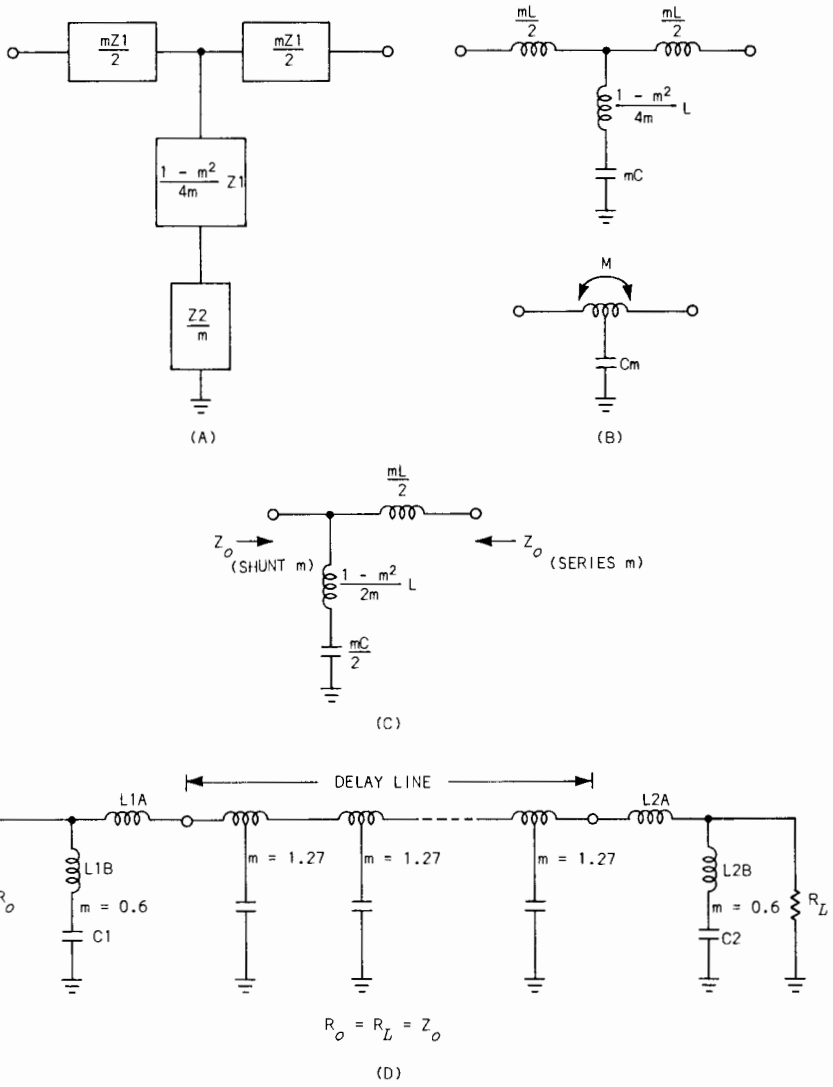


Fig. 4-8. Terminating a line consisting of m-derived sections with m-derived half sections.

reflections

Constructing lines from a chain or ladder of m-derived sections, terminated by an m-derived half section, virtually eliminates reflections as frequency varies. The sections may be constructed in either "T" or "π" configuration.

T-coil networks

Fig. 4-8 includes m-derived "T" models which receive treatment in a number of texts. Fig. 4-8A is the prototype model. The horizontal leg represents total series impedance and the vertical leg total shunt impedance. The counterpart appears in Fig. 4-8B. This circuit can be realized with a transformer having the proper amount of mutual inductance between series elements. Fig. 4-8B also contains the single-layer transformer which is the prototype equivalent. If one were to remove one-half of the series components and one-half of the shunt components, he would have an m-derived half section with exactly the characteristics of the original Fig. 4-8C.

Fig. 4-8D shows a delay line consisting of a ladder of m-derived sections terminated at either end by m-derived half sections. From a frequency standpoint, simple resistances, R_O and R_L, complete the termination satisfactorily:

$$R^2 = (Z_{\text{series m}})(Z_{\text{shunt m}})$$

From either end, the line appears to consist of an infinite number of m-derived sections. This fails as a close approximation for transient response. Therefore, terminations include reactances. These elements must then be carefully adjusted for optimum observed step response.

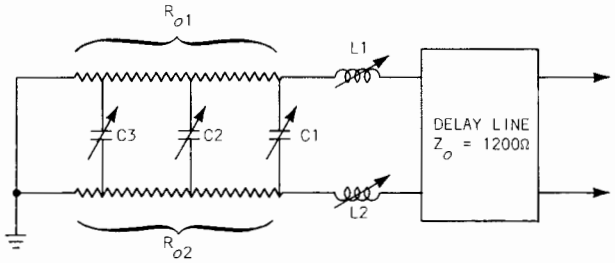


Fig. 4-9. Correcting for preshoot at the termination.

termination

When termination resistance (R_O) equals line surge impedance (Z_O), the line is properly terminated. Since Z_O varies in a lumped-parameter line, R_O must change with Z_O to properly terminate. Fig. 4-9 shows such a termination. At the lowest frequency component of a step waveform, DC, the termination functions as a pure resistance equal to Z_O. AC waveforms cause the termination to become reactive. R_O drops by the shunt value C2 and C3. Calibrating the reactances for optimum transient response creates an R_O that varies with Z_O.

L1, L2 and C1 represent m-derived half sections. One finds the m-derived structure used for delay lines, interstage coupling, and terminations. This is because the configuration offers a solution to the problem of delay variation with frequency. Proper selection of m creates the characteristic of constant group delay to quite high frequencies.

bridged T-coils

Bridged T-coils are an extension of m-derived sections. Under optimum conditions, a T-coil peaking network presents a constant resistance to an infinite number of frequencies. It also delays all frequencies linearly. A "perfect" transmission line presents a constant impedance to all frequencies. A T-coil peaking network is, therefore, one section of a lumped-parameter transmission line which simulates the smooth transmission line.

These circuits appear most frequently as amplifier output loads. This improves bandwidth over an RC-loaded amplifier developing the same gain. The formula. $\frac{1}{2\pi RC}$ represents RC-amplifier frequency

response. If input current remains constant, then output voltage varies with output impedance. Output voltage decreases to a 3-dB point when the output impedance decreases 30%. T-coil peaking extends the frequency at which the 3-dB point occurs.

T-coil peaking

With selected values a T-coil peaking circuit improves bandwidth by a factor of 2.74. Normally, $F_c = \frac{1}{2\pi RC}$. With optimum T-coil peaking $F_c = 2.74\left(\frac{1}{2\pi RC}\right)$ or $\frac{2.74}{2\pi RC}$.

T-coils, as components, make up only a portion of a T-coil circuit. Selected values of capacitance and resistance, added to a basic T-coil, complete the circuit. See Fig. 4-10. Here a coil, wound for the proper amount of mutual coupling is tapped halfway down its inductive length. A number of electronic texts describe this coil under the title "m-Derived Filters." Adding load resistance and capacitance makes the circuit more complete (Fig. 4-11). R1 and C1 have a direct relationship to the total inductance of L1. Normally, R1 and C1 values are known before determination of L1 and one other dependent variable, a bridging capacitor. The bridging capacitance depends upon the value of C1 and the coupling coefficient of L1.

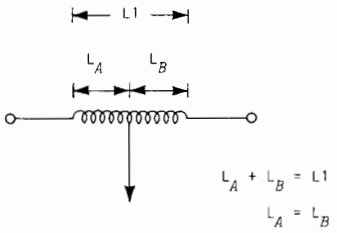


Fig. 4-10. Inductor tapped at electrical center.

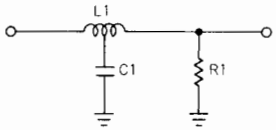


Fig. 4-11. Basic T-coil components.

Fig. 4-12 shows a completed T-coil circuit. With properly proportioned components, T-coil (L1), load capacitance (C1), load resistance (R1), and bridging capacitor (C2), the circuit defines an all-pass network. The impedance of the section equals R1 at all frequencies (ideal components).

series peaking

Useful bandwidth improvements between 2.6 and 2.8 result from application of T-coil techniques. Employing series peaking adds to the bandwidth improvement factor. See Fig. 4-13. Addition of L2-C3 improves bandwidth to a factor between 2.9 and 3.1. The LCR values must again properly proportion.

Circuit drive occurs at one of two points. Fig. 4-13 shows input drive at the junction of L2-C3 and output voltage taken across C1. Fig. 4-14 illustrates the alternate method. Input drive at C1-L1 develops output voltage across C3.

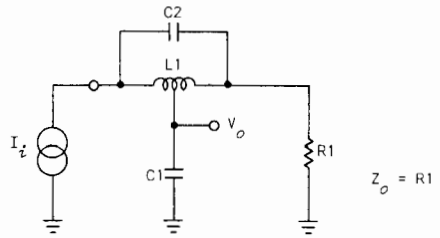


Fig. 4-12. T-coil circuit complete.

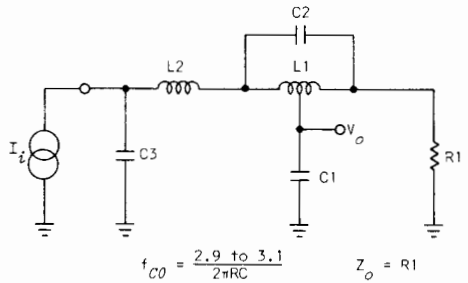


Fig. 4-13. T-coil with inductive peaking output taken across C1.

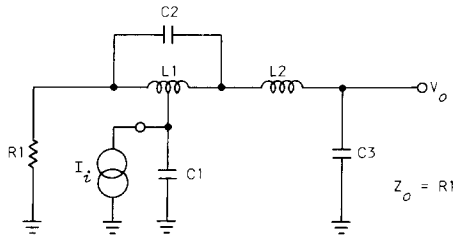


Fig. 4-14. T-coil with inductive peaking output taken across C3.

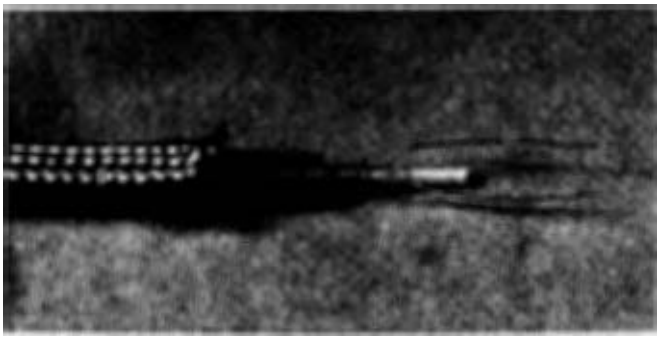


Fig. 4-15. Spiral-wound delay-line coax.

One encounters each of the circuits represented in Figs. 4-12, 4-13 and 4-14 in oscilloscope vertical amplifiers. The key to identification is coil configuration and resistance. Capacitances can be either components or distributed circuit capacitance. In any case, treat T-coil peaking as a transmission line terminated in its characteristic impedance.

coaxial delay lines

The transmission-line people didn't give up on coax delay lines. A superior delay line is manufactured using coaxial cable. The delay per foot has been increased by a factor of about 40, and the risetime characteristics improved. This cable is definitely *not* off-the-shelf or common coax.

The photo in Fig. 4-15 illustrates the method of spiral winding or braiding the two inner conductors in opposite directions about a common core.

Advantages include adjustment elimination, space and weight saving. Consider the following description: 140-nanosecond delay, 4.3-nanosecond risetime, 10-cubic-inch size and a fractional-pound weight! This is the package of Fig. 4-16.

Risetime does deteriorate with line length. Compare the approximate values listed below:

Delay Time	Risetime
140 ns	4.3 ns
170 ns	5.6 ns
195 ns	6.5 ns

Characteristic impedance is low, 93 Ω each side.

Oscilloscopes using vertical delay enable the operator to observe the leading edge of the waveform that triggers the horizontal sweep. Either a lumped-parameter or a fixed-tuned delay line may be used. If a fixed-tuned delay line is used it will be made of special coax and have a lower impedance than the lumped parameter.

Delay lines also function to establish phase coherence between parallel signal paths.

Unfortunately, no vertical-amplifier transmission line meets all requirements of impedance and phase. Several of the unfamiliar vertical circuits are attempts to optimize the balance between amplitude and phase distortion for better transient response.

evaluating vertical systems

Applying a complex waveform of known dimension as an input signal and observing the waveform dimension at the output, evaluates a vertical system.

Fig. 4-17 illustrates the use of a step waveform for vertical evaluation. Fig. 4-17A shows the unobtainable perfect system. A "perfect" step input results in a "perfect" step output.

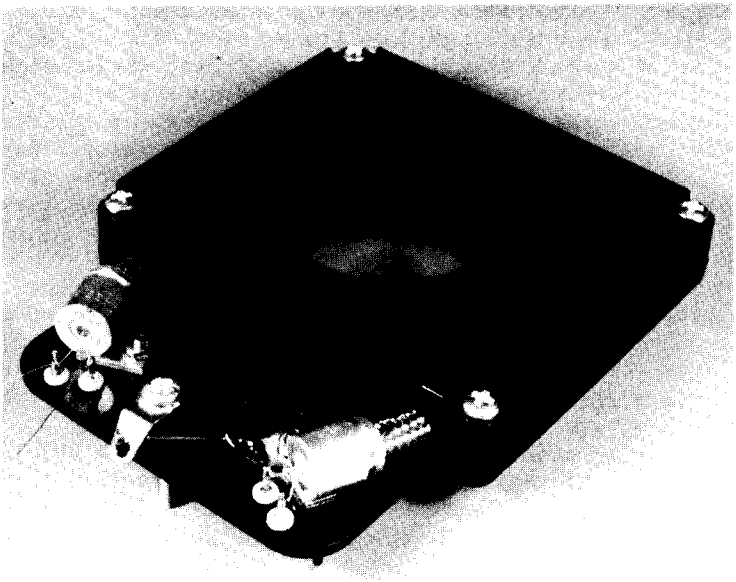


Fig. 4-16. Coax delay-line package.

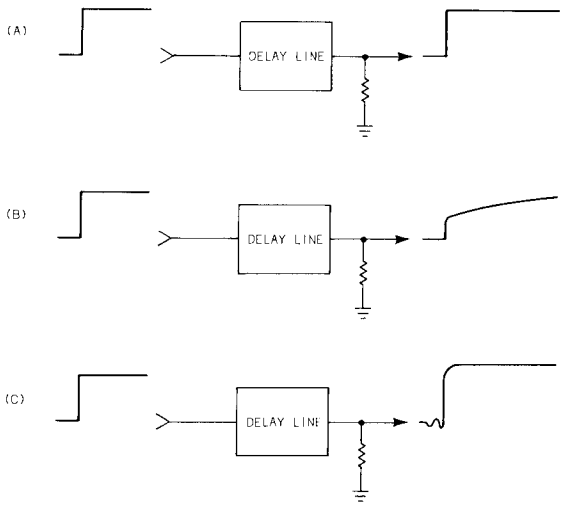


Fig. 4-17. Delay-line step response.

dribble-up

Fig. 4-17B represents a result known as "dribble-up." This is amplitude distortion. A "perfect" step drives the circuit. The resultant waveform steps a small amount then takes considerable time to reach full peak amplitude. Skin-effect, a transmission-line characteristic, causes high frequencies to be attenuated more than low frequencies. Rather than compensate at the termination for dribble-up, most vertical systems restore waveshape by following stage amplification. These amplifiers boost high frequencies and attenuate the lows to achieve overall system response.

Dribble-up is characteristic of coaxial and balanced shielded transmission lines. Naturally, the effect becomes more pronounced as line length increases. Therefore, delay lines constructed with either of these cable types impose dribble-up.

This does not apply to "special" coax, the inner conductors of which consist of a braided pair. Braiding introduces additional reactive components to what would have been a balanced shielded cable, increasing the delay per unit length. This "special" line imposes a velocity problem common to lumped-parameter transmission lines called

preshoot

"preshoot."

Fig. 4-17C presents this distortion. The name is derived from the illusion that the output circuit appears to anticipate energy arrival. Early arrival and algebraic summing of higher-frequency components cause preshoot. Higher-frequency components of the "perfect" step transit the line at a greater velocity than lower-frequency components.

The lumped-parameter line distorts because of sharp cutoff frequency (F_C), a characteristic smooth lines do not present. Networks constructed of L and C component sections in a chain or ladder pass frequencies below, but not above, F_C. F_C sets the point of abrupt change in phase velocity and Z_O. Variations of Z_O start considerably below F_C. Equations for Z_O and velocity appropriate for smooth lines also apply to lumped networks only at frequencies far below F_C.

T-coil use as delay-line termination helps eliminate preshoot. Fast-rise instruments which use the "special" coax delay lines develop preshoot as well as dribble-up. Amplifier boost or attenuation circuits correct dribble-up. Preshoot, however, results from unequal group delay which should be corrected as early as possible. Fig. 4-18 shows T-coil peaking applied to the line termination. Here three cascaded T-coil sections present an all-pass constant-resistance load. The 93-Ω terminating resistors are a part of the main vertical amplifier. None of the "T" networks attenuate an input signal. However, each section has an upper-frequency point, determined by part values, where signal delay occurs. Selection of component values causes section three to add delay to the lowest frequency component responsible for preshoot. Higher-frequency components encounter additional delay by sections two and three. All three sections delay the highest frequency components passed by the vertical delay line.

Inductors L1 through L4 and capacitors C1 through C6 correct for phase shift and cause the terminating impedance to equal Z_O at all frequencies.

resolving terminations

Complex terminations are not difficult to identify because of proximity to the delay line. When analyzing a circuit consider these terminations as merely extensions of the delay transmission line. Resistors, equal in value to nominal Z_O, usually

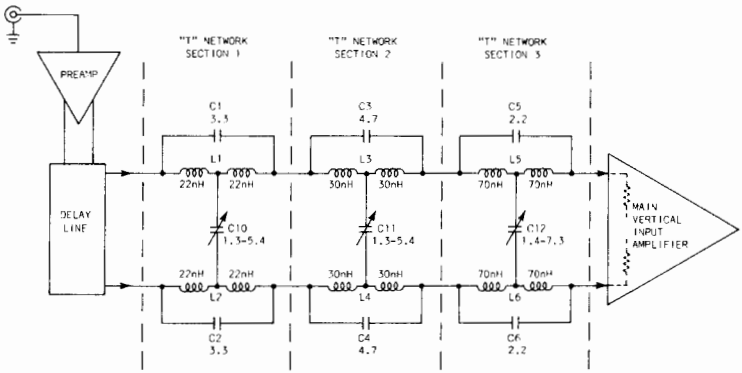


Fig. 4-18. Bridged T-coil compensation of the delay-line termination.

return the reactive termination to signal ground. Then Fig. 4-18 is a transmission line terminated in its characteristic impedance of 186 Ω (two 93-Ω resistors in the main vertical block).

Sometimes the resistive termination is not obvious. If one wishes to resolve the nominal termination impedance he still considers the DC resistance only. Fig. 4-19 illustrates a main vertical input amplifier driven, push-pull, by a preamplifier via the delay line. The main vertical input amplifier consists of an emitter follower with a complex input network for delay-line compensation and vertical-gain adjustment.

Typical push-pull drive is 100 millivolts per division. R11, common to push-pull current, functions as a bypassed resistor. 5 Ω approximates output impedance. R9-R10 are large compared to output impedance, so gain approaches unity.

Quite complex circuitry exists at the bases. All of the LCR network compensates and terminates the delay line. Termination for the delay line should match its characteristic impedance. Characteristic impedance for this delay line from one center conductor to the other is 186 Ω or from each center conductor to virtual ground, 93 Ω.

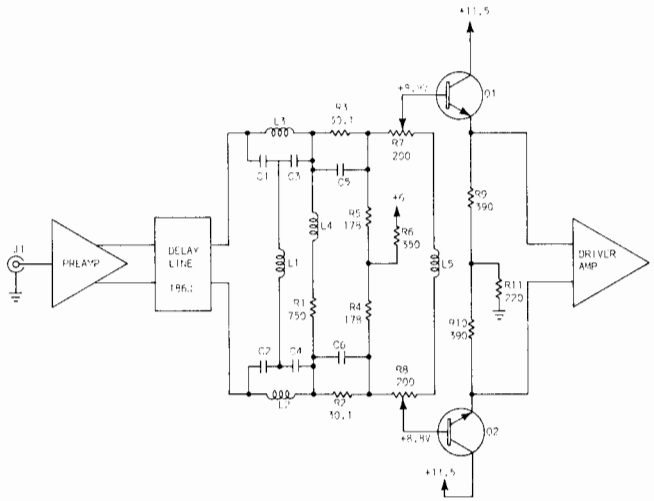


Fig. 4-19. Main vertical input amplifier.

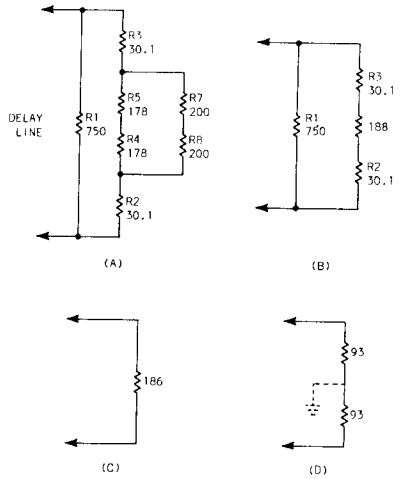


Fig. 4-20. Base circuit resistance of 4-19 equal to delay line Z_o.

R7 and R8, ganged, allow adjustment of vertical gain or deflection factor. Notice that these controls are not in the DC-current path. Adjustment at quiescence does not cause a vertical shift at the CRT.

R1 through R8, less R6, terminate resistively. R6 is a series dropping resistor for the preceding push-pull stage, thus the junction of R4-R5 becomes a common mode or virtual ground point. Fig. 4-20 step-by-step simplifies the resistive network. DC resistance matches the transmission-line surge impedance (Z_o).

interstage coupling T-coils

T-coils as interstage coupling networks should be treated as short sections of transmission line, terminated in Z_o.

Fig. 4-21 shows a series-peaked T-coil in the plate of V30. T-coil components consist of R35, L30, T31, L40 distributed and stray capacitance. Adjusting L30 proportions T-coil components.

The plate load for V30 is 1 kΩ. Assume the plate load consists of a transmission line terminated by a resistance (R35) equal to Z_O. Assume further that, with L30 properly set, Z_O remains constant and resistive over the circuit bandwidth.

One adjusts L30 for optimum step response as seen on the CRT.

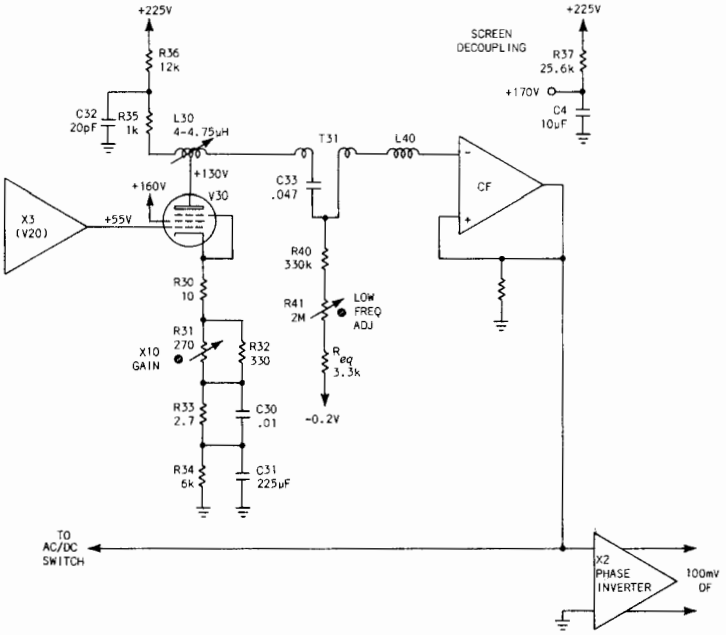


Fig. 4-21. Combination T-coil plate load.

T-coil drive occurs at one end of the coil as well as at the center tap. The impedance, Z_O, equals the terminator resistance. See Fig. 4-22. V2 drives a plate load of 1.2 kΩ (R2). Capacitances involved are V2 plate capacitance, shunt capacitance at the Driver input terminal, and L1 distributed capacitance. One empirically adjusts L1 for optimum LCR proportioning.

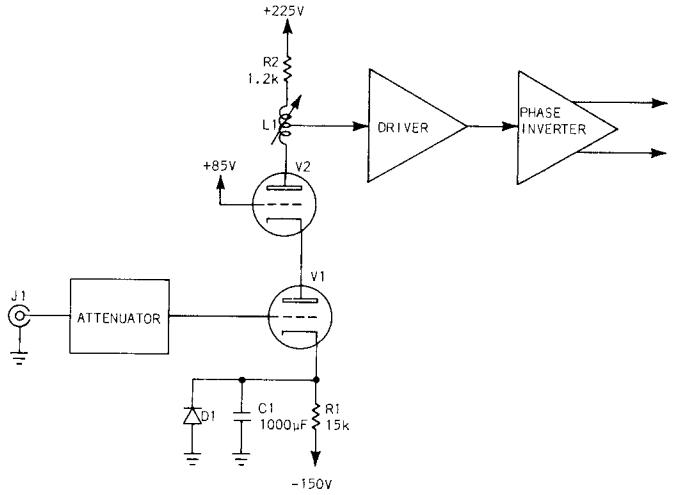


Fig. 4-22. Alternate T-coil connection.

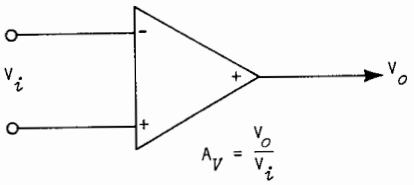


Fig. 5-1. Amplifier symbol.

5

SINGLE-ENDED AMPLIFIERS

If the signal amplitudes to be measured by an oscilloscope user always fell in the range of volts or tens of volts, the CRT might be driven by a single follower. The signal source could even drive the CRT plates directly. However, users require an oscilloscope to monitor millivolt amplitudes. Volts-per-division defines CRT deflection factors. Thus, a requirement for voltage gain exceeding unity for a vertical amplifier.

Vertical amplifier stages usually have a fixed sensitivity spoken of in terms of deflection factor. Proper selection of input attenuators maintains drive within the signal-handling capabilities of the amplifiers. Holding stage sensitivity constant allows the design to meet and maintain bandwidth requirements.

Stabilized to an optimum degree, an amplifier stage operation becomes almost independent of active device parameter changes. All circuits, in this chapter, are longtailed. Longtailing stabilizes an amplifier to a sufficient degree to consider the stage *virtually* independent of active device parameter changes. Following this line of reasoning one step further, one can assume that basic amplifier concepts parallel, without regard to active device type. The basic circuit components should bear the same relationship to one another whether the active device be tube, FET or transistor.

The three terminal triangle of Fig. 5-1 represents an amplifier. Input voltage, applied between the (-) and (+) input terminals, causes a voltage to develop at the (+) output terminal. The ratio output voltage (V_o) to input voltage (V_i) expresses voltage gain (A_V). These amplifiers may develop unity, less than unity or greater than unity gain.

Triangular symbols represent any number of complete amplifier stages. Polarity symbols relate terminal functions to those of a single stage:

Input (-)	represents a base, gate or control grid effect.
Input (+)	functions as emitter, source or cathode terminal.
Output (+)	denotes the collector, drain or plate.

Connecting the terminals to known circuit points identifies amplifier configuration. Grounding the (+) input terminal, as in Fig. 5-2, identifies the symbol as a common emitter, source or cathode amplifier. V_i, at the (-) input, causes signal current flow in the (+) input lead. This same current appears to flow in the (+) output lead.

Series current in the output and (+) input leads also occurs in common base, or gate, or grid, amplifiers. Fig. 5-3 shows this configuration. Signal voltage, applied to the (+) input lead, creates (+) input current which also flows in the output.

amplifier attempts to maintain input null

Both configurations react to signal voltages in a like manner. Input voltages develop *across* the input terminals to create signal current flow. Current quantity and net polarity, for a given

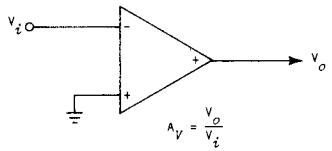


Fig. 5-2. Common emitter, common source or common cathode amplifier.

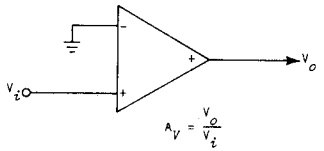


Fig. 5-3. Common base, common gate or common grid amplifier.

amplifier, depends upon signal deviation from input quiescence. These amplifiers react to input voltages by *attempting* to maintain quiescent voltage across the input terminals. The action is a current change of the net polarity and quantity necessary to maintain signal voltage nulls across the input terminals. An absolute null never happens. How closely an amplifier approaches an input signal null depends upon passive device configuration and active device capabilities. However, all amplifiers *attempt* to maintain quiescent voltage across the input terminals.

The common emitter model of Fig. 5-4 reacts as described to zero, positive and negative signal

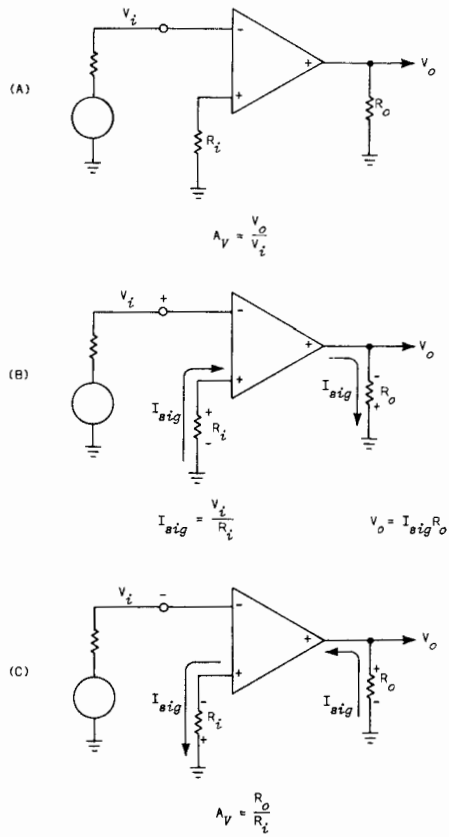


Fig. 5-4. Common emitter, common source or common cathode signal current flowing through R_o and R_i in series.

voltages. Fig. 5-4A is zero signal volts condition. This model includes gain determinates, input resistance (R_i) and output resistance (R_O). Zero V_i develops no signal current demand. Voltage between input terminals represents quiescence.

A + V_i appears at the negative input terminal in Fig. 5-4B. Input signal current (I_{sig}) now flows through R_i. To maintain the null across input terminals I_{sig} must drop V_i across R_i. I_{sig} flows into the (+) input terminal and out the (+) output terminal. Because this current flows through output resistance (R_O) and develops output signal voltage (V_O), gain computations now become exercises in Ohm's Law:

$$A_V = \frac{V_O}{V_i} = \frac{R_O}{R_i}$$

$$A_V = \frac{V_O}{V_i}$$

Substitute in the original gain formula:

$$V_O = I_{sig}\ R_O,$$

$$V_i = I_{sig}\ R_i$$

Substitute in the original gain formula:

$$A_V = \frac{V_O}{V_i}$$

$$A_V = \frac{I_{sig}\ R_O}{I_{sig}\ R_i}$$

$$A_V = \frac{R_O}{R_i}$$

The model in Fig. 5-4C includes the ratio R_O to R_i as an expression of voltage gain. This drawing also shows V_i as negative.

The resultant signal current flows through R_O, developing V_O; into the (+) output terminal out of the (+) input terminal, through R_i to ground, developing V_i across R_i.

Compare Figs. 5-4A, B and C for key points:

1. No current flows in the (-) input lead, indicating high input impedance or low signal source loading.
2. V_o develops out-of-phase with V_i.
3. Signal current quantity depends upon V_i amplitude and R_i. E = IR.
4. The ratio of output voltage to input voltage expresses true voltage gain. The same figure results from the ratio R_o to R_i.
5. The resistive ratio expresses voltage gain only because the amplifier tends to maintain a voltage null across input terminals.

component or function identification

This is a very simple analysis method once you identify components or functions. Identification problems include, ground, *net* signal current, R_i and R_o. Keep in mind that this method answers the how and why of functioning amplifiers. It does not satisfy the needs of new circuit design!

When is ground common? Response takes the form of another question: To what? There are three ground definitions:

actual ground

1. *Actual ground*, the common power supply return, most often the chassis. Actual ground functions as the common for all voltages, AC or DC.

apparent ground

2. *Apparent ground*, any point in the circuit which presents a low impedance to actual ground, thereby shunting signals to actual ground. Power supplies and filter capacitors represent apparent ground. For example, well-regulated collector, drain and plate supplies are apparent ground to both DC and AC signals. And filter or by-pass capacitors, returned to actual ground, establish apparent ground points for AC.

virtual ground

3. *Virtual ground* is much less obvious than either actual or apparent ground. Virtual ground appears more because of signal drive than any other factor. A virtual ground example appears in Fig. 5-5. Two voltage sources generate equal-amplitude, opposite-phase signals. The generators work into a common load, R_L. Since equal-amplitude opposite-phase signals develop across R_L, zero volts sets half-way along the resistive length of R_L. The midpoint of R_L remains zero volts, *virtual ground*, as long as the voltage ratio remains and phases oppose. Virtual ground would develop somewhere along R_L even if the signals were unequal amplitude, but opposite phase, as long as the amplitude ratio remained fixed.

   Fig. 5-6 illustrates unequal-amplitude opposite-phase signals developing virtual ground. The voltage across R_L always exceeds the output of G2 by 3. Therefore virtual ground sets 1/4 of the resistive length of R_L above the negative connection. The voltage ratio remains 1/4:

$$\frac{10\ V}{10\ V + 30\ V} = \frac{10}{40} = \frac{1}{4}$$

$$\frac{40\ V}{40\ V + 120\ V} = \frac{40}{160} = \frac{1}{4}$$

$$\frac{30\ V}{30\ V + 90\ V} = \frac{30}{120} = \frac{1}{4}$$

$$\frac{5\ V}{5\ V + 15\ V} = \frac{5}{20} = \frac{1}{4}$$

Virtual ground occurs most frequently in the differential amplifier family, (push-pull, phase inverters and comparators) and fed-back amplifiers. Actual and apparent grounds appear in all amplifier configurations. The standard ground symbol represents any or all signal grounds in simplified models.

net signal current

Net signal current is an artificial term which permits the simple amplifier model to work. For instance, current in longtailed amplifiers never drops to zero and never changes direction of flow. However, a measurable *change* in current does occur. The *change* in amplifier current is net signal current quantity. The quantity of change determines the apparent (net) direction of signal current flow.

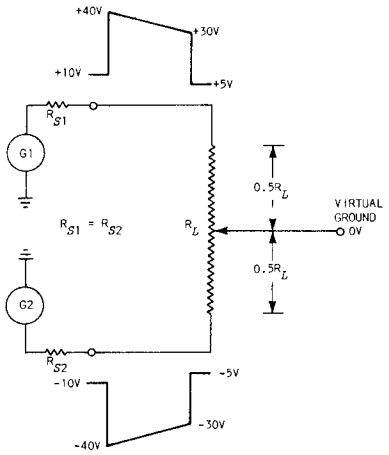


Fig. 5-5. Virtual ground.

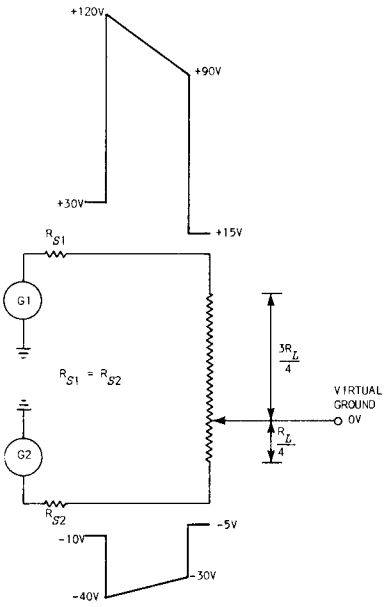


Fig. 5-6. Virtual ground.

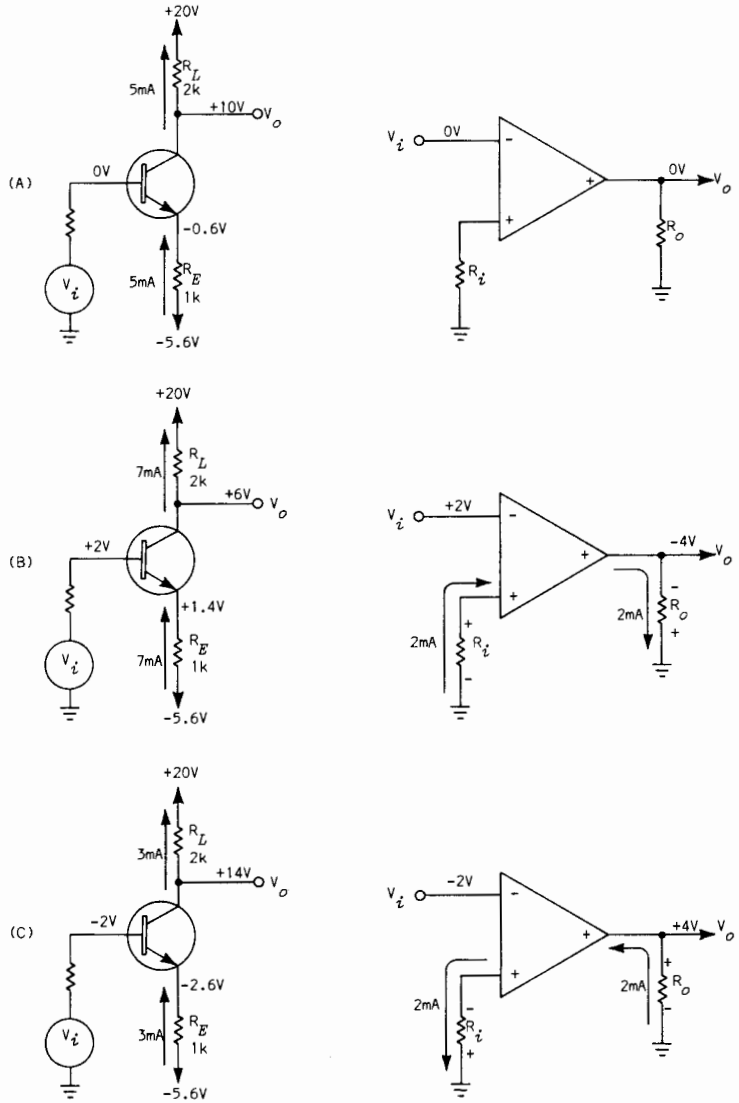


Fig. 5-7. Common emitter amplifier with simplified model.

Fig. 5-7 compares actual to net current flow. Fig. 5-7A is the quiescent state. The signal generator applies 0 base volts. Since this is an NPN transistor, and R_E returns to a negative voltage, the transistor is on. The emitter sets one junction below the base, 0.6 V for silicon. Therefore the device draws 5 mA emitter current at quiescence. Assume total emitter current flows as collector current. Collector current then drops 10 volts across R_L. V_O sets, quiescently, at +10 V. The adjacent amplifier model represents this quiescent condition: 0 V_i, 0 V_O and no current flow through R_i and R_O.

+2 volts V_i appear at the base in Fig. 5-7B. Emitter current increases to maintain 0.6 volts between base and emitter. This increased current flows through R_L dropping 14 volts. V_O decreases 4 volts, from +10 V to 6 V. The adjacent model shows this as a net current of 2 mA flowing into the (+) *input* terminal. Signal current flows from ground through R_i, developing V_i across R_i. This current then flows out of the amplifier, through R_O to ground. A negative V_O results. -4 volts V_O resulted from +2 volts V_i.

Fig. 5-7C shows amplifier reaction to a negative input. -2 volts V_i drops emitter voltage to -2.6 V. This represents an emitter current demand of 3 mA to maintain 0.6 base to emitter voltage. 3 mA collector current allows V_O to rise to +14 volts. The model shows this as a signal current phase reversal. Current flows out of the (+) input, developing V_i across R_i. *Net* current flows from ground, through R_O, into the (+) output terminal. +4 volts V_O results from -2 volts V_i.

Model net current began at zero, became 2 mA positive, then 2 mA negative. Emitter current began at 5 mA, increased to 7 mA then decreased to 3 mA. Both show a change of 4 mA.

The description of Fig. 5-7 applies to NPN common emitter, "n" channel common source, and common cathode amplifiers. Changing the active device to PNP or "p" channel doesn't change the concept but does change direction of active device current.

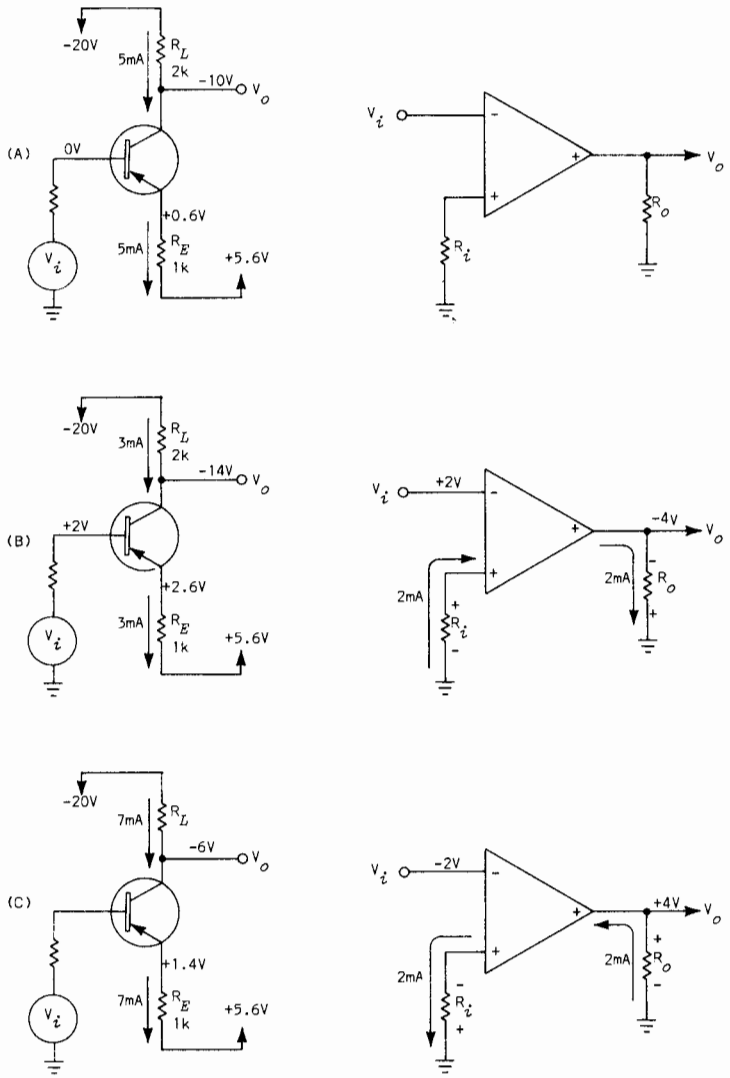


Fig. 5-8. Common emitter amplifier with simplified model.

Fig. 5-8 demonstrates differences and similarities. Active device current flows from collector to emitter, opposite to the direction of flow in the NPN device. For this device current decreases rather than increases with positive V_i and negative V_i causes an increase rather than a decrease in emitter current. However, the output voltage *change* remains the same.

The *net* model current changes the same, no matter the active device type.

Firmly implant the idea that net current direction can be contrary to actual circuit possibilities. Acceptance of this concept eases understanding of complex circuits in chapters to come.

If one were to apply information thus far presented to Fig. 5-7 and 5-8, he would deduct an implied definition of R_i and R_o: That R_E and R_i equal as do R_L and R_o. This is a close approximation only when the active device is a transistor and R_E is large. Recall, from the follower chapter, that input voltages develop across R_E or R_S or R_K in series with an internal component R_t, or r_{sd}, or r_k. R_i consists of R_E in series with R_t, or R_S in series with r_{sd}, or R_K in series with r_k. R_i then varies somewhat with active device configuration.

Consider first the common emitter amplifier as shown in Fig. 5-9. This is the classic basic circuit, an active device and a single passive device. The circuit equivalent shows input impedance as βR_t.

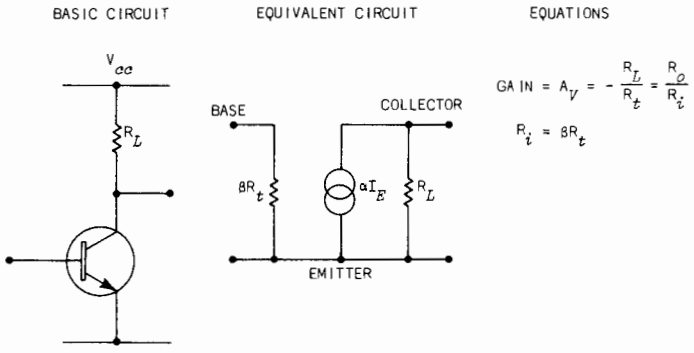


Fig. 5-9. Common emitter.

Input voltages across this impedance cause device current flow, from emitter to collector. An equivalent current generator represents emitter-to-collector effect. R_L is total external collector load.

Assume R_L is R_O and only external components determine R_L. Internal collector impedance (r_c) exists, shunting R_L. But, it is quite high compared to R_L. Due to a number of reasons, among them thermal noise, R_L seldom exceeds 20 kΩ.

The large value of r_c indicates that changes in collector current, voltage or impedance negligibly affect emitter conduction. R_t defines emitter conductance and, in this case, R_i. A_V is $\frac{R_O}{R_i}$, which is $\frac{R_L}{R_t}$.

The follower chapter presented "transresistance-resistance" (R_t). It consists of dynamic emitter resistance, r_e summed with reflected resistance, R_r. $R_t = r_e + R_r$. $\frac{26}{I_e(\text{mA})}$ establishes r_e. R_r, here, is base-spreading resistance, R_b divided by beta.

To identify useful values for R_i one needs a more complete circuit. The simplified model of Fig. 5-10 serves this purpose. $\frac{V_O}{V_i} = \frac{R_O}{R_i}$ expresses voltage gain. $R_L = R_O = 2.5$ k . However, R_E alone is not R_i. R_i consists of $R_E + R_t$. One need, therefore, to solve for R_t:

$$R_t = r_e + R_r.$$

$$r_e = \frac{26}{I_e(\text{mA})} = \frac{26}{2.8} = 9.3\ \Omega$$

R_r must include base resistance (R_B), as well as base spreading resistance (R_b).

$$R_r = \frac{R_B + R_b}{\beta} = \frac{1\ \text{k}\Omega}{50} + \frac{R_b}{50} = 20\ \Omega + \frac{R_b}{50}$$

$$R_t = r_e + R_r = 9.3\Omega + 20\Omega + 2.7\Omega = 32.0\Omega$$

Estimate a value for $\frac{R_b}{\beta}$ not to exceed 10 Ω. The value 2.7, chosen here, causes the R_t sum to be an

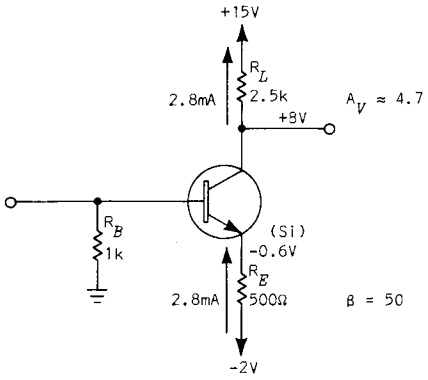


Fig. 5-10. Common emitter amplifier with more realistic component values.

even number, 32. 0.7 would work as well. Should $r_e + \frac{R_B}{\beta}$ be 30, $\frac{R_b}{\beta}$ would have been ignored -- assigned a value of zero.

$$R_t = 32\ \Omega$$

$$R_i = R_E + R_t = 532\ \Omega$$

$$A_V = \frac{R_O}{R_i} = \frac{2.5\ k\Omega}{.532\ k\Omega}$$

$$A = 4.7$$

Minimizing R_t allows R_E to represent R_i for useful gain approximations. Current driving the emitter (longtailing) reduces R_t but, more significant reductions occur when low impedance circuits develop signals at the base.

Longtailing implies large R_E and/or I_E values. Doubling I_E, of Fig. 5-10 reduces R_t from 32 Ω to about 26 Ω. This would increase gain to 4.75. Doubling R_E and R_L would increase gain more than doubling I_E.

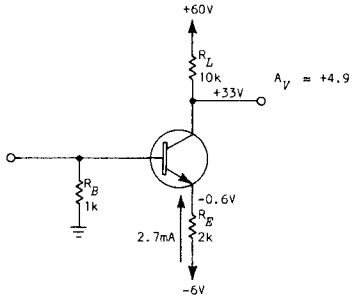


Fig. 5-11. Larger values of R_E allow $\frac{R_L}{R_E}$ to approximate voltage gain.

Fig. 5-11 shows gain approaching 5 by increasing R_E and R_L by 4. Gain of over 4.9 does approximate 5 closely enough for most purposes. However, lower R_L and V_{cc} values are preferred.

R_B prevents emitter circuit changes from affecting gain to a greater degree. R_B reflects 20 Ω into the emitter in all examples given. The model of Fig. 5-12A has a lower R_t than the original circuit, even though emitter and collector circuits are identical. Base impedance cannot exceed the follower output impedance. Follower configuration then determines the ohmic value of R_B.

Emitter follower coupling, Fig. 5-12B, presents minimum base resistance. 10 Ω represents a nominal output impedance. In this case ignore R_B:

$$R_t = r_e + R_r$$

$$r_e = \frac{26}{2.8} = 9.3\ \Omega$$

$$R_r = \frac{R_b}{\beta} = 0.7\ \Omega$$

$$R_t = r_e + R_r = 10\ \Omega$$

$$A_V = \frac{R_o}{R_i} = \frac{2.5\ k\Omega}{.51\ k\Omega} = 4.9$$

$$A_V \approx 5 = \frac{R_L}{R_E}$$

Cathode followers (Fig. 5-12C) present higher output impedance. The CF equivalent shown would not appreciably raise A_V. It still approximates 5. However, cathode follower output impedance increases with tube aging and filament power must be provided.

The source follower allows solid-state continuity and reliability, but reduces R_B less than other follower types.

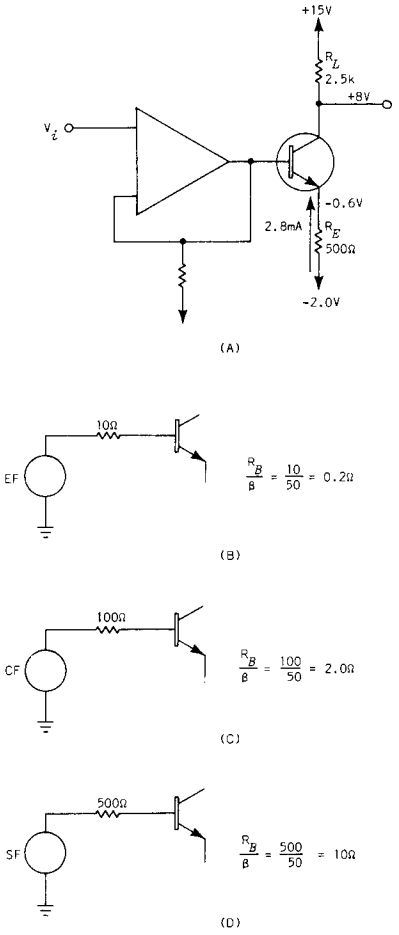


Fig. 5-12. Follower base drive reduces R_i.

Frequently one sees a cathode or source follower and an emitter follower cascaded to drive a common emitter stage. This presents the high impedance of a CF to input circuits and the low output impedance of an EF to the base of the common emitter amplifier.

thermal current

Low impedance base drive aids temperature stability in a somewhat indirect manner. For a given ratio of R_L to R_E, resistances can be kept low. Figs. 5-11 and 5-12 are comparative examples. Assume an EF drives the circuit in Fig. 5-12. Transistors are thermally unstable devices. A portion of the emitter current always consists of temperature-induced current. At room temperature, low power germanium devices contain from one to several μA thermal current. Silicon devices contain only fractional μA. This current increases with temperature. Thermally induced current, in germanium types, approximately doubles for each 10°C increase. Silicon doubles, approximately, for each 6°C increase. Thermal current change represents an unwanted signal. Thermal signals show up as a slow change approaching DC, and carry the name *thermal drift*. Capacitive coupling contains thermal drift within a given stage. This isolates operating-point changes and gives protection against self-destruction to the individual stage.

thermal drift

Oscilloscope circuits most frequently amplify DC, making direct coupling necessary. In this case thermal signals are amplified just as the wanted signals. Thermal conduction of one stage affects all following stages of direct-coupled amplifiers. One method of improving thermal characteristics uses heat sinks to maintain device temperatures at a low level. Passive component selection can combat the effects of thermal agitation.

The large value R_B and R_E in Fig. 5-11 degenerate thermal signals but the relatively high voltage across the transistor aggravates temperature effects. R_B reflects so much resistance into the emitter circuit that R_L and R_E have to be large so that the ratio R_o to R_i will approximate 5. This creates an advantage. Temperature increases raise emitter current which, in turn, increases the drop across R_E, reducing forward bias. A portion of emitter current flows as base current, $I_B \approx \frac{I_E}{\beta}$. Base current flows through R_B further reducing forward bias. Reducing forward bias, of course, reduces I_E.

This feedback action tends to maintain I_E constant over reasonable temperature ranges.

Raising the resistance of R_E would increase temperature stability, since smaller I_E changes would affect larger bias changes. However, there are disadvantages. To maintain voltage gain, R_L must increase proportionally. Increasing R_E and R_L demands higher supply voltages. This tends to nullify one semiconductor design advantage. Further, the transistor must dissipate more power as the voltage across the device increases:

$$P = EI = 33(27 \times 10^{-3}) = 89 \text{ milliwatts.}$$

Finally, the large R_L develops given output voltages during small (thermal) current changes:

If $\Delta I_e = 1$ μA

then

$$\Delta V_o = 1 \text{ μA } R_L = 1 \times 10^{-6} \times 1 \times 10^{4} = 10 \text{ mV.}$$

Developing the comparison backwards, the amplifier of Fig. 5-12 develops but 2.5 mV for each μA of thermal emitter current change. Quiescent power dissipation (EI) is also less because of the voltage across the device: $P = EI = 8(2.8 \times 10^{-3}) = 22$ mW, vice 70 mW. These are the major thermal advantages of the amplifier of Fig. 5-12. Adding these to the lower voltage supply requirements causes the circuit of Fig. 5-12 to be preferred.

Determining transistor amplifier gain is fairly simple: Let $A_V = \frac{R_O}{R_i}$. R_L can approximate R_O and R_E can approximate R_i. Solving for R_t tests the validity of $\frac{R_O}{R_i} = \frac{R_L}{R_E}$. To approximate R_t one assumes two constants for all transistor types: $\beta = 50$ and $r_e = \frac{26}{I_e(\text{mA})}$. He also assigns a rather arbitrary value to $\frac{R_b}{\beta}$ between 0 and 10 Ω. Finally he adds $\frac{R_b}{\beta}$. $R_t = r_e + R_r$. If $R_E + R_t$ changes R_E only slightly, ignore R_t! Assume $R_i = R_E$.

Assume $R_L = R_O$ when R_L is less than 20 kΩ. This will seldom be exceeded due to power supply and thermal considerations.

Common source amplifiers require some knowledge of one device characteristic, transconductance (gm). Fig. 5-13 shows the basic and equivalent circuits. Input voltage, applied to the gate, causes current flow through external source resistance (R_S), the channel (r_{sd}), and external load resistance (R_L) in series. FET drain resistance (r_{sd}) is high, comparable to r_o, thus R_L consists of external components only. $R_L \simeq R_O$.

$\frac{R_O}{R_i}$ defines voltage gain here also. R_i appears in the source as the sum of R_S and r_{sd}.

Knowing gm solves r_{sd}. $r_{sd} = \frac{1}{gm}$. If gm is unknown, assign gm value of 2000 μmhos -- an r_{sd} of 0.5 kΩ.

$$A_V = \frac{V_O}{V_i}$$

$$V_O = I_{sig} R_L$$

$$V_i = I_{sig} (R_S + r_{ds})$$

therefore

$$A_V = \frac{I_{sig} R_L}{I_{sig} (R_S + r_{ds})} = \frac{R_L}{R_S + r_{ds}}$$

$$R_O = R_L$$

$$R_i = R_S + r_{ds}$$

$$A_V = \frac{R_O}{R_i}$$

Pentode common cathode amplifiers have some characteristics of the semiconductors. See Fig. 5-14. V_i, applied to the control grid causes plate current flow (I_p) through the cathode component and R_L in series. Because of high plate impedance (r_p) external components make up R_L which approximates R_O.

R_i is more complex. R_i consists of both external cathode resistance (R_k) and dynamic cathode resistance, r_k. Inverting transconductance (gm)

solves r_k. Transconductance states the quantity of plate current change caused by a given control grid voltage change, with all other factors held constant. The plate current (I_p) change indicates *gm*, or r_k, is a plate component which we place in the cathode. R_k, on the other hand, affects both screen grid *and* plate circuit parameters. *Plate efficiency* (n) modifies R_k so it can be considered in series with the other plate components.

plate efficiency

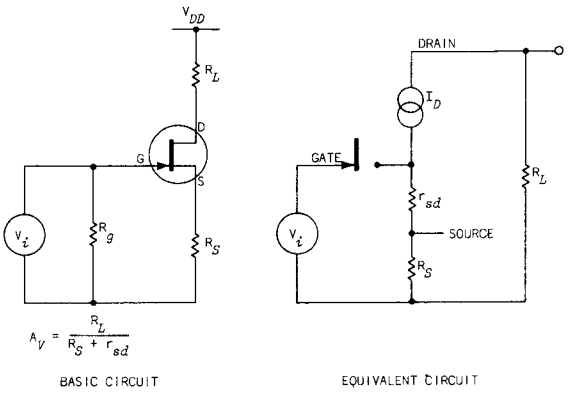


Fig. 5-13. Common source.

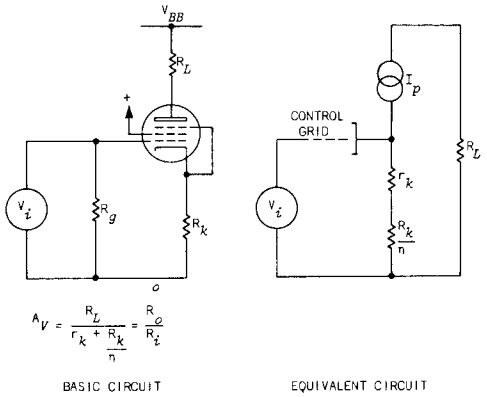


Fig. 5-14. Common cathode (Pentode).

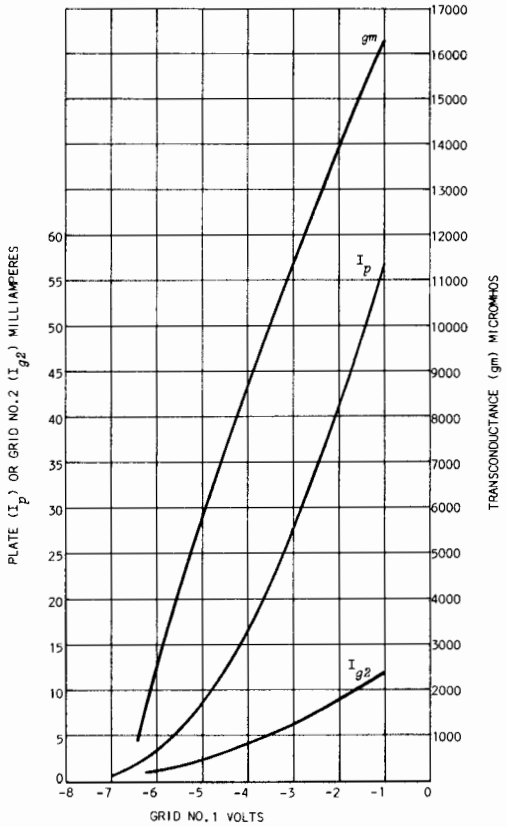


Fig. 5-15. Average characteristics of 12BY7-A.

Both screen grid current (I_{g2}) and plate current (I_p) flow through R_k. η is the percentage of cathode current (I_k) that flows as I_p. Called plate efficiency, η relates to the alpha of a transistor. Characteristic curves for a given pentode give the necessary information to determine η. First determine quiescent operating voltages, then apply them to the curves. The curves give I_{g2} and I_p. I_k is the sum of I_{g2} and I_p: $\eta = \frac{I_p}{I_k}$.

Assume 80% for η. The tube curves reveal that most pentodes yield an η between 70 and 95%. 80% is a good estimate for most circuit analysis. 80% η states that R_k, to the plate circuit, appears 25% larger than its component value. For example,

assume R_L = 5 kΩ, η = 80%, *gm* = 10 m mhos, and R_k = 2 kΩ. If, under these conditions, I_k changes, 80% of the change flows as I_p and 20% at I_{g2}. Assume I_k changes 5 mA:

$$I_p = \eta I_k = (0.8)\ 5 \times 10^{-3} = 4 \text{ mA}$$

$$I_{g2} = (1 - \eta)\ I_k = (0.2)\ 5 \times 10^{-3} = 1 \text{ mA}$$

I_k drops 10 volts across R_k:

$$V_k = I_k R_k = 5 \times 10^{-3} \times 2 \times 10^3 = 10 \text{ V.}$$

Considered in just the plate dimension, 10 volts across R_k changes I_p 4 mA; therefore R_k must have a resistance of 2.5 kΩ.

$$R = \frac{E}{I} = \frac{10}{4 \times 10^{-3}} = 2.5 \text{ k}\Omega$$

$$R_i = r_k + \frac{R_k}{\eta} = \frac{1}{10 \times 10^{-3}} + 2.5 \times 10^3 = 2.6 \text{ k}\Omega$$

$$A_V = \frac{R_\Omega}{R_i} = \frac{5 \times 10^3}{2.6 \times 10^3} \simeq 1.9$$

Fig. 5-15 shows a η of about 80% over a wide range of tube current: $\eta = \frac{I_p}{I_k} = \frac{I_p}{I_p + I_{g2}}$

At -1.2 V_{g1}, I_p = 55 mA and I_{g2} = 11 mA; $\eta = \frac{55}{66} \approx 83\%$.

At -4.8 V_{g1}, I_p = 10 mA and I_{g2} - 2.5 ma;
$\eta = \frac{10}{12.5} \approx 80\%$.

Besides constant plate efficiency, Fig. 5-15 points to the important relationship of *gm* and I_p. The *gm* curve almost parallels I_p. If one varies I_p he varies *gm*. It follows that holding I_p (thus *gm*) constant stabilizes gain. Longtailing allows only small changes in I_p (*gm*).

longtailing

Fig. 5-16 is an example of longtailing. I_k depends upon grid voltage, R_k and cathode return voltage. In this case R_k drops 150 volts establishing 4.6 mA I_k. This longtail holds *gm* fairly constant during signal processing. For example, 10 volts grid change creates 6.5% I_p change. Fig. 5-16 is the first step in developing a X10 amplifier with 10 mV input deflection factor. 10 divisions thus change tube current less than 1%.

Tube *gm* decreases with age. Longtailing minimizes the *gm* change, extending the useful life of the device. Longtailing also causes active devices of the same type to operate with similar parameters.

Negative feedback or degeneration imposed by longtailing stabilizes the amplifier at the expense of gain. R_O to R_i expresses voltage gain. R_O must exceed 400 kΩ for the circuit in Fig. 5-16 to develop A_V = 10. To prove this, and "build" a X10 vertical amplifier, consider circuit configuration then assume parameter values:

1. The amplifier will ultimately develop a gain of 10 with an input deflection factor of 10 mV/div, AC only.
2. R_L is R_O.
3. Plate voltage sets the operating point for the following direct-coupled amplifier. Relatively low plate voltage affects amplification (*gm*) far less than screen voltage.
4. Grounding the suppressor isolates plate circuit capacitance from other tube elements.
5. Screen grid voltage establishes basic *gm*. Returning the screen to a fixed voltage improves *gm* stability and reduces input capacitance.
6. Assume some rule-of-thumb values: r_k = 200 Ω, η = 80% and A_V = 10. Under these conditions, what resistance should R_L be?

$$R_i = r_k + \frac{R_k}{\eta} = 200 + \frac{33\ k\Omega}{0.8} \approx 41\ k\Omega$$

$$R_O = 10\ R_i \simeq 410\ k\Omega$$

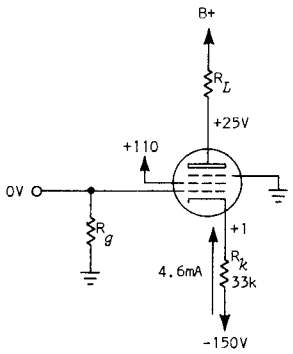


Fig. 5-16. Longtail stabilization.

410 kΩ is too large for at least two reasons: Unreasonable voltage supply required and risetime slow down. Also, the tube r_p must be considered for R_O to be this large. If r_p = 1.5 MΩ

$$\text{then} \quad R_L = \frac{r_p R_O}{r_p - R_O} - \frac{(1.5 \times 10^6)\ 410 \times 10^3}{(1.5-0.41)\ 10^6} \approx 550\ \text{k}\Omega$$

Since $I_p \approx 3.7$ mA and V_p +25 V then,

$$B+ = I R + 25 = (3.7 \times 10^{-3})\ (0.55 \times 10^6) + 25$$
$$= 2060 \text{ volts.}$$

Output risetime must also be considered: $t_r = 2.2\ RC$, assume output capacitance = 20 pF.

$$t_r = 2.2\ R_L C_O = 2.2\ (0.410 \times 10^6)\ (20 \times 10^{-12})$$
$$= 18\ \mu\text{s}.$$

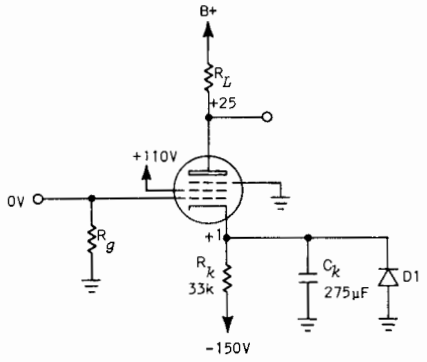


Fig. 5-17. Bypassing R_k reduces "fast" signal R_i.

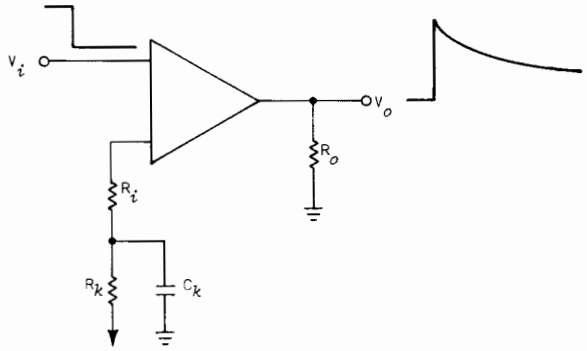


Fig. 5-18. Sag develops as C_k assumes a charge.

Both B+ and t_r are unacceptable. Reducing R_i also reduces the required R_O value. Fig. 5-17 shows one solution, C_k bypasses R_k. Cathode current, resulting from control grid fluctuations, flows from C_k, through the tube and R_L. C_k offers little opposition to even slow I_k changes. Therefore, $r_k = R_i$ and $R_L = R_O$. If r_k = 200 Ω, then R_L = 2.5 kΩ This represents considerable improvement.

Diode D1 protects C_k. A 275-μF capacitor is large electrically. To keep the physical size reasonable the device has a low breakdown voltage. This is acceptable during operation because cathode voltage

changes little. However, during warm-up or tube removal C_k charges toward -150 volts through R_k. D1 clamps when the charge exceeds -0.6 V preventing destruction of C_k.

sag

Capacitor bypassing improves risetime at the expense of a "flat-top." This long term response, *sag*, restricts the pulse width that an amplifier faithfully reproduces. In an individual stage, the cathode, emitter or source affects the initial sag slope more than any other circuit. Further, the initial sag slope of each amplifier stage adds directly giving an accurate prediction of total amplifier sag.

Negative sag results when net current reduces due to the charging of the bypass capacitor. Refer to Fig. 5-18. The amplifier draws sufficient current, through R_i, to maintain a voltage null between input terminals. Resultant current flowing through R_O sets output voltage (V_O). This describes what happens during transit of the input step. Gain times V_i develops as V_O.

C_k, during step transit, is an apparent ground. However, C_k immediately charges toward V_i at an initial rate set by time constant, R_iC_k. As C_k assumes the new charge, voltage across R_i decreases, reducing net signal current, which in turn results in output voltage reduction -- sag. The output waveform decays, even though the input waveform remains at the new level. Rate of initial output decay follows the charge rate of C_k. Call this the *initial sag-slope*, which establishes ultimate sag.

Output decay becomes slower after the initial slope. More of the net current begins to flow through R_k. Larger percentages of net current flows through R_k as C_k charges. Eventually, C_k reaches full charge and total current flows through R_k and R_i in series.

Gain is now $\frac{R_O}{R_i + R_k}$, therefore $V_O = V_i \frac{R_O}{R_i + R_k}$.

Interstage RC coupling and, in the case of pentodes, screen grid decoupling contributes to output sag. Initial sag-slope of each contributor adds directly

to determine output sag. Only C_k and R_i determine the initial slope contributed by the cathode:

$$\text{Cathode slope} = \frac{100\%}{R_i\ C_k} = \%\ \text{sag/second.}$$

This states that an output pulse of any width, immediately after reaching maximum amplitude, decays at a rate of $\frac{100}{R_i\ C_k}$ % per second. It does not, however, describe the entire long-term pulse shape. R_k determines whether the pulse has only a small spike at the leading edge; or appears to develop with considerable droop; or even continues to decay, ramp-like, at the initial slope rate.

Fig. 5-19 shows three possibilities:

1. $R_k = 0$. There is no sag.
2. $R_k = R_i$. The output decays from maximum at the initial slope rate, then more slowly to 50%. This is because R_i varies with time. Initially, $R_k = 0$, since C_k shunts R_k. As C_k charges, R_i increases exponentially until total cathode current flows through R_k. Now, $A_V = \frac{R_o}{R_i + R_k}$.

   If $R_k = R_i$, V_o decays to 50% of maximum. Increasing R_k increases the percentage of decay.
3. The initial sag slope represents total decay when R_k is an open circuit.

Interstage coupling circuits also contribute additive sag:

$$\text{Coupling circuit slope} = \frac{100\%}{R_c\ C_c} = \%\ \text{sag/second.}$$

Total % sag/second = cathode slope + coupling slope.

% sag/second formulas apply to triodes, transistors and FET's. Substitute, with semiconductors, r_t or r_{ds} for r_k. External component symbols also change but circuit placement makes substitution obvious.

pentode sag

The screen grid complicates pentode sag approximations for two reasons:

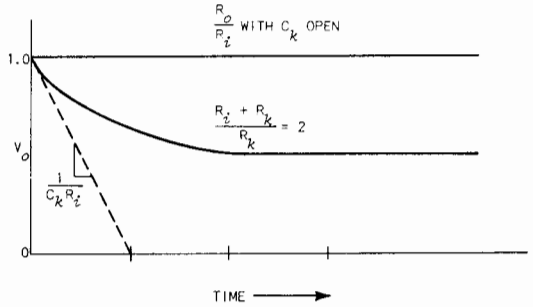


Fig. 5-19. C_k and R_i independently cause the initial sag slope, while the overall sag effect depends upon R_K.

1. Screen decoupling adds to the sag rate:

   $$\text{Screen slope} = \frac{100\%}{r_{g2}\ C_{g2}} = \%\ \text{sag/second}$$

   where $r_{g2} = \frac{\Delta V_{g2}}{\Delta I_{g2}}$ and C_{g2} = screen decoupling capacitance.

   Therefore total initial % sag/second = cathode slope rate + coupling RC slope rate + screen decoupling slope rate.

2. Eta (η) states that a percentage of cathode signal current flows a screen current. Thus, even when no screen decoupling circuits appear, screen signal current still contributes to the charge rate of the bypass capacitor.

Fig. 5-17 includes no screen grid decoupling or interstage coupling circuits. Compute the initial cathode sag-slope twice. First ignore screen current using 200 ohms as an approximation of r_k; then recompute after reducing r_k by 50 ohms to account for screen signal current:

1. $$\frac{100\%}{200 \times 275 \times 10^{-6}} =$$

   $$\frac{100\%}{5.5 \times 10^{-2}} =$$

   1,820% per second, or,

   1.8% per millisecond.

2. $\frac{100\%}{150 \times 275 \times 10^{-6}} =$

$\frac{100\%}{4.25 \times 10^{-2}} =$

2,400% per second, or,

2.49% per millisecond.

This is far too much sag for the amplifier being "built." Increasing the R_i C_k time reduces the initial sag-slope. Adding an adjustable resistor in series with C_k increases R_i C_k time and gives gain calibration capability.

gain adjustment

A gain adjustment completes the cathode circuit as shown in Fig. 5-20. R3 added to r_k sets R_i. However, to estimate the effect of R3 it must be put in the plate dimension: $\frac{R3}{\eta} = \frac{500}{0.8}$. R3 has a maximum effective value of 600 ohms. If r_k = 200 and $R_i = r_k + \frac{R3}{\eta}$, adjusting R3 varies R_i between 200 and 800. This is well within reason: R4 = R_O. $A_V = \frac{R_O}{R_i}$; $10 = \frac{6000}{R_i}$. Incidentally, midrange settings apply to most Tektronix circuitry, giving a check on the accuracy of a gm (r_k) estimate.

R3 affects the % sag/second. The true value of R3 must be added to r_k, modified for screen current, in the formula:

$$\text{Cathode Slope} = \frac{100\%}{C1\ (R3 + r_k - 50)} = \frac{100\%}{0.127}$$

$$= 780\%/\text{second} \simeq 0.8\%/\text{ms}.$$

The cathode slope alone determines the sag. This is because the plate couples directly to the follower and there is no screen decoupling. The amount of sag introduced by C1 and R1 is yet unsatisfactory. Fortunately plate decoupling combats sag. As originally used, plate decoupling circuits reduced interstage coupling via the common voltage supply. The purpose of the "decoupling circuit" of Fig. 5-21 is to overcome sag. Basically, R5 and C2 increase R_O with R_i, keeping voltage gain constant for a greater time.

Let R4 = R_L, R5 = R_d, and C2 = C_d.

$$\text{Initial decoupling slope} = \left(\frac{1}{R_L C_d} + \frac{1}{R_d C_d}\right) - \frac{1}{R_d C_d}$$

$$= \frac{1}{R_L C_d}$$

$$\%\ \textit{positive}\ \text{sag/second} = \frac{100\%}{R_L C_d}$$

$$= \frac{100\%}{(6 \times 10^3)\ (6.25 \times 10^{-6})}$$

$$= 2.6\%/\text{ms sag.}$$

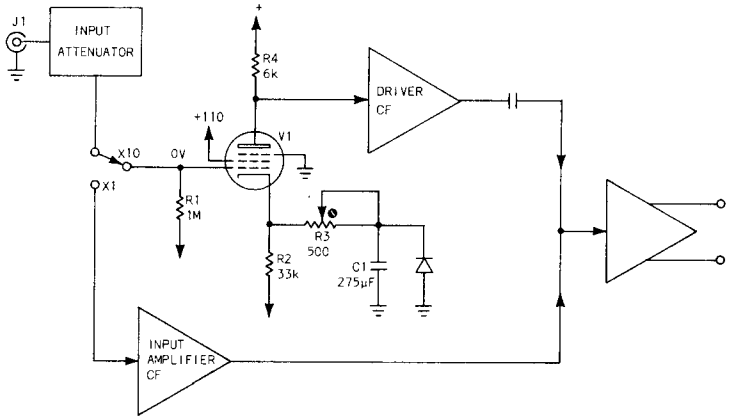


Fig. 5-20. Cathode gain adjustment.

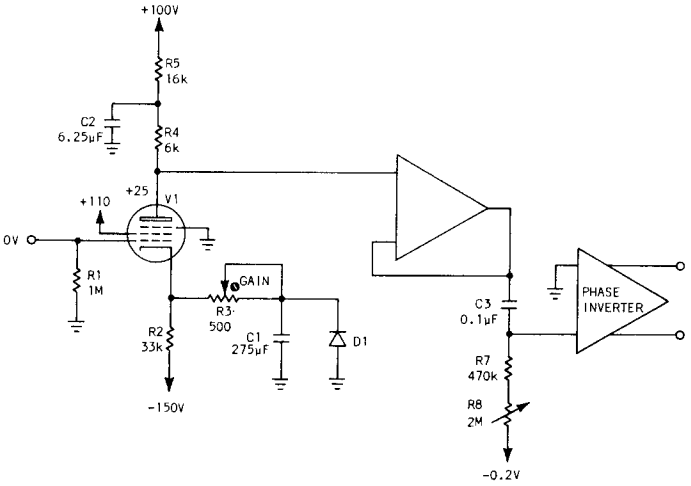


Fig. 5-21. Slope compensation.

plate decoupling overcomes cathode sag

Plate decoupling seemingly overcompensates for cathode sag. This is true as the cathode imposes 0.8%/ms negative sag. However, the coupling circuit at the follower output contributes negative sag which adds to the negative sag of V1. One adjusts R8 to set the initial slope of the coupling circuit. When coupling circuit slope, added to V1 cathode slope, equals decoupling slope, the phase inverter input is sag compensated: Let R7 + R8 = R_C, and C3 = C_C.

$$\text{Coupling circuit slope} = \frac{100\%}{R_C C_C} = \%/\text{second sag.}$$

$$\text{Coupling slope} = \frac{100\%}{(R7 + R8)\ C3}$$

$$\text{Max coupling slope} = \frac{100\%}{(470 \times 10^3) \times 0.1 \times 10^{-6}}$$

$$\simeq 2\%/\text{ms}$$

$$\text{Min coupling slope} = \frac{100\%}{(2.47 \times 106) \times 0.1 \times 10^{-6}}$$

$$\simeq 0.4\%/\text{ms}$$

These calculations show that some setting of R8 will give a negative coupling circuit slope, which added to the cathode slope equals the positive decoupling circuit slope. This does not take into account part tolerances, V1 *gm* variation, or following stage sag. R8 has sufficient range to account for these variables; and, fortunately, one sets R8 empirically.

One adjusts R8 while observing a train of squarewaves for minimum sag slope. The squarewaves must have known qualities such as flat tops, about 20 milliseconds wide.

Flat top deterioration, or sag, and the compensation techniques generally apply to any active device. The relationships between transconductance, resistance and capacitance remain whether the device be pentode, triode or semiconductor.

Flat top reproduction is important but so is minimum risetime. Passive components at the output establish the minimum possible risetime. R4, and output capacitance (C_O) set this restriction in Fig. 5-21. R4 is obvious. C_O consists of several shunt capacitances lumped together. V1 interelement capacitance at the plate and follower input capacitance, adds to stray and distributed capacitance. Part selection, part placement and assembly techniques combine to produce C_O. Rule-of-thumb C_O values, for tubes, vary between 8 pF and more than 20 pF. These are very general values listed only to give the reader a feel for output capacitance values. Using these values one can approximate the range of plate risetime possibilities:

$$t_r = 2.2\ R4C_O.$$

If C_O = 8 pF, t_r 105 nanoseconds.

When C_O = 20 pF, t_r = 265 nanoseconds.

The output waveform rises no faster than the charge time of C_O. However, the charge rate also depends upon the quantity of charging current available. V1 *gm* establishes maximum current delivered to C_O for a given control grid voltage. Risetime then depends upon two factors, active device parameters *and* output RC. To account for this a tube "figure-of-merit" defines the initial output slope.

figure of merit

The gain-risetime ratio becomes the "figure-of-merit" for RC amplifiers:

$$\frac{\text{Gain}}{\text{Risetime}} = \frac{A_V}{t_r} = \frac{1}{2.2R_i C_O}$$

When $A_V = \frac{R_O}{R_i}$

and $t_r = 2.2\ R_O C_O$

and $R_i = r_k + \frac{R_k}{\eta}$ or $\frac{1}{gm} + \frac{R_k}{\eta}$

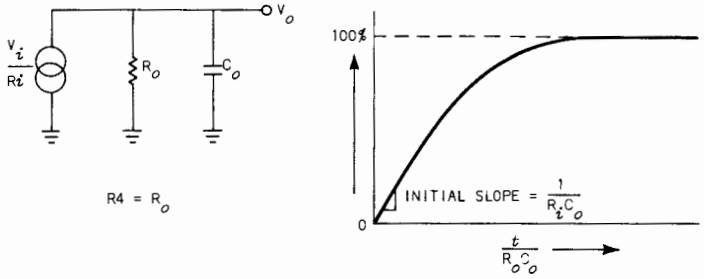


Fig. 5-22. Equivalent output circuit. $R_L << r_p$.

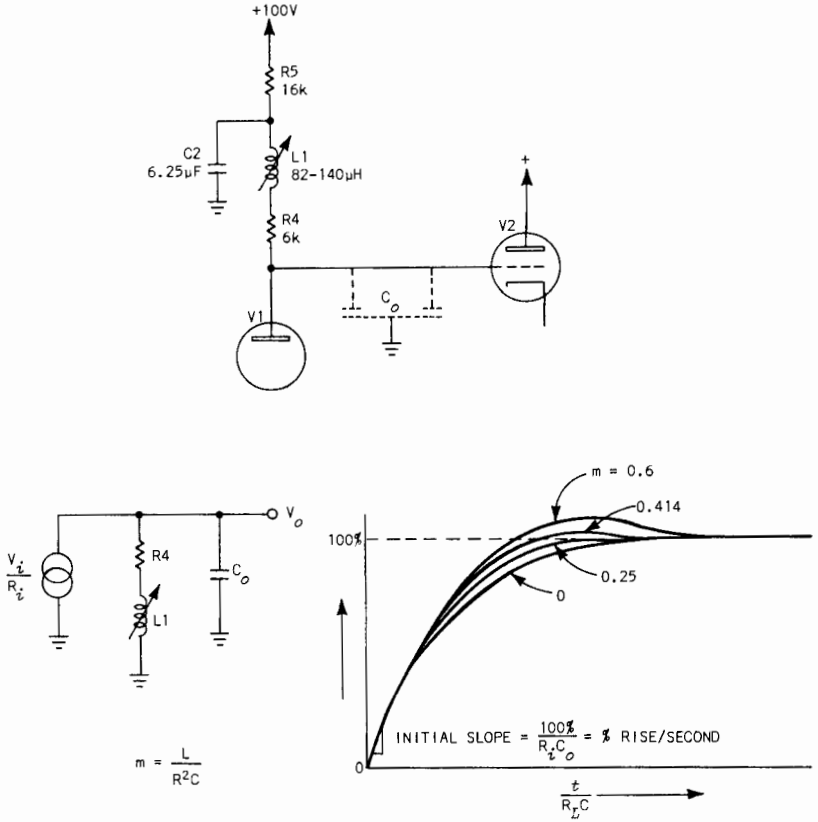


Fig. 5-23. Shunt peaking.

Fig. 5-22 is the equivalent V1 circuit. The current generator delivers charging current to C_O as a result of an ideal input voltage step. Output voltage rises, initially, at a rate determined by the current generator and C_O. Initially current flows entirely in C_O, then as output voltage rises, R_O shunts more and more current, developing an RC response curve.

So far, the only risetime improvements one can imply is to reduce R_i, R_O, C_O and increase *gm*. However, R_i and R_O have been justified in this circuit, and there are practical limits to C_O and *gm*. Overall circuit performance and part availability dictate compromises. These compromises sometimes justify added circuit complexity to improve risetime.

shunt peaking

Fig. 5-23 shows L1 added to the plate circuit as a risetime improvement called *shunt peaking*. L1 substantially improves risetime compared to the basic RC.

There are two things L1 does not do:

1. L1 does not change amplifier gain.
   $A_V = \frac{R_O}{R_i}$, and R_O = R4.
2. L1 does not affect the figure of merit.
   $\frac{A_V}{t_r} = \frac{1}{2.2\ R_i C_O}$. The tube fixes both *gm* and C_O and the gain desired sets total R_i.

Basic capacitor and inductor characteristics explain why shunt peaking works. Applying a voltage causes *maximum* current flow in C_O and *minimum* current flow in the inductor. Further, to charge C_O as rapidly as possible total generator current should flow through C_O. With or without L1 initial current flows entirely in C_O, but as V_O rises it creates a current demand through R4. L1 opposes any current change in this branch, maintaining capacitive charge current. Making L1 large enough slows the shunting of R4 so much that C_O voltage overshoots the final V_O.

L1 is shown as adjustable. One adjusts L1 for fastest rise without overshoot. The graph and equivalent circuit show the effects of L1 once factor m is identified. Factor m travels under other names such as: Q, the circuit Q when

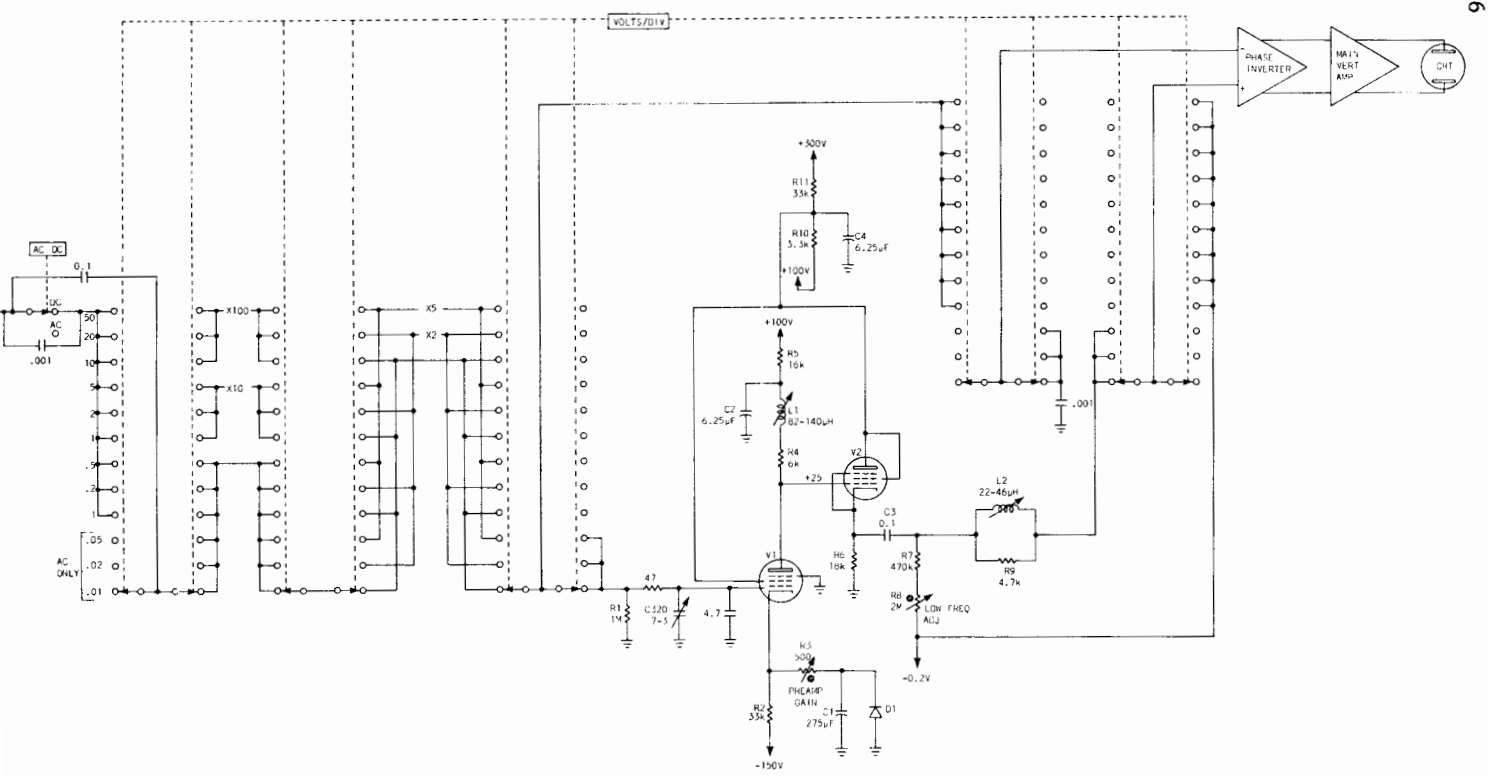


Fig. 5-24. Input X10 amplifier complete.

X_L = R; or Q, the circuit Q at resonance when $F_O = \frac{1}{2\pi\ LC}$. Since this discussion leans toward time domain, use: $m = \frac{L}{R^2C}$.

The graph shows that the initial slope cannot exceed the original, with or without L1. When L1 = 0 the curve follows the RC response as shown earlier. Adding L increases factor m, causing overshoot at m values over 0.25.

L1 can be adjusted to give an m of 0.25. Use values already given: R_L = 600 Ω, R_O = R4 = 6 kΩ and assume C_O = 12 pF.

$$m = L1/R_O{}^2C_O$$

Setting L1 to min:

$$m = \frac{82 \times 10^{-6}}{(6 \times 10^3)^2 \times (12 \times 10^{-12})}$$

$$m = \frac{82 \times 10^{-6}}{4.32 \times 10^{-4}}$$

$$m \approx 0.2$$

Setting L1 to max:

$$m = \frac{140 \times 10^{-6}}{4.32 \times 10^{-4}}$$

$$m \approx 0.3$$

Keep in mind these figures result from an approximation of C_O. If C_O were less m would increase. For example:

If C = 10, L1 varies m from 0.24 to 0.4.

If C = 12, L1 varies m from 0.2 to 0.3.

If C = 14, L1 varies m from 0.17 to 0.28.

Any of these capacitive values allow an m value of 0.25, resulting in fastest rise without overshoot.

The amplifier is almost "built." See Fig. 5-24. This vertical amplifier utilizes the X10 amplifier described.

The basic deflection factor of the phase inverter is 100 mV/div. This becomes apparent by mentally placing the VOLTS/DIV selector to 0.1: The (-) phase inverter input connects in a short circuit, via the switching program to the input connector. Higher VOLTS/DIV selections switch in some attenuation. The (+) terminal connects to signal ground for any selection between 50 and 0.1 VOLTS/DIV.

Selecting input deflection factors of 0.05, 0.02 or 0.01 volts/div signal grounds the (-) input terminal and connects the (+) terminal to the preamplifier output. Input signals now drive the grid of V1. Selecting 10 mV AC couples signal voltages to the grid of V1 without attenuation. A_V of 10 satisfies the phase inverter deflection factor of 100 mV/div. V1 correctly inverts the input signal since input (+) rather than input (-) now receives signal drive.

V1 control grid circuit includes an adjustable C. This allows one to compensate the input voltage divider of V1 to that of the phase inverter (-) input.

V1 cathode, suppressor and plate circuits are as explained. V2 was but an amplifier triangle. R6 and quiescent control grid voltage longtail V2. Plate current flows through a decoupling network (R10, R11 and C4) shared by V1 screen current. This arrangement prevents voltage changes at V2 plate or V1 screen. Signals at the screen of V1 appear inverted at the plate of V2 thereby canceling.

Cathode follower V2 improves circuit risetime by isolating V1 plate components from the coupling circuit consisting of C3, R7 and R8. Series peaking, R9 and L2, appears for the first time.

series peaking

Series peaking maintains capacitive charge current to improve risetime. Circuits using shunt peaking realize greater risetime improvement than with series peaking. However, series peaking is used here as a simple method of improving risetime without affecting the sag or low frequency adjustment. Phase inverter input capacitance is that of concern, the greatest portion of which consists of switch capacitance.

V2 output capacitance (C_o), L2 and phase inverter input capacitance (C_i), make up the series peaking reactive components. Upon application of a voltage step, L2 opposes any current flow through C_i. Total C_i current must flow through R9. After the first instant current flows through L2, increasing through L2 and R9, at an L/R rate until L2 totally shunts R9. L2, now drawing total current, still opposes any current change. This current is charging current for the phase inverter input capacitance.

Series peaking circuits have an "m factor" similar to shunt peaking:

$$m = \frac{L}{R^2 C}$$

$$L = L2$$

$$C = C_o + C_i \text{ and}$$

$$R = R9.$$

For a comparison of shunt and series peaking refer to Fig. 5-25. Notice that shunt peaking imposes no step delay, while series peaking imposes a delay. Both represent risetime improvement with shunt peaking providing the least risetime.

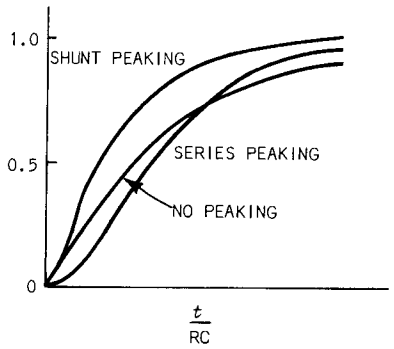


Fig. 5-25. Shunt and series peaking compared.

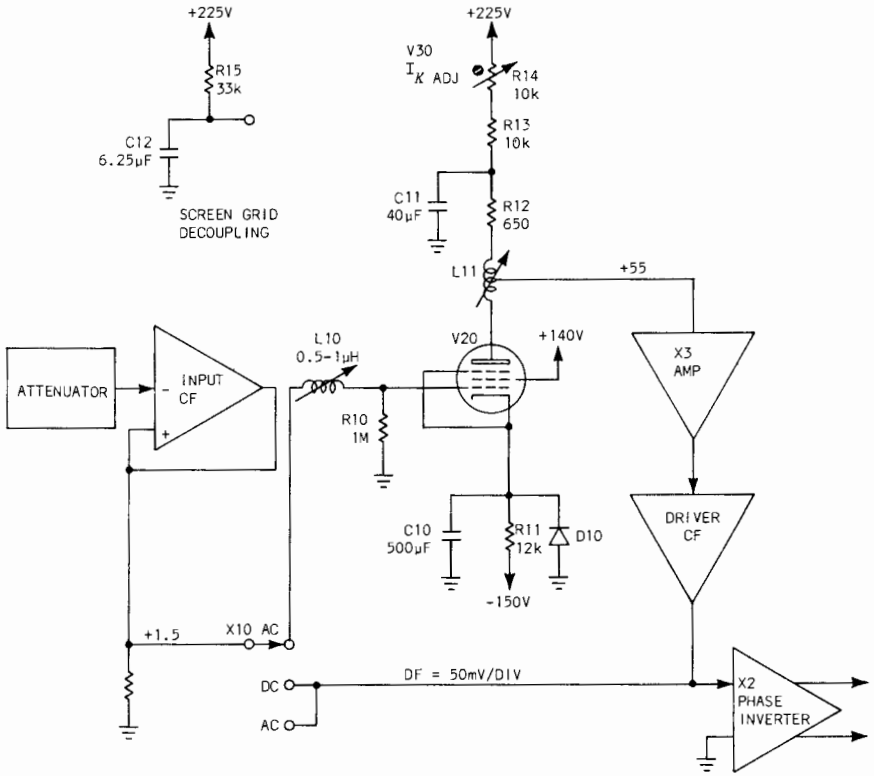


Fig. 5-26. Input stage of the X10 amplifier.

Using the information given consider the amplifier of Fig. 5-26. V20 appears in a preamplifier with a basic deflection factor of 50 mV/div. The AC-DC switch on the front panel has a third position labeled X10 AC. Selecting this position multiplies sensitivity -- divides deflection factors -- by 10. Switching the three stage X10 amplifier into the circuit decreases the input deflection factor to 5 mV/div.

The X10 amplifier must provide gain, degrading risetime as little as possible. Selecting DC, this preamplifier risetime, at the phase inverter output, is about 6 ns. X10 amplification increases risetime by only 2 or 3 ns. To accomplish this the X10 amplifier uses three low-gain, compensated stages.

risetime improvement

The first risetime improvement circuit appears in the grid of V20. L10, placed between switch capacitance and V20 input capacitance, series peaks. L10 has no effect upon the control grid DC level, about +1.5 V.

The control grid voltage causes slightly more than 150 volts drop across R11, longtailing V20. C10, protected by D1, bypasses R11.

sag

Bypassing R11 gives the required gain determinate at the expense of sag. V20 introduces sag at both cathode and screen grid:

$$\text{Initial } k \text{ slope} = \frac{100\%}{R_i\ C10} = \text{sag \%/sec}$$

$$\text{Initial } g2 \text{ slope} = \frac{100\%}{r_{g2}\ C12} = \text{sag \%/sec}$$

These slope contributions add, establishing the plate compensation necessary. C11, R12, R13 and R14, the plate decoupling network, compensates for sag: $\text{Initial (+) slope} = \frac{100\%}{R12\ C11} = \text{sag \%/sec.}$

Adjusting R14 negligibly affects sag. This is because the sum of R13 and R14 considerably exceeds R12 resistance at any setting of R14. R14 sets V20 plate voltage which in turn controls gm of the following direct coupled amplifier.

The sag compensation formula ignored L11, listing R12 as R_O. This is also true for gain calculation.

For now, consider the T-coil (L11) as a short section of transmission line, terminated by R12. Therefore, since Z_O = R12, R12 = R_O.

Use resistance ratio, R_O to R_i, as gain, assuming r_k = 200:

$$A_V = \frac{R_O}{R_i} = \frac{R4}{r_k} = \frac{650}{200} = 3.25$$

One can ignore T-coil peaking while computing basic gain. L11 with associated components affects output risetime only.

One can assume that designing V20 to work into a low resistance plate load represents a gain sacrifice to improve risetime. If R_O = R12 = 650 Ω, and C_O = total output circuit capacitance = 12 pF then,

$$t_r = 2.2\ R12\ C_O = 2.2\ (6.5 \times 10^2) \times 1.2 \times 10^{-11}$$
$$= 16\ ns.$$

Recall that gm and C_O control the initial output slope:

Initial slope = $\frac{1}{R_i\ C_O}$. Since $R_i = r_k$, then

initial slope = $\frac{100\%}{r_k\ C_O} = \frac{100\%}{(200)\ 12 \times 10^{-12}} \approx 40\%/ns.$

Reducing C_O improves both characteristics. This is one effect of L11.

L11 removes V30 (X3 amp) input capacitance (C_i) from the total output capacitance (C_O) at the plate of V20. Unfortunately, the detailed effects of L11 are far more complex, too complex for this book. The reader must settle for a generalized description.

Fig. 5-27 shows V20 as a current generator restricted to a quantity by R_i. Generator current develops V_O across the complex LCR network, which presents an impedance equal to R12. L11 and R12 represent themselves while C_O is plate capacitance, C_i following stage input capacitance, and C_L the lumped capacitance of L11. These component values bear important relationships to the network. Properly proportioned, the LCR components appear purely resistive, equal to R12. A pure resistance

T-coil

imposes no phase shift or impedance change. The T-coil should therefore reproduce a perfect step. Part tolerances and unpredictable stray reactances reduce T-coil effectiveness. One empirically adjusts L11 for optimum LCR proportions by tweaking for fastest displayed risetime within overshoot limits of 1 or 2%.

L11 improves risetime, over R12 C_O, by at least 2: $t_r' = \frac{2.2\ RC}{2}$. Adding a series peaking coil, as in Fig. 5-28 improves risetime by about 3: $t_r'' = \frac{2.2\ RC}{3}$.

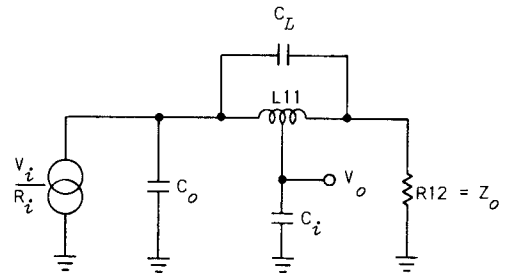


Fig. 5-27. Equivalent circuit of 5-26.

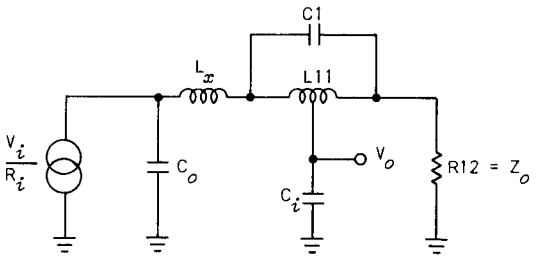


Fig. 5-28. Series peaking reduces basic T-coil risetime slightly.

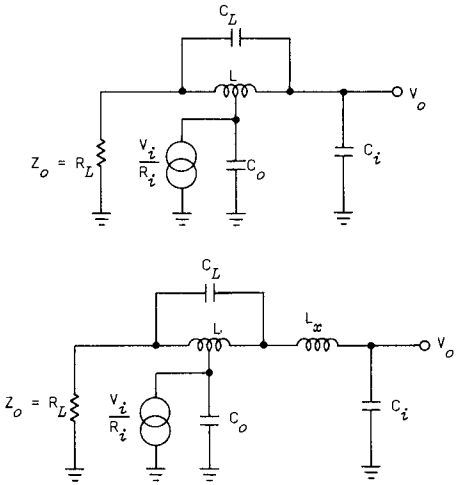


Fig. 5-29. Alternate T-coil drive.

V20 drives one end of L11 with output voltage taken across capacitance at the centertap. The active device drives the center tap in some configurations. Fig. 5-29 illustrates center-tap drive. The circuit reacts the same in either configuration. Generally speaking, the larger capacitance should connect to the center tap. V20 output capacitance is apparently less than following stage input capacitance. This is not a rule, proved by the second amplifier stage. (Fig. 5-30).

Drive at the centertap of L30 is not because of high V30 output capacitance, but the need for series peaking at the CF input. The T-coil circuit consists of R35, L30, V30 output capacitance and stray capacitance shunting the coupling network. Capacitance from the body of C33 to chassis ground makes up a large portion of output capacitance. L30 isolates this capacitance from the plate of V30. L40 prevents this stray from shunting CF grid capacitance directly. L30 and L40 improve plate circuit risetime characteristics as a combination T-coil series-peaking network.

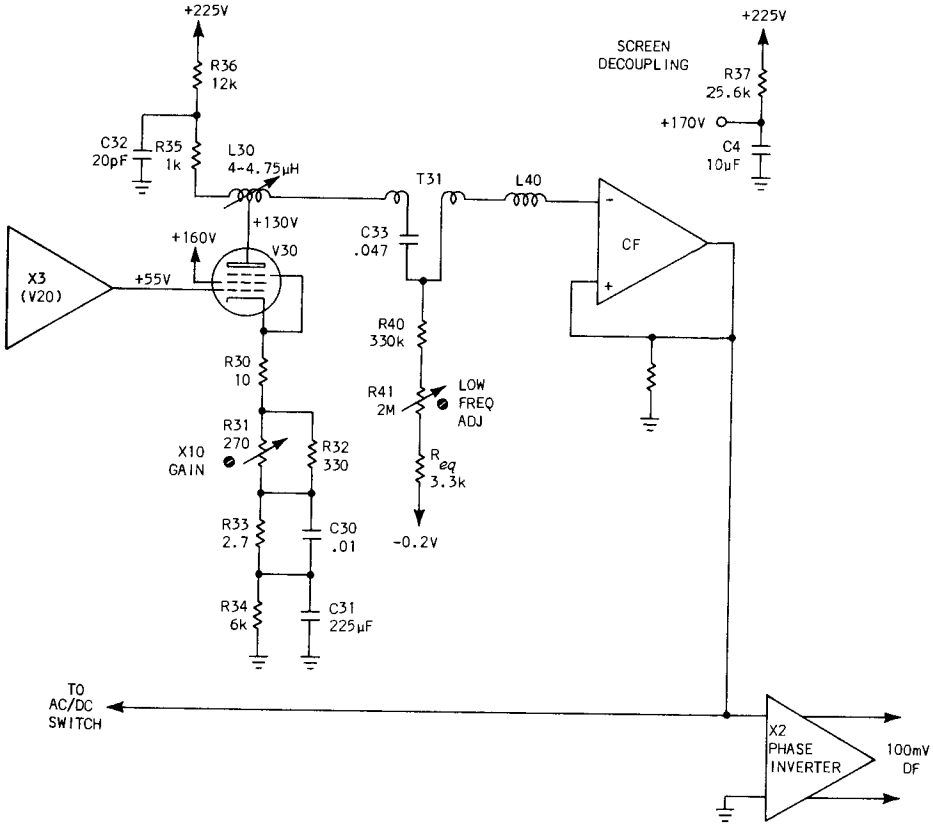


Fig. 5-30. X10 amplifier second stage.

T31 reduces the quantity of signal loss due to stray capacitance (C_S) associated with C33. T31 is a pair of wires wound, one or two turns, about C33. Signal current flows through C_S, the quantity of which depends upon input signal "speed." Faster signals demand greater C_S current. This current, however, must flow through the primary of T31 which transformer-couples signal power to the CF input. Increasing C_S current only increases the power coupled by T31. T31 adds to the inductance of L40 for series peaking considerations.

R35 represents plate load value. Treat L30, T31, and L40 as a short section of transmission line properly terminated by R35. R35 is also R_O to slow-changing signals, which develop at the CF grid via coupling network, C33, R40, R41 and R_{eq}.

R_{eq}

R_{eq} is the equivalent resistance of the CF bias adjustment. Adjusting bias changes the return voltage by several millivolts maintaining R_{eq} at 3.3 kΩ.

One adjusts R41 for minimum sag. V20 and V30 plate decoupling overcompensate for V20 and V30 sag contributions, thereby presenting a range of adjustment to R41. The formula, $\frac{100\%}{R_C\ C_C}$ expresses the percent of sag slope introduced by the coupling RC, when R_C = R40 + R41 + R_{eq} and C_C = C33.

To compute gain as the resistive ratio, $\frac{R_O}{R_i}$, one must first identify R_O and R_i. R_O = R35 = 1 kΩ. R_i identification remains. Factors that affect V30 R_i are: V30 quiescent grid voltage and X10 amplifier gain adjustment.

V20 plate circuit includes a means of setting plate voltage. V20 plate voltage is also V30 control grid voltage. Only V30 reacts to the adjustments thus the name, V30 1k adjustment. Quiescently setting V30 grid voltage fixes V30 *gm*.

V30 grid voltage establishes *gm* quite predictably for two reasons:

1. Eta (η), for a given pentode type, varies little. Assume an η of 0.8 here.
2. R34 and R37 are precision resistors.

I_p and V_{g2} fix *gm* over a wide range of plate voltage. One sets V30 grid voltage for 55 volts across precision longtail R34. This sets I_k to 9.2 mA, within the tolerance of R34 and the measurement. 80% η causes 7.35 mA I_p, leaving 1.85 mA to flow as I_{g2}. V_{g2} now results from the drop across R37, another close-tolerance part.

gain-control effects

The small gain-control resistance requires that *gm* be predictable and repeatable. To show gain-control effects, first simplify Fig. 5-30. C31 bypasses R34 making the top of R34 apparent ground. Notice that C31 needs no protective diode because both C31 and R34 return to ground. R33 and C30 cathode peak. For now ignore C30. The gain adjustment consists of R31 shunted by R32. Lumping these components results in a resistance of 0 to 150 Ω. 85 Ω is the resistance with R31 set to midrange. R30 insures cathode degeneration, with R31 shorted, damping oscillations.

Refer to Fig. 5-30 for the simplified model. Signal currents flow through R_k which consists of R33, R_G and R30. Continue to ignore C30. $R_i = r_k + \frac{R_k}{\eta}$. Assume R_G set to midrange:

$$R_i = r_k + \frac{R30 + R_G + R33}{\eta} = 200 + \frac{10 + 85 + 2.7}{0.8} \simeq 322$$

Since R_O = R35 = 1 kΩ then,

$$A_V = \frac{R_O}{R_i} = \frac{1000}{322} = 3.1$$

The cascade gain of the two stages ≈ 10.0 (3.25 x 3.1).

Notice that all gain and quiescent calculations were based on the same rule-of-thumb η and *gm* values for all pentode amplifiers. Measurements were then made in random samples of Tektronix instruments from which these circuits were taken. Measurements varied less than 5% from calculated figures even though tube

types varied. Figs. 5-14 through 5-31 include at least one of the following tube types: 6AU6, 6BH7, 12BY7 and 5654. Applying rule-of-thumb gm and η values and the R_O to R_i gain ratio gives workable results.

Cathode peaking techniques occur most frequently in push-pull amplifiers. They also appear in semiconductor circuits bearing the element name: emitter or source peaking. The concept is the same for all devices. V30 cathode peaking reduces R_i during fast input voltage changes. During an initial rapid voltage change, C30 shunting reduces R_i by the value of R33, thus increasing gain for a short interval. V30 cathode peaking fails to meet the classic description because it reduces R_i by only 1% or so. This peaking corrects for short-term rolloff the equivalent time constant of which equals (R33)(C30).

Basically, cathode peaking consists of R_k bypassed by a small capacitor, sacrificing gain for risetime. Optimum risetime without overshoot results from cathode peaking when the cathode time constant, R_kC_k, equals the output time constant, R_OC_O. The simplified model of Fig. 5-32 includes the components of interest.

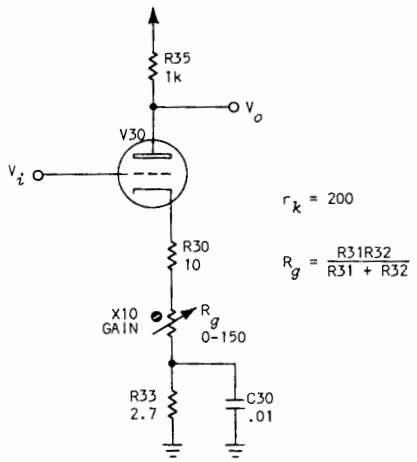


Fig. 5-31. Gain determinants of 5-30.

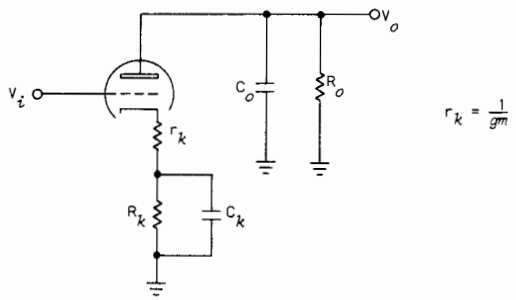


Fig. 5-32. RC amplifier gain-risetime components identified.

cathode bypass

The highest gain the model of Fig. 5-32 can achieve is $\frac{R_O}{r_k}$. This occurs when C_k bypasses R_k: $A_V = \frac{R_O}{R_i}$, $R_i = R_k + r_k$ and when $R_k = 0$, $A_V = \frac{R_O}{r_k}$. R_i also affects risetime. The output step can rise no faster than the initial slope:

Initial slope $= \frac{100\%}{R_i\ C_O}$ = %/second. When $R_i = r_k$ the initial slope $= \frac{100\%}{r_k\ C_O}$. Beyond the initial slope, output R and C components restrict risetime: $t_r = 2.2\ R_O\ C_O$. From these characteristics one can evolve some related functions.

Since $A_V = \frac{R_O}{R_i}$ then R_i represents a value of attenuation. Assign 1 the value of least attenuation and represent total attenuation by k. Minimum R_i is r_k. Therefore, $k = \frac{r_k + R_k}{r_k} = 1 + \frac{R_k}{r_k}$. Now consider that R_O remains constant, and k changes: If $k = 1$ attenuation is minimum or gain is maximum. If $k = 2$ attenuation doubles -- gain

halves. Assigning $k = 2$ states that r_k and R_k equal. This is the basis for the graph in Fig. 5-33.

The circuit graphed has either R_k alone or fully bypassed. Further, R_k equals r_k or $k = 2$. When fully bypassed ($C_k = \infty$) the output rises to maximum voltage as though $k = 1$. Removing C_k causes the output to rise half as far. The initial slopes differ, gain differs, but risetimes equal. $t_r = 2.2\ R_O C_O$ in both cases. Initial slopes differ: when $C_k = \infty$ the initial slope $= \frac{100\%}{r_k\ C_O}$ and when $C_k = 0$ the initial slope $= \frac{100\%}{(r_k + R_k)\ C_O}$. $C_k = \infty$ looks better, but remember that sag begins shortly after reaching 100% V_O. The problem is to maintain output voltage (gain) along the initial slope for as long as possible without introducing sag. This is cathode peaking.

The Attenuator chapter introduced the concept of compensated voltage dividers: When R1C1 = R2C2 then $\frac{Z1}{Z2}$ remains constant and equal to $\frac{R1}{R2}$. Substituting in the gain formula: $A_V = \frac{R_O}{R_i} = \frac{Z_O}{Z_i}$, when $R_k C_k = R_O C_O$. Because r_k cannot be bypassed it does not appear as part of the input time constant. But, C_k bypasses R_k at the first portion of an input step, allowing r_k and C_O to establish the initial slope.

Therefore, the ratio of $R_k C_k$ to $R_O C_O$ holds. $\frac{R_k C_k}{R_O C_O}$ defines ρ (rho).

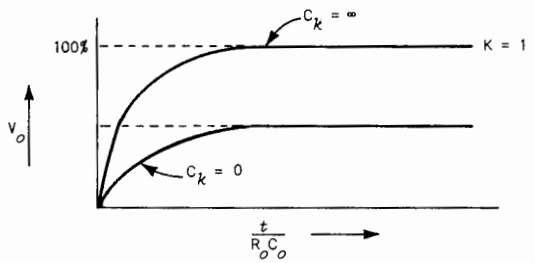


Fig. 5-33. Step response comparison of bypassed and unbypassed R_k when $R_k = r_k$.

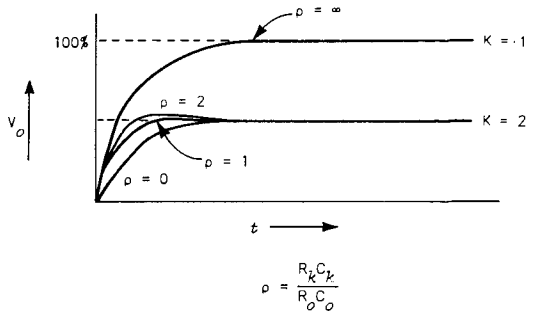


Fig. 5-34. When $R_k C_k = R_o C_o$ on RC amplifier responds with least risetime without overshoot, at the expense of gain.

Fig. 5-33 shows the results by bypassing R_k with small capacitances. The output waveform rises along the initial slope of a fully bypassed R_k. Then, as C_k assumes a charge, the output rises exponentially toward the level determined by k. Keeping C_k small eliminates sag. Exceeding $\rho = 1$ causes sag. The decay is rapid enough when ρ slightly exceeds 1 that "spike" rather than "sag" describes the observed result.

As long as k is greater than 1 a risetime improvement results, assuming $\rho = 1$:

$$t_r = \frac{2.2\ R_o C_o}{k}.$$

These curves resemble those for shunt peaking. Keep in mind that the inductive-peaking methods improved risetime without sacrificing gain.

Fig. 5-33 and 5-34 apply to transistors and FET's as well as electron tubes:

$$k = \frac{R_t + R_E}{R_t} \quad \text{or} \quad k = \frac{r_{sd} + R_S}{r_{sd}}$$

Either C_E or C_S designates the bypass capacitor.

Cathode, source or emitter peaking also travels under the name *current peaking*. This is apt.

During the short interval that the bypass capacitor charges, an additional surge of current flows through R_O.

Electron tubes are victims of technology. Because triodes contain but three elements, cathode, control grid and plate, they are far simpler than pentodes. However, for years the much higher *gm* of pentodes made triodes less acceptable as pulse amplifiers. Then triodes, such as the 6DJ8, with *gm* which exceeds most pentodes, became available. High-performance, readily available transistors came into the picture at about the same time. These high *gm* devices exhibit one poor feature, low input impedance. Therefore, triodes appear in very few newly designed circuits in configurations other than cathode followers.

Triode amplifiers do occur, in the single-ended, common-cathode configuration, as shown in Fig. 5-35. The triode shown performs as a beam-position-indicator driver. Beam-position indicators, usually neon bulbs, help an operator locate displays. Although signals affect a beam-position indicator circuit, it usually requires control by positional voltage.

beam-position indicators

Here a resistive voltage divider, from the lower CRT plate to a positive 100 volts, sets the operating point of V1. Network R1, R2 and R3 is large to prevent output amplifier loading. R2 is adjusted during center screen or quiescent operation. Quiescently B1 and B2 are off. Adjusting R2 sets the voltage at V1's plate halfway between +225 volts, return for B1, and +325, return for B2. 50 volts ignites neither.

When the displayed trace deflects downward, the lower CRT plate becomes the more positive and V1 grid follows at an attenuated level. A positive-going grid increases tube current, decreasing plate voltage. Voltage at the junction of B1-B2 moves toward +225 and away from +325. When voltage across B2 exceeds 55 volts the neon fires, indicating a below center trace.

Upward deflection causes negative-going V1 grid voltage and B1 ignites.

triode amplifiers

Circuits as simple as 5-35 hardly require detailed description. Sophisticated amplifiers to follow utilize triodes in configurations which require understanding of triode amplifier parameters in general.

The quotient of output voltage (V_o) divided by the input voltage (V_i) expresses true voltage gain (A_V). Quotient of $\frac{V_o}{V_i}$ equals the quotient of output resistance (R_o) divided by input resistance (R_i) with proper identification of R_o and R_i. This is true for all active devices.

Since useful gain approximations utilize resistance ratios, conductance receives considerable attention. The *gm* of an active device establishes a portion of R_i:

$$gm = \frac{1}{r_e} = \frac{1}{r_{sd}} = \frac{1}{r_k}$$

Semiconductors and pentodes utilize longtailing to stabilize *gm*, thus R_i, making the resistance ratio useful as a gain approximation. Semiconductor collector or drain circuits have little effect upon *gm* as long as R_o is relatively small. The

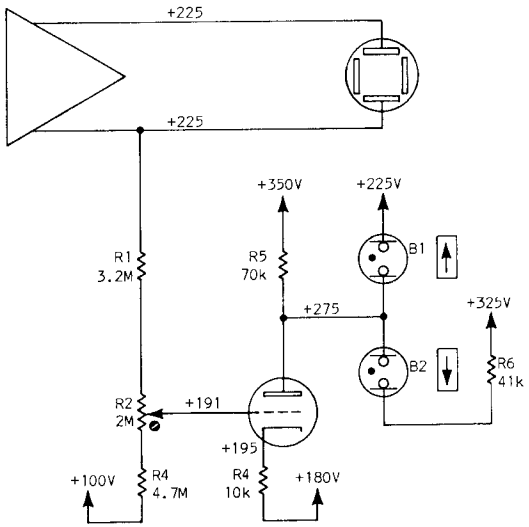


Fig. 5-35. Beam position indicator.

same is true of pentode plate parameters when connected as a pentode. Screen grid voltage has considerable control of *gm*. Screen grid parameters add complexity, but improve broadband performance by isolating the plate.

Triodes, lacking a screen grid, exhibit the lowest dynamic output impedance (r_p). It ranges from 2 k to 10 kΩ, compared to 0.5 M to 1.5 M for pentodes, increasing the probability of r_p reducing the estimated R_O. To ignore r_p, the external plate load must be quite small.

Low r_p values also imply that plate voltage affects *gm*:

$$r_p = \frac{\Delta V_p}{\Delta I_p}, \text{ grid voltage constant.}$$

Since changing plate voltage changes plate current, *gm* must also change:

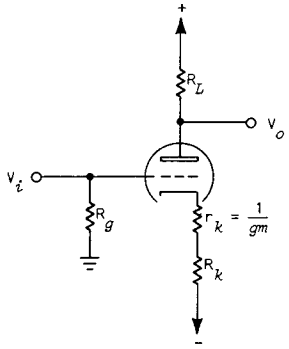
$$V_i \; gm = I_p, \text{ with } V_p \text{ constant.}$$

Grid voltage, of course, has much greater control of I_p (I_k).

Refer to Fig. 5-36 for a parameter discussion. R_O cannot exceed r_p since r_p shunts R_L. Increasing plate voltage increases r_p but can increase r_k more resulting in a loss of gain. Raising V_p from 100 to 250 volts, in one triode type, causes 7% r_p increase, 42% r_k increase, and plate current changes about 10%.

Changing plate current 250% creates more dramatic effects. Assume the tube in question, a 6DJ8, operating with 90 plate volts:

1. I_k = 1 mA
   gm = 2500 µmhos
   r_p = 13 kΩ
2. I_k increased to 2.5 mA
   gm = 4000 µmhos
   r_p = 7 kΩ

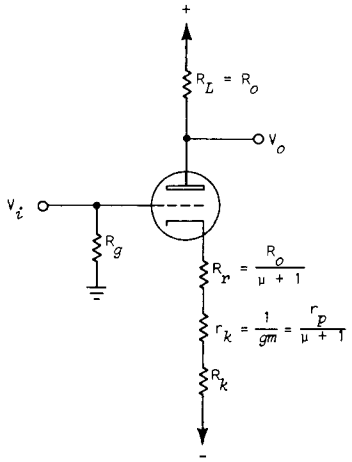


$$A_V = \frac{V_o}{V_i} = \frac{R_i}{R_i}$$

$$R_o = \frac{R_L r_p}{R_L + r_p}$$

$$R_i = r_k + R_k$$

Fig. 5-36. Triode common cathode amplifier model.



$$A_v = \frac{R_o}{R_i}$$

$$R_o = R_L$$

$$R_i = R_k + r_k + R_r$$

Fig. 5-37. Triode common cathode model 2.

All parameters change appreciably. Inserting these values into the formulas one can easily see the effects of plate voltage or plate current changes.

Fig. 5-36 was presented as a current generator which delivered $\frac{V_i}{R_i}$ amps. The internal generator impedance r_p, shunted R_L to establish R_o. Changing

R_O or plate voltage changes tube parameters. The parameter change is similar to the effect of transistor Beta. That is, plate loading (R_L) reflects into the cathode to oppose signal current. Considered from this angle, only R_L appears as output load:

$$A_V = \frac{V_O}{V_i} = \frac{R_O}{R_i}$$

$$R_O = R_L$$

$$R_i = R_k + \frac{r_p + R_L}{\mu + 1} = R_k + r_k + \frac{R_L}{\mu + 1}$$

This book utilizes the latter approach since it readily adapts to the "thumb-rule" gain approximations:

1. R_O is easy to identify
2. R_i approximations are similar to those used with other devices.

Fig. 5-37 is a model of the approximation. When tube parameters are unknown use: r_k = 200 Ω. Another thumb rule estimates R_p: Assume $\mu + 1 = 20$. This gives an idea of the effects of r_p upon circuit gain.

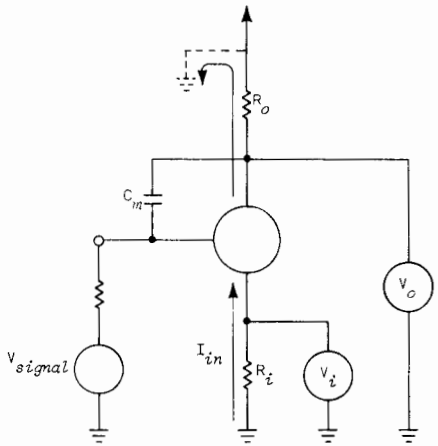


Fig. 5-38. Output to input feedback called "Miller effect."

Circuit approximations, quick and handy as they are, contain an inherent danger -- the danger of overlooking a key circuit characteristic. Most commonly one forgets loading effects at the bases of transistors and at the plates of triodes. Quick tests for Beta (50) and μ (20) pay dividends.

Miller-effect

Triodes, along with other three terminal active devices, experience degenerative feedback via capacitance grid-to-plate, or base-to-collector or gate-to-source. This is "Miller-effect"named after the discoverer. Fig. 5-38 includes capacitor C_m. The "m" represents "Miller". C_m occurs between device elements as a result of construction. Quiescently, C_m adds a few picofarads at most to input capacitance. However, during signal processing C_m increases A_V times:

If $A_V = 10$, and $C = 5$ pF,

$$C_m = C\ (1 + A_V)$$

$$C_m = 5\ (1 + 10)$$

$$C_m = 55 \text{ pF}$$

"Miller-effect" draws a very real capacitive current from the signal source. For example, if the signal source developed +1 volt, all capacitances, other than C_m, draw sufficient current to charge to +1 volt. +1 volt also develops at one plate of C_m but, for a X10 amplifier, -10 volts develops at the other plate. C_m must change charge by 11 volts. Signal source loading, both phase and amplitude, is the same as increasing C_m eleven times.

C_m is another limitation to short-risetime, high-gain amplifiers of the common-emitter, common-source or common-cathode configuration. Pentodes also suffer from Miller-effect but to a much lesser degree than triodes. C_m is control-grid to screen-grid capacitance multiplied by gain. Gain in this case refers to signal voltage which develops at the screen grid. Decoupling or low impedance screen voltage supplies minimize signal voltage development at the screen grid. Therefore, C_m contributes slight additional input capacitance.

Screen grids also reduce output capacitance by shielding the plate from the control grid. C_m charging current flows through the triode plate load

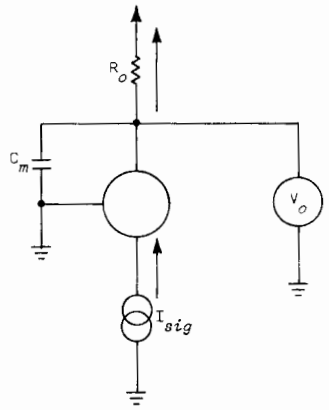


Fig. 5-39. C_m charge current isolated from the signal source.

isolating input element reduces risetime

(or collector load, or drain load) as well as the signal source. It seems then that isolating the control grid, or base, or gate, of three-terminal devices should reduce both input and output capacitance; and the reduction will reduce circuit risetime. This is the basis for the common-base, or common-gate, or common-grid amplifier.

See Fig. 5-39. Signal current flows into the emitter, source or cathode and develops output voltage across R_o. C_m and the negative input terminal return to ground. C_m makes up a part of output capacitance (C_o) but none of the input capacitance (C_i). The major advantage of a grounded grid amplifier, isolating C_m and the input, represents risetime improvement.

Gain relationships remain $A_V = \frac{R_o}{R_i}$. R_o and R_i consist of the same components. However, since signal generators drive emitters, sources or cathodes, input resistance is very low. Further, output current, input current and signal generator current are one and the same. Therefore, the active device merely isolates R_o and the signal current generator, without inverting the signal.

Not all signal generators perform as current sources. Fig. 5-40 is driven by a voltage generator. The voltage source develops input voltage across R_i. R_i consists of the sum of voltage source internal resistance, external resistance and $\frac{1}{gm}$. Ohm's law establishes input current (I_{sig}) which is output current (I_{sig}). Recall that amplifiers attempt to maintain a voltage null between input terminals.

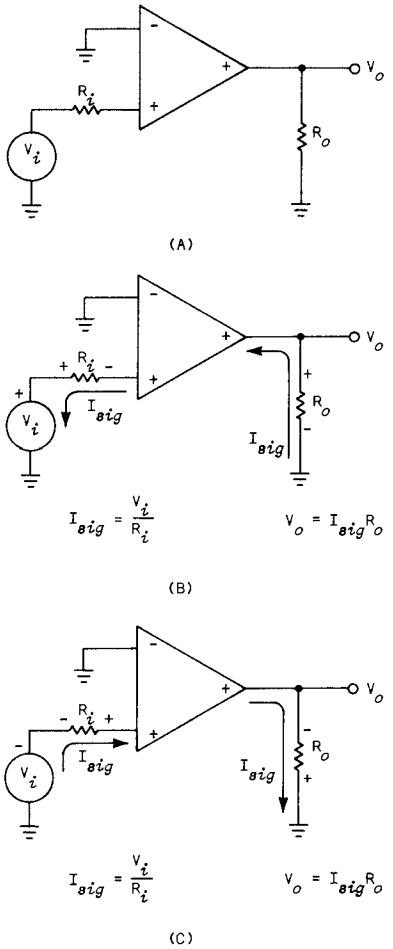


Fig. 5-40. Common base, common gate or common-grid signal current flows through R_o and R_i in series.

Fig. 5-40 shows the (-) terminal grounded, which may be *actual* ground, *apparent* ground or *virtual* ground. Therefore R_i shunts the signal source to ground. This is one reason grounded (-) input amplifiers seldom occur as a single stage in vertical amplifiers.

cascoding amplifiers

Amplifier combinations do occur. Connected in series, a common-cathode amplifier drives a common-grid amplifier in Fig. 5-41. *Cascoding* amplifiers in this fashion makes use of the best features of both: Lower input capacitance and lower output capacitance than the common cathode amplifier alone, yet the signal source need not furnish amplifier current.

The technique of cascoding causes a triode amplifier pair to appear as an efficient pentode amplifier. These triodes connected in series work into a T-coil plate load. Common-cathode amplifier, V1, drives common-grid amplifier, V2. V2 grid, returned to apparent ground, isolates output voltage variations from the input of V1. All of the signal current generated in the cathode of V1 flows in the output load, L1-R2. This is an advantage over pentodes. (No signal current diverted to the screen circuit.)

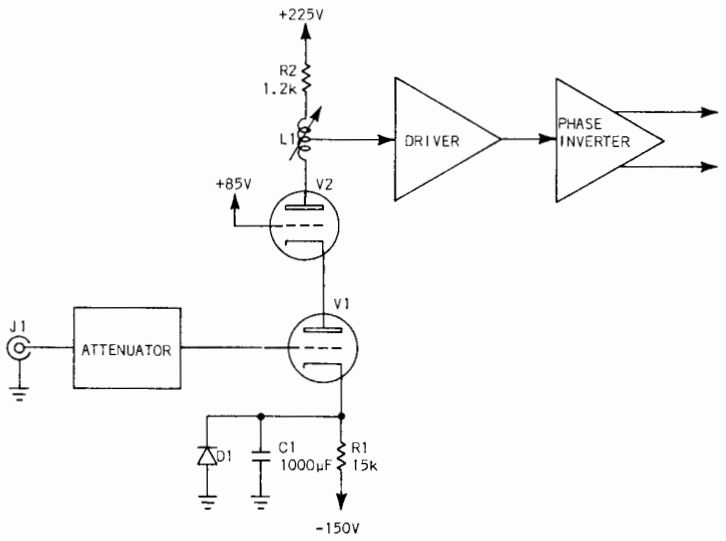


Fig. 5-41. Cascoding.

Stabilized by longtailing and plate voltage regulation, V1 is a common-cathode, AC voltage amplifier. Capacitor, C1 bypasses longtail resistor R1, and D1 clamps to protect C1. V1 drives a very low resistance load, the internal cathode resistance of V2. V2 also tends to function as a series regulator, holding V1 plate voltage constant. This results from V2 grid returning to a low impedance, regulated voltage source.

Before appreciable voltage variations occur across V1, quite large signal currents must be generated.

Cascoding reduces reflected resistance by about the square of μ. R_i develops in the cathode of V1: Assuming C1 bypasses R1, $R_{i1} = r_k + R_p$, $r_k = \frac{1}{gm} \approx 200\ \Omega$, and $R_p = \frac{R_o}{\mu + 1} \simeq \frac{R_o}{20}$.

R_o, for V1, is the internal cathode impedance of V2, R_{i2}:

$$R_{i2} = r_k + R_p = \frac{1}{gm} + \frac{R2}{\mu + 1} \simeq 200 + \frac{1200}{20} \simeq 260\ \Omega.$$

Therefore:

$$R_{i1} = r_k + R_p = \frac{1}{gm} + \frac{R_{i2}}{\mu + 1} \simeq 200 + \frac{260}{20} \simeq 213\ \Omega.$$

R_p, in this case, is small enough to ignore:

Consider r_k of V1 as R_i.

An advantage, besides parameter improvement, results from the characteristics of V1 plate and V2 cathode junction. This junction provides a low capacitance, low impedance point for additional circuitry such as switching, additional current feed, or even signal pick-off.

V2 drives a terminated transmission line. Output impedance appears resistive to a broad frequency spectrum. Output capacitance of V2, input capacitance of the driver amplifier, and L1 make up the transmission line reactive components. R2 terminates the line. Adjusting L1 matches line impedance to terminator resistance.

Compute gain as the resistance ratio, $\frac{R_o}{R_i}$. R_o = R2 and R_i = r_k (V1). Assume V1 r_k = 200 Ω:

$$A_V = \frac{R2}{r_k} = \frac{1200}{200} = 6.$$

One can solve for gain ignoring V1 plate circuit and V2 cathode circuit because signal current flows through V1 and V2 in series, and V1 cathode circuit determines total signal current.

Solved individually, the product of V1 gain and V2 gain gives total stage gain. Although more cumbersome this method reveals circuit characteristics:

Assume V1 and V2 are the same tube type. V1 then has a gain of about −1 and C_m is about 2 C_{gp}.

V1) R_o = V2 r_k + R_r, and R_i = V1 r_k.

$$A_V = \frac{260}{200} = 1.3$$

$$C_m = C_{gp}\ (1 + A_V) = 2.3\ C_{gp}$$

V2 has a higher gain (r_k = 200) and no Miller-effect.

V2) R_o = R2 and R_i = V2 r_k + R_r

$$A_V = \frac{1200}{260} = 4.63$$

$$\text{Total gain} = A_{V1}\ (A_{V2}) = 1.3\ (4.63) \simeq 6.$$

Reducing the gain of V1 reduces Miller-effect. Replacing V2 with a higher *gm* device would accomplish the reduction since R_o for V1 ≈ $\frac{1}{gm}$ (V2). One might very well replace V2 with a transistor. In fact, replacing either V1 or V2 or both with semiconductors is possible. Cascoding concepts do not change.

6

DIFFERENTIAL AMPLIFIER FAMILY

signal drive

The differential family consists of three amplifier types: push-pull, paraphase and differential. Basically, signal drive determines whether the amplifier functions as push-pull, paraphase or differential. Block (A) of Fig. 6-1 represents the differential family. Input voltage applied across the input terminals appears, amplified and inverted, as output voltage across the output terminals. One can easily imply voltage changes at both input terminals of (A). Blocks such as (A) therefore usually indicate either push-pull or differential amplification. Block (B) symbolizes paraphase amplification specifically. Grounding the (+) input restricts signal voltages to single-ended. The input voltage then develops across the output as push-pull.

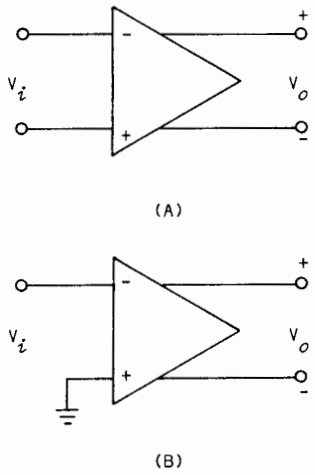


Fig. 6-1. Blocks representing the differential family.

Push-pull amplifier configuration constitutes the bulk of vertical amplifier stages. Early in the signal's history push-pull conversion occurs and CRT vertical deflection plates receive drive in push-pull form to provide optimum linearity. Generally, increasing stages of push-pull amplification, between input and CRT, improves signal balance. Drive to a conventional vertical amplifier input, usually single-ended, becomes phase inverted after one to four stages of single-ended amplification. Phase splitters as input amplifiers do exist but are an exception, in conventional, real-time, vertical amplifiers. Single-ended amplifiers provide a simpler means of switched attenuation and small signal (AC) frequency compensation. Once the advantages of single-ended amplification are realized, a phase inverter acts on the signal. One single-ended stage is most common, four being most uncommon. Single-ended amplifiers usually drive a phase inverter at a fixed deflection factor. From the phase inverter to the CRT, a vertical system is a high-fidelity voltage amplifier, usually direct-coupled.

single-ended input

Push-pull amplifiers in this book share in general some characteristics:

1. They are direct coupled.
2. Input signal currents develop in the emitter (source or cathode) circuit.
3. They are emitter (source or cathode) coupled.
4. They are stabilized by longtailing.
5. Small collector (drain or plate) load resistance maintains risetime requirements ($2.2\ RC = t_r$).
6. Miller-effect exists as a function of gain. $C_m = C_{gp}\ (1 + A_V)$ or $C_m = C_{bc}\ (1 + A_V)$ or $C_m = C_{gd}\ (1 + A_V)$.

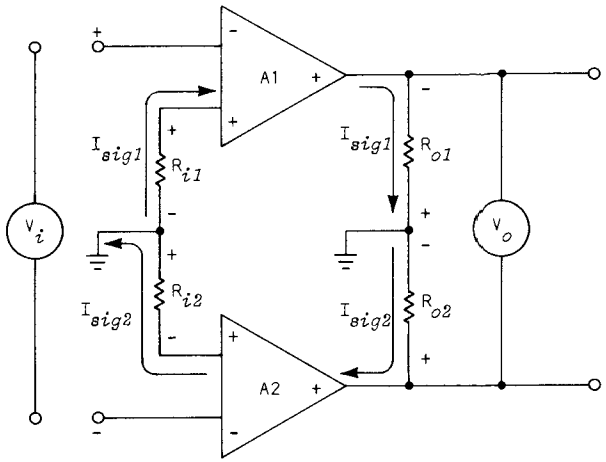


Fig. 6-2. Push-pull amplification.

To "build" a push-pull amplifier one need only drive an identical pair of common-emitter, common-source or common-cathode amplifiers push-pull. Fig. 6-2 shows this configuration. A1 and A2 are identical amplifiers: $R_{i1} = R_{i2}$ and $R_{o1} = R_{o2}$. V_i is a push-pull voltage. The positive voltage applied to A1 equals, in amplitude, the negative voltage applied to A2. This causes a negative voltage to develop across R_{o1} equal to the positive voltage which develops across R_{o2}.

Amplifiers *attempt* to maintain a null across the input terminals. A1 reacts to the positive input by dropping an equal voltage across R_{i1}. Signal current (I_{sig}) flows from ground, through R_i and into the (+) input terminal. I_{sig1} flowing out of A1 and through R_{o1} to ground, develops a negative voltage across R_{o1}.

A2 reacts in the same fashion: To maintain the null across input terminals, A2 must drop a voltage across R_{i2} equal to the voltage at the (-) input terminal. I_{sig2} develops input voltage across R_{i2}. I_{sig2} *apparently* flows from ground, through R_{o2}, developing a positive output voltage, and into the output terminal of A2. I_{sig2} then flows out of the (+) input terminal, through R_{i2} to ground.

A1 and A2 need not be identified as separate amplifiers: V_i creates I_{sig1} and I_{sig2}. Since $R_{i1} = R_{i2}$, and $R_{O1} = R_{O2}$, then $I_{sig1} = I_{sig2}$. Further, the origin of one current is the return for the other. Therefore, one assumes series input current (I_{sig}) equal to either I_{sig1} or I_{sig2}. $I_{sig} = I_{sig1} = I_{sig2}$. Now follow the closed loop: I_{sig} flows out of A1, through R_{O1}, R_{O2}, into the output terminal of A2, out the (+) input terminal of A2, through R_{i2}, R_{i1}, and into the (+) input terminal of A1.

Following the same line of reason, I_{sig} develops V_i across R_{i1} and R_{i2}: $V_i = I_{sig}(R_{i1} + R_{i2})$. Why not combine R_{i1} and R_{i2} for total input resistance? $R_i = R_{i1} + R_{i2}$, therefore $V_i = I_{sig}R_i$. Treat R_{O1} and R_{O2} the same way: $V_O = I_{sig}(R_{O1} + R_{O2})$. Total $R_O = R_{O1} + R_{O2}$. $V_O = I_{sig}R_O$.

Simplify by combining components. See Fig. 6-3.

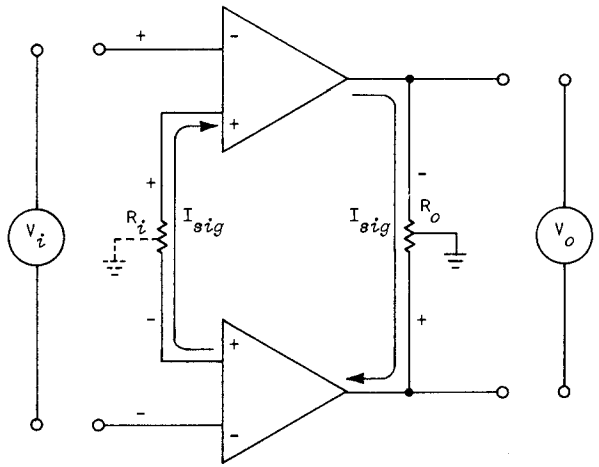


Fig. 6-3. Push-pull amplifier.

voltage difference

I_{sig} results from the voltage *difference* across R_i: $V_i = +V-(-V)$. If +1 volt appeared at the upper input terminal and -1 volt at the lower: $V_i = +1 - (-1) = 2$ V. It is important to think of V_i as the voltage *difference* between input terminals. Series signal currents satisfy expressing voltage gain by the ratio $\frac{R_o}{R_i}$.

signal ground

Fig. 6-3 shows signal ground at the center of R_i and R_o. Signal ground can be one of three types:

1. Actual ground -- chassis or common return.
2. Apparent ground -- a low-impedance point to actual AC ground, such as a bypass capacitor or power supply.
3. Virtual ground -- a summation or meeting point for two signals of equal amplitude and frequency but of opposite phase.

Actual or apparent grounds frequently appear at the electrical center of R_o; occasionally this is a virtual ground. On the other hand push-pull amplifiers, connected as shown, always develop a virtual ground along the electrical length of R_i. This is because when a negative voltage develops at one end of R_i a positive voltage develops at the other end. Zero volts (virtual ground) must then develop somewhere along the resistive length of R_i. If V_i were perfectly balanced, virtual ground would appear halfway along R_i. Unbalanced signals shift virtual ground proportional to the imbalance.

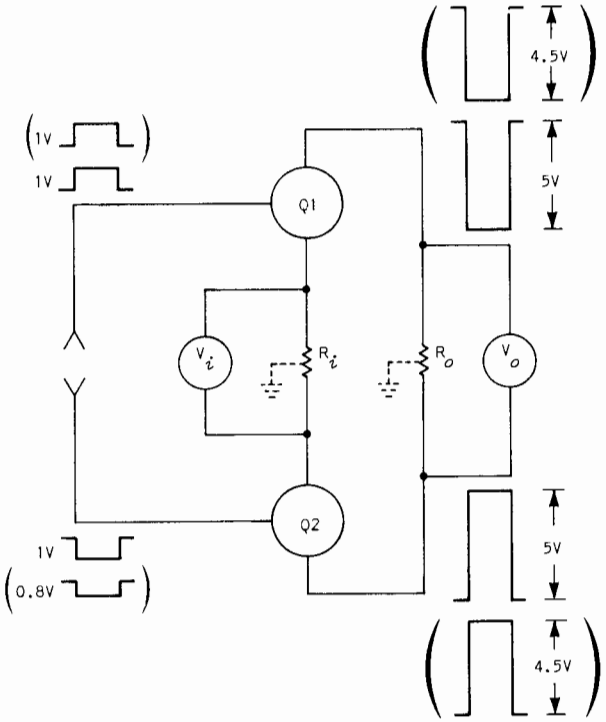


Fig. 6-4. Push-pull model balances signal voltages.

push-pull balances input signal

Push-pull amplifiers tend to correct unbalanced signal drive. Assume the active devices are transistors. Refer to Fig. 6-4 and ignore, for now, the bracketed waveforms. Voltages, of equal amplitude and opposite phase, drive the bases of active devices Q1 and Q2. Input voltage difference across R_i causes signal current to develop. Quantity of current depends upon the value of R_i and the difference voltage amplitude (measured from the base of Q1 to the base of Q2). $I = \frac{E}{R}$. This total emitter current flows through the active devices and R_o. Output voltage develops across R_o.

Signal ground appears at the center of R_i. Signal current flows through R_i, Q1, R_o and Q2. Voltage gain results from the ratio $\frac{R_o}{R_i}$. R_o consists of collector load components (collector of Q1 to the

collector of Q2). R_i consists of the internal resistance of Q1, plus external components from emitter of Q1 to emitter of Q2, plus the internal resistance of Q2.

Virtual ground helps illustrate the balancing action of an emitter coupled, push-pull amplifier. In Fig. 6-4, a 2-volt signal, and R_i, cause current flow through R_o developing 10 volts output signal. Voltage gain ($\frac{V_o}{V_i}$) is 5, so $\frac{R_o}{R_i}$ must be 5. Signals measured from either input to ground, as measured with an oscilloscope, are equal at one volt amplitude. Output voltage amplitude, from either Q1 or Q2 to ground, is 5 volts. Voltage gain then can also be expressed as $\frac{R_o}{R_i}\ \frac{(Q1)}{(Q1)}$ or $\frac{R_o}{R_i}\ \frac{(Q2)}{(Q2)}$, R_i being from one input terminal to *virtual* ground, and R_o from one output terminal to *apparent* ground. Virtual ground appears at the resistive center of R_i because the input signal voltages are of equal amplitude but opposite polarity. Unequality shifts virtual ground off the center point of R_i. Refer to the bracketed waveforms in Fig. 6-4.

The bracketed waveforms show that a gain of five remains. Output waveforms balance though the inputs do not. Measured from the input terminal of Q1 to ground one sees a one-volt signal. At the input terminal of Q2 one measures an opposite polarity but unequal amplitude signal, 0.2 volts less than the Q1 input. Emitter coupling causes the virtual ground to shift, decreasing Q1 voltage gain and increasing Q2 voltage gain. Total circuit gain remains the same. 9 volts output results from a 1.8 volts input: $\frac{V_o}{V_i} = \frac{9}{1.8} = 5 = \frac{R_o}{R_i}$. However, Q1 gain is now 4.5 and Q2, approximately 5.6.

Complete balancing, indicated here, does not occur. Output signals closely approach balance and each additional stage of push-pull amplification brings them into better balance. Further, all explanations assume coincidence of input pulses.

emitter-coupled push-pull amplifier

Fig. 6-5 is a typical emitter-coupled push-pull amplifier. The circuit features gain control and emitter peaking.

A quiescent "on" condition exists. The emitters return to a positive supply through resistors R2 and R3, and the bases set at zero volts. R2 and R3 should be well matched so little DC current flows through R1. Some circuits replace R2 and R3 with a potentiometer, set for no quiescent current flow in R1.

Total signal current demanded results from the signal voltage difference across the total emitter-to-emitter resistance. If one ignores C1, emitter resistance (R_E) is R1 in parallel with R2 and R3. Maximum input resistance for this circuit is about 140 Ω and minimum; R_{t1} plus R_{t2}. Input resistance determines stage degeneration or gain so R1 is labeled GAIN.

gain

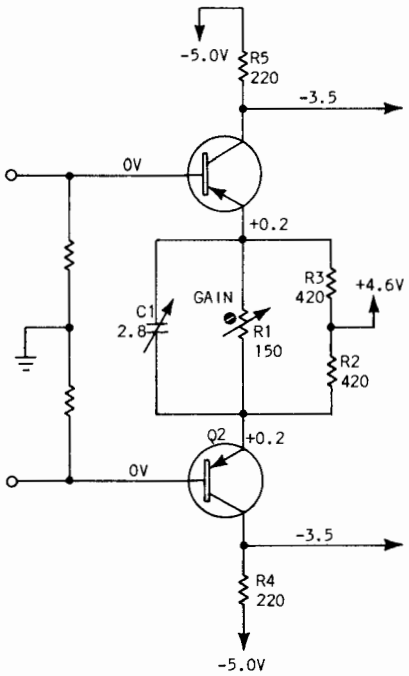


Fig. 6-5. Typical emitter coupled amplifier.

Gain approximation is a ratio of output to input resistance. R_O is the sum of collector loads, R4 and R5, in this case. One expects 60 millivolts V_O resulting from 10 millivolts drive (adjustments set to midrange):

$$A_V = \frac{R_O}{R_i}$$

$R_i = R_t + R_E$ $\qquad$ $R_O = R4 + R5$

$R_E = \frac{R1\ (R2 + R3)}{R1 + R2 + R3}$ $\qquad$ $R_O = 440$

$R_E(\text{max}) = \frac{150\ (840)}{150 + (840)} = 127\ \Omega$

$R_E(\text{min}) = 0$

* R_E (R1 centered) $= \frac{75\ (840)}{75 + 840} = 69\ \Omega$

$R_t = (2)(\frac{R_B}{\beta} + \frac{R_D}{\beta} + r_e)$

$r_e = \frac{26}{I_e\ \text{mA}}$ (Q1 or Q2) $= \frac{26}{10.5} = 2.5\ \Omega$

* $R_t \simeq 6$

$R_i = 6 + 69 = 75\ \Omega$

$A_V = \frac{R_O}{R_i} = \frac{440}{75} \simeq 6$

Notice that R_t has little effect upon the gain approximation. When about 10 mA quiescent emitter current flows one can frequently ignore R_t and assume $R_i = R_E$. For example, round off R_E of Fig. 6-5 to 70. A_V then solves to 6.3. Realizing that R_i is low, one rounds off to: $A_V \simeq 6$.

Capacitance in the output exists whether shown schematically or not. This capacitance is not a fixed and unvariable value but does become a part of an output RC. Emitter peaking optimizes risetime when $\rho = 1$. C1, selected to cover a wide range of output capacitance, adjusts to empirically match input to output RC. C1 can also be over or under peaked to compensate for overall system deficiencies. Chapter 5 covers this peaking technique in more detail under the heading "Cathode Peaking." When $\rho = 1$ (output RC equals input RC) output impedance

to input impedance and output resistance to input resistance ratios equal. Gain then should be constant for all waveshapes.

If $\rho = 1$, $RC_O = RC_i$, then $\frac{Z_O}{Z_i} = \frac{R_O}{R_i}$.

$$R_O = R4 + R5$$

$$C_O = Q1\ C_O + Q2\ C_O$$

$$R_i = R_E$$

$$C_i = C1$$

R2 and R3 shunt R1 to prevent quiescent current flow through R1. Q2 emitter current flows through R2 and Q1 through R3. If there were no requirement for a gain adjustment, a single resistor could serve for both transistors. This is one advantage of push-pull operation: Both emitter currents flow through a common return, which need not be bypassed by a sag-producing capacitor.

Fig. 6-6 contains a longtail (R3) common to Q1 and Q2 emitters. During center-screen operation equal voltage appears at the base of Q1 and Q2. Q1 and Q2 therefore draw equal current through R3, about 2 mA quiescently. This configuration has two basic advantages:

1. Push-pull currents effectively bypass R3 with no sag.
2. R3 appears twice the component value to either Q1 or Q2.

Quiescently Q1 and Q2 each draw about 2 mA I_e for a total of 4 mA through R3. A negative signal slightly over 100 millivolts, at the base of Q1, increases Q1 emitter current to 2.5 mA. Q2 simultaneously decreases emitter current demand to 1.5 mA, since Q2 base voltage must swing positive with Q1 positive base voltage. Current through R3 remains 4 mA. Therefore, the voltage drop across R3 doesn't change. A bypass capacitor is extra baggage.

To either transistor R3 has an apparent value of 66 kΩ. Balanced, each device draws about 2 mA I_e, which drops 130 volts across R3. Apply Ohm's Law to solve for R3, using either Q1 or Q2 emitter

current and the drop across R3 as known values. R3 = 66 kΩ. Longtailing to this extent tends to oppose an unbalanced signal as a common mode-signal.

push-pull amplifiers reject common-mode signals

Q1 and Q2 react as a push-pull amplifier only when driven push-pull. Gain times the voltage *difference* between the base voltage of Q1 and Q2 still holds. In-phase signals of equal amplitude which arrive coincident are common mode. These could result from power supply fluctuations, transients coupled through a ground loop, or noise from the preceding stage.

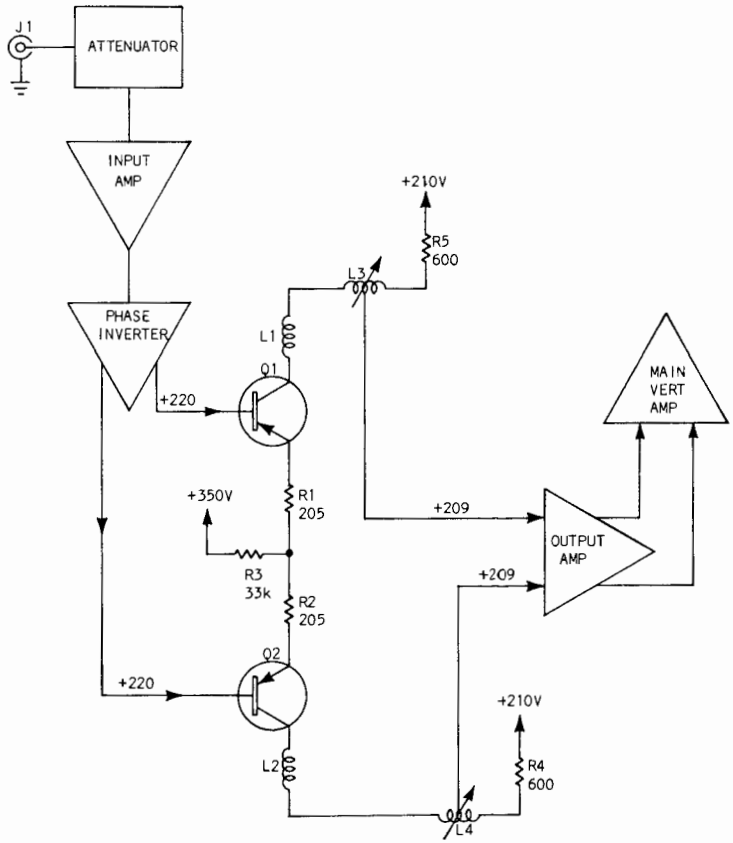


Fig. 6-6. Preamplifier driver amplifier.

Push-pull amplifiers tend to *reject* common-mode signals. Assume Q1 and Q2 base voltage become one volt more positive: According to an earlier statement, the input voltage difference is zero, therefore output voltage is zero. This is true due to longtailing. Both transistors reduce conduction causing about zero gain:

$2\ (R3) = R_i$ for each. $R5 = R_o$.

$$A_V = \frac{R_o}{R_i} = \frac{R5}{2\ (R3)} \text{ or } \frac{R4}{2\ (R3)} = \frac{0.6\ k\Omega}{66\ k\Omega} \simeq 0.009$$

Each collector becomes 9 mV more negative for each 1000 mV common mode signal at the input. The following push-pull stage rejects the 9 mV signal similarly.

A figure called *common-mode rejection-ratio* (CMRR) expresses the limitation of a differential amplifier to reject common mode signals. CMRR gives the amplitude of input signal necessary to develop one unit of output common mode signal. The amplifier in Fig. 6-6 develops 9 mV out for each 1000 mV in. $CMRR = \frac{1000}{9} = 110{:}1$. This is a fairly high figure for push-pull type amplifiers.

The quotient of $\frac{R_o}{R_i}$ for push-pull gain includes R4 and R5 but not R3: $R_o = R4 + R5 = 1.2\ k\Omega$.

$R_i = R_{t2} + R2 + R1 + R_{t1}$. Check r_e: $r_e = \frac{26}{I_e\ mA} = 13\ \Omega$, so assign each R_t a value of 20.

$$R_i \simeq 20 + 205 + 205 + 20 \simeq 450\ \Omega.$$

$$A_V = \frac{R_o}{R_i} \simeq \frac{1.2\ k\Omega}{0.45\ k\Omega}$$

$$A_V \simeq 2.6.$$

Q1 output capacitance, L1, L3, following stage input capacitance, and R5 make up a series peaked T-coil load. Q2 output capacitance, L2, L4, following stage input capacitance, and R4 perform in the same fashion. T-coil peaking improves risetime, which one empirically sets with L3 and L4.

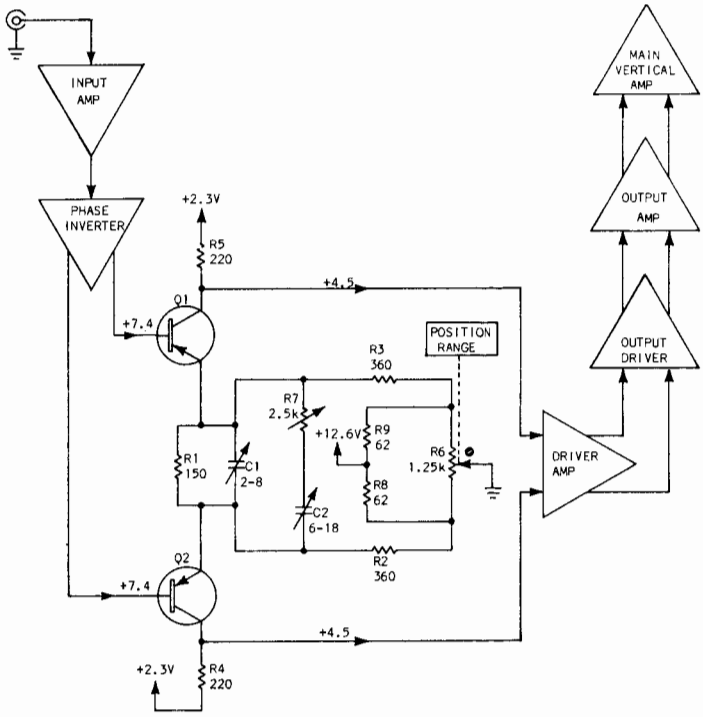


Fig. 6-7. Low signal driver amplifier.

low-signal driver amplifier

Because of low impedance, emitter circuits frequently contain both steady state and transient adjustments. The circuit of Fig. 6-7 is an example. This amplifier produces a gain of 3.5, contains emitter peaking, and provides an internal adjustment to calibrate a front panel control.

First determine quiescent emitter current assuming R6 set to midrange: I_e must develop 7.6 volts at Q1 and Q2 emitters. Further, Q1 I_e = Q2 I_e. Therefore solve for Q1 only: Total Q1 emitter current flows through R3 then splits, a portion flows through R9 and a portion through R6. R9 and R6 present an equivalent resistance of 56 ohms returned to +11.5 volts. I_e drops about 4.1 volts across 416 ohms, total emitter resistance of Q1.

$$I_e = \frac{V_i}{R_E} = 10 \text{ mA.}$$

10 mA I_e causes R_t to equal about 5 Ω. Ignore R_t when computing R_i for the push-pull gain approximation: R_i, for "slow" inputs, consists of R1 paralleled by network, R2, R3, R6, R8 and R9. The network presents a total resistance of 832 Ω, emitter to emitter. 150 Ω shunts 832 Ω to develop R_i: R_i = 125 Ω.

$$A_V = \frac{R_O}{R_i} = \frac{R4 + R5}{R} = \frac{440}{125}$$

$$A_V \simeq 3.5$$

C1, C2 and R7 emitter peak:

1. Output capacitance (C_O) shunts R4 and R5 (R_O).
2. When $\rho = \frac{R_E C_E}{R_O C_O} = 1$, the stage degrades risetime the least, with minimum overshoot.
3. C1, C2 and R7 set $R_E C_E$.

C2 and R7 establish the initial slope of an output step, and C1 controls the percentage of overshoot. Also, keep in mind that an individual stage might be "overpeaked", compensating for preceding or following stage reaction.

centering

Position Range, R6, really functions as an internal centering adjustment for the front panel POSITION control. Under no-signal conditions with the front panel POSITION control centered, the CRT display should vertically center. If, under these conditions, the trace fails to center, adjustment of R6 corrects the off-center display. R6 adjustments change the percentage of total emitter current drawn by each transistor. This causes different collector DC levels, changing the level of each following direct-coupled stage.

The above explanation assumes unbalanced following stages. Should Q1 and Q2 base voltages quiescently differ, adjusting R6 redistributes longtail current. This minimizes quiescent current flow through R1.

Please note: In Tektronix instruments, an adjustment should never be at an extreme setting. If an adjustment sets more than several degrees off center, suspect a discrepancy.

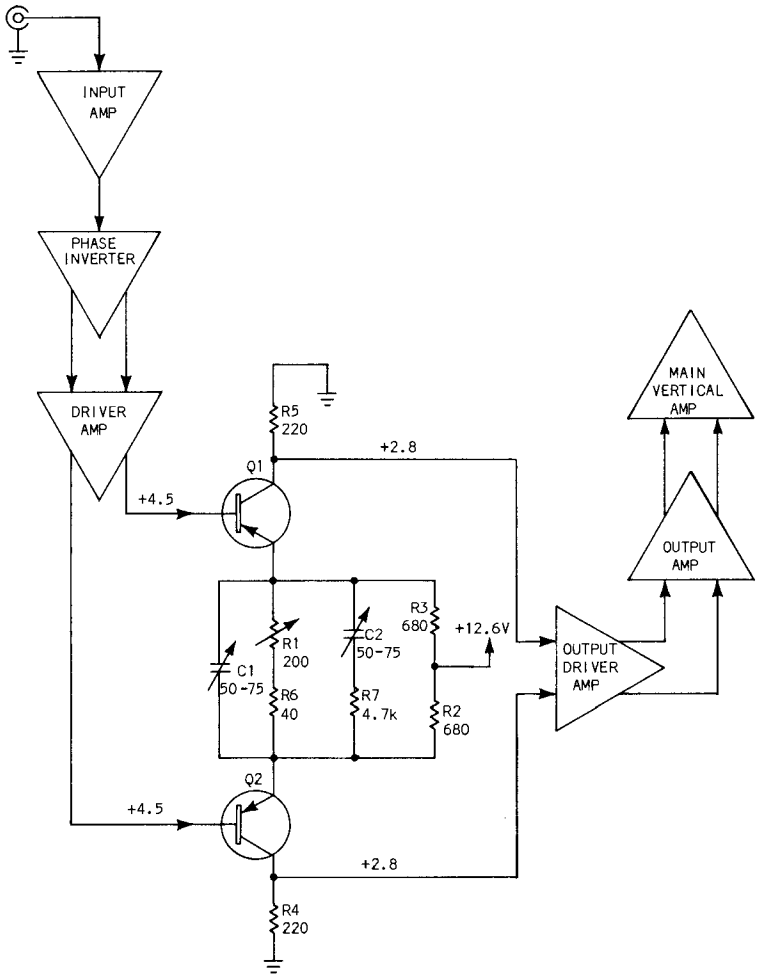


Fig. 6-8. Low signal driver amp.

Fig. 6-8 shows a circuit very similar to Fig. 6-7. R2 and R3 longtail. Q1 or Q2 quiescently draw 12 mA. C1, C2 and R7, combined with the output RC, emitter peak. R1 sets stage gain.

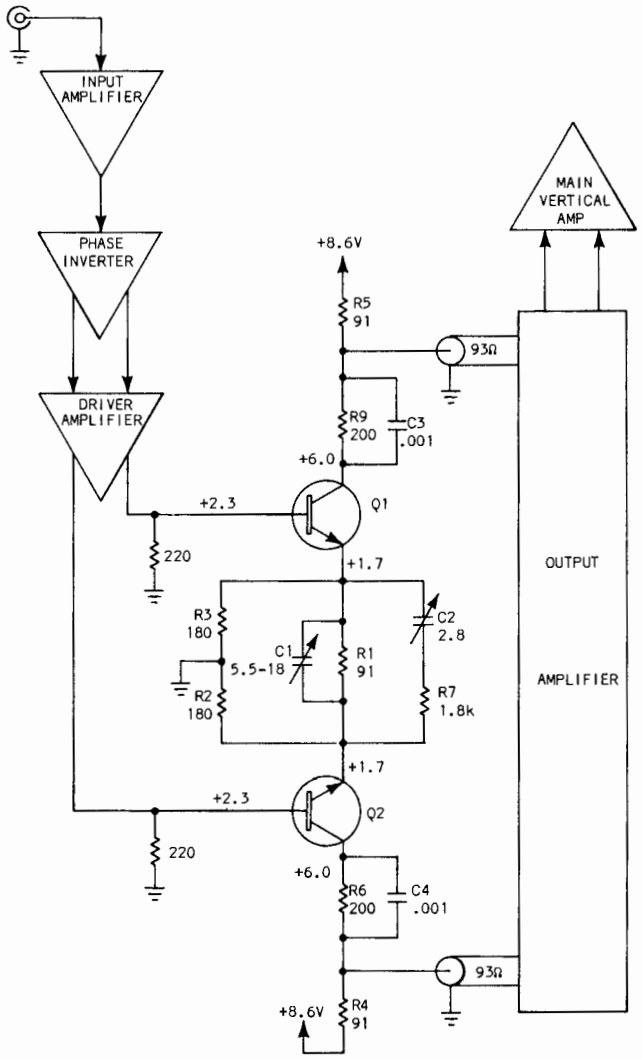


Fig. 6-9. Output driver amplifier.

Again, since I_e = 12 mA, one can ignore R_t. R1 and R6, paralleled by R2 and R3, fix R_i. R_o = R4 + R5. R1 adjustments set R_i to:

Max $R_i \simeq 200\ \Omega$.

Min $R_i \simeq 39\ \Omega$ (should probably add R_t here = 6 Ω or so).

$$\text{Mid } R_i \simeq 125\ \Omega.$$

$$A_V = \frac{R_O}{R_i}$$

$$A_V = \frac{R4 + R5}{125}$$

$$A_V = 3.5.$$

Preamplifier output amplifiers frequently provide a voltage gain of unity or less. They usually function as impedance matching and isolation devices. For these reasons followers appear most often as preamplifier outputs. In the following case a common-emitter push-pull amplifier drives a coaxial transmission line.

coax-driver amplifier

Refer to Fig. 6-9. The push-pull amplifier, driving a 93-ohm coaxial line, features emitter peaking and temperature compensation. Low impedance-low voltage about sums up this circuit. R2 and R3 are balanced to prevent flow of quiescent currents through R1. Since Q1 and Q2, silicon devices, drop 0.6 volts at their emitter-base junctions, 9.2 mA of quiescent emitter current develops.

temperature compensation

R6 and R9, bypassed by C3 and C4, temperature compensate. This technique imposes, on Q1 and Q2, maximum power dissipation at quiescence. To prove this, first identify component functions for possible elimination.

C1, C2 and R7 emitter peak. This is a circuit where neither R_i nor R_O are obvious. Prior knowledge of the overall block helps. Deflection factors at both input and output are 100 mV/div: $A_V = \frac{R_O}{R_i} = 1$, Therefore $R_O = R_i$. One can still utilize the rules-of-thumb and arrive at an approximation of unity gain.

Output signals are taken across R4 and R5. R4 and R5 values and the Z_O of the coax cable about match. Assume that R_O consists of R4 paralleled by Z_O and R5 paralleled by Z_O: $\frac{(91)\ 93}{91 + 93} + \frac{(91)\ 93}{91 + 93} \simeq 91\ \Omega.$

Prior knowledge of the unity gain requirement allows one to assume R_i = R1; $A_V = \frac{R_O}{R_i} = 1$ and $R_O = 91\ \Omega$.

Lack of this evidence requires a judgment about R_t for an accurate gain approximation. R1, shunted by R2 and R3, couples the emitters with 73 ohms. Ignoring R_t, gain is 1.25. This should seem strange enough to test:

$$R_t = r_e + \frac{R_b + R_B}{\beta}, \text{ assume } \beta = 50$$

$$\text{Q1 or Q2 } r_e = \frac{26}{I_e \text{mA}} = \frac{26}{9.2} = 2.8\ \Omega$$

$$\frac{RB}{\beta} = \frac{220}{50} = 4\ \Omega$$

$$R_t = 5.6\ \Omega + 8\ \Omega + 2\ (\frac{R_b}{3}) = 13.6 + 2\ (\frac{R_b}{3})$$

$$R_i = R_E + R_t$$

$$R_i = 73 + 13.6 + 2\ (\frac{R_b}{3})$$

$$R_i = 86.6 + 2\ (\frac{R_b}{3})$$

Assign the last factor a value of zero

$$A_V = \frac{R_o}{R_i} \simeq \frac{91}{86.6} \simeq 1.05$$

This is close enough to unity to justify assigning R_i to R1. When gain estimates seem unreasonable, and R_i approaches the resistance of R_o, suspect the requirement for adding R_t. This is especially true when R_o and R_i are small resistance values, as in Fig. 6-9.

Signal current flows through R9 and R5 in series. With C3 out of the circuit, "Miller-effect" results, degrading signals of even medium risetime. R9 corrects for relatively slow thermal changes. Therefore, C3 bypasses R9 to reduce "Miller-effect" without affecting temperature compensations. C3 takes sufficiently long to charge that Q1 collector voltage changes little during an input step transition. Signal current does flow through R_o (R5 and coax Z_o), developing the output step. Q2 collector-circuit components, C4, R6 and R4 react the same.

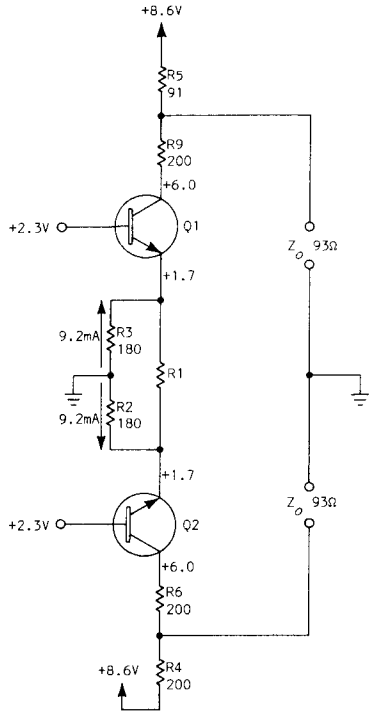


Fig. 6-10. Temperature compensating Q1 and Q2 by developing $V_C = \frac{V_{CC}}{2}$.

The components needed to discuss temperature compensation, Q1, Q2, R1, R2, R3, R4, R5, R6, R9 and the coax Z_O appear in Fig. 6-10. R2 and R3 return to ground, making V_{CC} equal to the +8.6 V collector supply. Thermal compensation results when Q1 and Q2 dissipate maximum power at quiescence. This only occurs when V_C, at quiescence, equals one half V_{CC}. In other words R3, R9 and R5 should drop 4.3 volts, leaving 4.3 volts to develop across Q1. Meeting this condition, any collector current change reduces Q1 and Q2 power dissipation.

sag

Signals resulting from heat effects are slow moving. Thermal signals occur at less than 80 kHz, or in terms of transit response, produce sag. Sag can be positive or negative. How much V_{ce} differs from $\frac{V_{CC}}{2}$ sets the initial slope rate. Ri determines the ultimate sag: Output waveform error $\simeq \frac{V_{ce} \text{ bias error}}{R_E}$.

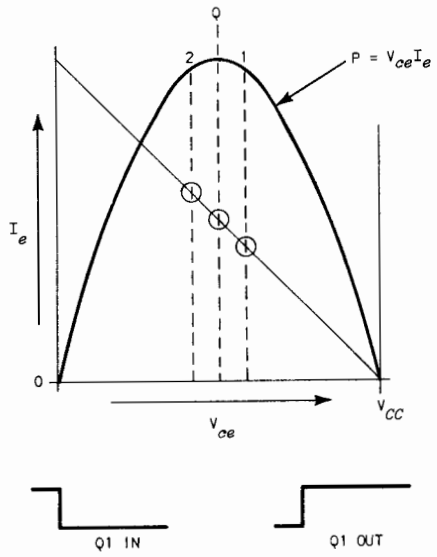


Fig. 6-11. $V_{ce} = \frac{V_{CC}}{2}$. Optimized, differential, temperature tracking.

Fig. 6-11 shows the optimized plot. This figure, and the two following include Q1 input and output waveshapes. Assume Q2 waveshapes differ only in polarity. Q1 and Q2, biased at 1/2 V_{CC} (Q), dissipate maximum power at quiescence. An input signal changes I_e of each transistor causing both to cool. Junction temperature slowly reduces, creating junction voltage (V_{be}) changes. Temperature and V_{be} changes track, developing a common-mode signal equal to V_{be}. There is no distortion since the signal *difference* between input terminals remains the same.

thermal signal

Dissipating less than maximum power at quiescence results in thermal signal differences across the input terminals. The thermal signal adds to, or subtracts from, desired signal voltages, increasing or decreasing effective gain. If V_{ce} is below 0.5 V_{CC}, effective gain decreases, producing negative sag. Setting V_{ce} above 0.5 V_{CC} results in positive sag.

Fig. 6-12 represents the V_{ce} plot of Q1 and Q2 when V_{ce} is less than $V_{CC}/2$. Quiescently, Q1 and Q2 dissipate less than maximum power. With a negative input to Q1, Q1 current decreases but power increases, while Q2, receiving a positive input, current increases reducing device power. ΔP is negative:

Q1 heats,

Q2 cools,

Q1 V_{be} decreases,

Q2 V_{be} increases.

Effective signal, or gain, decreases, creating negative sag.

Reversing step polarity, a positive input to Q1 and a negative to Q2, only reverses the device heated. Negative sag still develops:

Q1 cools,

Q2 heats,

Q1 V_{be} increases,

Q2 V_{be} decreases.

Effective signal, or gain, again decreases, producing negative sag.

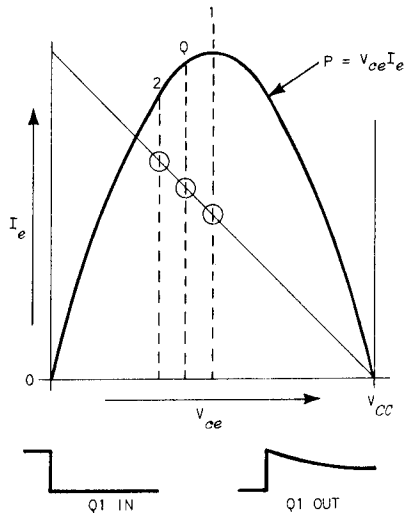


Fig. 6-12. $V_{ce} < \frac{V_{CC}}{2}$. Long-term thermal effect is negative sag.

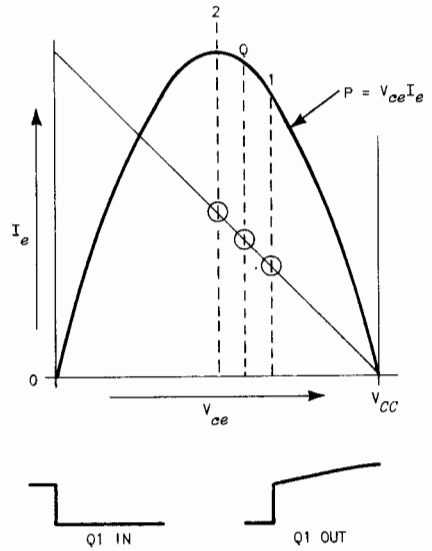


Fig. 6-13. $V_{ce} > \frac{V_{CC}}{2}$. Long-term effect is positive sag.

Fig 6-13 represents the plot when V_{ce} exceeds 1/2 V_{CC}. ΔP is positive developing a "hump" in the output step. With a negative input, Q1 conduction and power decreases and Q2 conduction and power increases:

Q1 cools,

Q2 heats,

Q1 V_{be} increases,

Q2 V_{be} decreases.

With a positive input Q1 power increases and Q2 power decreases:

Q1 heats,

Q2 cools,

Q1 V_{be} decreases,

Q2 V_{be} increases.

Either step polarity suffers effective signal or gain increase -- positive sag.

The thermal distortion usually occurs when $V_{ce} \neq \frac{V_{CC}}{2}$. It applies to common-emitter, common-base and common-collector amplifiers. Keep in mind that these are *slow* changes affecting the flat-top of a step.

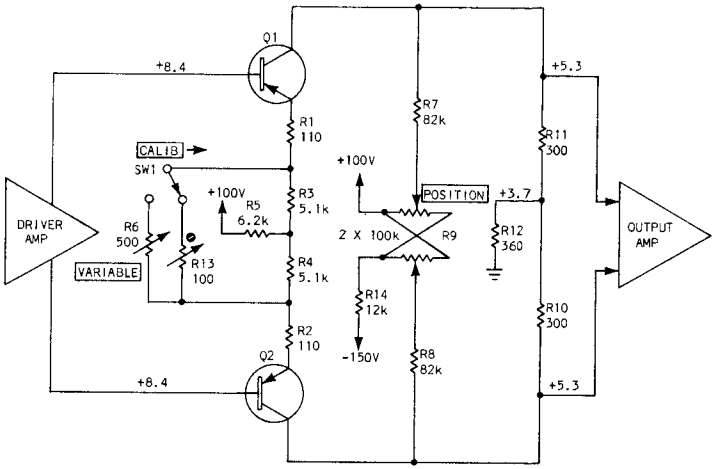


Fig. 6-14. Driver amplifier.

"control" amplifier

An appropriate term for the amplifier of Fig. 6-14 might be "control" amplifier. The circuit realizes a gain of about 2, but primarily provides balanced push-pull output, internal gain adjustment, and front panel controls (VERTICAL POSITION and VARIABLE VOLTS PER DIVISION).

R3, R4 and R5 longtail the amplifier. R1 and R2 degenerate and R5 added to R3 and R4 establishes common mode rejection.

Changing R13 varies gain, or degeneration, but not output DC levels. The ratio of output resistance to input resistance determines stage gain. The sum of R1, R2 and R13 defines R_i. No DC current flows in R13, so adjustment produces no positional drive to the next stage.

R6 affects the circuit as R13 except R6 adds more signal degeneration because of its greater resistance. The operator switches in R6, called VARIABLE VOLTS

PER DIVISION. Switched in, this control provides the user an *uncalibrated*, between-step, adjustment of system deflection factor.

Another operator control, R9, appears in the collector circuits of Q1 and Q2. Called VERTICAL POSITION, R9, moved off center, changes the DC level at the collectors in equal and opposite directions. Small differences in level, amplified by following direct coupled stages, move the trace vertically. High resistance of R7 and R8, shunting load resistors R10 and R11, insures negligible signal loading by the POSITION control.

Fig. 6-15 through 6-18 include circuit calculations. Emitter coupling circuits by now require little explanation.

Fig. 6-15 shows the equivalent circuit with R9 set to one extreme. First, recognize that collector voltage changes from quiescence represent a small percentage of the position control voltage return. Assume, therefore, that R7 drops 95 volts and R8 and R13, 145 volts. Now apply step-by-step logic and few computations are necessary:

1. 5.2 mA flows in each collector for a total of 10.4 mA.
2. R8 and R13 contribute 1.55 mA while R7 consumes 1.15 mA.
3. The difference between these currents yields a contribution of 0.4 mA.
4. 0.4 mA less current need flow through R12, thus 10 mA is the R12 current demand.
5. Q2 collector current flows from two sources, ground and the -150 volt supply. R8 and R13 provide 1.55 mA leaving 3.65 mA as current demand through R10. 1.55 + 3.65 = 5.2. 3.65 mA drops 1.1 volts across R10. +4.1 V_O results.

6. Q1 collector current originates at ground. However, the same source must provide 1.15 mA for the drop across R7. 5.2 + 1.15 = 6.35 mA. This current drops 1.9 volts across R11, setting V_O at +5.5 volts.

The difference between collector output voltages (800 mV) drives the following stage as positional voltage. 1600 mV (+800 to -800) represents a few CRT diameters.

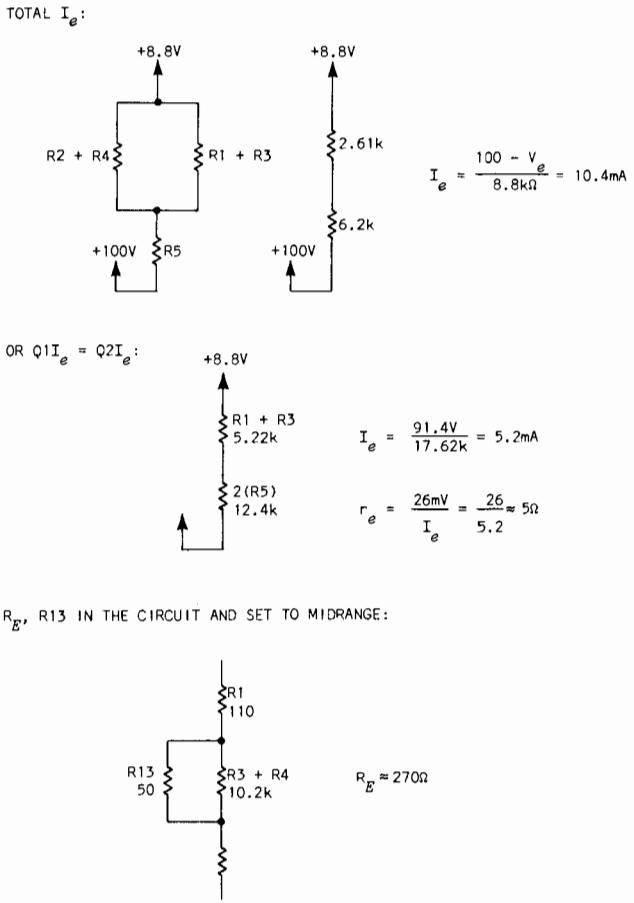
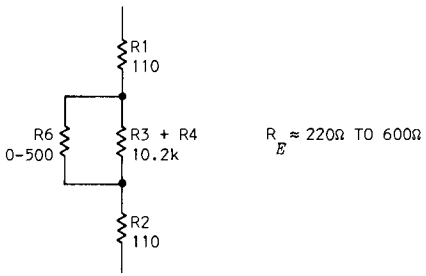


Fig. 6-15.

R_E, R6 IN THE CIRCUIT SET TO MAXIMUM AND MINIMUM:



$R_o = R10 + R11 = 600\Omega$

$R_i = R_E + R_t$

$R_i \approx 270 + 20 = 290\Omega$, R13 SET TO 50Ω

OR

$R_i = 220 + 20 = 240\Omega$, R6 SET TO 0Ω

$R_i = 600 + 20 = 620\Omega$, R6 SET TO 500Ω

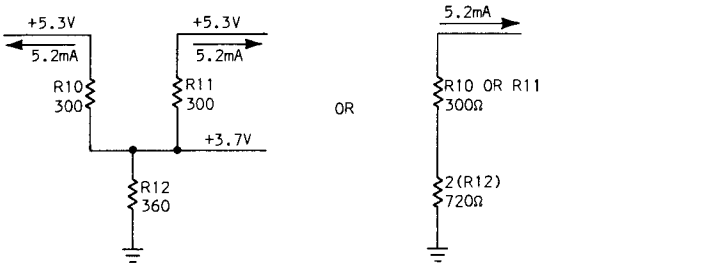
$$A_V(\text{BASIC}) = \frac{R_o}{R_i} = \frac{600}{290} = 2.04$$

$$A_V(\text{BASIC}) \approx 2.0$$

$$A_V(\text{VARIABLE}) = \frac{R_o}{R_i} = \frac{600}{240} \approx 2.5 \text{ OR } \frac{600}{620} \approx 1$$

Fig. 6-16.

ZERO SIGNAL V_o WITH R9 CENTERED:



$V = I_R = 10.4 \times 10^{-3} \times .51 \times 10^3$

$V \approx 5.3V$

$V = I_R = 5.2 \times 10^{-3} \times 1.02 \times 10^3$

$V \approx 5.3V$

POSITION CONTROL CENTERED:

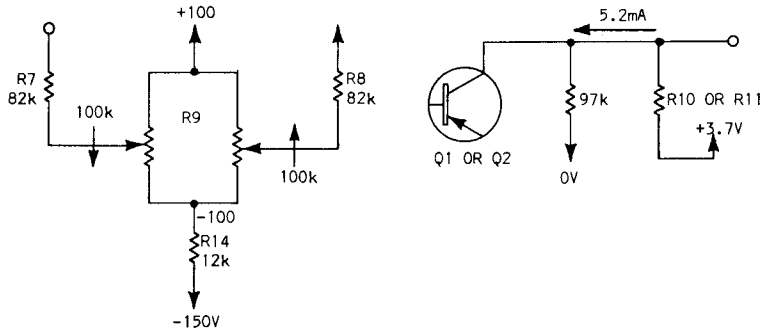


Fig. 6-17.

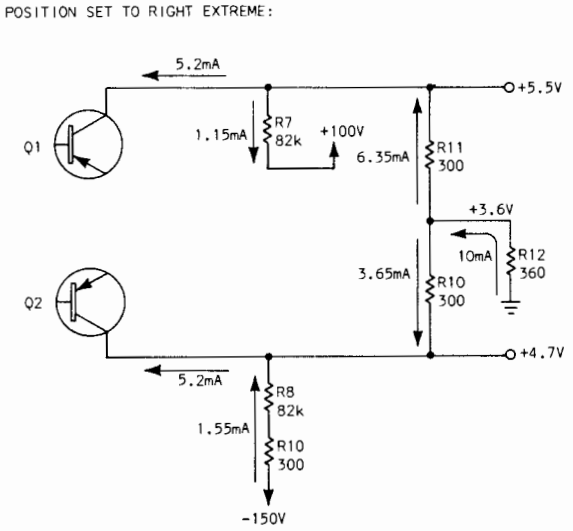


Fig. 6-18.

switched gain amplifier

A switched gain amplifier allows selection of more deflection factors without increasing the number of input attenuator networks. See Fig. 6-19, a push-pull amplifier, longtailed by active devices, with a selectable R_O, RC compensation in the emitter circuit, and an internal system gain adjustment.

Q3 and Q4 solidly longtail this circuit. Balance control, R9, in the emitter circuits of Q3 and Q4, equalizes Q1 and Q2 emitter currents for no quiescent current through R1.

R1 is R_i. Because the longtail circuit presents a very high impedance, and internal resistance of Q1 and Q2 represents only a few ohms, consider R1, R_i.

Mechanically ganged to the input attenuator switch, SW1 changes the vertical deflection factor in calibrated steps. R_O changes with the position of SW1, VARIABLE VOLTS PER DIVISION, changing stage gain. $A_V = \frac{R_O}{R_i}$. R2 and R3 return the collectors to V_{CC}. With SW1B positioned as shown, R_O consists of R2 and R3 paralleled by R5, R6 and R7 (set to midrange). The stage realizes maximum gain in this case. R_O = 67 kΩ, R_i = 1.6 kΩ, $A_V = \frac{R_O}{R_i}$ = 42.

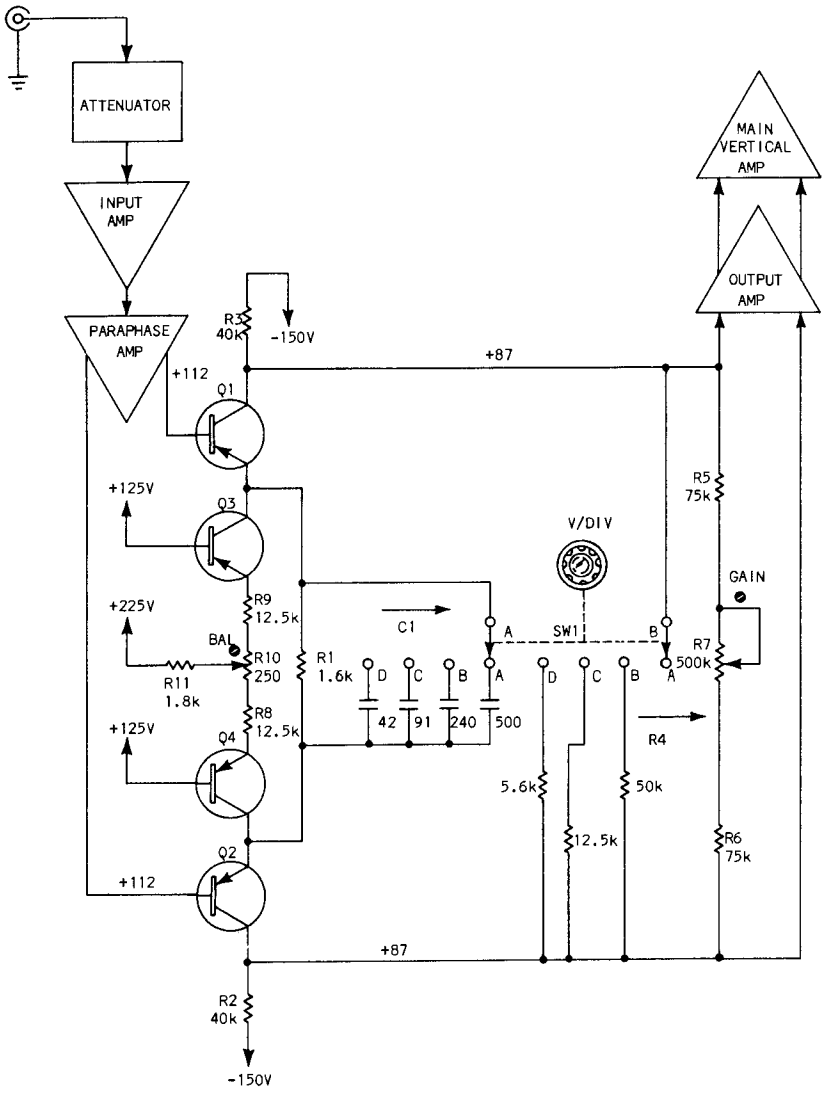


Fig. 6-19. Switched gain amplifier.

Adjusting R7 sets basic R_O or system gain. Actuating SW1B shunts the basic R_O with resistances in descending values. The minimum resistance or gain occurs when SW1B contacts position D. Shunting with 5.6 kΩ reduces R_O to about 5 kΩ. $A_V \approx 3$.

emitter peaking

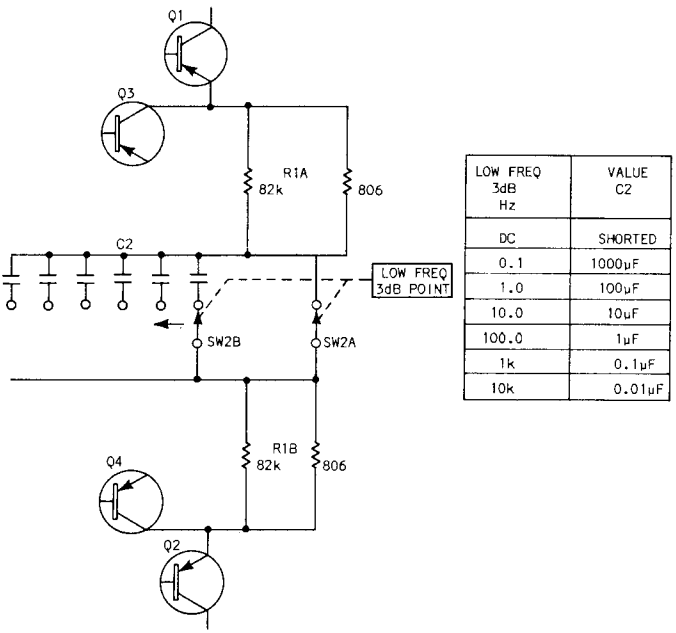
Also ganged to SW1B and the input attenuator, SW1A coordinates emitter peaking with changing collector resistance. Actuating SW1 obviously affects the collector circuit time constant. For proper response the emitter RC must match the collector RC. SW1A accomplishes a match by switching emitter capacitance as SW1B switches collector resistance.

low-frequency response

In amplifier concepts discussed to this point, no attempt to restrict frequency response has been pointed out. Seemingly one desires a vertical system that amplifies frequencies from DC to infinity. Yet if one desires to measure one small segment of the frequency spectrum, all other signals become clutter, noise, or objectionable positional voltages. AC coupling at the input eliminates DC. This limits low-frequency response to a few hertz or even a fraction of a hertz. One might wish to restrict low-frequency response even more in calibrated 3-dB steps. A modification of the amplifier in Fig. 6-19 accomplishes a step-selected, calibrated, low-frequency response.

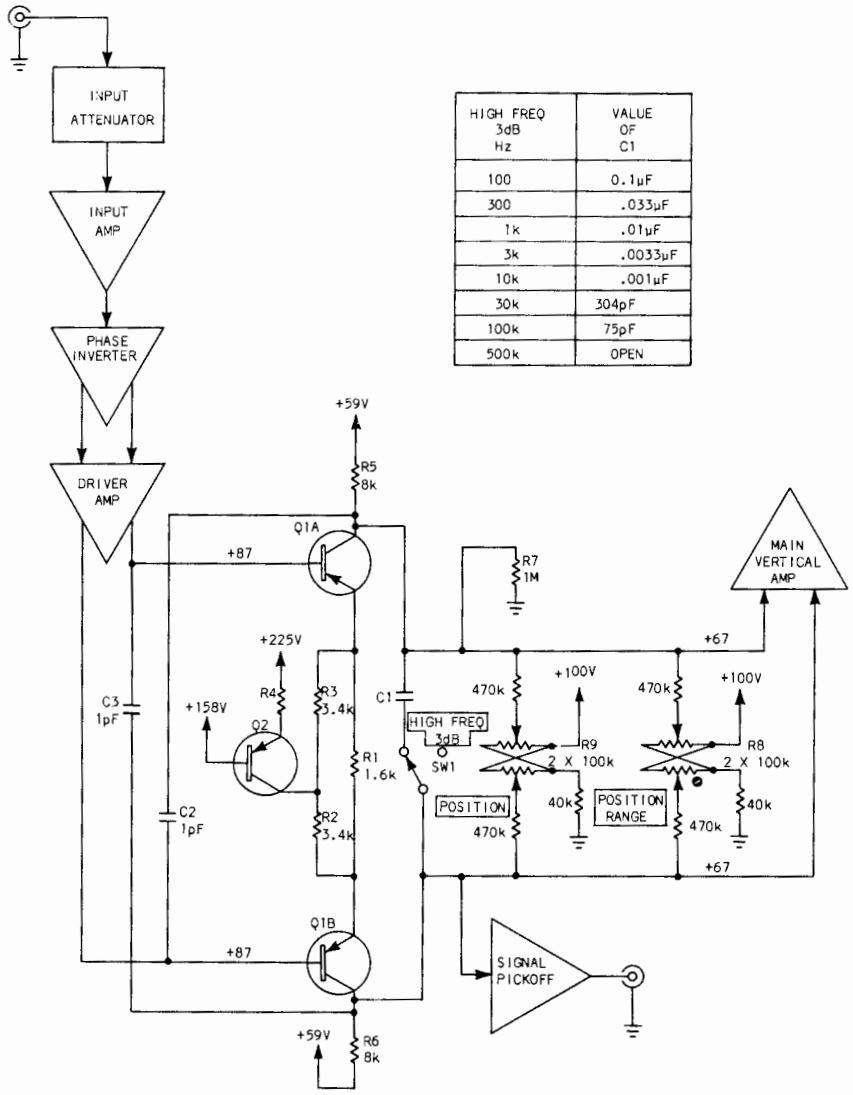
To accomplish the modification of Fig. 6-19 all components, except R1, remain as shown. Refer to Fig. 6-20. The only components shown are those replacing R1 of Fig. 6-19. Keep in mind that all components other than R1 remain. SW2A, positioned as shown, maintains R_i at 1.6 kΩ. However, throwing SW1A removes the short across C2, causing R_i to increase with a decrease in frequency. Capacitance of C2 now determines low-frequency degeneration. SW2B selects capacitance or low-frequency cut-off as listed in the table included in Fig. 6-20. LOW FREQ 3 dB POINT, a front panel selector, actuates ganged switches 2A and 2B.

Circuits of this type are not intended for pulse reproduction. The extreme sag introduced by C2 precludes step response, the price usually paid for selectable low-frequency response. Amplifiers with selectable upper-frequency response also cannot normally be expected to reproduce pulses with fidelity. These instruments meet the need for measurements in a fairly narrow band.



LOW FREQ 3dB Hz	VALUE C2
DC	SHORTED
0.1	1000μF
1.0	100μF
10.0	10μF
100.0	1μF
1k	0.1μF
10k	0.01μF

Fig. 6-20. Switching F_{co} of the switched gain amplifier.



HIGH FREQ 3dB Hz	VALUE OF C1
100	0.1μF
300	.033μF
1k	.01μF
3k	.0033μF
10k	.001μF
30k	304pF
100k	75pF
500k	OPEN

Fig. 6-21. Preamplifier output stage with position and F_{co} controls.

See Fig. 6-21. In this figure, a push-pull amplifier incorporates several concepts:

1. Temperature balance.
2. Longtailing.
3. Capacitive neutralization.
4. HIGH FREQ 3 dB POINT, a front panel control.
5. POSITION control.
6. Internal, vertical position calibration.
7. Compensation for signal pick-off loading.

Q1A and Q1B share temperature environment, the same envelope. Equal signals due to thermal agitation generate in each device. The push-pull configuration tends to cancel these signals. Equal-amplitude in-phase signals develop across the longtail network. Therefore, only *differences* in amplitude generate signal current. How much rejection a common-mode signal of this type receives depends upon the extent of longtailing. Q2 provides longtailing extensive enough to reject reasonable amplitudes of common-mode signal.

longtailing affects CMRR

R_i in Q1 emitter circuit consists of R1 paralleled by R2 and R3.

R_o is the sum of R5 and R6. A number of resistive networks appear in the collector circuit. The composite resistive value remains high enough to ignore shunting effects.

Miller capacitance

C_m, the product of base-to-collector capacitance and the quantity one plus voltage gain, feed a degenerative signal to the base. C1 and C2 neutralize C_m by feeding back a regenerative signal. Another explanation: C_m draws charging current from the source in opposition to signal currents. Neutralization capacitors provide an additional source of charging current, reducing the current drawn from the source by C_m.

selectable frequency response

Selecting frequency response improves some measurements by eliminating unwanted signals. The circuit in Fig. 6-21 accomplishes selectable high-frequency response by shunting R_o with capacitance. R_o, then decreases with frequency and, as R_o decreases, stage gain decreases. $\left(A_V = \frac{R_o}{R_i}\right)$.

Actuating SW1 selects the capacitance which establishes upper frequency response. SW1, shown simplified, has several positions. Fig. 6-21 includes a table listing switch logic.

positioning

Front panel POSITION control, R9, inserts positional voltage when moved off center. Vertical Position Range, R8, an internal adjustment, provides calibration of DC collector level when POSITION control indicates center screen display. Range and POSITION resistive networks present high resistance signal loading.

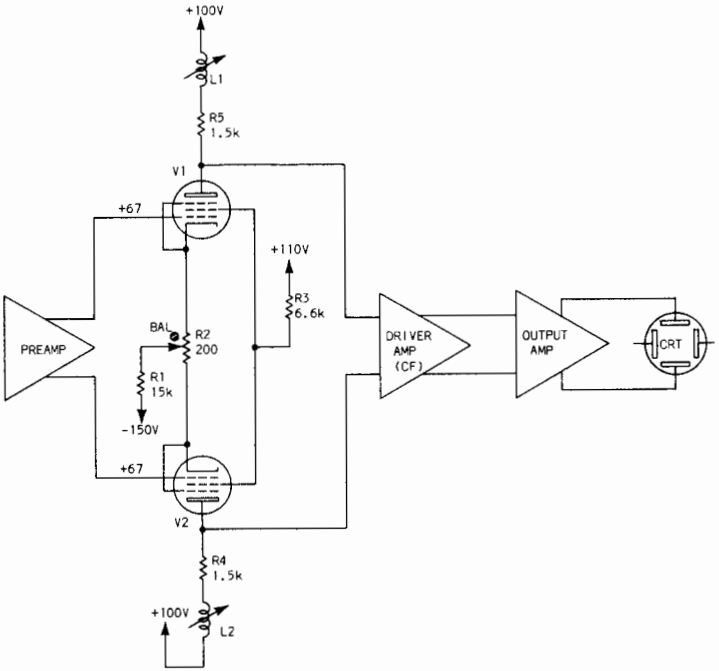


Fig. 6-22. Main vertical input amplifier.

signal pick-off

A signal pick-off amplifier robs some signal power from the collector of Q1B. A nominal load, R7, appears in Q1A collector to balance this loss of signal power. Equal signal loading insures balanced drive to the main vertical amplifier.

Typically, preamplifiers provide push-pull signal drive and DC operating level to a main vertical amplifier.

balances

Fig. 6-22 shows an amplifier which develops balanced broadband voltage drive to an output amplifier. The circuit is simple and straight forward. Since push-pull currents flow, only R2 adds signal degeneration. Signals develop across the load represented by R4 and R5. Adjustable shunt peaking coils, L1 and L2 improve risetime. An adjustable R2 allows correction for unequal input signal amplitude or following stage imbalance.

Changing R2 varies neither quiescent levels nor stage gain. R2 comprises such a small percentage of total cathode resistance that adjustments have little, if any, effect upon plate current. The ratio $\frac{R_O}{R_i}$ determines voltage gain. R_O = R4 + R5. R_i = r_{k1} + r_{k2} + R2 (corrected for screen current losses). Moving the wiper of R2 towards V1 increases V1 gain while decreasing V2 gain correspondingly. Stage gain remains the same.

An amplifier of this type drives the output stage directly or, as in Fig. 6-22, via a cathode follower.

output amplifiers

Output amplifiers drive a capacitive load to large voltage changes. Therefore, output amplifiers, in general, carry more current than other amplifiers in a vertical system.

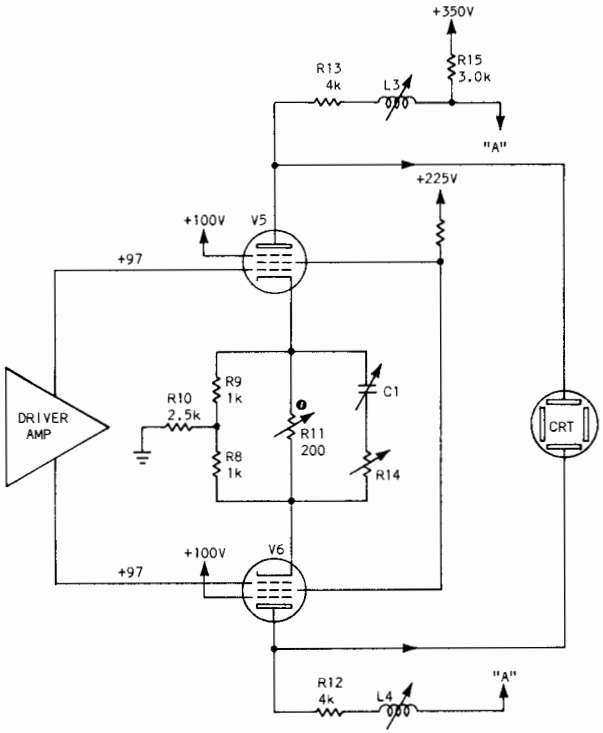


Fig. 6-23. Main vertical output amplifier.

See Fig. 6-23, a pentode push-pull amplifier. The amplifier cathode circuit includes longtailing, an adjustable R_i and cathode peaking. Isolated from the cathode, the suppressor grid returns to a fixed voltage. A shunt-peaked plate circuit aids risetime.

R8, R9 and R10 longtail. R8, R9 and R11 determine R_K. R11, an internal gain adjustment, appears out of the DC current path. Since no DC current flows through R11, one may adjust gain without experiencing vertical trace shift. C1-R14 provide cathode peaking.

Returning the suppressor grids to a regulated low-impedance source prevents injection of reactive suppressor characteristics into the cathode or input circuits.

R12 and R13 define R_O.

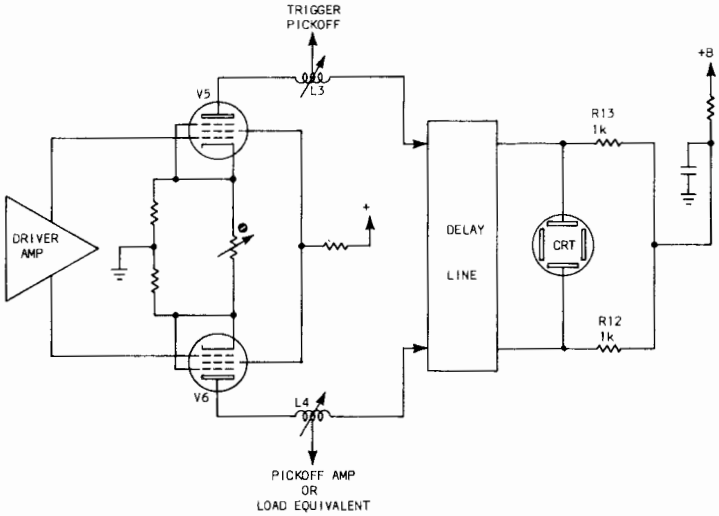


Fig. 6-24. Output amplifier with delay line.

Adjustable cathode peaking and shunt peaking allow empirical calibration for minimum risetime within overshoot limits.

output amplifier with delay line

Circuit concepts of Fig. 6-23 apply to Fig. 6-24 except in the plate circuits. A delay line in Fig. 6-24 appears between the plate circuits and the CRT. Shunt output capacitance of V5 and V6, and T-coils L3 and L4 make up one section of a transmission line, adjustable to match delay line characteristics. The L3 and L4 center-taps provide trigger pick-off points.

trigger pick-off

Utilizing input capacitance of the trigger pick-off circuit as a T-coil component prevents unpredictable loading. The center tap feed also makes balancing fairly simple. L4 center tap may feed another pick-off circuit or an equivalent circuit. A single capacitor could represent the load equivalent to the trigger pick-off.

$R_i = \frac{R_K}{\eta} + r_{k2} + r_{k1}$. R_o = R12 + R13. R_o is delay-line Z_o. R12 and R13 as transmission line terminators must equal Z_o.

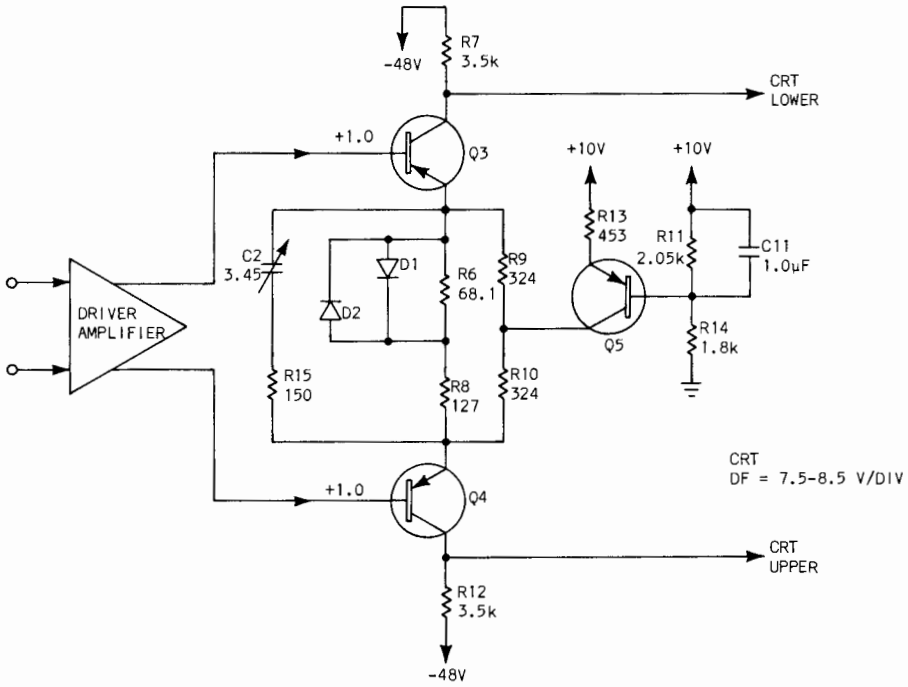


Fig. 6-25. Output amplifier includes compression compensation.

compression compensation

Fig. 6-25 shows a high gain amplifier which provides compensation for compression. The term compression refers to a signal display that seems to be squeezed or *compressed* when positioned near the upper or lower display limits.

Q3 and Q4 develop a gain between 40 and 50. R_i consists of R6 and R8 paralleled by R9 and R10. R7 and R12 constitute R_o. C2 and R15 emitter-peak this longtailed amplifier.

D1 and D2 change gain to correct for compression. Amplifier circuitry, the CRT, or both cause an increased deflection factor when the signal position approaches the upper or lower CRT extremes. Counteracting the increased deflection factor, this amplifier gain increases with off-center positioning. Position information develops as unequal (Q3 and Q4) base voltages. When position reaches the unbalance representing an approach to the compression area, either D1 or D2 begins to conduct. Whether D1 or D2 conducts depends upon polarity of positional voltage. Turning on either shunts R6, reducing R_i.

Longtailing device Q5 establishes total emitter current for this amplifier. Q5 base voltage, in turn, sets collector current. C11 maintains emitter current during short-term power-supply fluctuations: +3.6 volts drops across R14, setting base, thus emitter, voltage. 6.2 volts across R13 develops longtail current, which should remain constant. Without C11, fluctuations in the +10 volt supply change Q5 emitter current. Assume C11 open:

$$V_b = +10 \left(\frac{R14}{R14 + R11}\right) = +3.6 \text{ V.}$$

$$V_e = V_b + 0.2 = +3.8 \text{ V}$$

$$*I_e = \frac{6.2 \text{ V}}{453 \ \Omega} = 13.6 \text{ mA}$$

Should the +10 V supply drop to +9 V:

$$V_b = +9 \left(\frac{R14}{R14 + R11}\right) = +3.26$$

$$V_e = V_b + 0.2 = +3.46$$

$$*I_e = \frac{5.54}{453} = 12.2 \text{ mA}$$

C11 prevents the change in I_e by maintaining the voltage across R11, thus R13. C11 charges to the voltage across R11, nominally 6.4 volts. Should the +10 volt supply change, C11 initially contains 6.4 volts charge. Base voltage therefore follows supply fluctuations holding emitter current constant. Assume the +10 volts, after an hour or so operation, drops to +9 volts for a short time:

Initial

V_b = +3.6 V

V_e = +3.8 V

*I_e = 13.6 mA

V_{R11} = 6.4 V

Supply fluctuates to +9 V:

$$V_b = +9\ V - V_{R11} = 9 - 6.4 = +2.6\ V$$

$$V_e = V_b + 0.2 = +2.8\ V$$

$$*I_e = \frac{9 - 2.8}{R13} = \frac{6.2}{453} = 13.6\ mA$$

I_e remains constant for only short duration fluctuations. C11 begins to assume the new charge, about 5.7 V, immediately. Q5 base circuit time constant determines the charge rate, 750 μs.

Those who wish to use Fig. 6-25 for analysis exercises should consider all semiconductors germanium.

risetime limitations

Active device limitations imposed a barrier to the development of fast-rise instruments. Depending upon signal amplitudes to be processed, conventional circuitry and tube construction, including the CRT, seemed to reach a limit at about 7 ns.

stiff beam

The CRT in a broad-band instrument must have a high velocity beam -- as risetime decreases, beam velocity must increase. Because the beam so rapidly passes deflecting elements, it carries the name *stiff beam.* The necessarily large plate dimensions of a pair deflecting a stiff beam create bad effects. Capacitive loading is excessive. And before the beam leaves the deflection plate influence, signal phase possibly reverses giving a net deflection of zero.

distributed-deflection

This led to the development of the *distributed-deflection* CRT.

A distributed-deflection CRT provides a reasonable deflection factor with a stiff beam. This configuration consists of a lumped-parameter transmission line which deflects the beam. Deflection power travels sequentially across the plates and dissipates at the termination. Matching propagation velocity with electron beam velocity extends CRT bandwidth.

One Tektronix instrument for years demonstrated the effectiveness of distributed deflection using just the CRT as a vertical system. The CRT receives signals to one side of the transmission line, the other side by-passed to ground. Specifications list risetime at 0.35 ns, and bandwidth from DC to more than 1 GHz.

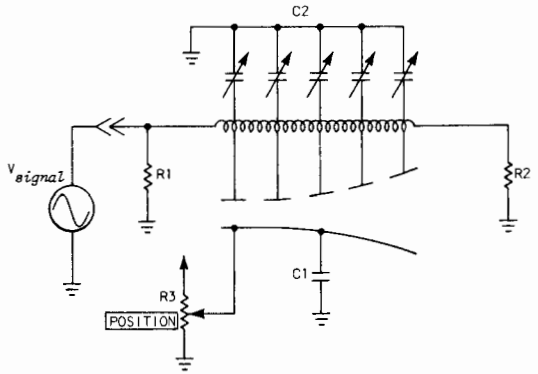


Fig. 6-26.

single-ended distributed deflection

Fig. 6-26 schematically illustrates the single-ended distributed-deflection system. Input signals transit the transmission line to dissipate in the forward termination, represented by R2. R1 and R2 must equal the characteristic impedance of the transmission line. The transmission line consists of a tapped inductance and parallel capacitance at each tap. Adjustable portions of C2 parallel the upper vertical deflection plate segments.

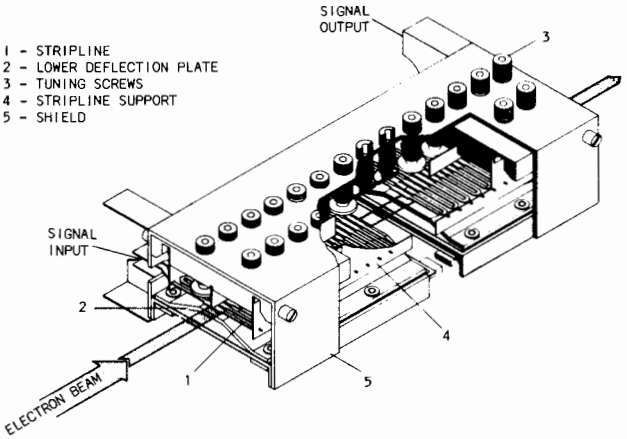


Fig. 6-27.

Fig. 6-27 shows a cutaway drawing of this vertical deflection assembly. The upper vertical deflection plate and transmission line consist of a continuous, "S" shaped, metal strip called a stripline (1). Stripline shape creates inductance and mechanical strength. Capacitive coupling occurs between the lower deflection plate and the stripline surface. The tuning screws also capacitively couple to the stripline surface, paralleling deflection plate capacitance.

stripline

Fig. 6-28 plots the effects of electron beam velocity (V_e) and signal velocity (V_s) upon deflection.

Fig. 6-28A plots intercept points where electron beam velocity (V_e) and signal velocity (V_s) match. From these curves one plots the curves in Fig. 6-28B.

Curve 1: V_e exceeds V_s. A velocity mismatch occurs over the entire frequency spectrum. Electron beam deflection attenuation begins at a low frequency.

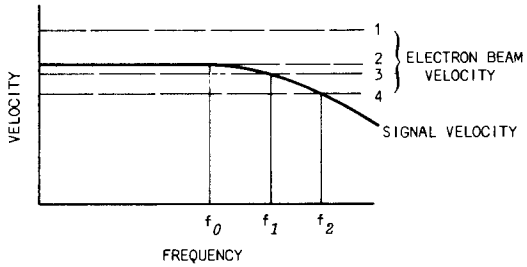
Curve 2: V_e and V_s equal. The mismatch begins at f_0 as the signal velocity curve rolls off.

Curve 3: V_e a little slower than V_s. Velocity match occurs at a higher frequency, f_1. Consider electron beam deflection on this curve equal from DC to f_1.

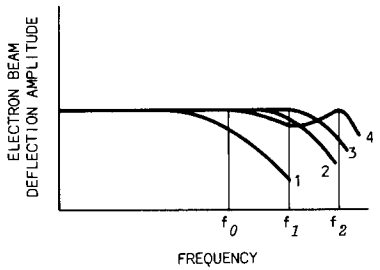
Neglect the attenuation between f_0 and f_1. (A) shows this attenuation more clearly than (B).

Curve 4: V_e much slower than V_s. Velocities match at a much higher frequency, f_2. However, beam deflection attenuates at frequencies both above and below f_2.

The CRT discussed connects directly to the signal source of interest. Further, CRT construction allows only single-ended deflection. The high-frequency response required preempts the generally preferred push-pull deflection. State-of-the-art amplifiers do not extend to fractional nanosecond response.



(A) VELOCITY VS. FREQUENCY



(B) AMPLITUDE VS. FREQUENCY

Fig. 6-28.

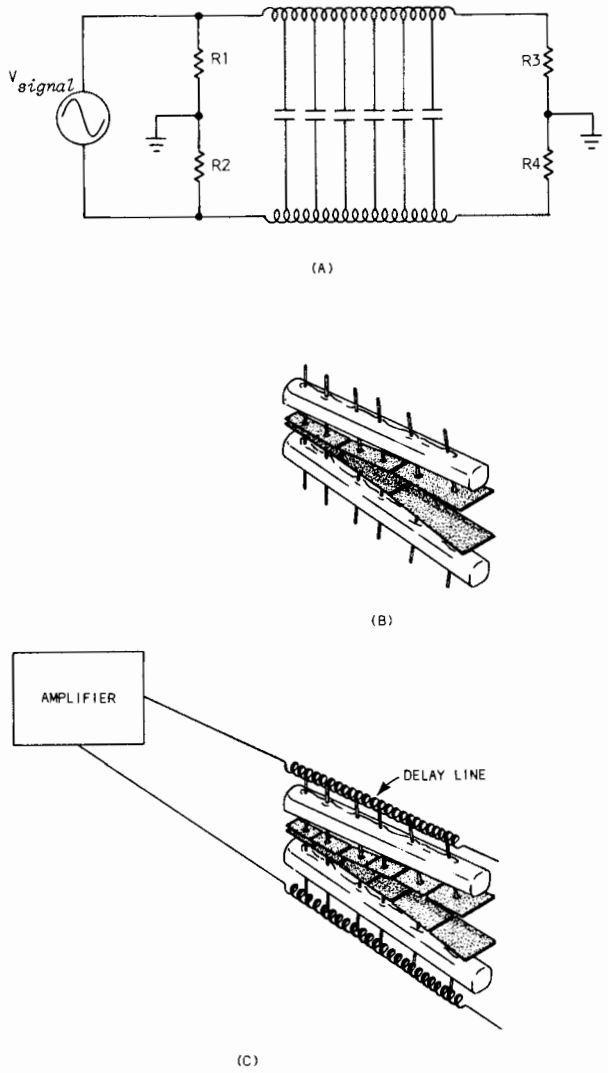


Fig. 6-29. Push-pull distributed deflection CRT.

push-pull distributed deflection

Distributed deflection does occur in push-pull instruments which display fast-rise waveforms. Fig. 6-29A schematically represents the distributed-deflection assembly. Push-pull signal voltage, applied across R1 and R2, travels down the transmission line at a velocity determined by lumped L and C values. Signal energy dissipates in forward

terminators R3 and R4. At some upper frequency limit, signal velocity becomes less than electron beam velocity, reducing deflection *sensitivity*. Figs. 6-29B and C show simplified construction models.

distributed amplifiers

The word *distributed* also applies to amplifier configuration. Distributed amplifiers come into use when risetime requirements exceed the possible limits of cascade amplification. For a comparative presentation, this writer prefers to refer to distributed amplifiers as "additive amplifiers" and cascade amplifiers as "product amplifiers." These terms are quite accurate and much more descriptive. Additive amplifiers provide a means of increasing circuit transconductance.

product amplification

Product amplification has the advantage until risetime requirements become quite severe. A point is reached where the most efficient networks, combined with the "best" tubes, just don't do the job. Combinations of shunt peaking, series peaking and T-coil peaking *might* provide network efficiency of 4. Tubes, however, restrict stage performance to the gain/risetime quotient:

$$\frac{A_V}{t_r} = \frac{R_O}{R_i} \times \left(\frac{1}{2.2\ R_O C_O} \right) = \frac{1}{2.2\ R_i C_O}.$$

Assume the designer possesses the lowest output capacitance and highest transconductance tube type; that he combines it with the most efficient network; that he meets the overall risetime requirements in a single stage only by reducing stage gain to 2; and that he must develop an overall gain of 12. Unless tube development reduces C or increases *gm*, product amplification just won't do the job:

$$A_V = 2 \times 2 \times 2 = 12; \text{ but, } t_r^2 = t_{r1}^2 + t_{r2}^2 + t_{r3}^2$$

additive amplification

Additive amplification solves the problem. It even works when each tube contributes less than unity gain. A *stage* of additive (distributed) amplification consists of paralleled active devices. The name *section* applies to each active device circuit. Parallel control grid drive and a common plate load derive a summing voltage gain. The *stage* gain is the sum of *section* gain. Theoretically, *gm* increases by the number of sections, improving gain-risetime ratio: $\frac{A_V}{t_r} = \frac{n\ gm}{2.2\ C_O}$.

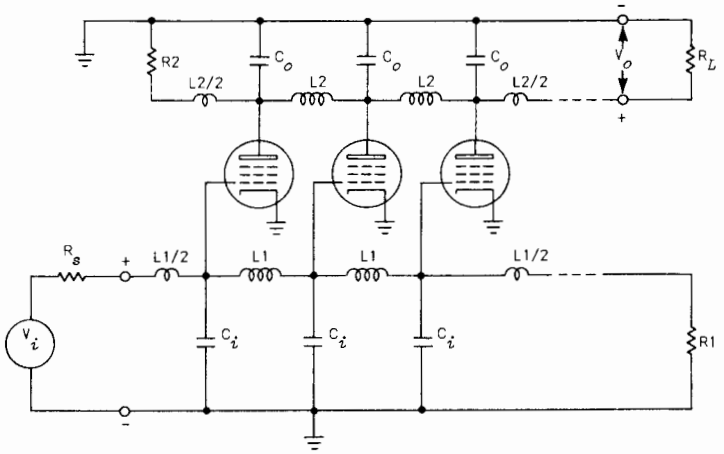


Fig. 6-30. Distributed amplifier.

The model of Fig. 6-30 shows the basic idea of additive amplification. V_i develops along a terminated, lumped parameter, transmission line. Grid line sections consist of an inductor between the input capacitance of each tube. V_i appears at each grid, sequentially, at the transmission line propagation velocity. Internal source resistance (R_s) and Z_O equal, preventing reflected energy. Output capacitance of each tube and inductance make up the plate line. No reflections occur since R2 and load resistance (R_L) terminate the line. Both lines impose the same phase velocity.

Assume neither line attenuates the signal:

$$Z_{O1} = R1 = \sqrt{\frac{L1}{C_i}}$$

$$Z_{O2} = R2 = \sqrt{\frac{L2}{C_o}}$$

$$\text{Phase velocity} = \frac{1}{\sqrt{L1 \cdot C_i}} = \frac{1}{\sqrt{L2 \cdot C_o}}$$

$$I_{sig} \text{ (each tube)} = \frac{V_i}{R_i}, \text{ if } R_i = r_k: \frac{V_i}{r_k} \text{ or } gm\ V_i.$$

Individual plate currents add because of equal grid and plate line velocities.

$$I_o = I_{p1} + I_{p2} + I_{p3} + \ldots$$

or

$$I_o = \frac{n\ V_i}{R_i}$$

and since $R_L = R2$, $R_o = \frac{R2}{2}$

$$A_V = \frac{n\ R_o}{R_i}$$

where n = number of sections (tubes).

All of which states that each section contributes gain of $\frac{R_o}{R_i}$, and total (stage) gain is the sum of the individual section gains. Each section can contribute less than unity gain, yet achieve any stage gain by adding enough sections. This is not possible with cascade amplification: One to any power is one.

Input impedance

Active device input impedance considerably affects grid-line attenuation. When 7 ns exceeds instrument reaction, input impedance effects become serious. Input impedance consists of both capacitance and conductance. The latter component attenuates signals traveling the grid line. Tube input conductance increases with the square of frequency, so as risetime decreases, attenuation finally exceeds section gain. Adding more tubes only degrades performance.

Expect to select tubes and "retweak" lines. Input conductance is proportional to cathode lead inductance and cathode-to-grid transit time. The designer considered these factors when selecting the tube type. However, tube parameters vary: With age, between types of the same manufacturer, and especially between tubes of different manufacturer. Therefore, replacement of one tube might very well require replacement of several more, if not all. Further, both input and output capacitance in all probability change, requiring a "line tweak."

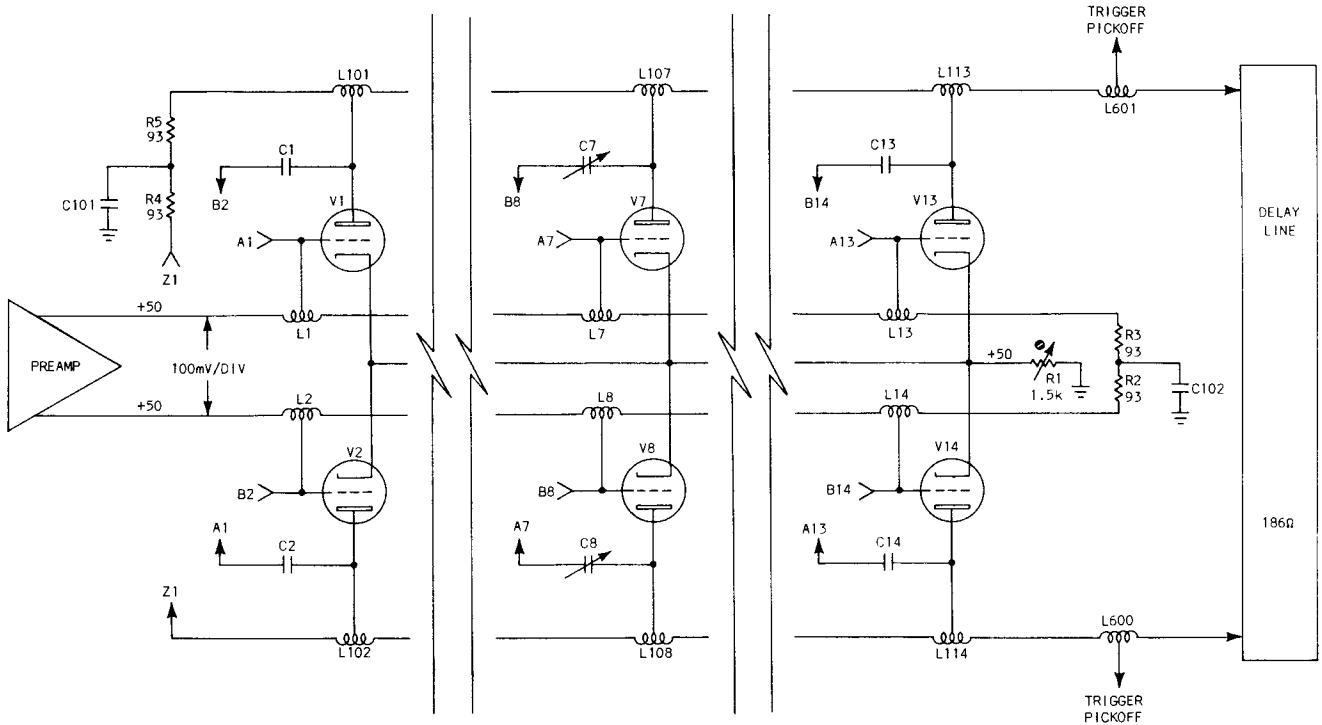


Fig. 6-31. Main vertical input amplifier.

Some additive amplifiers, in use, have a section gain of less than unity. Fig. 6-31 shows a main vertical input amplifier. This amplifier consists of seven sections of additive amplification. Only three sections are shown since all but the fourth are identical. Section gain of 0.36 results in stage gain of 2.5: $0.36 \times 7 \approx 2.5$.

The preamplifier drives a terminated transmission line. T-coils L1 through L14, stray capacitance, interelectrode capacitance, R2 and R3 make up a terminated line.

R1 sets gain by controlling gm (R_i).

The plate load also consists of a terminated transmission line. Section output capacitance, L101 through L114, R4 and R5 appear as part of the transmission line. One must consider L600, L601 and the delay line as a continuation of the plate line. Neutralization capacitors prevent input capacitance changes due to Miller-effect (C1, C2, C7, C8, C13 and C14 shown). Although neutralization appears in each section, only one (V7 and V8) provides adjustable feedback.

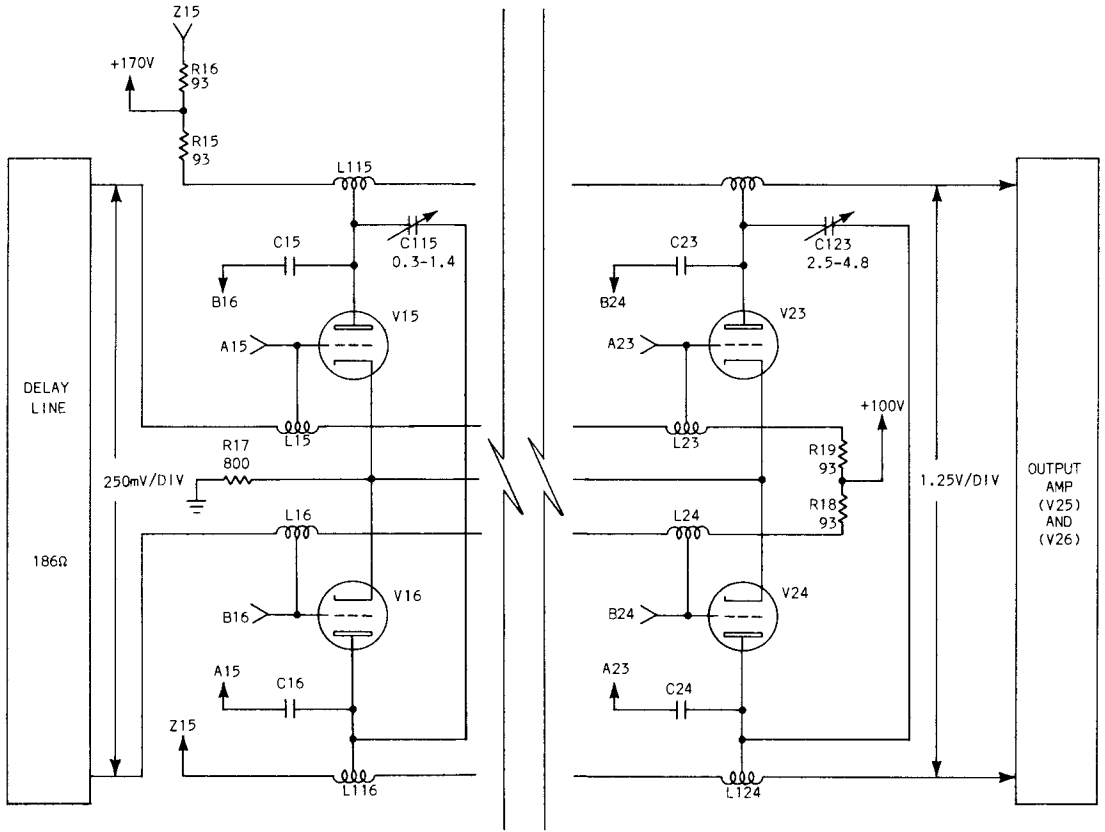


Fig. 6-32. X5 additive amplification.

250 mV/div develops across the plate line which continues through the delay line and on to the following stage grid line. Fig. 6-32 contains the remaining plate line components. L15 through L23, L16 through L24, R18 and R19 complete this transmission line. Input-amplifier output-voltage drives the grids of the driver amplifier in Fig. 6-32, another distributed amplifier. Five push-pull neutralized sections make up the driver amplifier.

line termination

This circuit differs from 6-31 because it includes adjustments for each section of the plate transmission line, and the line is terminated at one end only. Adjusting C115 balances the phase velocity at the output of V15 and V16. Each section contains an identical component across the plates, except V23 and V24. C123 is adjusted for the same result but is of different value due to components in the grid circuits of V25 and V26.

Terminating only one end of the line gives a gain advantage at the expense of reflections: R_O = R15 + R16, $R_i \simeq$ R18 + R19, $A_V = 1$ for each section or $A_V = \frac{5R_O}{R_i} = 5$ for the stage. Reflections are not objectionable when the line is carefully balanced.

Distributed amplifiers require careful termination. Z_O of lumped parameter lines drops abruptly at F_C. Phase cannot then be proportional with frequency. Acceptable amplifier transient response depends upon maintaining phase shift with frequency. Causing the termination impedance to vary with Z_O solves the problem since grid and plate line impedance change together.

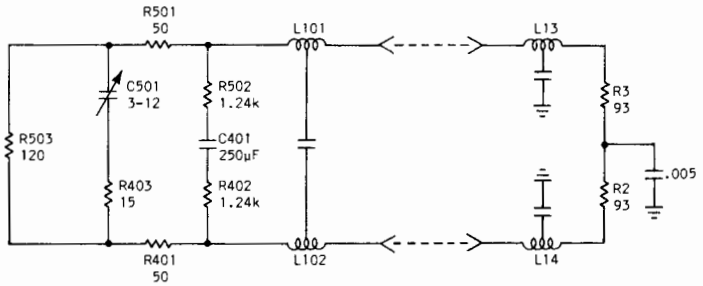


Fig. 6-33. Plate line termination for amplifier Fig. 6-31.

Fig. 6-33 illustrates the complex termination, represented by R4 and R5 of Fig. 6-31. During slow signal changes, the termination consists of R401, R501 and R503. Delay line Z_O shunts this value to develop R_O. R2 and R3, in the following stage grid line, terminate at the opposite end of the delay line. As signal risetime decreases, C501 and R403 shunt R503, dropping termination impedance. Careful adjustment, including part selection, causes termination impedance to follow Z_O changes. This also allows the grid-line load to be simple resistors, R2 and R3. R402, R502 and R401 compensate for sag.

Plate line termination for 6-32 appears in Fig. 6-34. R151, R161 and R152 approximate Z_O. C161 shunts R152 to reduce termination impedance. This is a simpler termination for two reasons: First, the plate line is much shorter than the delay line; second, one balances the m of each section, e.g. C115, increasing the termination effectiveness. Some signal energy does travel back down the line, causing a small "hump" along the top of a displayed step. Hump amplitude depends upon how much signal power develops across the termination. Quantity of reflected power in turn depends upon the adjustments of each section, termination resistances, and the setting of C161.

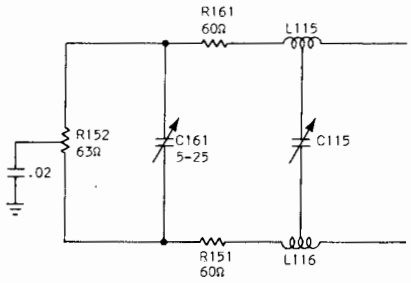


Fig. 6-34. Plate line termination for amplifier Fig. 6-32.

Combining Fig. 6-31 and 6-32 cascades a X2.5 additive and a X5 additive amplifier. This combination yields X12.5 gain: 2.5 x 5 = 12.5. Product and additive amplification can be combined. The determination between cascade, or distributed, or some combination comes down to a choice of the fewest parts which give the desired performance.

Tubes used in 6-31 and 6-32 are very high *gm* triodes. Before these triodes were available, pentodes served as active devices in distributed amplifiers. Conceptually, the circuit reacted the same with the added complexity of screen and suppressor grids.

transistor amplifiers

Don't expect to encounter transistors in additive configuration. Transistorized distributed amplifiers exist. But, transistor *gm* is so high that some form of cascading gives the desired performance with fewer parts and simpler alignment. Transistor base current also presents the problem of input transmission line loading.

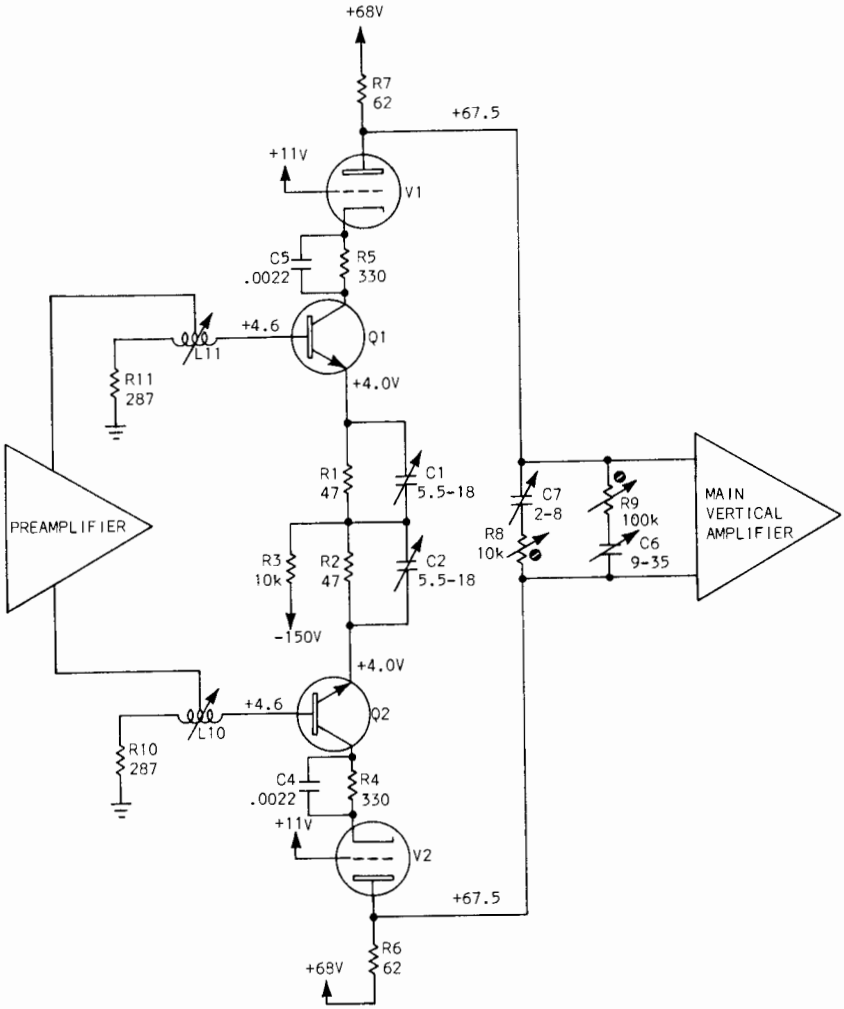


Fig. 6-35. Hybrid cascode amplifier.

hybrid cascode amplifiers

The preamplifier and output amplifier of Fig. 6-35 takes advantage of high-*gm* devices driving grounded-grid amplifiers -- a hybrid, cascode amplifier driven push-pull. Hybrid cascode amplifiers show to good advantage when a large difference between quiescent input and output voltage exists. Push-pull high-*gm* devices, Q1 and Q2, drive grounded-grid amplifiers V1 and V2. Collector DC levels regulate to a value about eight times less than the output voltage level. Control grids, returned to apparent ground, not only regulate V_{CC}, but reduce overall capacitance.

V1 and V2 control grids serve as shields, preventing "Miller-effect" degeneration. Signals develop at the cathodes of V1 and V2, the amplitude of which depends upon input impedance (r_k). These small signals, combined with the reaction of C4 and C5, prevent appreciable degeneration via C_m at either Q1 or Q2. C4 and C5 bypass temperature compensation resistors, R4 and R5.

Another fast-rise technique appears in Q1 and Q2 base circuits. T-coils L10 and L11 cause R_B to appear resistive, equal to R10 or R11. This resistance, divided by β, reflects into the emitter as part of R_i -- perhaps 4 ohms.

R3 longtails, driving each transistor with about 8 mA I_e. R_t, for Q1 or Q2, consists of 3 ohms r_e, 4 ohms R_r, plus something for base spreading resistance.

$$R_i = R1 + R2 + R_tQ1 + R_tQ2 \simeq 110\ \Omega$$

$$R_O = R6 + R7 = 124\ \Omega$$

$$A_V = 1+$$

When computing basic cascode gain assume series signal current through R_i and R_O. R_i is the emitter-to-emitter impedance and, in this case, R_O the plate loads for V1 and V2. Unity voltage gain is fairly conservative for this amplifier. However, should β drop to about 20, gain would be unity. In any case, a previous preamplifier stage sets overall preamplifier gain, accounting for variance of the output amplifier.

sag

C1 and C2 bypass R1 and R2 to emitter peak. These capacitors create short-term sag, compensated for by C7 and R8, in V1 and V2 plate circuits. Compensation for sag of longer duration shunts C7 and R8.

C6 and R9 compensate for the sag introduced by C4 r_{k2} and C5 r_{k1}. This is longer-term than that contributed by Q1 and Q2 emitter circuits because cathode time constants considerably exceed $R_{t1}C1$ and $R_{t2}C2$.

signal injection

Cascode configuration provides a low-impedance point for signal injection at the cathodes of the common-grid amplifiers. This could be positional current or signal current. Either would develop output voltage without affecting the common-emitter amplifiers. This is true no matter what active devices appear in the circuit. The input to the common-base, common-grid, or common-gate amplifier is an attractive low-impedance point for injection or switching currents.

signal switching

Fig. 6-35 has another circuit point suitable for signal switching. If the T-coil components be properly balanced to the switch capacitance, various amplifiers could be selected to drive the center tap of L10 and L11. A diode matrix could allow any one of a number of driver amplifiers to function as a signal source for this amplifier.

signal pick-off

Cascoding not only provides a signal injection point but, with more series devices, also adds signal pick-off points. Fig. 6-36 contains three active devices cascoded in each half of the push-pull driver amplifier. This amplifier drives a delay line and develops the proper DC voltage level for an output amplifier. It also provides an isolated pick-off point for such circuits as trigger amplifier, vertical signal monitor and beam-position indicators. Hybrid cascoding allows considerable difference between input and output DC levels. High-*gm* devices generate total signal current to drive grounded grid amplifiers, V3 and V4, and grounded base amplifiers, Q3 and Q4.

Consider just the upper half of the amplifier. The emitter circuit of Q1 controls total current through V3. V3 control grid keeps Q1 collector voltage at a constant and reasonable level. Signals to the delay line develop across R11. Q3, a busy

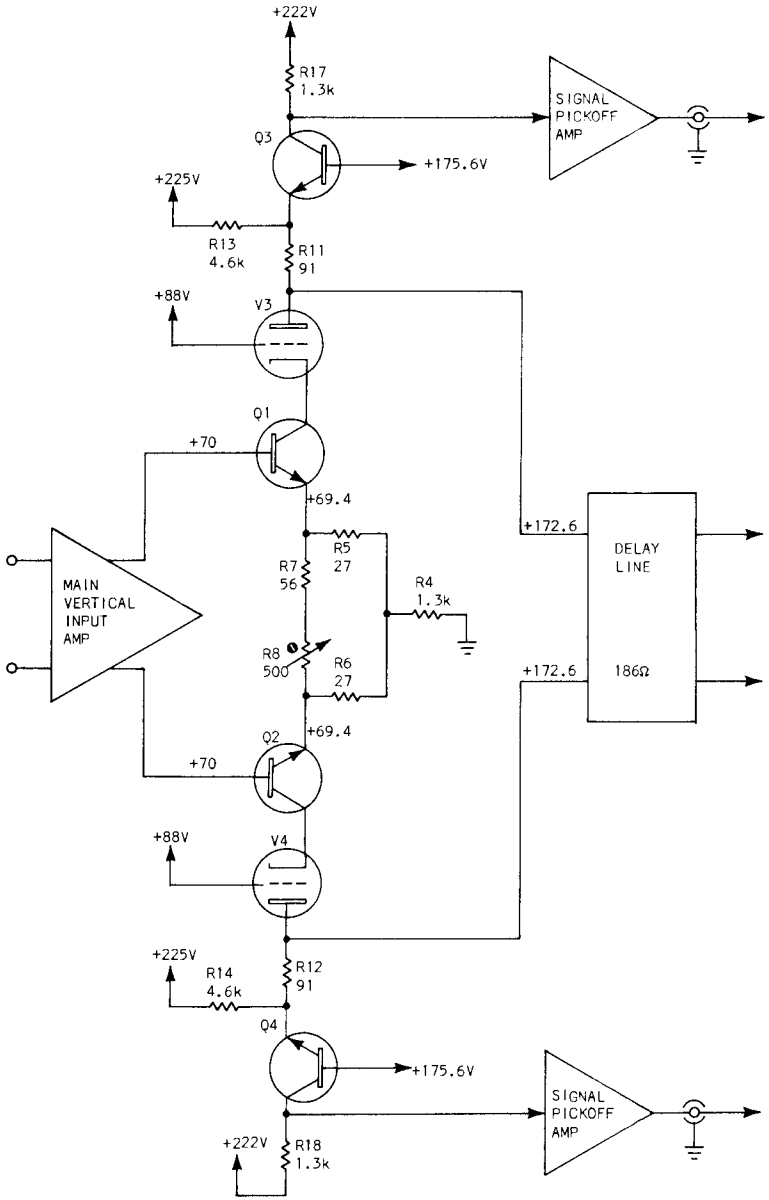


Fig. 6-36. Delay-line driver.

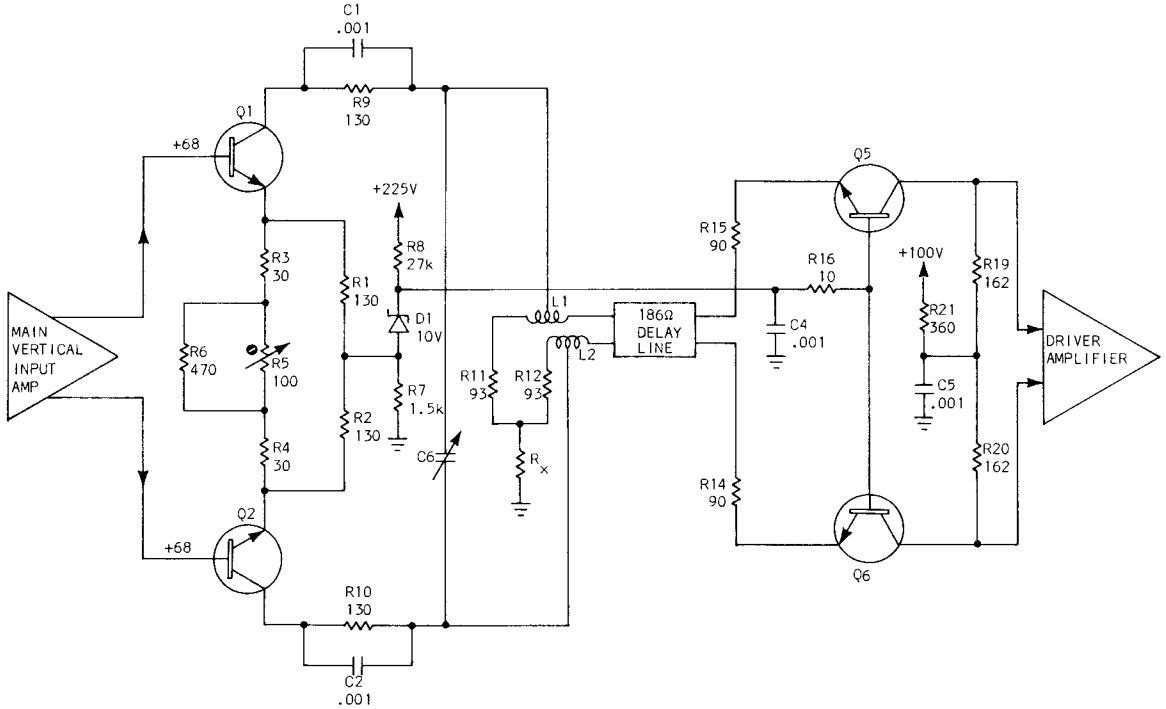


Fig. 6-37. Cascoded delay-line driver.

device, functions as a voltage regulator, a grounded-base amplifier and a terminator. Regulated base voltage fixes Q3 emitter potential, providing E_{bb} for V3. As an extension of the cascode amplifier, Q3 develops in its collector circuit a pick-off signal. Since apparent signal ground appears at the emitter, R11 plus the emitter-base impedance of Q3 terminates the delay line.

Quiescent circuit current is excessive for Q3, so R13 shunts about 40% of this current. The lower half of the circuit functions as described for the upper half.

R4 longtails the circuit. R_i consists of R7 and R8, paralleled by R5 and R6 (about 45 Ω). R11 and R12 paralleled by delay line Z_O make up R_O (about 93 Ω). R_O for signal pick-off is the sum of R17 and R18. R_i for signal pick-off must be modified for losses through R13, R14 and the delay line.

all-transistor cascode amplifiers

Cascode amplifiers need not be hybrid. The circuit shown in Fig. 6-37 is a transistor push-pull amplifier. The collector-emitter junction of a cascode amplifier represents low impedance. A terminated coax delay line also presents low impedance. Quite logically, the low-impedance delay line appears at the collector-emitter junction of this cascode amplifier.

R_i, longtailing, and collector-to-emitter voltage regulation appears in Q1 and Q2 emitter circuits. Resistive network: R1, R2, R3, R4, R5 and R6 determine R_i. Notice that DC currents do not flow through internal gain adjustment, R5. The longtailing circuit consists of R7, D1 and R8.

D1, a zener diode, maintains a constant voltage across Q1 and Q2 during common-mode inputs. Holding V_{CE} constant aids thermal stability. Should quiescent common-mode voltage change at Q1 and Q2 bases, most of the change develops across R7. Elevated 10 volts by D1, this change appears at the bases of Q5 and Q6. These emitters follow one silicon junction lower. Therefore, quiescent collector voltage of Q1 and Q2 changes almost volt for volt with input base levels (common-mode).

Q1 and Q2 collector circuits contain temperature compensation, the delay-line load, the delay line, adjustable compensation, and provision for signal pick-off.

Collector circuit temperature compensation networks consist of R9 and R10 bypassed by C1 and C2.

L1, L2, R12, R13, C6 and distributed capacitance make up the delay-line load. C6, adjustable, makes possible empirical compensation.

R_x represents a possible signal pick-off point. R11 and R12 cannot return directly to ground because of V_{CC}. They can return to signal ground through an active device, as R14 and R15, a passive device, or R_x can be done away with and R11 and R12 lumped into a single 186 Ω resistor. All three configurations are used. Assume 50% of the signal currents flow in R_x and 50% through the delay line.

Q5 and Q6 emitter circuits terminate the delay line. The collector circuits contain R_O. R14, R15 and emitter-base junction of Q5 and Q6 terminate. The sum of R19 and R20 constitutes R_O. Remember that only 50% of the total signal current develops output voltage across R_O. RC network R16-C4, in the Q5 and Q6 base circuit, filters noise generated by zener diode, D1.

compensation

Q5 and Q6 collector circuits normally appear more complex, usually including L/R circuits for dribble-up compensation. See Fig. 6-38. Shown here, the more complex collector circuit is for thermal and dribble-up compensation. C7-R17 and C6-R18 temperature compensate. R27-C5 decouple V_{CC}. The remaining L/R networks provide high-frequency boost, or dribble-up compensation.

Frequently another amplifier stage must be added to further aid leading edge and flat-top compensation. It can be a fairly simple low-gain stage, as shown in Fig. 6-39. This push-pull amplifier develops unity gain when reacting to slow signals. Gain increases with signal rate-of-change, compensating for dribble-up.

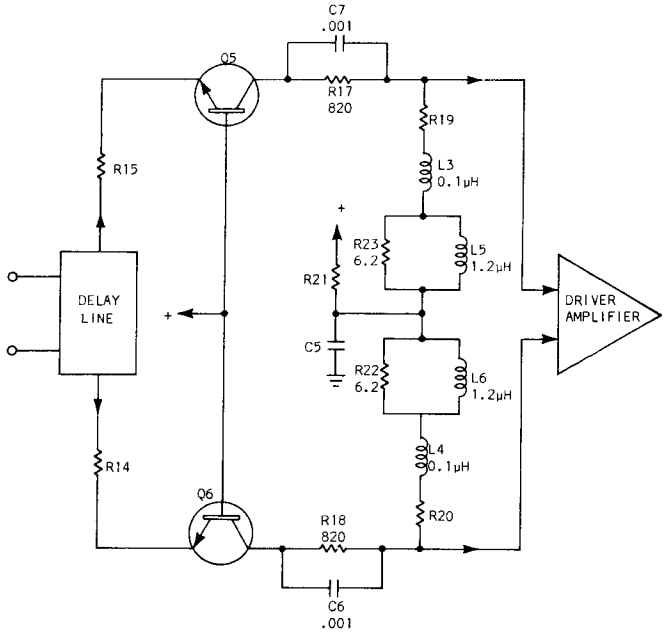


Fig. 6-38. Collector circuit details.

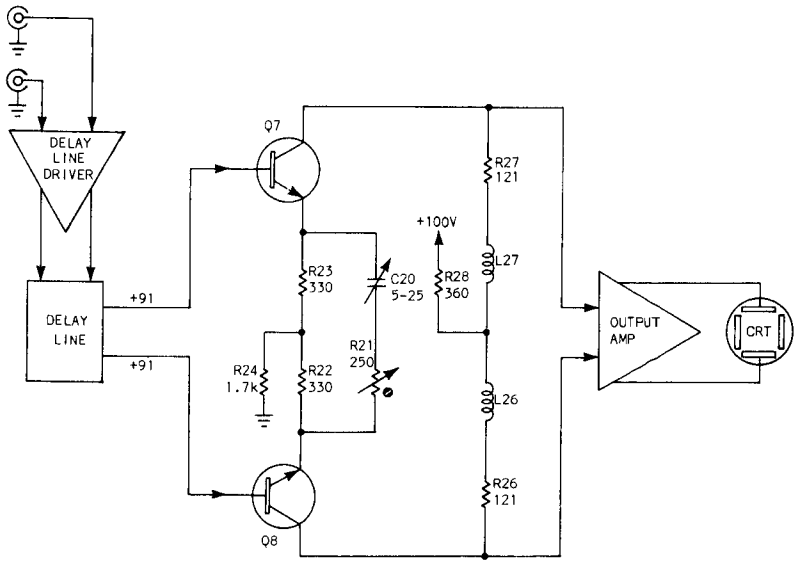


Fig. 6-39. Driver amplifier.

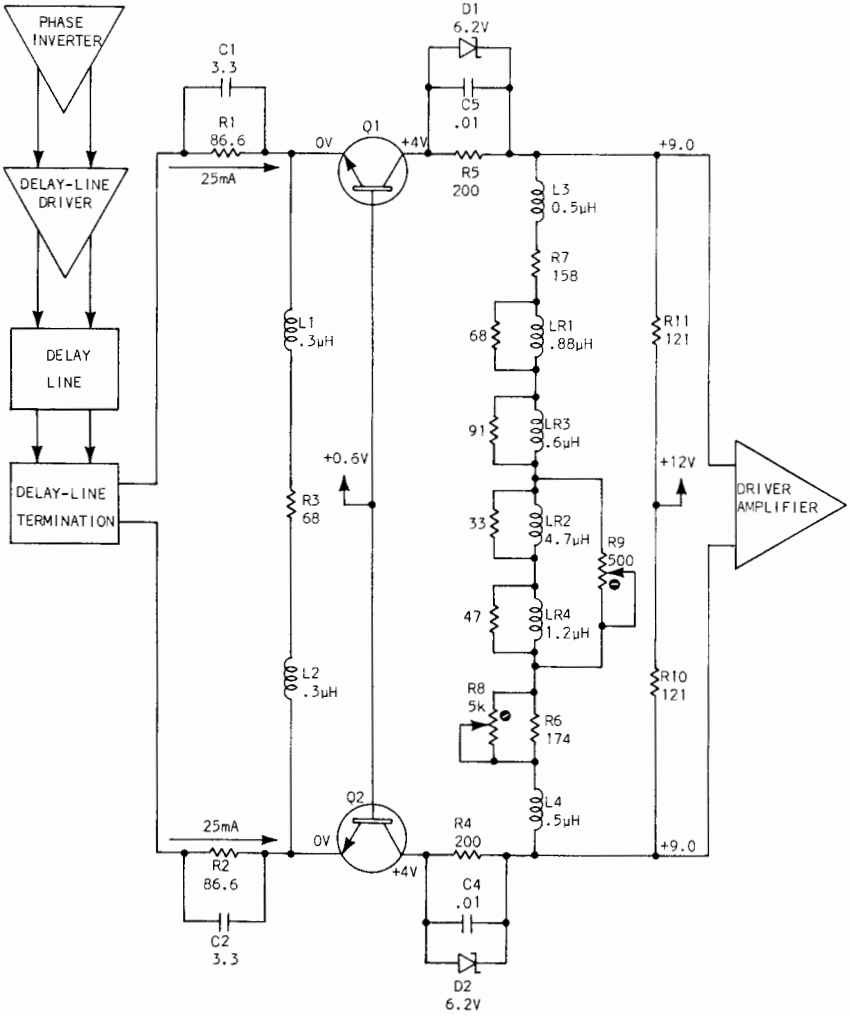


Fig. 6-40. Delay line termination amplifier.

Q7 and Q8 receive signal drive from the delay line driver. R24 longtails the circuit. R_i consists of R22 and R23. C20 and R21 shunt R_i to emitter peak. R26 and R27 make up R_o for slow or low-frequency signals. L26 and L27 increase R_o with frequency, correcting amplitude distortion due to delay-line characteristics.

delay-line output amplifier

Common base amplifiers at the delay-line output are attractive because of the low-input impedance and the input-to-output isolation. This allows the amplifier input to terminate the delay line and output circuit compensation for delay line imposed dribble-up.

See Fig. 6-40. R1, R2, emitter resistance of Q1 and Q2, shunted by R3, present 186 Ω termination. C1 and C2 compensate for the characteristic inductive inputs of grounded-base amplifiers. L1, L2 and R3, added to Q1 and Q2 thermal characteristics, correct for output stage thermal shift, giving a more positive position control. The complex collector circuit temperature compensates, prevents saturation and contains shunt peaking.

Active devices present a somewhat reactive load to signal sources. Generally, sources driving the base work into a capacitive load, but driving the emitter work into an inductive load. Q1 and Q2 inductively load the delay-line driver which, shunted by stray capacitive components, causes overshoot or ringing. Including C1 and C2 adds capacitive reactance in series, countering Q1 and Q2 inductive reactance. R1 and R2 must also be considered part of this network.

Shunt peaking improves collector step response. Adjusting R8 and R9 sets the peaking network L/R. $R_o \simeq 160\ \Omega$ at DC.

Zener diodes D1 and D2 shunt the temperature compensation network, curbing the saturation of Q1 and Q2. Large signals drive Q1 or Q2 into saturation due to the drop across R4 or R5. The resultant distortion could be unimportant since saturation occurs at an off-screen voltage. However, these transistors recover too slowly to be allowed to saturate. Therefore, D1 or D2 turns on when the drop across R4 or R5 exceeds 6 volts, averting saturation of the appropriate transistor.

Fig. 6-40 design calls for input waveform distortion. It creates an overpeaked waveform which sags. This corrects for the termal roll-off characteristics of the final amplifier stage. The roll-off is relatively long-term. If left uncorrected, the CRT trace would vertically shift. By including shift correction, the operator need not continually readjust the vertical position control.

Signals encounter a form of emitter peaking. The leading edge of an input step causes the shunt impedance of L1, L2 and R3 to reach maximum. Maximum emitter (collector) signal current flows. After the transistion L1 and L2 impedance decays, reducing shunt impedance to the value of R3. R3 then shunts about 20% of the signal current.

This peaking is a short-term effect which insures "fast" leading edge reproduction. L1 and L2 decay produces sag, but this is far too short-term to consider it compensation for output amplifier thermal distortion. R_e (R3) does enter the calculations.

The resistance of R_e sets distortion amplitude. There is a lower limit to R_e that causes nonlinear sag. Output waveform error is proportional to:

$$\frac{V_{ce} \text{ bias error}}{R_e}$$

Purposely operating Q1 and Q2 at a low V_{ce} develops the desired sag slope. Q1 and Q2 V_{ce} = 4 V, two less than $\frac{V_{CC}}{2}$.

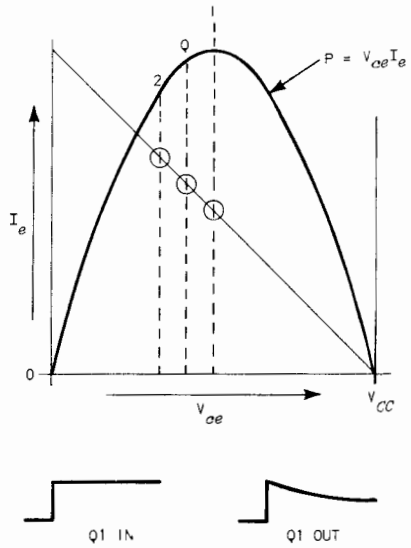


Fig. 6-41. $V_{ce} < \frac{V_{CC}}{2}$. Long-term thermal effect is negative sag.

Dissipating less than maximum power at quiescence results in thermal signal differences across the input terminals. Fig. 6-41 represents the V_{ce} plot of Q1 and Q2. Quiescently, Q1 and Q2 dissipate less than maximum power. With a positive input, Q1 current decreases but power increases, while Q2 current increases reducing device power. ΔP is negative:

Q1 heats

Q2 cools

Q1 V_{be} decreases

Q2 V_{be} increases

Effective signal, or gain, decreases creating negative sag.

Keep in mind that these are *slow* changes affecting the flat-top of a step. The termination amplifier introduces sag to cancel the output amplifier distortion which is biased for V_{ce} greater than 1/2 V_{CC}.

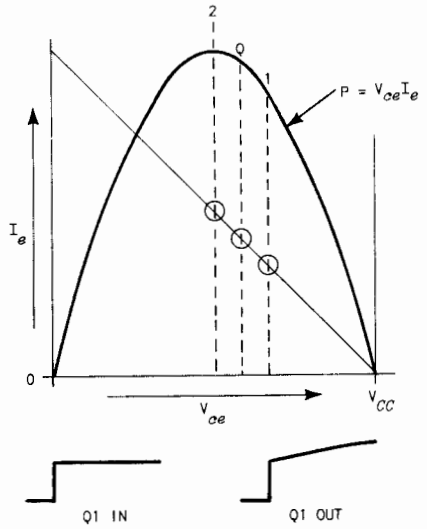


Fig. 6-42. $V_{ce} > \frac{V_{CC}}{2}$. Long-term effect is positive sag.

Fig. 6-42 represents the plot of output amplifier power. ΔP is positive developing a "hump" in the output step. With a positive input, Q1 conduction and power decreases and Q2 conduction and power increases:

Q1 cools

Q2 heats

Q1 V_{be} increases

Q2 V_{be} decreases

Effective signal, or gain, increases.

Correctly biased, the two stages give an overall flat response as effective as the "ideal" biasing: $V_{ce} = \frac{V_{CC}}{2}$.

driver amplifier

The amplifier of Fig. 6-40 direct-couples to the driver amplifier shown in Fig. 6-43A, a cascode amplifier which provides centering calibration and a selectable bandwidth.

Q1 and Q2 emitter circuits contain emitter peaking RC networks. R1 and R2 determine degeneration.

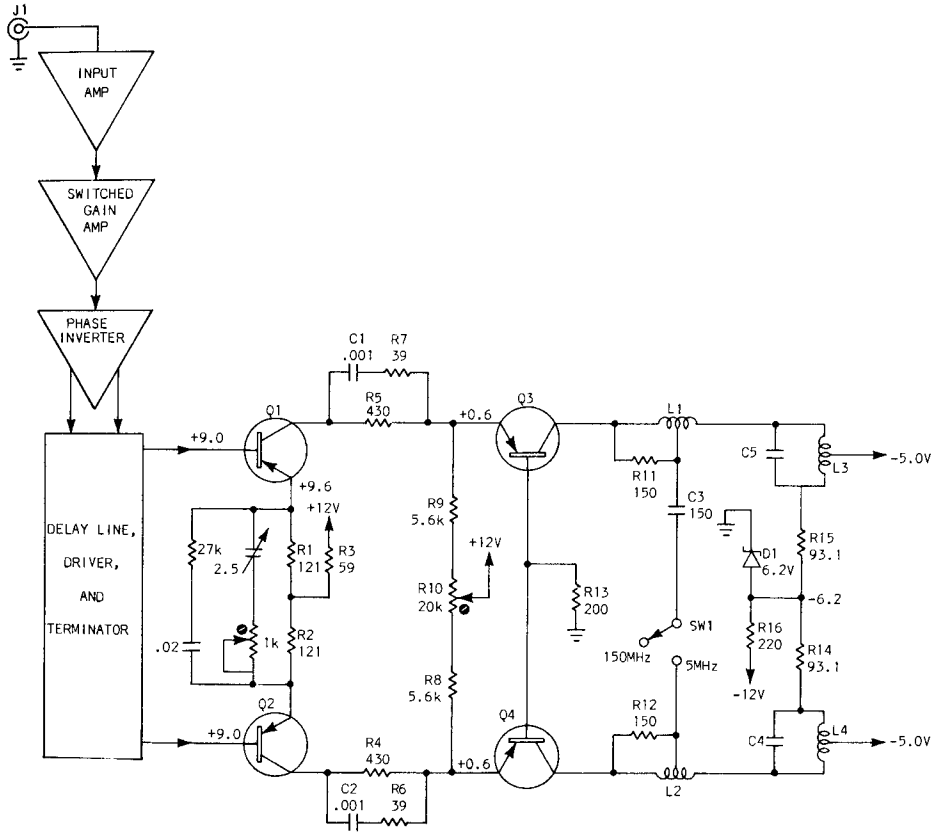


Fig. 6-43A. Main vertical driver amplifier.

Q1 and Q2 collector circuits include temperature compensation, oscillation damping, and a positioning adjustment. R4 and R5 bypassed by C1 and C2 temperature compensate. Distributed capacitance and input inductance of common-base amplifiers Q3 and Q4 form a resonant circuit. R6 and R7 load the tank circuit, preventing oscillations. Resistive network R8, R9 and R10 injects a small quantity of current into Q3 and Q4. Moving the wiper of R10 changes the percentage of current injected into Q3 and Q4 emitters, correcting for any quiescent imbalance.

Q3 and Q4 collector circuits contain a switch, SW1. Positioning SW1 as shown, places no restriction on *system* response. Signals develop across bridged T-coils, L3-C5-R15 and L4-C4-R14. Throwing SW1 to the 5 MHz position increases output capacitance, reducing *system* upper frequency -3 dB point to 5 MHz. Networks L1-R11 and L2-R12 allow frequency response above 5 MHz to roll-off at a 6 dB per octave rate.

upper frequency response

R16 and D1 develop collector voltage as long as collector current drops less than 6 V across R16.

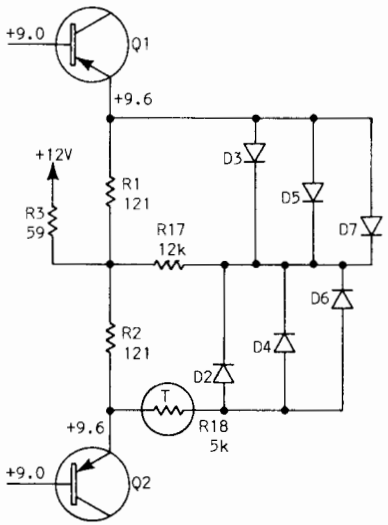


Fig. 6-43B. Diode and thermistor temperature compensation. All semiconductors silicon.

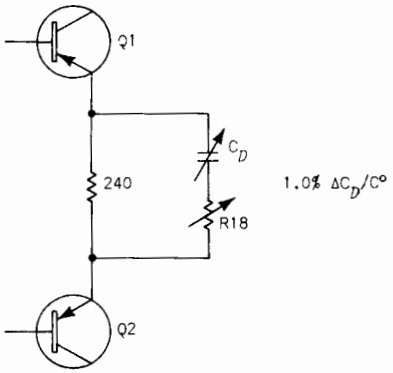


Fig. 6-43C. Peaking circuit equivalent of the diode-thermistor configuration.

thermal compensation

Transistor amplifiers suffer an increase in risetime with temperature. "Standard" thermal techniques, satisfactory for instruments of about 4 ns or more risetime, are insufficient for "faster" instruments. Thermal compensation results from added components to the emitter circuit of Fig. 6-43.

thermistor

Fig. 6-43B, a partial emitter circuit, shows the additional components shunting R_i (R1 + R2). Q1, Q2 and all diodes are silicon. R18, the 5 k thermistor has a negative temperature coefficient. R17 limits diode current. However, diode current flows only during interruption of Q1 or Q2 conduction. The diodes remain reverse biased under normal operating conditions.

The reverse-biased diodes and R18 function as RC emitter peaking, variable with temperature. Reverse-biased diodes present capacitance which varies with applied voltage or temperature. In this case voltage across the diodes changes too little for consideration. Capacitance, of these particular diodes, varies 1.0% for each degree C change.

Diode capacitance increases and resistance of R18 decreases as temperature increases. The result is a peaking as shown in Fig. 6-43C. Emitter peaking increases with temperature hindering risetime slowdown.

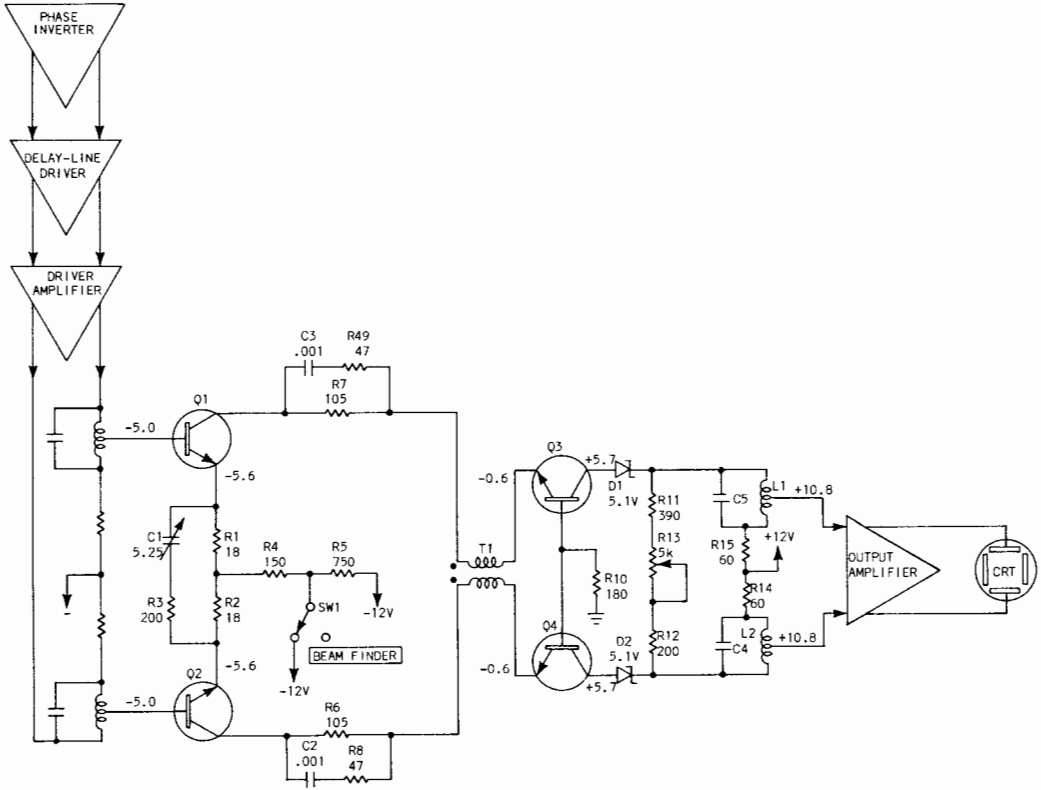


Fig. 6-44. Intermediate driver amplifier.

intermediate driver amplifier

The circuit of Fig. 6-43 drives a stage as the cascode shown in Fig. 6-44. This circuit provides a beam finder circuit, common-mode suppression and an internal gain adjustment.

beam finder

Energizing BEAM FINDER switch, SW1, restricts vertical deflection to the CRT central viewing area. Throwing SW1 changes Q1 and Q2 emitter operating point. In the emitter circuits, C1 and R3 develop emitter peaking, R1 and R2 determine degeneration (R_i) and R4, or R4 and R5, establish circuit current. Normal operating conditions exist with SW1 positioned as shown. Voltage across R4 generates total current available to develop push-pull signals across R_o.

Throwing SW1 to BEAM FINDER position increases longtailing resistance by R5. Increasing emitter return resistance by 600% reduces total current available by the same amount. I_e reduced by 6 increases r_e by 6. Deflection factor (gain) decreases so that vertical trace deflection cannot exceed the central CRT viewing area.

Q1 and Q2 collectors contain temperature compensation networks C2-R6 and C3-R7. R8 and R9 suppress oscillations due to emitter (Q3-Q4) inductance and stray capacitance. T1 cancels common-mode signals. Consider common-mode signals in-phase current at the collectors of Q1 and Q2 such as power supply induced noise, unequal amplitude signals, unequal signal phase shift, and in-phase oscillations. T1 acts as a straight-through connection to push-pull signals. In-phase signals oppose T1 transformer action and are severely attenuated.

D1 and D2 maintain reasonable collector-to-emitter voltage across Q3 and Q4. Bases of Q3 and Q4 return to zero volts DC. Their collectors return to +10 volts through low resistance bridged T-coil networks. D1 and D2 add 5.1 V to the drop across T-coil networks, L1-C5-R15 and L2-C4-R14. Reducing collector-to-emitter voltage reduces active device power dissipation (E1).

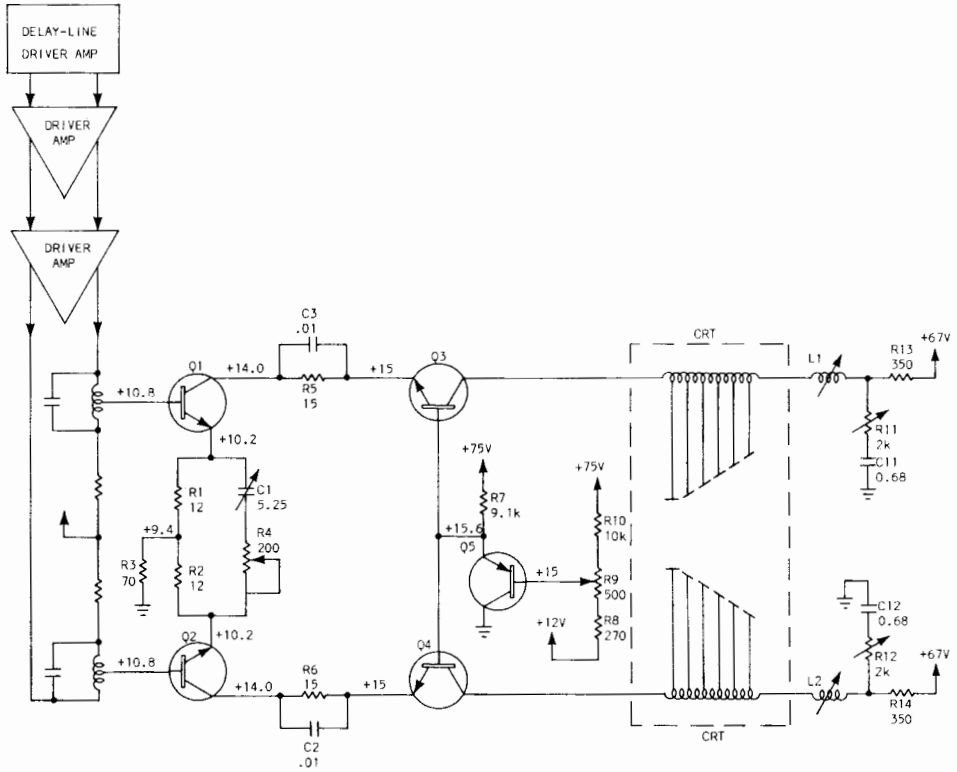


Fig. 6-45. Main vertical output amplifier.

T-coil networks shunted by the resistive network, R11, R12 and R13 comprise R_o. Adjusting R13 through its range varies R_o by about 15%. $A_V = \frac{R_o}{R_i}$.

2.5 ns output amplifier

The circuits beginning with Fig. 6-40 finally drive the output amplifier shown in Fig. 6-45, a push-pull cascoded amplifier driving a distributed deflection CRT. The circuit features an adjustable common-base return, controlling active-device power dissipation.

Quiescent base voltage and the low value of common-emitter return resistance, R3, indicates a large quantity of emitter current. R1 and R2 determine R_i. C1 and R4 provide emitter peaking.

Collector voltage of Q1 or Q2 depends upon values of R5, R6 and Q5 emitter voltage. Adjusting collector voltage, across Q1 and Q2, sets active-device thermal characteristics. This collector potential changes volt for volt with the Q3 and Q4 base setting. Emitter follower Q5 is a low-impedance, adjustable, base supply. Regulating the NPN base voltage with a PNP provides thermal tracking.

Consider V_{CC} the difference between the drop across R3 and Q3 or Q4 emitter voltage. V_{ce} exceeds 1/2 V_{CC} at quiescence. This was done to prevent saturation of Q1 or Q2 while processing high-amplitude signals. Although saturation would occur off-screen, these devices take longer to recover from saturation than from cut-off. Since this is a push-pull amplifier, if one transistor were saturated, the other would probably be cut off. Operating with V_{ce} greater than 1/2 V_{CC} prevents saturation, at the expense of thermal distortion. The resulting distortion precludes flat-top reproduction. DC measurements shift, or gain increases, at the rate of Q1 and Q2 junction temperature changes.

distortion correction

Opposing distortion developed by an earlier amplifier (Fig. 6-40) corrects for output amplifier distortion. By the time an "ideal" input step arrives at the bases of Q1 and Q2, it appears as an overpeaked waveform with sag. Adding Q1 and Q2 distortion to the waveform results in a fast-rise

step with a flat-top. To accomplish cancellation, the opposing distortions should track. The setting of R9 then determines flat-top response. This is true because adjusting R9 varies collector voltage, or power curve operating point, for Q1 and Q2.

4 ns output amplifier

The output amplifier just presented is part of a vertical specified at less than 2.5 nanoseconds risetime. Amplifiers required to respond one or two nanoseconds slower are simpler. Fig. 6-46 is such an amplifier. This amplifier contains longtailing, RC temperature compensation, common-mode oscillation rejection and series peaking networks.

Emitter circuits of Q9 and Q10 generate total circuit current. R28, R29 and R30 longtail. R29 and R30 paralleled by R32 establish R_i.

Collector circuits of Q9 and Q10 contain temperature compensation and common-mode oscillation rejection. C9-R31 and C10-R34 thermally compensate. T1 provides common-mode rejection. T1 presents negligible impedance to push-pull currents. In-phase or common-mode signals "buck" transformer action, developing high impedance. Cascode amplifiers tend to break into high-frequency, common-mode, oscillations. T1 action causes a large voltage swing, during in-phase

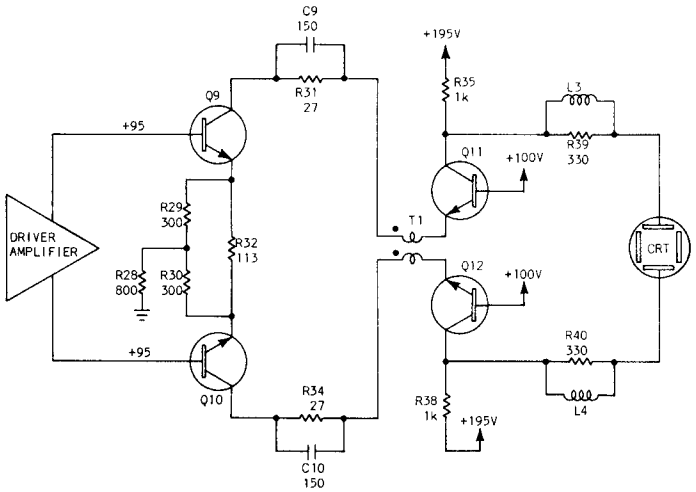


Fig. 6-46. Main vertical output amplifier.

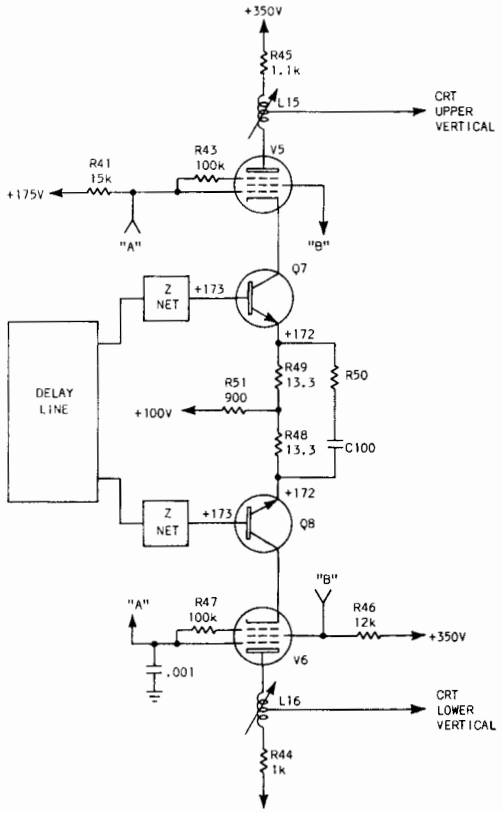


Fig. 6-47. Hybrid cascode output amplifier.

oscillation, at Q9 and Q10 collectors. Degenerative feedback to Q9 and Q10 bases due to Miller-effect damps the oscillation. T1 also rejects common-mode signals such as power-supply transients.

Output circuits are series peaked. R_O consists of R35 and R38. L/R networks L3-R39 and L4-R40 combined with stray capacitance form a series peaking network.

hybrid cascode output amplifier

Output cascoded amplifiers are not restricted to pure transistors. See Fig. 6-47, a hybrid cascode amplifier.

Z networks, in the driver amplifier base circuits, terminate the delay line. R51, in the emitter circuit, longtails; R48 and R49 control gain (R_i); and R50-C100 emitter peak. Collector circuits regulate at, approximately, the control grid voltage of V5 and V6.

Returning V5 and V6 control grids to a fixed DC level cause these to be grounded-grid amplifiers. T-coil peaking allows R_O to appear resistive over a broad band of frequencies. R_O, within design limitations, equals R44 and R45. Adjusting L15 and L16 compensates for circuit variables.

phase inverters

Emitter-, source- or cathode-coupled phase inverters are differential amplifiers with one input terminal grounded. The ground can be actual, apparent or virtual.

drive to push-pull amplifiers

Variously called phase splitters, paraphase amplifiers and phase inverters, these amplifiers convert single-ended signals to push-pull, or double-ended signals to drive push-pull amplifiers. Conceptually, method of drive is the difference between a push-pull amplifier and a phase inverter.

See Fig. 6-48. The bracketed waveforms represent a push-pull signal. Applying this signal across R_i generates signal currents which, flowing through R_O, develops the output signal voltage. Voltage ratio (V_O/V_i) and thus resistance ratio (R_O/R_i) indicates a push-pull gain of 5.

Phase-inverter amplifiers react the same as push-pull. Refer to the nonbracketed input waveforms of Fig. 6-48. 2 volts across R_i develops signal currents that generate 10 volts push-pull output.

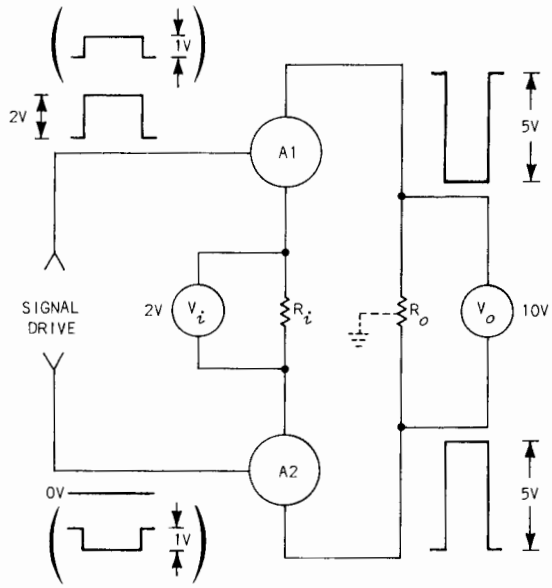


Fig. 6-48. Phase inversion.

Voltage ratios (V_O/V_i) and resistance ratios (R_O/R_i) remain the same for push-pull or phase inversion amplifiers.

Input signal comparisons show the only difference. Referred to ground, the A1 input push-pull signal appears 1 volt in amplitude and maintains 180° phase relation to the A2 1-volt input signal. 2 volts develops across R_i. Considering the same terminals for phase inverter drive, the A2 input remains fixed at 0 volts, and A1 appears as a 2 volts single-ended signal. 2 volts again develops across R_i. Push-pull amplifiers driven single-ended act as phase inverters.

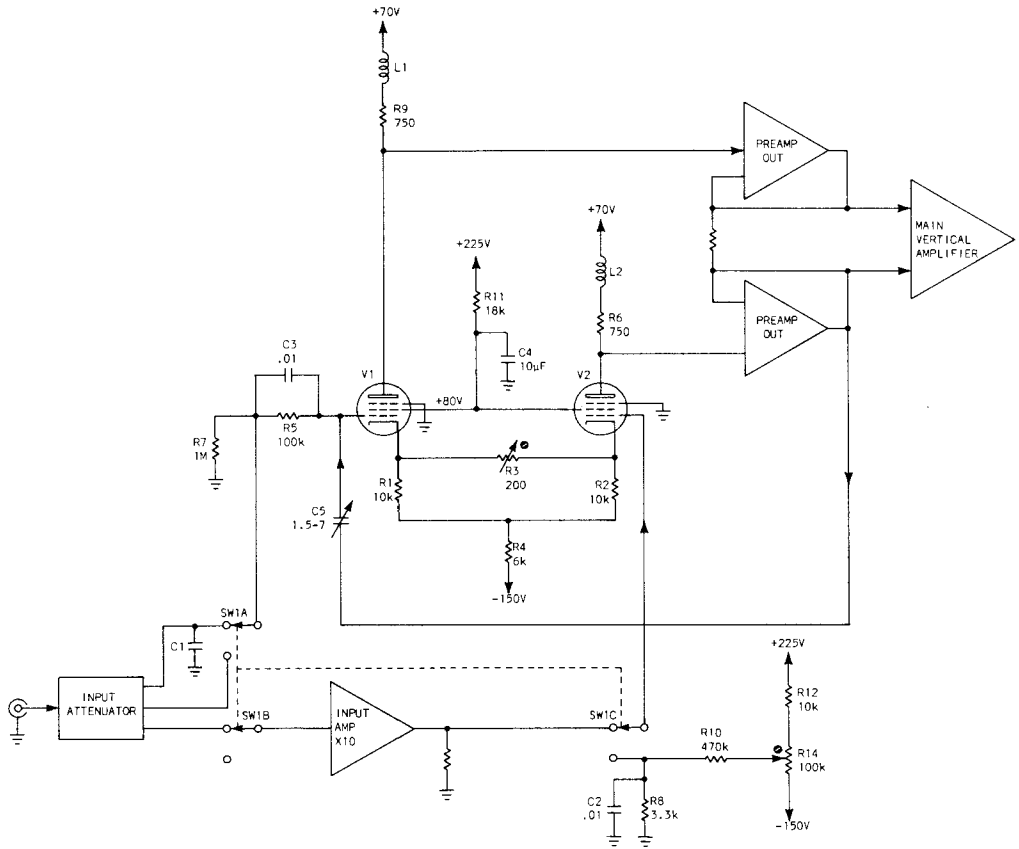


Fig. 6-49. Phase inverter with switched input terminals.

Fig. 6-49 is an example of a signal drive determining phase-inverter action. By switch selection, either input terminal receives signal drive or returns to apparent ground. Adjustable neutralization prevents input capacitance changes when the phase inverter functions as an input amplifier.

Fig. 6-49 shows the amplifier with two modes. Selecting mode 1, as drawn, the amplifier functions as a preamplifier phase inverter, driving the push-pull preamplifier output stage. Actuating SW1 initiates mode 2 operation. V1 and V2 become a phase-inverting input amplifier, providing push-pull drive to the cathode-follower output amplifiers.

SW1 A, B and C are mechanically ganged to the input attenuator switch. Front panel control VOLTS/DIV provides operator selection of SW1 positions.

Consider mode 1 circuit action. The X10 input amplifier acts as a signal source, driving the V2 control grid via SW1C. V1 control grid returns to apparent ground through C1, via SW1A. Signals develop across R_i, composed of r_{k1}, r_{k2} and R3. Longtail circuitry, R1, R2 and R4, stabilize r_{k1} and r_{k2}. Comparison of R3 to network R1, R2 and R4 indicates a desirable ratio of R_i to longtail R. R_o consists of R6 and R9, shunt-peaked by L1 and L2. R11 and C4 decouple V1 and V2 screen grid signals.

Mode 2 operation results from selection of a deflection factor that places SW1A, B and C in the "down position. V1 becomes the driven device and V2 the grounded-grid device. Signals from the input attenuator develop across R7 to drive V1. The control grid of V2 returns to apparent ground through C2. R_i, longtail, R_o and screen grid decoupling elements remain as described for mode 1. Input terminal circuitry differs.

DC balance

V2 control grid circuitry now provides adjustable DC balance. Signal voltages across R_i represent the voltage difference between V1 and V2 control grids. Any difference in quiescent control grid voltage develops across R_i and appears as a positional voltage to following stages of amplification. Resistive network R8, R10, R12 and R14 allows one to adjust V2 control grid, about 1 volt either side

of zero volts for quiescent balance. A balanced condition also allows one to adjust stage gain without vertically shifting the CRT display. R3 sets stage gain and under balanced conditions no DC current flows through this resistor.

compensation

V1 control-grid circuitry is an attempt to maintain attenuator loading (R and C) balanced. Either the X10 amplifier grid circuit or the V1 grid circuit shunts the compensated attenuator. To maintain compensation input RC time constants must be the same.

Resistance balance is fairly simple. R7 and the X10 counterpart are selected for equal resistance.

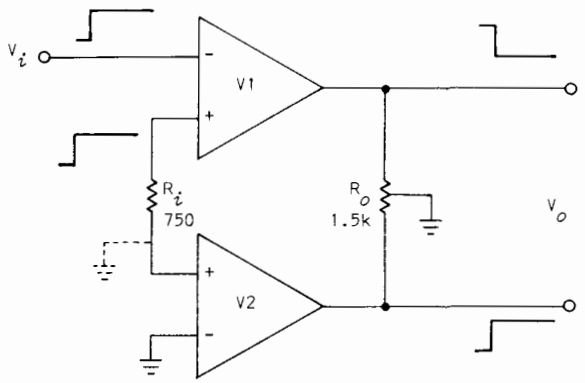
Capacitive compensation is also simple. One adjusts C5 and one other capacitor for attenuator compensation balance between V1 and the X10 amplifier.

neutralization

Dismissing C5 as a neutralization capacitor leaves explanatory gaps. Further, "neutralization" of this type appears in many differential amplifiers. Classically, neutralization takes the form of regenerative feedback which neutralizes "Miller-effect" degeneration, thereby stabilizing gain. C5, however, stabilizes V1 input capacitance. The initial setting of C5 adds a calibrated quantity of input capacitance to V1. Parameter changes of V1 or V2 change input capacitance. These changes also change gain, which changes the quantity of current drawn by C5. This current adds to or subtracts from input capacitance, stabilizing it at the original value.

Before investigating the elements responsible for input capacitance, eliminate those having negligible effect, then determine gain. Suppressor grid reactive components have small effect since these grids return to ground. Decoupling and push-pull currents minimize screen-grid loading. "Miller-effect" depends upon multiplication of the small plate-to-grid capacitance by gain.

$A_V = \frac{R_O}{R_i}$. Fig. 6-50 shows input voltage applied to the (-) input terminal of V1 and signal ground at the (-) input terminal of V2. V1 and V2 attempt to maintain a null between input terminals. Therefore,



$$A_V = \frac{V_o}{V_i} = \frac{R_o}{R_i} \approx 2$$

$$R_o = R6 + R9$$

$$R_i = r_{k1} + \frac{.5R3}{n} + r_{k2}$$

Fig. 6-50. Equivalent circuit.

V_i develops at the (+) input terminal of V1 and virtual ground at the (+) input terminal of V2. This voltage across R_i creates the current which flows through R_o to develop V_o. R_o consists of R6 and R9. R_i is made up of r_{k1}, r_{k2} and R3, set to mid-range and modified for screen current. Gain is 2.

Gain refers to voltage developing across the output terminals. Unity gain develops from either output terminal to ground. Notice that V1 inverts the input signal and V2 does not. This demonstrates the quantity of "Miller-effect" and C5 action.

Miller-effect develops across V1: $C_m \approx C_{pg}$. $(1 + A_V) \approx 2\ C_{pg}$. This is small enough, in this case, to ignore.

C5 connects the output of V2 to the input terminal. With outputs balanced and X2 gain, C5 has small effect. When an imbalance develops, current flows through C5 "neutralizing" the changing input capacitance.

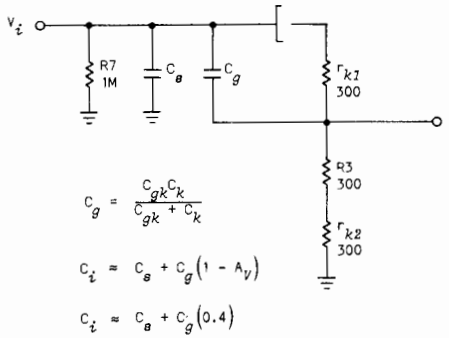


Fig. 6-51. V1 equivalent input circuit without C5.

input capacitance

Input capacitance changes result from signal voltage division across R_i. The equivalent input circuit appears in Fig. 6-51. Input capacitance, at rest, consists of stray components, C_s, shunting grid-to-cathode, C_{gk}, and cathode-to-ground, C_k, capacitances. Combining C_{gk} and C_k for simplicity, yields C_g. Dynamically, C_s retains its original value but C_g reduces by the gain factor from grid to cathode of V1.

The percentage of V_i that develops at the connection of C_g and R_k (R3) establishes the effective capacitance of C_g: $C = C_g\ (1 - A_v)$. Voltage divider r_{k1}, r_{k2} and R3 determines gain. Fig. 6-51 shows C_g reduced to 40% of its original value. This is the balanced condition: $r_{k1} = r_{k2}$.

If V1 and V2 were always balanced, C5 would have been unnecessary. C_g would have remained at a fixed value. Seldom do two tubes present equal *gm*. Further, *gm* changes with tube age. The resulting imbalance changes input capacitance, V1 and V2 gain and causes feedback current flow through C5. To illustrate this, assume a large imbalance. $r_{k1} = 100$, R3 = 100 and $r_{k2} = 500$. Although R_i, therefore paraphase gain, remains unchanged, C_g varies:

$$C = C_g\ (1 - A\ )$$

$$C = C_g\ (1 - 0.85)$$

$$C = 0.15\ C_g$$

Balanced, $C = 0.4\ C_g$

Reversing the *gm* differences:

r_{k1} = 500, R3 = 100 and r_{k2} = 100,

$C = C_g\ (1 - 0.14)$

$C = 0.85\ C_g$

C_g changes, smaller than those above, affect the input attenuator compensation. Thus the need for input capacitance stabilization such as "neutralization" capacitor C5.

preamplifier phase inverter

Phase inverters, isolated from the input attenuator and with less stringent risetime requirements are simpler than in Fig. 6-49. Fig. 6-52 is such an amplifier. This amplifier performs three functions:

1. Develops push-pull drive for the main vertical amplifier.
2. Greatly amplifies the input signal voltage.
3. Provides the front panel POSITION control.

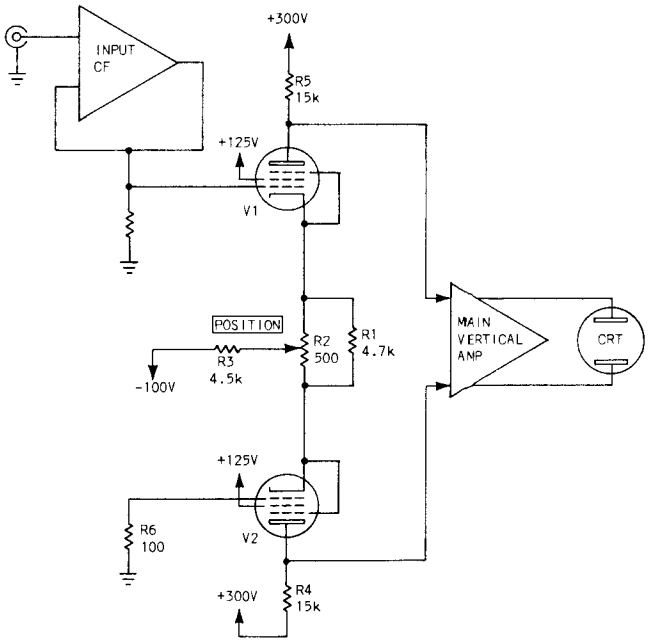


Fig. 6-52. Phase inverter as preamplifier output amplifier.

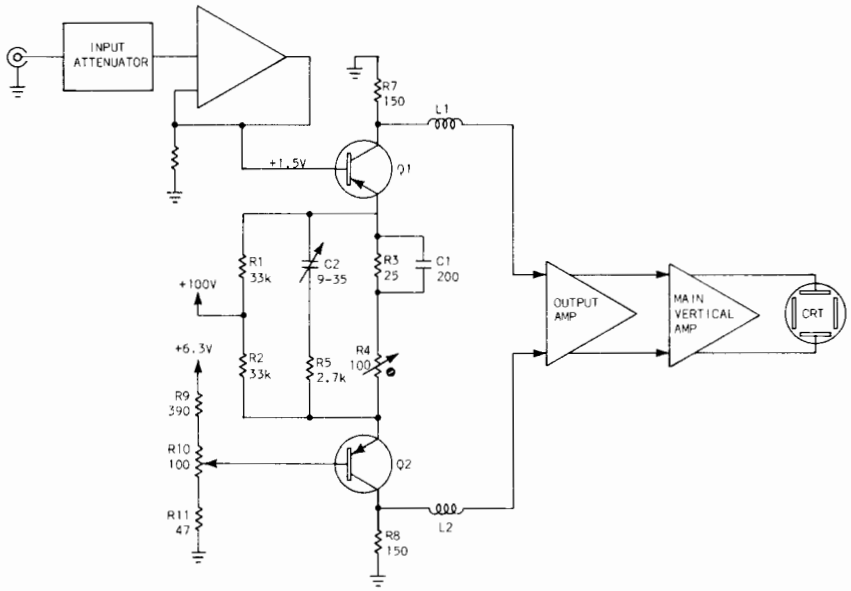


Fig. 6-53. Transistorized phase inverter.

The input cathode follower serves as a voltage source driving the control grid of V1. V2 control grid returns through a low resistance, R6, to ground. Input signal voltages develop across R_i, consisting of r_{k1}, plus R1 paralleled by R2 (corrected for screen current) and r_{k2}. A large value R_o, R4 and R5, develops high gain. Equivalent resistance of R1, R2 and R3 longtail the circuit.

Moving the wiper of R2 changes output level but not voltage gain. Changing the wiper effects small changes in total longtail current flowing through R4 and R5. Tube transresistances change in opposite directions, if at all, R_i, ergo voltage gain remains the same.

transistor phase inverter

Transistors present too low an impedance to appear as input amplifiers. Low input base impedance also adds to circuit complexity of the common-base half of a transistor phase inverter. See Fig. 6-53. This circuit develops a voltage gain of about 4, driving the preamplifier output amplifier push-pull. Circuit features include longtailing, internal gain adjustment, a position or balance control, and high-frequency compensation.

Single-ended signals applied to the base of Q1 develop across R_i. R_i consists of R_{t1}, R3, R4 and R_{t2}. R7 and R8 make up R_o. Setting R4 controls the ratio R_o/R_i. Longtail resistors R1 and R2 DC-shunt R3 and R4.

Risetime improvement appears in both the emitter and collector circuits. Networks C2-R5 and C1-R3 emitter peak. Inductors L1 and L3 are part of a series peaking network.

balance

Adjustable voltage at the base of Q2 represents either an internal DC Balance adjustment or a front panel POSITION control. One sets R10, as a balance adjustment, under no-signal conditions. Proper Q2 base voltage matches Q2 collector current to Q1 collector current. This calibration also insures no DC current through gain adjust, R3.

position

Connecting R10 to a front panel POSITION control allows the operator to empirically match or mismatch collector currents. He, of course, observes the results at the CRT. Any base voltage difference,

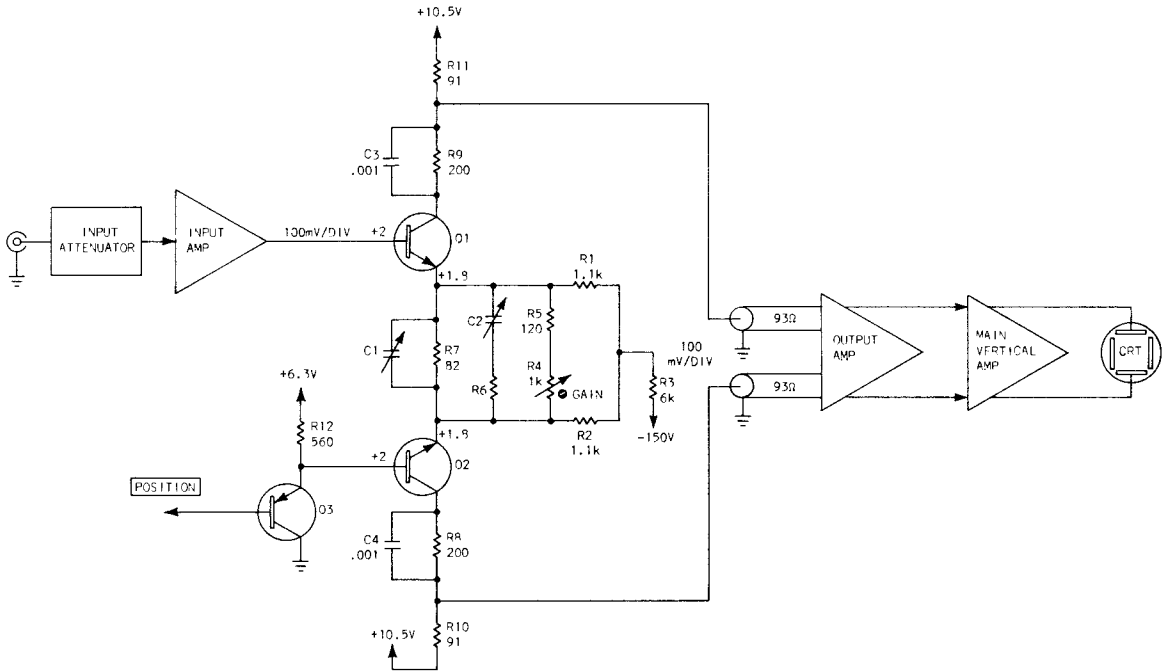


Fig. 6-54. Low impedance, common base drive.

between Q1 and Q2, appears across R_i and develops positional output voltage. Amplified, this voltage vertically deflects the CRT display. R10 as a position control results in three possible undesirable effects:

1. Gain calibration vertically shifts the trace, except at center screen.
2. R_i and thus gain changes with positioning.
3. Q1 and Q2 gain balance changes with vertical positioning.

Base circuit resistance reflects into the emitter of any transistor. Approximately $1/\beta$ times base circuit resistance adds to transistor emitter resistance. Changing R10 changes R_i, changing total circuit gain. Q2 gain changes more than Q1 gain, so an unbalanced gain condition results. These effects are negligible if the reflected resistance represents a small percentage of R_i. A better method would change bias from a voltage source of constant low impedance.

Fig. 6-54 represents improved common-base drive. R1, R2 and R3 longtail the circuit. R_i consists of the equivalent resistance of R1, R2, R4, R5, R7, R_{t1} and R_{t2}. R10 and R11, shunting Z_O, define R_O and terminate the transmission lines. C3-R9 and C4-R8 provide temperature compensation. Emitter peaking results from C1, C2 and R6. The circuit improvement appears in the base of Q2.

The emitter follower provides positional drive to common-base amplifier, Q2. Voltage changes at the base of Q3 appear almost volt for volt across R_i. Base circuit resistance divided by the β of Q3 appear in the emitter. Q3 emitter resistance divided again, this time by the β of Q2, adds to R_i. Ignore it. Consider the base of Q2 apparent ground.

When dealing with tubes keep in mind the close relationship between gm and I_k. Also remember that adding components usually increases stray reactance. Refer to Fig. 6-55

The phase inverter shown contains six notable features:

1. Longtailing.
2. Adjusting gm sets gain.
3. A variable, uncalibrated VOLT/DIV control is available.
4. Cathode current balanced by adjusting V2 conduction.
5. Returning suppressor grids to apparent ground prevents reactance associated with the suppressor grids from appearing in the cathode circuits.
6. Plate loads consist of combination peaked T-coils.

The input amplifier develops a single-ended signal at the control grid of V1. Signal voltages develop across R_i consisting of r_{k1} and r_{k2}. (SW1 normally shorts R6.) Resistive network R2, R3, R4 and R5 longtails the amplifier. Adjusting R5 sets total tube current, thus gm, thus r_{k1} and r_{k2} which constitute R_i. Since voltage gain is R_o/R_i, R5 adjusts gain.

Actuating SW1 decreases gain by the value of R6. R6, a front panel control provides the operator a between-step, uncalibrated, VOLTS/DIV control. Changing degeneration (R6) does not shift the vertical display as long as V1 and V2 cathode currents balance.

Controlling V2 control-grid voltage balances cathode currents. V1 and V2 suppressor grids, and V2 control grid, return to a common point -- the wiper of R7. C1 causes the wiper to function as an apparent ground. V1 and V2 suppressor grids return to the same apparent ground.

Plates work into a form of lumped-parameter transmission line, combination-peaked T-coils. R8 and R9 make up R_o. The transmission line action causes R_o to appear resistive and constant over a broad frequency spectrum.

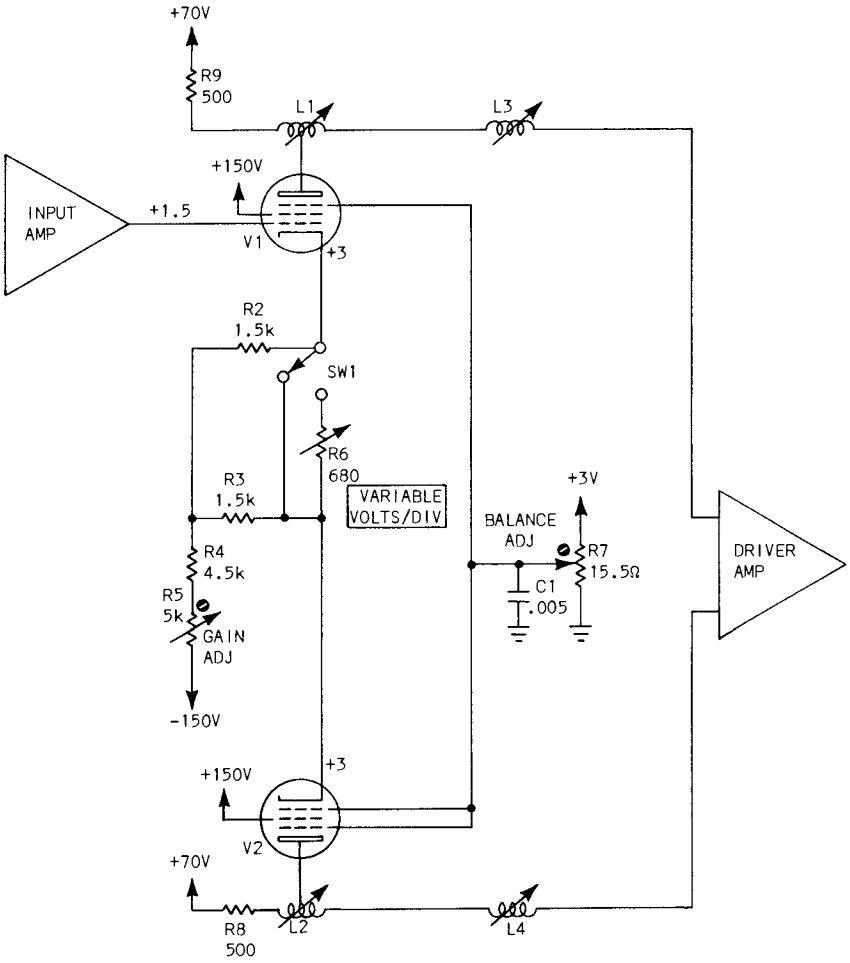


Fig. 6-55. Adjusting gm adjusts gain.

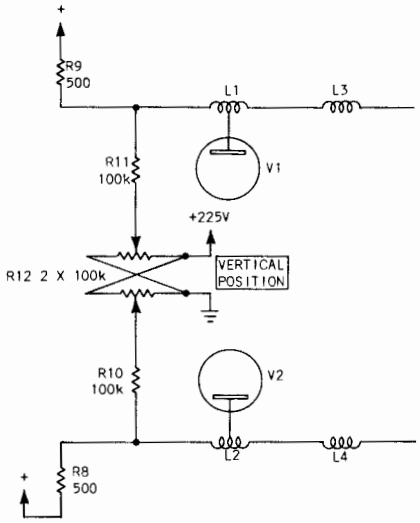


Fig. 6-56. Position control circuit added.

Position control circuitry may also appear in the plate circuits of this amplifier. Proper selection and adjustment of T-coil components causes the stray capacitance of the additional circuitry to become a part of the peaking network. Fig. 6-56 shows addition of the resistive position control network R10, R11 and R12. This arrangement allows plate voltage changes without loading R_O. Adding the network at the termination, and proportioning L1 and L2, lumps capacitive loading associated with additional components into T-coil peaking. Resistive shunting is negligible, R_O = R8 + R9.

Another circuit, which a points-of-interest listing summarizes, appears in Fig. 6-57:

1. Longtail adjustment sets following stage operating point.
2. A cathode follower drives the grounded grid section.
3. Plate circuitry enhances position control action.
4. R_O contains unusual T-coil configuration.
5. Plate circuitry includes sag (DC shift) compensation.

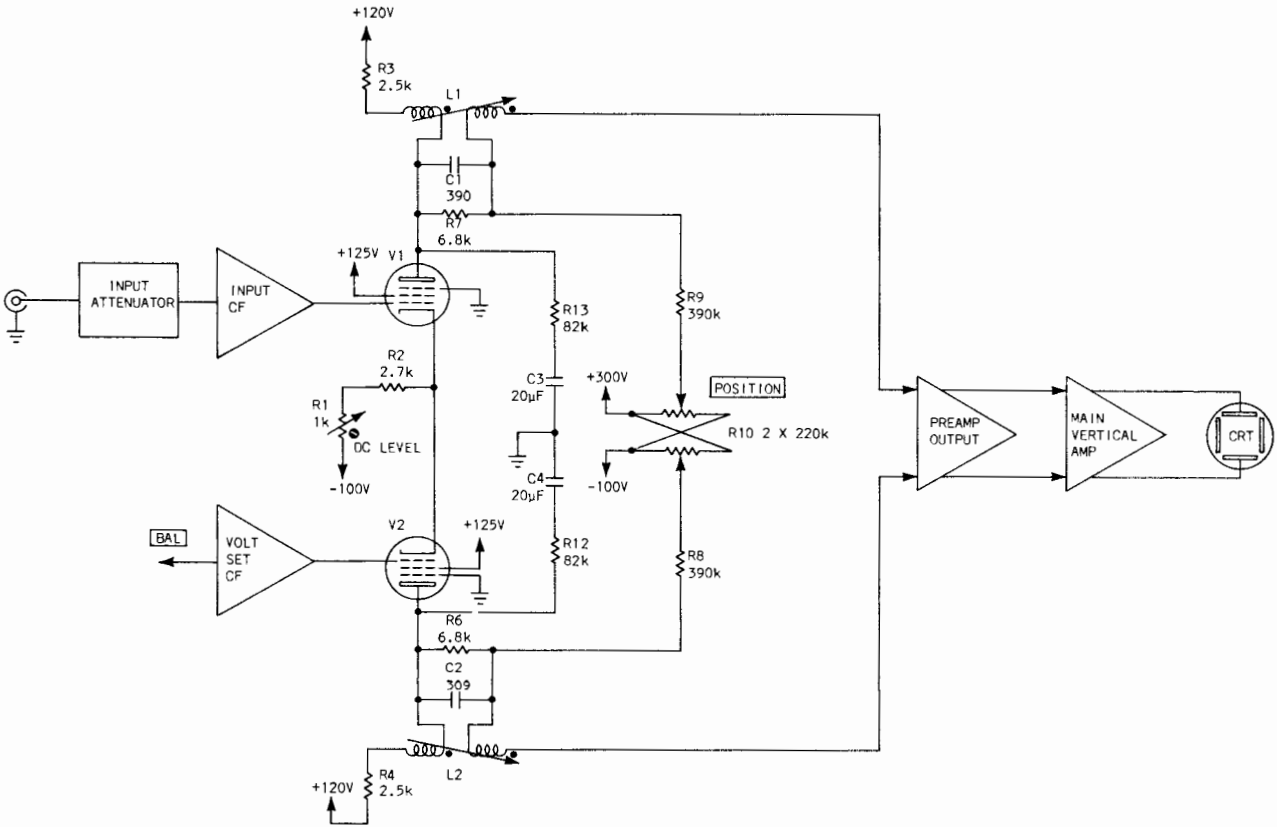


Fig. 6-57. DC components removed from T-coil peaking.

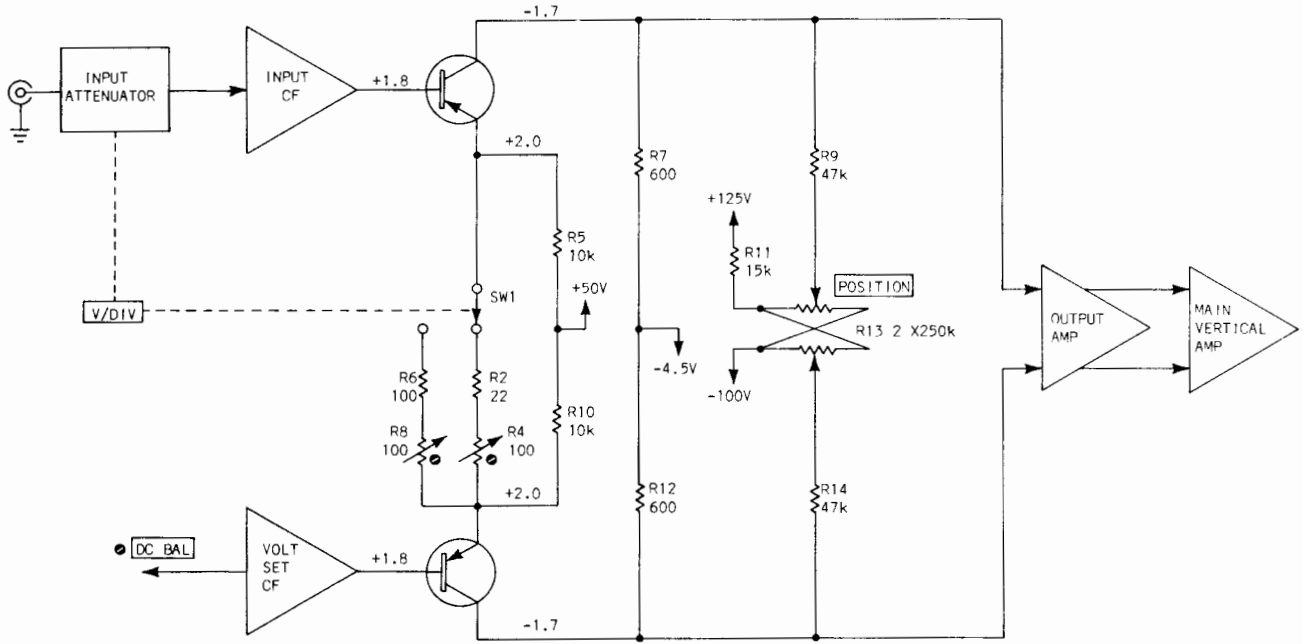


Fig. 6-58. Switched gain paraphase amplifier.

Single-ended input signals to V1 develop across R_i made up of r_{k1} and r_{k2}. The control grid of V2 works into the low output impedance of a cathode follower. R1 and R2 longtail the circuit. Adjusting R1 affects gain, but mainly sets quiescent plate voltage for optimum operating point of the preamplifier output-amplifier. R_O consists, essentially, of a terminated transmission line. Consider R_O the sum of R3 and R4. The remaining plate circuitry varies R_O to develop desirable output voltages.

Resistive network R6, R7, R8, R9 and R10 provides position control circuitry. Tapping position-control voltage at the junction of R7-R9 and R6-R8, vice the junction of R3-R7 and R4-R6, allows a larger percentage of position voltage to drive the following stage with smaller (V1-V2) plate voltage changes. Center taps of T-coils L1 and L2 separate to accommodate this voltage divider action.

Connecting components to T-coil center taps reduces the capacitive loading these components introduce. L1 and L2 act as center-tapped T-coils during voltage transitions. Signals unaffected by reactive T-coil elements become slightly attenuated by the position-control divider action. For example, DC signals experience about 2% attenuation. This balances the losses imposed by sag compensation.

DC shift compensation

R12-C4 and R13-C3 reduce R_O about 3% during transit of output signals. Sag compensation is sometimes called DC shift compensation. The explanation is that an increase in low-frequency gain occurs below about 1 Hz. DC shift networks correct by shunting R_O at frequencies above 1 Hz, thus allowing R_O to increase for frequencies below 1 Hz.

switched-gain paraphase amplifier

Several of the phase inverters presented included a variable VOLTS/DIV control. These controls cause no vertical shift in a balanced emitter circuit. In a balanced circuit no DC current flows through the degenerative coupling resistance. Therefore, one should be able to switch-select calibrated, fixed resistors, thereby selecting deflection factor. Such is the case in Fig. 6-58.

Q1 and Q2 reflect equal resistance into their respective emitters since each is driven by a cathode follower. Properly adjusted for balance, DC currents

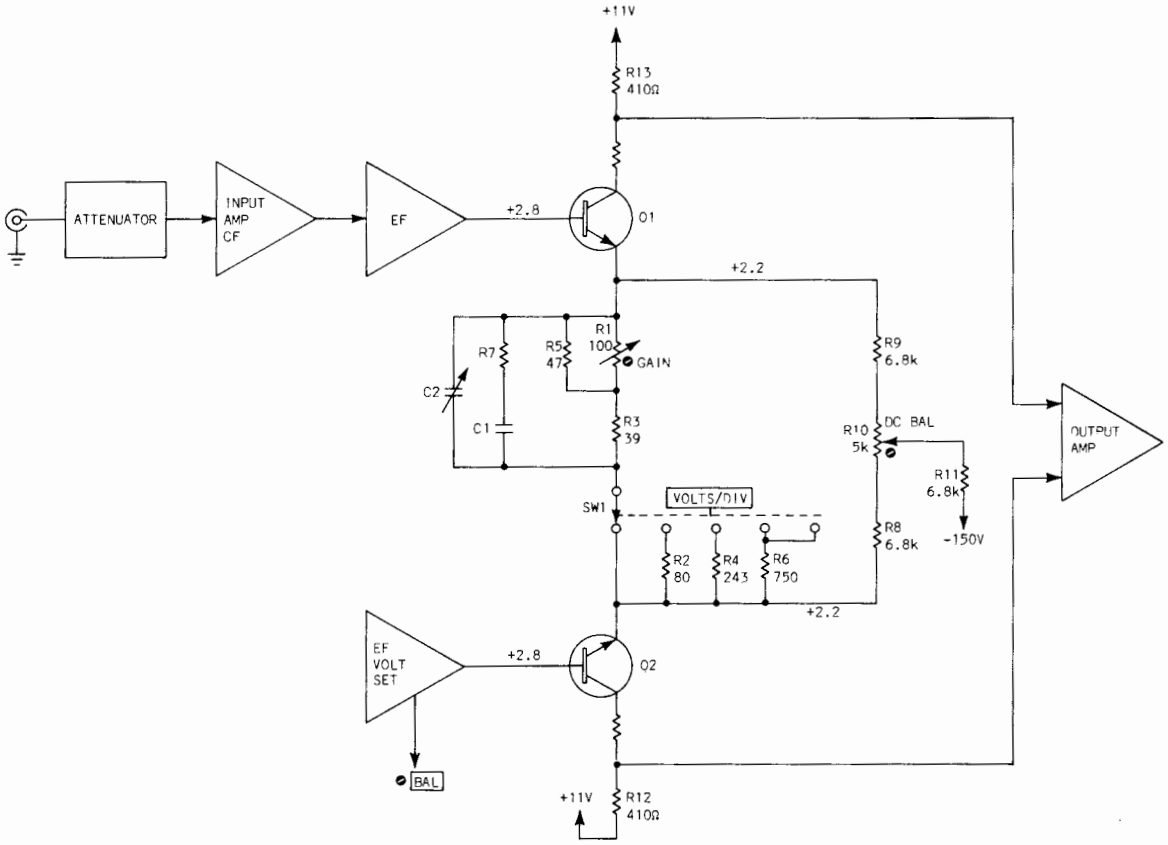


Fig. 6-59. Preamplifier switched gain phase inverter.

flow around external R_i components. R_i consists of R_{t1}, R_{t2} and either R2-R4 or R6-R8. Voltage gain of 16 approximates the circuit as shown. Switching in R6-R8 drops gain by half. Adjusting R4 and R8 calibrates gain. SW1 is an extension of the input attenuator, controlled by the VOLTS/DIV selector.

Placing position control circuitry in the collector circuit isolates positioning changes from gain and balance determinates.

Cathode followers present higher output impedance than emitter followers. Further the common terminal of a grounded-base amplifier should be operated as near signal ground as possible. Fig. 6-59 shows the preferred emitter-follower drive. Equal low impedances drive both Q1 and Q2. A very low resistance reflects into the emitters to add to R_i. The longtailing network R8, R9, R10 and R11 provides a form of coarse balance adjustment. C2, C1 and R7 emitter peak. R_i consists of R_{t1}, R_{t2}, R1, R3 and the resistance selected via SW1.

deflection factor

SW1, an extension of the input attenuator switch, allows a step-selectable calibrated gain. Output deflection factor remains constant at 50 mV/DIV (push-pull). Input deflection factor is selected at the front panel:

5 mV/DIV, as drawn;

10 mV/DIV when R2 selected;

20 mV/DIV when R4 selected;

50 mV/DIV when R6 selected.

R6 remains in the circuit for all settings above 50 mV/DIV. The input attenuator sets the deflection factor for these higher settings.

positioning

Added components, such as POSITION controls, add capacitance. These controls then should appear in low-impedance circuit points to prevent risetime degradation. This, however, is not so simple in emitter-coupled phase inverters. The low-impedance point, in the basic phase inverter, occurs in the emitter circuit. Placing position controls here creates an amplifier imbalance. Thus positional circuitry usually becomes part of the collector, plate or drain load, particularly when there is a need to minimize the number of active and passive

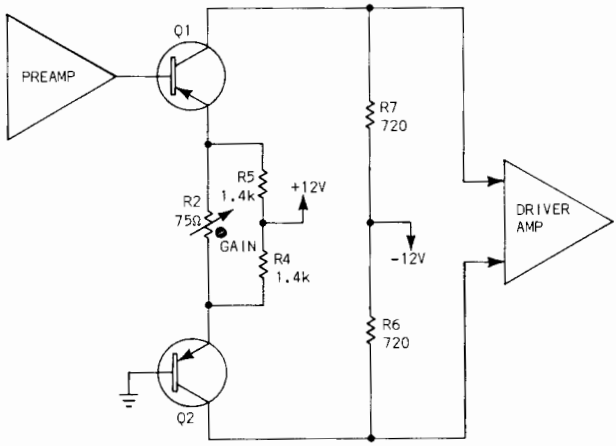


Fig. 6-60. Simple phase inverter.

devices. Lifting restrictions upon component quantity allows placement of positional circuitry in the emitter-coupling network.

To develop this, begin with the simple phase inverter shown in Fig. 6-60: R4 and R5 longtail, R2 is R_i and R6 plus R7 R_o. R4 and R5 match, so that gain calibration affects no vertical trace displacement. Modifying this basic circuit can provide the POSITION control and the VARIABLE. The modification removes R4 and R5, adds feedback to the base of Q2, but retains R2, R6 and R7.

Fig. 6-61 shows the modification. A dynamic longtail replaces R4 and R5 consisting of Q4, Q5, R8, R9 and the POSITION control network. The longtail circuit determines total emitter current for Q1 and Q2.

Moving the POSITION control routes a different quantity of current through Q1 than through Q2. Differing collector levels which result appear to following circuits as positional signals.

Feedback to the base of Q2 precludes longtail current flowing through R2. The feedback creates a current demand, within Q2, precisely equal to the current supplied by Q4. No DC current flows through R2.

Longtailing is extensive enough that the emitter coupling resistance may be considerably increased without creating additional position signals. Thus SW1 and the VARIABLE also appear in the emitter circuit. R_i changes are independent of positional voltages even though both appear in the emitter circuit.

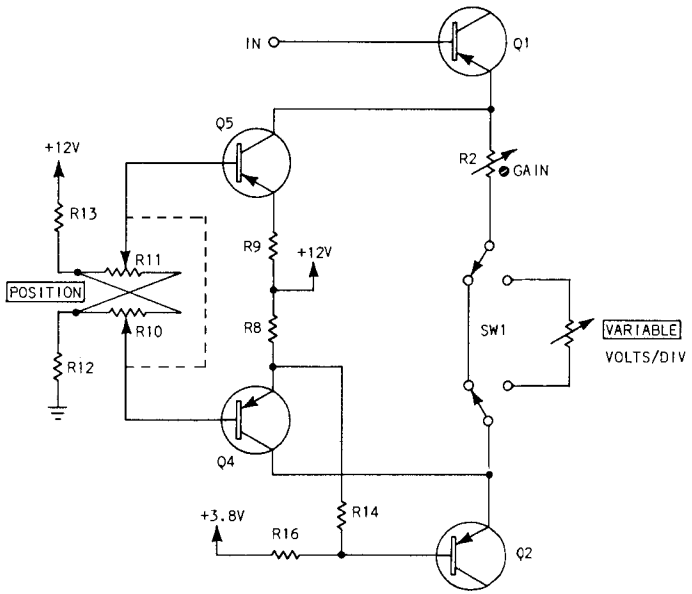


Fig. 6-61. Position and variable added to the simple phase inverter.

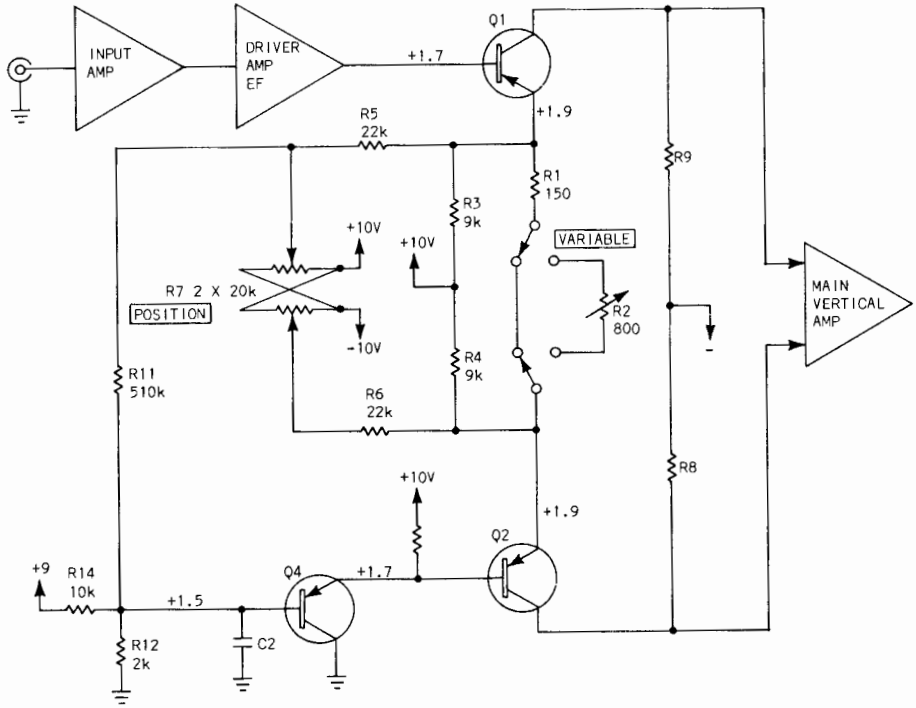


Fig. 6-62. Phase inverting preamplifier output amplifier.

This concept appears in other configurations. Fig. 6-62 is an example which conserves current in the longtail. Single-ended signals to this output amplifier cause signal current flow through R1 or R2. The resultant signal current develops push-pull voltage across R8 and R9.

Proportioning longtail current causes positional output voltage to develop. However, positioning current must not develop voltage differences across R_i. Feedback maintains Q1 and Q2, no signal, emitter voltages equal.

R3, R4, R5, R6 and R7 longtail the circuit. Moving R7 changes the quantity of longtail current available to Q1 and Q2. Centering R7 causes an equivalent longtail of 6.8 kΩ, returned to +7.5 volts, for each transistor. Both devices draw about 0.8 mA emitter current. Moving the wiper of R7 off-center changes equivalent longtail resistance little. Changes in the emitter return voltage cause position current flow. Assume R7 set to one extreme: One emitter draws current from an equivalent resistance of 7 kΩ returned to +10 volts. The other draws from an equivalent 7 kΩ returned to +3 volts. Emitter currents of more than 1 mA and less than 0.15 mA result. This develops output positional voltages. It also develops unequal emitter voltages.

Feedback equalizes Q1 and Q2 emitter voltage differences resulting from position control movement. The feedback network consists of R11, R12 and Q4. 4 mV of each volt change, at the R5-R7 connection, develops across R12. Q4 couples the voltage across R12 to the base of Q2. Since this voltage equals, in amplitude and phase, Q1 emitter voltage change, no voltage difference develops across R1 or R2.

Q4 is necessary to match base impedances. Emitter followers drive both Q1 and Q2 to minimize base impedance. R12 and R14 set the quiescent base voltage for Q2 via Q4. C2 decouples all but slow changes thus holding the base of Q2 at apparent ground.

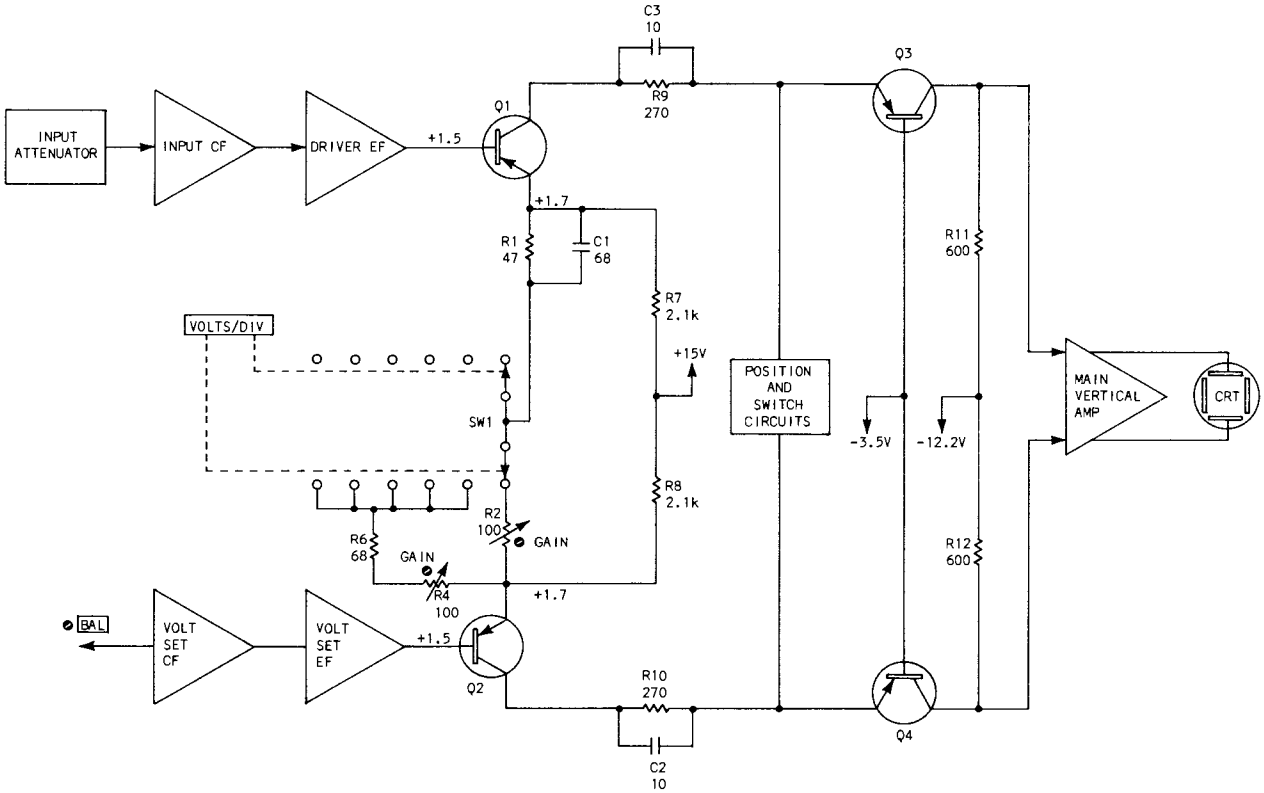


Fig. 6-63. Preamplifier output amplifier.

Moving the POSITION control causes a gain imbalance. Positional inputs cause one transistor to draw more current than the other. This changes R_t of one more than the other ($R_t = R_r + r_e$ and $r_e = 26/I_e$mA). Gain will not be symmetrical.

All phase inverters suffer the imbalance to some degree, since the input signal develops at one input while the other remains at signal ground. Fortunately, each following stage of push-pull amplification recognizes the imbalance as a common-mode signal. Each push-pull stage rejects common-mode signals to some degree, thereby improving signal symmetry.

cascode phase inverter

When one thinks of low-impedance circuit points he should keep in mind cascode amplifiers. The junction of the driving and driven devices represents apparent ground. Capacitance of added components at this junction increases risetime very little. Fig. 6-63 shows a cascoded phase inverter.

Signal currents generated by emitter-coupled drivers, Q1 and Q2, develop push-pull voltages in the collector circuits of driven grounded-base amplifiers, Q3 and Q4. R_i appears in the emitter circuit of Q1-Q2 and the collector load for Q3-Q4 is R_o.

A low impedance represents base circuitry for both Q1 and Q2. Q1 receives signal drive from a cathode follower via an emitter follower. Q2 receives balancing voltage from a cathode follower via an emitter follower. Low and approximately equal impedances reflect into the emitters of Q1 and Q2.

R1, R2 (with SW1 positioned as shown), R_{t1} and R_{t2} make up R_i. One calibrates gain by adjusting R2. R7 and R8 longtail the circuit. The adjustable base voltage of Q2 insures the quiescent current flows only in the longtail. Thus actuating SW1 changes R_i without developing positional voltages. C1 and R1 develop current (emitter) peaking. C3-R9 and C2-R10, in Q1 and Q2 collector circuits, temperature compensate.

Inputs to driven elements Q3 and Q4 present a low impedance. Negligible circuit loading results from adding circuits here. Signal pick-off, signal injection and/or switching networks are some

possibilities. For example: A preamplifier with multiple channels has identical circuitry up to and including the cascode drivers (such as Q1 and Q2). Switching circuits, at Q3 and Q4 emitters, determine which channel drives Q3 and Q4. Modern oscilloscopes use manual switching, gated switching or a combination of both.

hybrid cascode phase inverter

Phase inverters also appear in hybrid cascode configuration. Hybrid cascode amplifiers combine the advantages of vacuum-tube high-voltage capabilities and transistor low-impedance, high-gm characteristics.

Fig. 6-64 shows a transistor driver and a transistor-tube driven amplifier. V1 and V2 reduce V_{CC} to a reasonable level. Q3 and Q4 act as impedance transformers, reducing the driver-driven junction to a very low impedance.

Single-ended signals at the base of Q1 develop across R_i. R1, R_{t1} and R_{t2} define R_i. Apparent ground appears at the base of Q2. The adjustable Q2 base voltage balances longtail currents, allowing VARIABLE control. Driver signal currents flow through grounded base amplifiers Q3 and Q4 and grounded grid amplifiers V1 and V2 to develop push-pull output voltages across R6 and R7. R6 and R7 are R_O. Adjusting R8 sets the output amplifier operating point.

Quiescent voltage drop across the transistors is about 6 volts and across the tubes about 55 volts. Consider just V1, Q3 and Q1: Self bias causes V1 cathode voltage to be a volt or so more positive than V1 grid voltage. The emitter of Q3 follows a few tenths of a volt below its base. Collector to emitter, Q3 drops about 6 volts. Q1 collector and Q3 emitter are common. Base voltage of Q1 establishes Q1 emitter voltage. The emitter-to-collector potential, therefore, approximates 6 volts.

Grounded-base amplifier input impedance is many times less than grounded-grid amplifier input impedance. Placing Q3 and Q4 in the circuit reduces the junction impedance of the driver and driven amplifiers to apparent ground. Negligible circuit loading results from adding switching or control circuits at point "S."

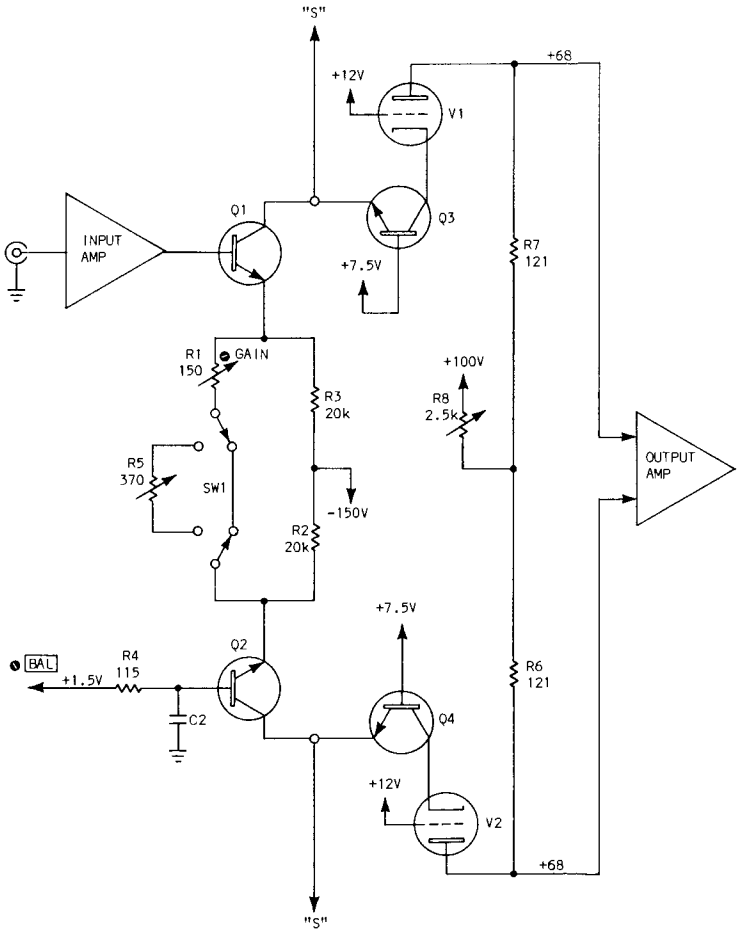


Fig. 6-64. Hybrid cascode phase inverter.

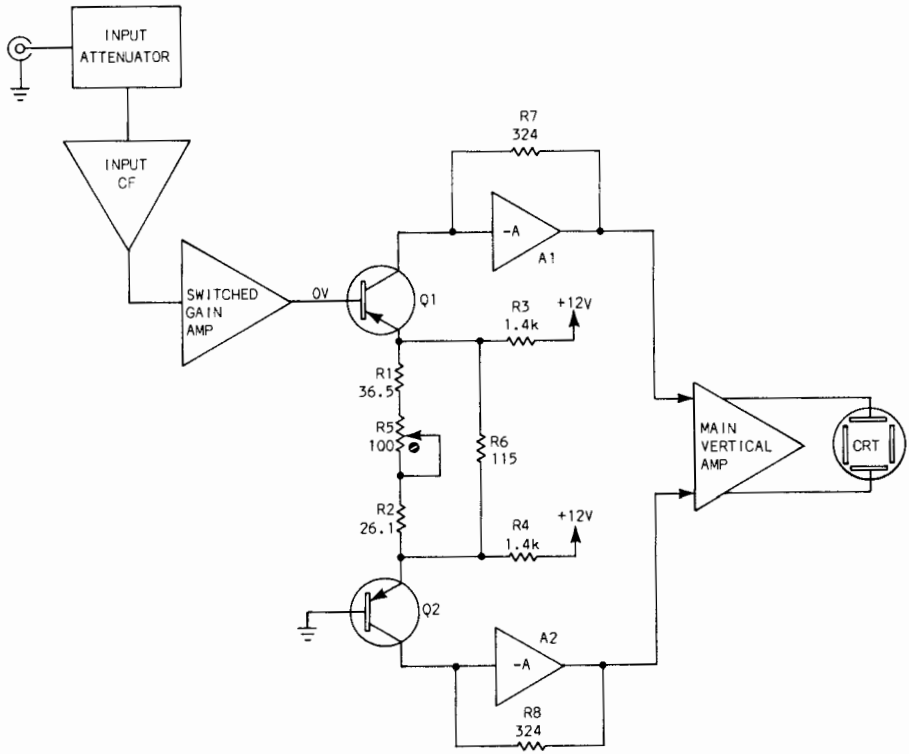


Fig. 6-65. Phase inverter drive to a feedback amplifier.

fedback amplifiers

Substituting fedback amplifiers for grounded-base amplifiers gives the effect of cascoding. The input to a fedback amplifier represents virtual ground. As with cascode amplifiers, this low-impedance point provides a convenient spot to add switching circuits.

Fig. 6-65 shows a transistor pair driving fedback amplifiers A1 and A2. The by-now-familiar method locates R_i in the emitter circuits of Q1 and Q2. R_O is not so obvious.

Very slight voltage changes occur at the inputs of fedback amplifiers. Gain expressed in terms of voltage becomes meaningless. However, all signal currents *appear* to flow in feedback resistors. A meaningful voltage measurement at A1 and A2 outputs expresses voltage gain. The ratio R7 + R8/R_i expresses voltage gain from the base of Q1 to the outputs of A1 and A2. For voltage gain considerations assume the sum of R7 and R8 equals R_O.

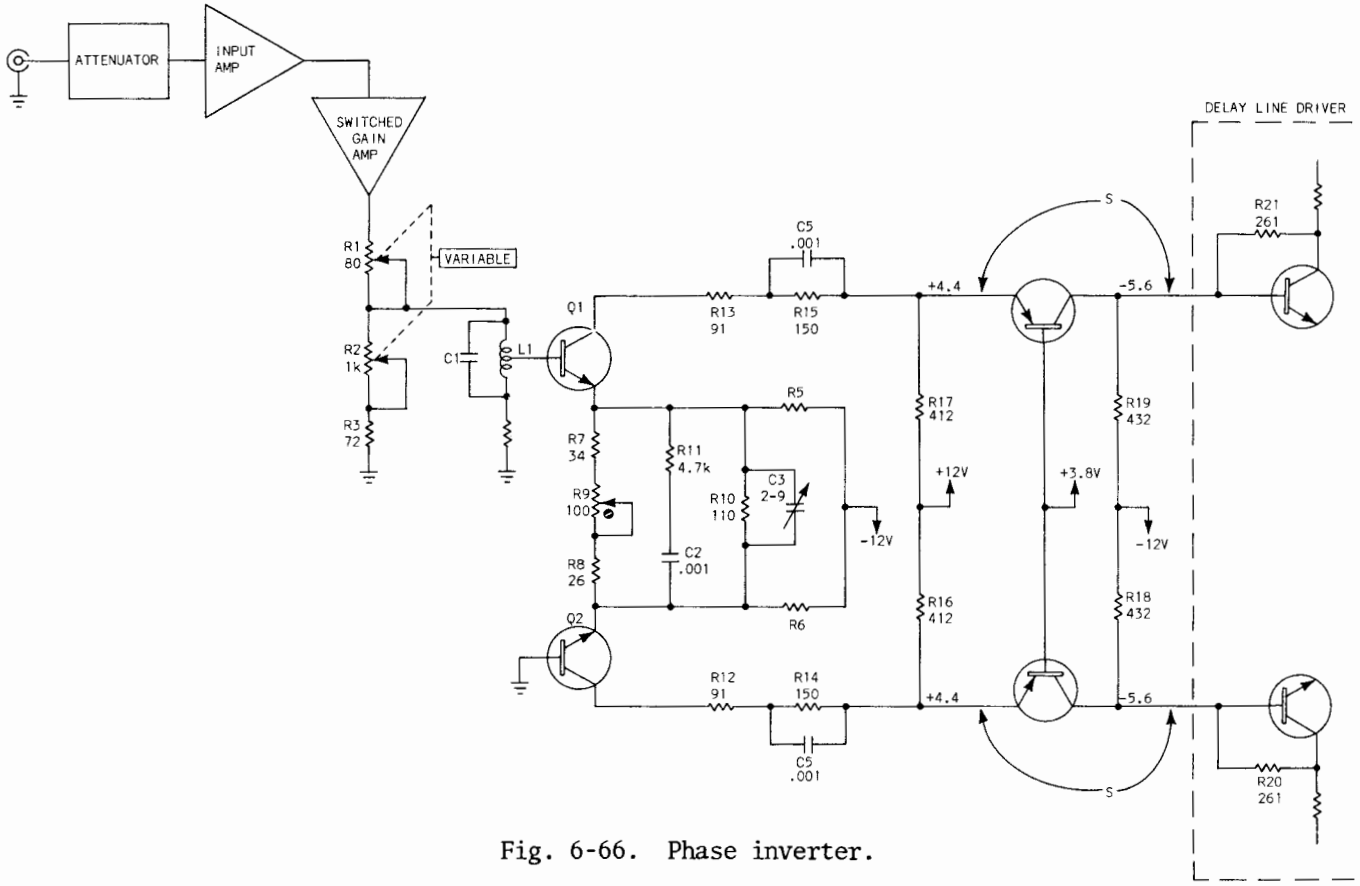


Fig. 6-66. Phase inverter.

Extending the cascode by driving the fedback amplifier with a common-base amplifier adds complexity but doesn't change the basic concept. See Fig. 6-66. This cascoded phase inverter drives a fedback amplifier. An NPN driving a PNP in cascode allows the use of relatively low-voltage power supplies. Cascoding provides an *apparent* ground at the grounded-base amplifier emitters (isolated points for pick-off or switching). The phase inverter also has pick-off or switching points in the collector circuits. Because the phase inverter drives a fedback amplifier a *virtual* ground develops. Labeled S, arrows indicate the possible switching points. Front panel control VARIABLE and an internal gain adjustment appear as part of the phase inverter circuitry.

Q1 base circuit contains high-frequency and constant-source loading considerations. R1 and R2, connected as an L-pad attenuator present a constant load resistance to the switched gain amplifier. Only under a position-centered condition does zero volts appear across resistive network R1, R2 and R3. Therefore, actuating the VARIABLE with a (vertically) off-center trace positionally changes the display. Coupling input signals via a bridged T-coil improves bandwidth compared to RC coupling. L1, C1 and R4 constitute a bandwidth improvement approaching the theoretical factor, 2.74.

Emitter circuits of Q1 and Q2 contain longtailing, gain determination, and emitter-peaking networks. R5 and R6, returned to -12 volts, longtail the amplifier. Series resistance of R7, R8 and R9 paralleled by R10 determines R_{ℓ}. Emitter peaking results from R11-C2 and C3 shunting R_{ℓ}.

Q1 and Q2 collector circuits feature a regulated V_{CC}, temperature compensation and degenerative feedback. Q3 and Q4, PNP silicon devices, connected as common-base amplifiers, regulate V_{CC} for Q1 and Q2. A forward-biased, PNP, grounded-base amplifier maintains an emitter voltage one junction more positive than the base, in this case 0.6 volts above a fixed base potential.

R14 and R15 temperature compensate and C4 and C5 bypass high frequencies. Q1 and Q2 dissipate maximum power (EI) at quiescence due to the voltage drop across R14 and R15.

R13 increases Q1 input capacitance with collector current surges, enhancing the effectiveness of T-coil coupling. To realize maximum effectiveness of T-coil coupling, base reactance must decrease linearly with frequency. Emitter impedance reflects into the base. A current peaked emitter impedance (R11, C2, R10 and C3) decreases with frequency at a nonlinear rate. This nonlinear change causes a nonlinear voltage change across R13. Voltage developed across R13 determines base-to-collector capacitance. This change in capacitance, with emitter current, tends to make the input capacitance appear the same at all frequencies. A constant capacitance decreases impedance with frequency linearly.

R12 in the collector of Q2 provides balanced degeneration for equal push-pull signals.

R16, R17 and Q1-Q2 longtailing establishes Q3-Q4 operating point. Base return for Q3 and Q4 sets the voltage at the emitter end of R16 and R17. The voltage across R16 and R17 and the resistive value establishes total current demand. Longtail circuitry controls Q1 and Q2 current contribution. Q3 and Q4 must provide any additional current required for the proper voltage drop across R16 and R17.

R18 and R19 return Q3 and Q4 collectors to V_{CC}.

Consider that all signal currents generated in Q1 and Q2 emitter circuits flow in Q3 and Q4 collector circuits.

Fig. 6-66 includes R20 and R21 from the next amplifier stage to illustrate voltage gain. One can measure an input signal voltage to the phase inverter but at no other point can he measure meaningful signal voltages. The delay-line-driver collectors do provide a voltage measurement point, related to phase-inverter gain. All input signal current appears to flow in the feedback components of a fedback amplifier (with high open loop gain). Since all signal currents generated by the phase inverter appear to flow through R20 and R21, one may approximate voltage gain. $A_V = \frac{R_O}{R_i}$. One solves Q1-Q2 emitter coupling for R_i and designates the sum of R20 and R21, R_O.

differential amplifiers

The last member of this family of amplifiers carries the family name "differential." In block form there is no difference between this and the other members. Differential amplifiers, also called comparators and difference amplifiers, develop an output signal representing the difference between two input signals multiplied gain times.

Fig. 6-67 through 6-70 illustrate the three modes of differential amplification. Fig. 6-67 is push-pull and 6-68, paraphase. The voltage difference between input terminals appears across R_i as V_i. V_o is gain times V_i. Ratio R_o to R_i defines voltage gain. This is also true for Fig. 6-67 and 6-68. These latter figures, however, represent the differential or comparator mode.

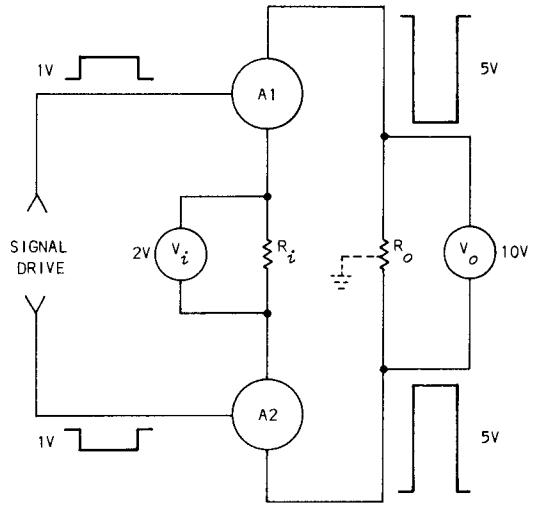


Fig. 6-67. Push-pull. The difference between input 1 and 2 appears across R_i as V_i.

$$V_o = A_V V_i. \quad A_V = \frac{R_o}{R_i}.$$

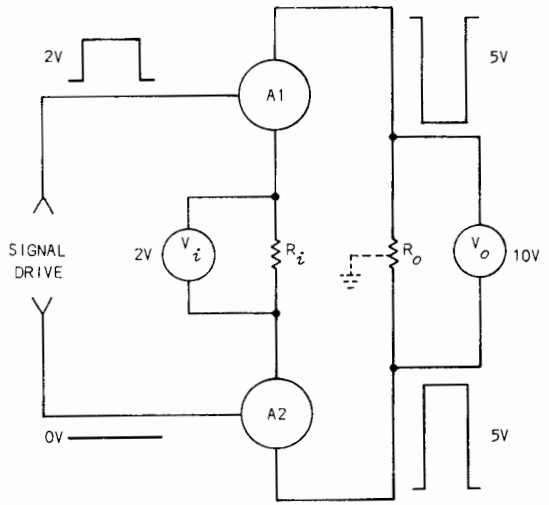


Fig. 6-68. Paraphase. The difference between input 1 and 2 is V_i. $V_o = V_i A_V$.

$$A_V = \frac{R_o}{R_i}.$$

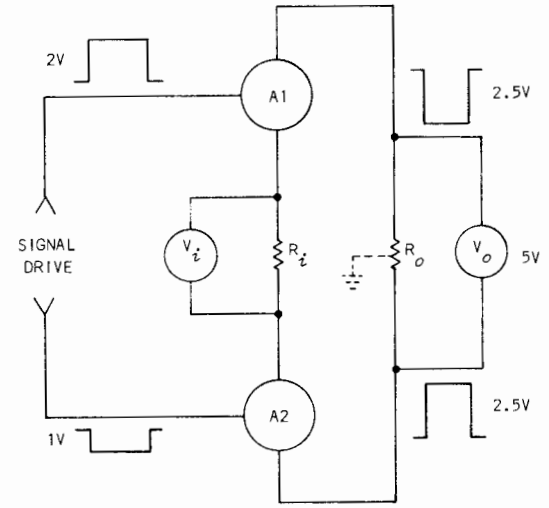


Fig. 6-69. Differential. The difference between input 1 and 2 is V_i. $V_o = V_i A_V$.

$$A_V = \frac{R_o}{R_i}.$$

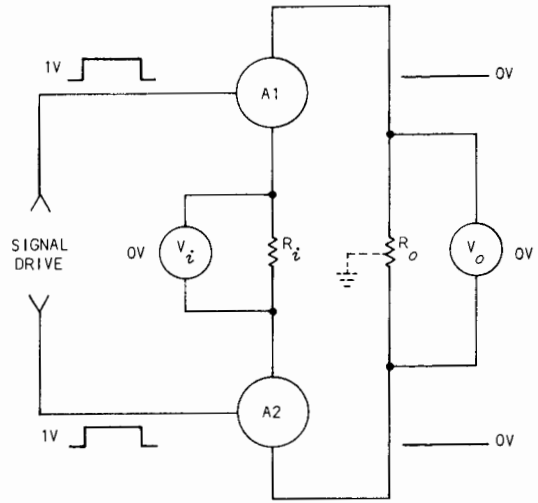


Fig. 6-70. Differential. V_i has zero value. Input 1 and 2 cancel. 0 volts across R_i generates no current to flow through R_o. $\frac{R_o}{R_i}$ still defines voltage gain, but V_o cannot exceed the product of A_V and V_i.

In Fig. 6-70 the input signals arrive simultaneously, equal in amplitude and phase coherent. Theoretically, V_O remains constant with an infinite common-mode voltage input. Practically, limits exist. Unequal signal delay or attenuation from signal source to amplifier input terminals impose limitations, outside the amplifier. From the input terminals each differential amplifier has a common-mode-rejection limit.

common-mode rejection-ratio

The term common-mode rejection-ratio, expresses the merit of a differential amplifier. Abbreviated CMRR, this ratio reveals to what extent common-mode input signals develop an output voltage. A CMRR of 1000:1 states that 1000 units of input common-mode signal develop one unit of output common-mode signal.

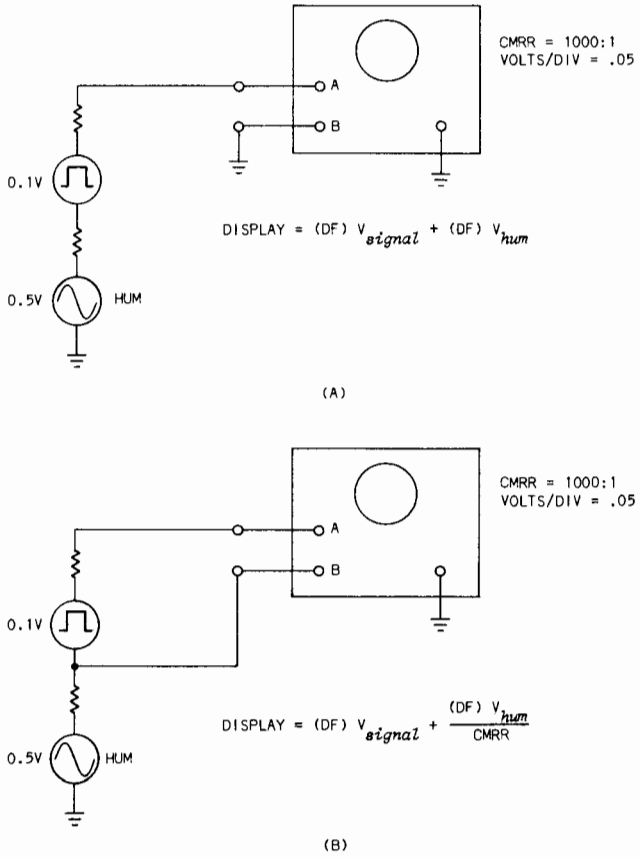


Fig. 6-71. Using the differential mode to reduce noise.

Fig. 6-71 shows a measurement problem: The operator wishes to observe the output of a signal source and connects his scope to the source in conventional form (A). However, a common-mode signal is present, possibly induced in a ground loop by the power line. These signals add. The desired signal represents 2 divisions, at the input terminal, while hum voltage, 5 times larger, is 10 divisions. Measurement of the desired source is difficult if not impossible.

(B) shows a solution using the differential scope mode. Signal voltage, develops across terminals A and B again as a 2-division input. Hum, however,

develops as 10 divisions of common-mode signal, appearing in-phase at A and B. CMRR states the attenuation of the common-mode signal. Due to the CMRR, hum in Fig. 6-71 represents 0.01 divisions in the differential mode.

This explanation assumes equal-amplitude, phase-coherent hum voltages at A and B.

Generally, an amplifier current source approaching the theoretical current generator allows high CMRR. For instance, an infinitely high-impedance longtail, returned to an infinitely high supply voltage. Differential amplifier complexities reflect design attempts to approach an ideal current source, or to overcome CMRR degeneration resulting from unequal, amplifier, phase shift and amplification.

The circuit shown in Fig. 6-72 utilizes four triodes to develop single-ended difference signals. Either input A or input B, monitored alone, develops conventional output signals. Applying signals simultaneously, to A and B, result in differential or A-minus-B output to the driver amplifier.

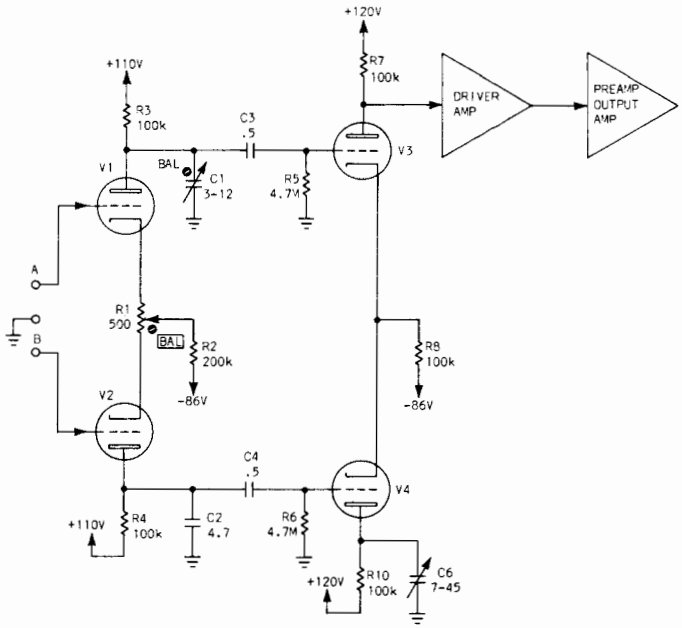


Fig. 6-72. Differential amplifier.

A signal appearing at one input terminal, with the other grounded, becomes phase split by V1 and V2. V3 and V4 act as push-pull amplifiers with only one output monitored. Voltages develop across R7 in-phase with input A. Signals applied to A, with B grounded, appear at the driver amplifier input as amplified reproductions of the input AC component. Grounding A and applying signals to B results in phase reversal. Signals developing across R7 realize voltage amplification and phase inversion from input B to the driver amplifier input. V4 balances the circuit.

balancing

Successful differential action requires dynamic balance to achieve high CMRR. R2 longtails V1 and V2. R1 dynamically balances V1 and V2 gain. Adjusting R1 might unbalance quiescent plate levels, but coupling capacitors nullify the effects of DC. C1 and C2 introduce high-frequency degeneration. However, placing these components in the circuit provides empirical phase balance.

V3 and V4, connected push-pull, aid balancing, thus CMRR, and improve response:

1. Input C to V3 and V4 closely match.
2. Push-pull amplifiers inherently attenuate common-mode signals. $R8/R_{\ell}$ approximates V3 and V4 CMRR.
3. Push-pull currents, through longtail R8, cause the common-cathode end of R8 to appear virtual ground. To achieve the longtailing effect of R8, single-ended amplification requires doubling the resistive value of R8. Additionally, the bypass capacitance required to approach the push-pull response is awkward.
4. C6 affects cathode balance. The plate impedance of a triode reflects into the cathode approximately $1/\mu$ times. One adjusts C6 for optimum rejection while monitoring a train of pules or high frequency sinewaves (common mode).

This circuit accepts small AC signals with fair CMRR. Common-mode rejection results from longtailing and extensive balancing. Push-pull configuration of V3 and V4 aid balance.

The single-ended output is not necessary or even common. Most designs use the push-pull form as shown in Fig. 6-73. V1 and V2 capacitively couple differential outputs to the push-pull driver amplifier. R2 longtails this circuit. R1 allows adjustment for best low-frequency CMRR. C1 and C2 shunt the output load impedance and, adjustable, provide high-frequency balance for optimum CMRR.

Small signal handling capability and only fair CMRR, of Figs. 6-72 and 6-73, results from circuit simplicity. Balancing and isolation circuitry between input jacks and input amplifiers aids CMRR improvement. More solidly anchoring active device dynamic parameters increases signal handling capabilities.

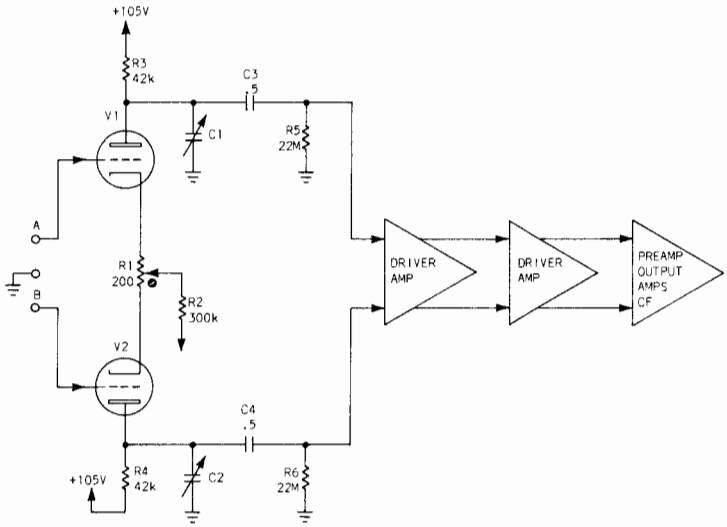


Fig. 6-73. Utilizing push-pull outputs.

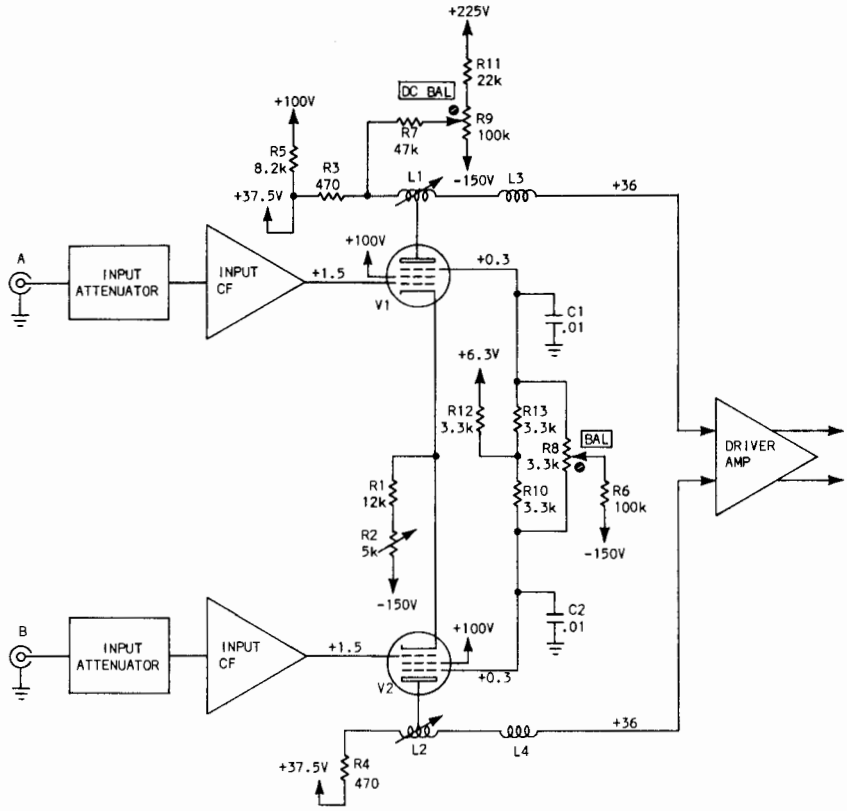


Fig. 6-74. CMRR improvement.

CMRR improvement

See Fig. 6-74. Input attenuators and cathode followers isolate V1 and V2 from input loading. Careful balance of input amplifier circuitry improves CMRR. The input attenuators reduce input signal voltages to a reasonable level and cathode-follower isolation improves response. Differential amplifiers V1 and V2 show improved amplitude and frequency signal handling.

R1 and R2 longtail V1 and V2. Adjusting R2 sets gain by controlling quiescent tube current, thus *gm*. Screen grids return to a regulated, low-impedance voltage supply. Resistive network R6, R8, R10, R12 and R13 set suppressor-grid voltage. Adjusting R8 balances V1 and V2 *gm*. C1 and C2 decouple, preventing signal degeneration at the suppressor.

Returning screen grids and suppressor grids to a fixed supply maintains η (plate efficiency) constant. Since pentodes suffer slight plate loading effects, V1 and V2 maintain fairly constant dynamic parameters. The circuit may then compare large amplitude signal voltages keeping CMRR high.

High-frequency design considerations include three major items: Low output impedance of cathode followers, low-input capacitance of longtailed pentodes and combination peaked T-coil plate loads. T-coil loading for V1 consists of L1, L3, R3 and distributed capacitance; and for V2: L2, L4, R4 and distributed capacitance. R_O appears a constant resistive load to all frequencies, within design limitations, equal to R3 and R4.

DC balance control, R9, is set for optimum DC CMRR. This is a direct-coupled system. Low-frequency response extends to DC. Voltage divider R5, R3, R7, R9 and R11, restrict voltage changes, resulting from adjusting R9, to a few volts and shunts terminator R3 little.

Differential amplifiers of this type handle 2 volts signal amplitude at each grid. Frequency response, for good CMRR, extends from DC to several megahertz.

Three factors restrict the total effectiveness of this differential amplifier.

1. Longtailing: The perfect longtail maintains a constant current no matter the input voltage. R1 and R2 approximate this condition as long as input voltage remains a small percentage of the -150 V return. An appreciable current change through R1 and R2 changes dynamic parameters of V1 and V2.
2. Triode action, screen grid-to-cathode: Suppressor voltage controls η only with constant screen-to-cathode μ. V1 and V2 screen grids return to a fixed supply. Large cathode voltage swings change cathode to screen μ. This dynamic parameter varies from one active device to another. Adding a varying μ to a changing longtail current degenerates CMRR at all frequencies.
3. Unequal terminator loading: Though slight, loading of R3, by resistive network R5-R7-R9-R11, exists. Unequal output loading causes unbalanced voltage gain and phase shift which is most noticeable at high frequencies.

In Fig. 6-75, V1 and V2 accept input voltages of about ±100 V before common-mode current flows in the plate load. Longtailing approaches a theoretical current generator; screen grid-to-cathode voltage remains constant; and plate line terminators approximate a match.

V4 and Q1 longtail, appearing as an extremely high impedance. Total circuit current generates in Q1 emitter circuit. Base voltage, emitter return voltage and emitter resistance set total current quantity. Current flow remains constant until collector voltage changes cause parameter shifts in Q1. Triode V4 reflects plate voltage changes to Q1 collector. These changes, reduced by μ of V4, must reach large amplitudes to measurably affect longtail current: If V4 μ = 20, and voltage change = 40 V, collector voltage change ≈ 2 volts. Further, little current change results from Δ2 collector volts.

Adjusting R6 controls gain by controlling current or *gm*.

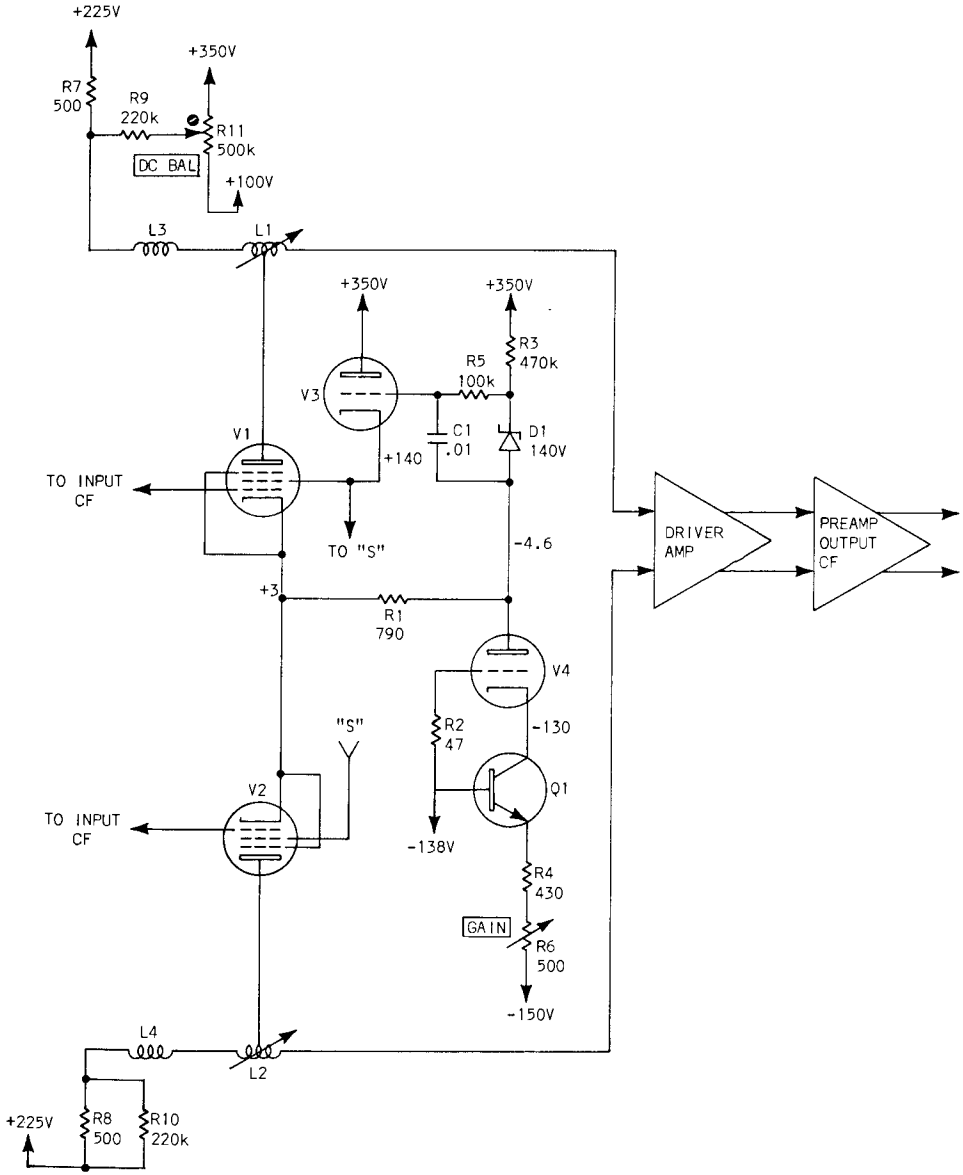


Fig. 6-75. Extending the longtail and controlling screen-grid μ.

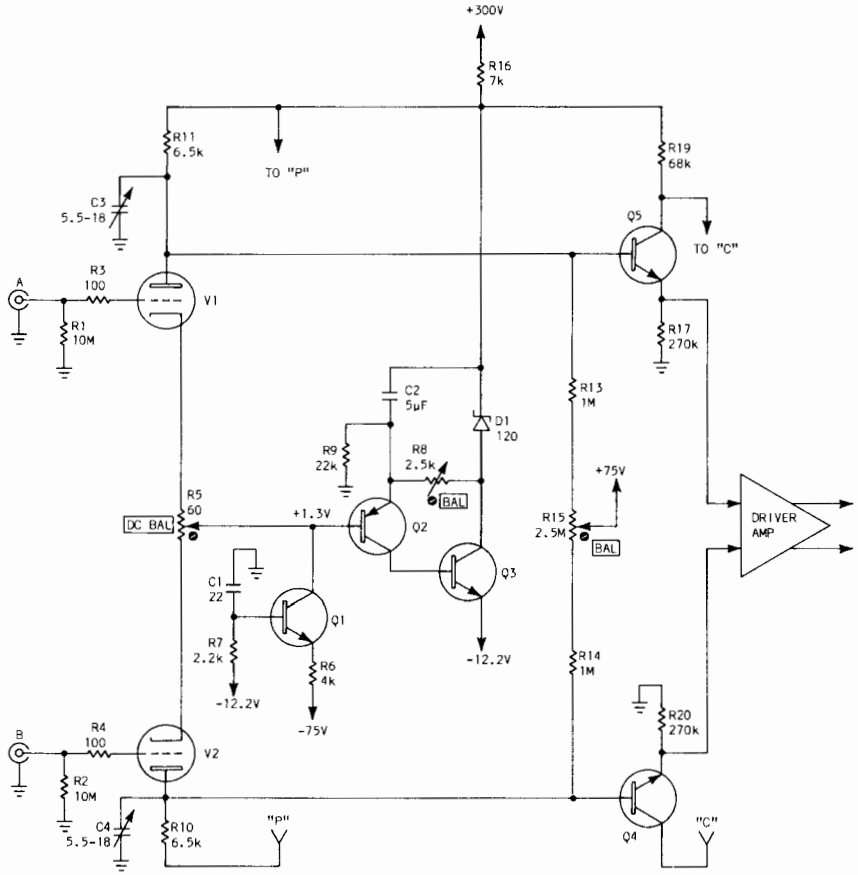


Fig. 6-76. Plate voltage feedback maintains μ constant.

Cathode follower V3 holds screen grid-to-cathode voltage constant. Cathode voltage changes (common-mode) develop at the plate of V4. D1, through R3, offsets this voltage 140 volts. R5-C1 decouple silicon spikes associated with the zener diode. V3 and associated circuitry couples cathode signals to the screen, elevated 140 volts. Ergo, screen μ remains constant during application of common-mode voltages.

Shunts appear across both plate line terminators. R9 plus some portion of R11 parallels R7. R10 shunts R8. Terminations closely, though not precisely, match.

Nuvistors save space. Since one can control triode μ, as the cathode-to-screen of Fig. 6-75, he should be able to incorporate nuvistors. This is one circuit function shown in Fig. 6-76.

V1 and V2 are input amplifiers. Q1 longtails the circuit. Q2 and Q3 make up a noninverting, unity-gain amplifier. This amplifier couples common-mode cathode signals, which develop across the longtail, to the common positive return. Emitter followers Q4 and Q5 illustrate the complete current demand through R16. Adjustments R5, R15, C3 and C4 provide empirical balancing for DC through high-frequency signals.

V1 and V2 μ remains constant even though large common-mode input signals appear. Q1 sets total tube current. Common-mode signal voltages appear at the wiper of R5. Amplifiers Q2 and Q3 cause E_{BB} for V1 and V2 and V_{CC} for Q4 and Q5 to change with common-mode voltages. $E_{BB}(V_{CC})$ changes equal, in amplitude and phase, common-mode signals keeping plate-to-cathode voltage constant. Constant I_p and constant E_p insure constant μ.

Q3 collector current makes up most of the total current drawn by Q2 and Q3. Common-mode signals develop at the base of Q2. Q2 emitter attempts to follow the base signals. However, collector current cannot exceed base current of Q3. Changing Q3 base current changes Q3 collector current. Q3 generates sufficient collector current to drop the required voltage across R9. The drop across R9 represents Q2 base voltage -- Q2 base-emitter null.

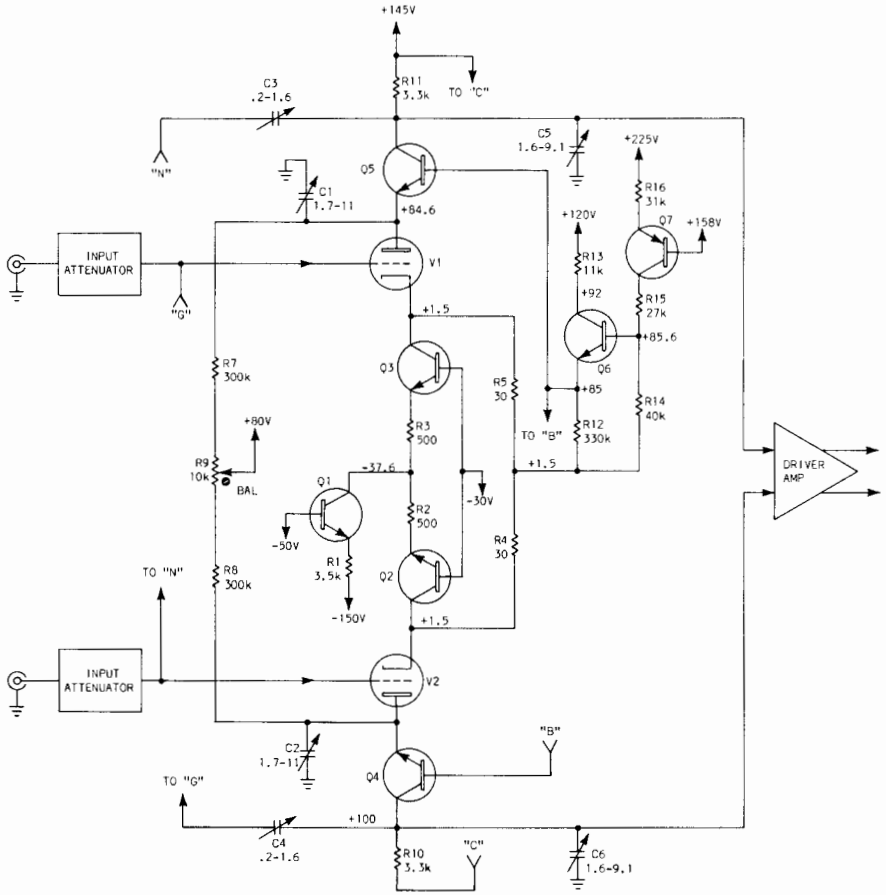


Fig. 6-77. Adding more extensive longtailing and neutralization capacitors.

Theoretically, shorting R8 develops unity gain from the base of Q2 to the collector of Q3. 100% of Q3 collector signal fails in this case to develop across R16. D1, a part of the output load, drops a percentage of signal voltages (about 5%). One then adjusts R8 for unity gain across R16, referred to the amplifier input terminals. C2 bypasses D1 generated spikes.

Fig. 6-76 includes the following balancing controls:

R5, quiescent balance

C3-C4, high-frequency balance.

R15, mid-frequency balance.

Dynamic longtailing restricts common-mode voltage amplitudes the amplifier accepts before CMRR deteriorates. CMRR deterioration initiates when Q1 collector voltage change causes significant Q1 collector current change.

extending longtailing

A hybrid longtail series in an earlier circuit extended longtailing voltage range. Series transistors accomplish the same objective.

Fig. 6-77 includes three active devices, Q1, Q2 and Q3, which extend longtail dynamic voltage range. Cascoding allows input amplifiers, V1 and V2, to work into a low-impedance plate load, isolated from output voltage swings. V1 and V2 plate-to-cathode voltage remains constant due to feedback from regulator Q6-Q7 to the bases of Q4 and Q5.

Longtail Q1, isolated by Q2 and Q3, generates a constant current. Q1 base voltage, resistive value of R1, and emitter return voltage define total circuit current available. Q2 and Q3 create equal longtail current demands and attenuate cathode voltage changes which develop at the collector of Q1.

Differential signal voltages across r_{k1}, R4, R5 and r_{k2} generate signal currents. These currents flow through V1-Q5 and V2-Q4, developing output signal voltages across R10 and R11. Grounded-base amplifiers Q4 and Q5 act as regulators, holding V1 and V2 plate voltage constant. Resistive network R7, R8 and R9, injects additional current into Q4 and Q5 emitters. Adjusting R9 proportions the current to set quiescent collector levels.

Adjusting capacitances balances response and neutralizes. Although phase shift and risetime are important to the design, most important to proper comparator action is balanced response. When the response is balanced, common-mode components that develop are further attenuated, or rejected, by each following push-pull stage, including the CRT.

C3 and C4 neutralize. Neutralization of this type is necessary when the input amplifier is a differential. Differential amplifiers are generally longtailed and tightly coupled. This prevents constant grid-to-cathode gain. Attenuator load capacitance varies, preventing stable voltage divider compensation. C3 and C4 add dynamic capacitance to the attenuator output. The capacitive variations are inverse to control-grid capacitive variations. Thus capacitance across the attenuator output remains constant. One adjusts C3 and C4 as part of each input attenuator compensation.

Fedback voltages to V1 and V2 plates maintain μ constant during common-mode signal duration. Junction R4-R5 voltage develops as mean differential cathode voltage. Junction voltage changes, volt for volt, with common-mode signals. Voltage across R14 remains constant; thus, common-mode changes appear at the base of Q6, emitter of Q6, base of Q5 and Q4, and plates of V1 and V2. Constant plate current plus constant plate voltage results in constant μ.

During this common-mode feedback, Q4 and Q5 act as emitter followers. High-frequency emitter follower gain depends upon V1 and V2 plate capacitance. Balancing plate capacitance, by adjusting C1 and C2, therefore extends the bandwidth of the common-mode feedback.

input followers

Fig. 6-77 functions as an input amplifier, and, due to cascoding, functions very well. Many times input amplifiers precede the differential stage. These amplifiers take the form of cathode or source followers. Isolating the input and differential amplifier with a follower improves frequency response, balance and large-signal capabilities.

Input followers for differential amplifiers range from straight-forward cathode followers to complex circuitry. Circuit complexities result from attempts to increase large signal capabilities and extensive balancing, improving, system common-mode-rejection-ratio.

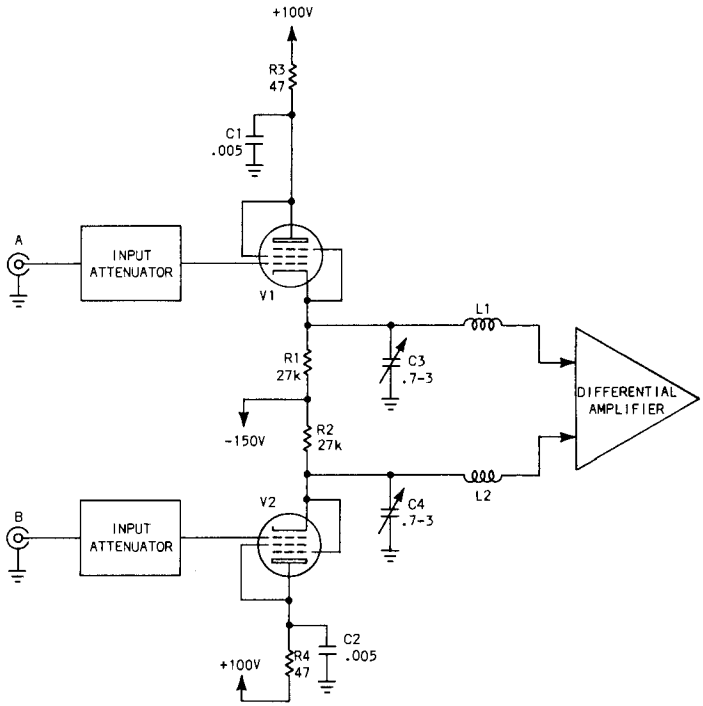


Fig. 6-78. Input amplifier for a differential preamplifier.

Fig. 6-78 is an example of the straight-forward configuration. Nothing "special" here. More complex circuitry extends the usefulness of differential amplifiers enough to justify the complexities.

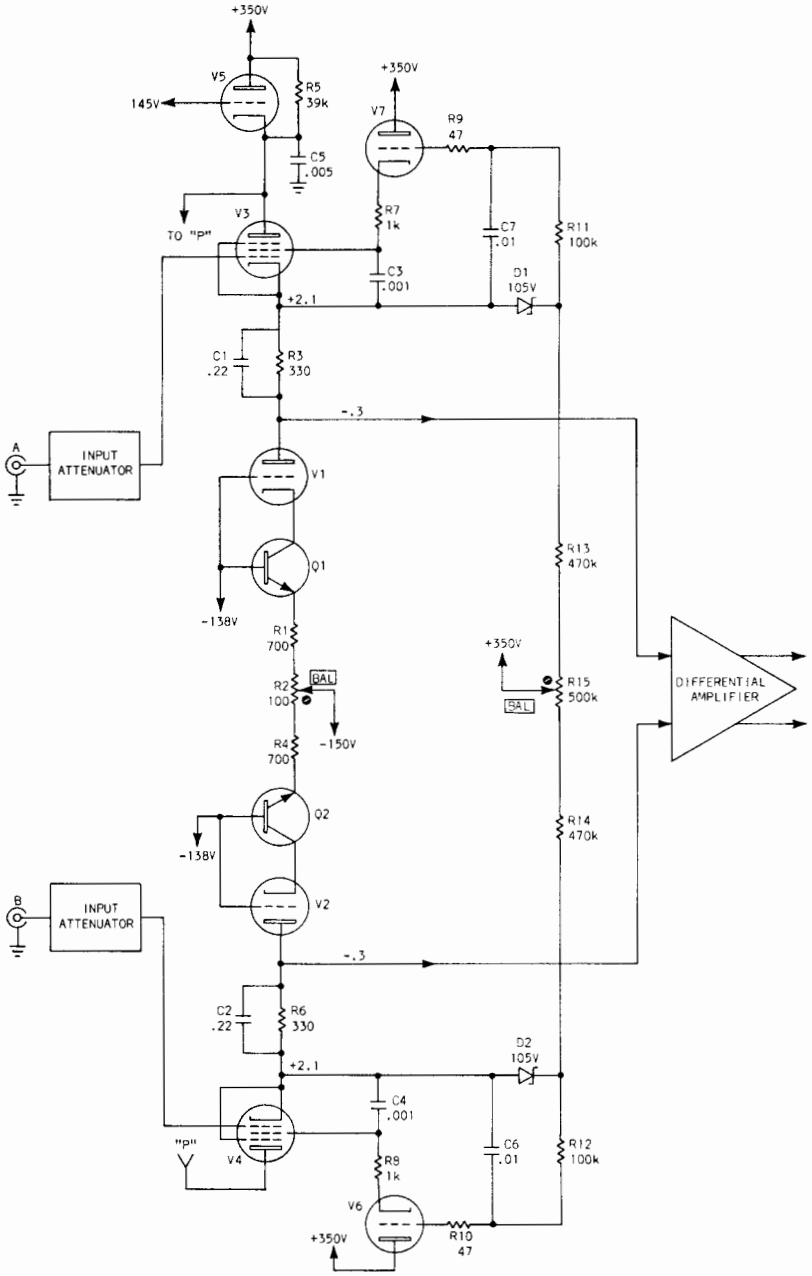


Fig. 6-79. Coupler input to a differential preamplifier.

See Fig. 6-79. Extensively longtailed, this circuit also features a low impedance, regulated, plate voltage supply and a constant, cathode-to-screen grid, μ.

Output signals develop at the plates of V1 and V2. Longtail circuit V1-Q1 and V2-Q2 present a very high signal impedance. For this reason gain approaches unity.

V5 acts as a low-impedance plate voltage source for both V3 and V4.

Cathode followers, V6 and V7, couple elevated cathode signals to input amplifier screen grids. These in-phase signals maintain μ, cathode-to-screen grid.

The long string of electron tubes, shown in Fig. 6-79, act as heat generators. Heat generated and physical size of electron tubes require a fairly large package volume plus a filament power source. An all-semiconductor amplifier solves the space, heat and additional power source problem. Transistors, though, present too low an input impedance for use as input amplifiers. However, the availability of practical field-effect transistors allows greater design freedom. FET input impedance equals or exceeds that of a pentode. Designers then can consider an all-semiconductor input amplifier.

source follower input amplifier

Fig. 6-80 shows source follower input amplifier circuits driving the differential amplifier stage. Q1 and Q2 dynamically longtail. Q3 and Q4 function as source followers. Emitter followers Q7 and Q8 reduce output impedance. Emitter followers Q5 and Q6 feed output voltages to Q3 and Q4 drains, maintaining a fixed drain-to-source potential. Devices D1, D2 and Q9 protect against semiconductor reverse breakdown.

This stage linearly amplifies ±5 volt signals at either gate. Considered at 1 millivolt per division deflection factor, the amplifier passes signals 5000 times its basic sensitivity. The amplifier distorts gate signal variations greater than, about, 6 volts. Proper input attenuator selection, however, allows one to monitor larger input signal variations.

Adjusting R5 proportions Q3-Q4 longtail current to balance transconductance, thus gain, thus input capacitance. R10 adjustments also affect gain but change self-bias to a greater degree than transconductance. One therefore sets R5 for step attenuator balance and R10 for DC balance.

Most of the signal voltage that appears at the source of Q3 and Q4 develops across R18 and R17*, allowing emitter followers Q5 and Q6 to set and maintain drain-to-source voltage. Holding voltage across the FET constant stabilizes dynamic parameters.

C11-R13, in the collector of Q7, and C12-R14, in the collector of Q8, slow collector voltage changes as part of the protective circuit action.

protective circuitry

Protective circuits create a nonlinear condition during either excessive positive or negative excursions. Gate excursions more positive than 6 volts or more negative than 42 volts initiate protective action.

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*Voltage dividers in this circuit require compensating capacitors. The writer omitted these capacitors to reduce component density of Fig. 6-80.

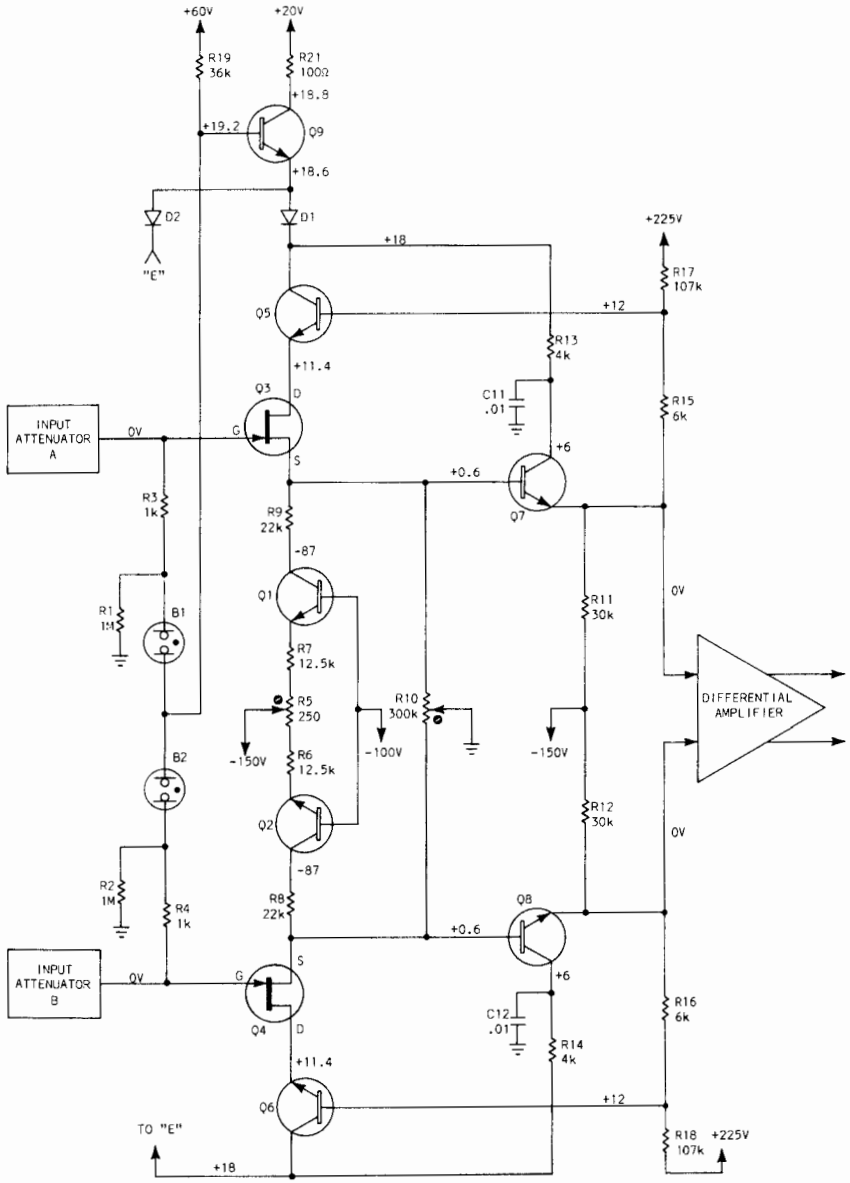


Fig. 6-80. Source follower input to a differential preamplifier.

To explain protective circuitry action, assume that gate of Q4 (channel "B") is grounded and signal voltage appears at the gate of Q3 (channel "A") only. 10 positive volts at the gate of Q3 actuates protective circuits which limit gate current. +10 V appears at the gate and source of Q3 and at the base and emitter of Q7. Collector-to-base junction of Q7 acts as a forward-biased diode.

C11 functions as a Q7 collector current source allowing the R15-R17 connection to rise toward +21 volts.

Collector-to-base junction of Q5 forward biases. Q5 collector, demanding reverse current through D1, causes D1 to turn off.

The forward-biased emitter-base junction of Q5 conducts. Q3 drain current flows through the junction, but supply impedance, R15 paralleled by R17, severely restricts drain current.

Only source current, longtail generated, less the small drain current flows in the source-gate junction of Q3.

Assume now that "B" remains grounded and -50 volts is applied to input "A". -50 volts at the gate of Q3 couples through the input amplifier. Emitter follower Q5 lowers Q3 drain voltage to a safe value. With no further circuit action, Q5 and Q7 collector-base potential exceeds reasonable values. B1 fires to initiate protective action.

Most of the gate voltage develops across R1. Junction B1-B2 returns to +19 volts at the base of Q9. Almost 70 volts then appears across B1. B1 fires. B1 drops a voltage across R19. Q9, as an emitter follower, lowers collector voltage of Q5 and Q7.

Q9 functions as V_{CC} source for "B" channel as well as "A" channel. The lowered V_{CC} also appears at Q6 and Q8 collectors. As Q6 and Q8 collector to base current starts to flow, D2 disconnects. Removing V_{CC} prevents collector-to-base reverse breakdown.

Input amplifiers covered so far separated neatly from the differential amplifiers as stages. One cannot always cleanly separate the two stages.

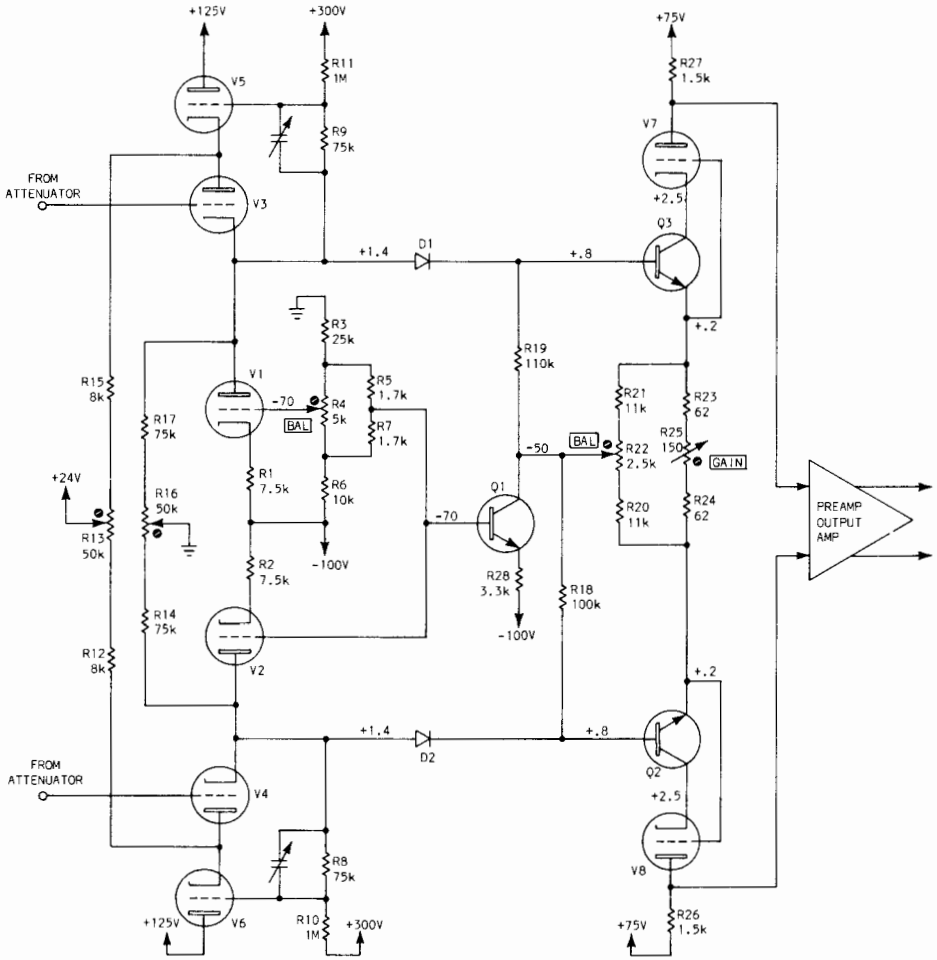


Fig. 6-81. Input and differential amplifier stage.

Fig. 6-81 is a case in point. The cathode follower pair drives a hybrid, cascoded, differential amplifier. The differential amplifier longtailing references to input amplifier longtailing. Differential longtail also provides "keep-alive" current for coupling diodes, D1 and D2.

V1 and V2 longtail the input cathode followers, V3 and V4. Adjusting R4 controls V4 conductivity, matching V3 cathode DC level to V4. Cathode followers, V5 and V6, couple elevated signals to the plates of V3 and V4.

Resistive networks R12-R13-R15 and R14-R16-R17 perform similar balance functions. Adjusting R13 proportions cathode follower gain of V5-V6, thus μ-balance of V3 and V4. Adjusting R16 balances the dynamic impedance at the bases of Q2 and Q3.

Coupling diodes D1 and D2 protect Q2 and Q3. Large difference signals cutoff either Q2 or Q3. The cutoff transistor might suffer base-emitter reverse breakdown. D1 or D2, as appropriate, opens, removing reverse breakdown base voltage.

Differential current flows through R20-R21-R22. One adjusts R22 for balanced currents through Q2 and Q3. therefore no quiescent current flows through R23-R24-R25. Gain adjustments then do not vertically deflect the CRT presentation.

Collector voltage for Q2 and Q3 equals operating bias for V7 and V8. This voltage remains constant over the operating range of the amplifier. Emitter changes couple to the collector via the cathode follower action of V7 and V8.

Hybrid cascoding allows a large voltage difference between input and output. It also provides excellent input-to-output isolation.

Balancing and isolation improve common-mode rejection. This amplifier accepts ±15 volts common-mode signals.

The magic of extensive balancing networks performs only for calibrated systems. A means of checking calibration for best CMRR maintains performance.

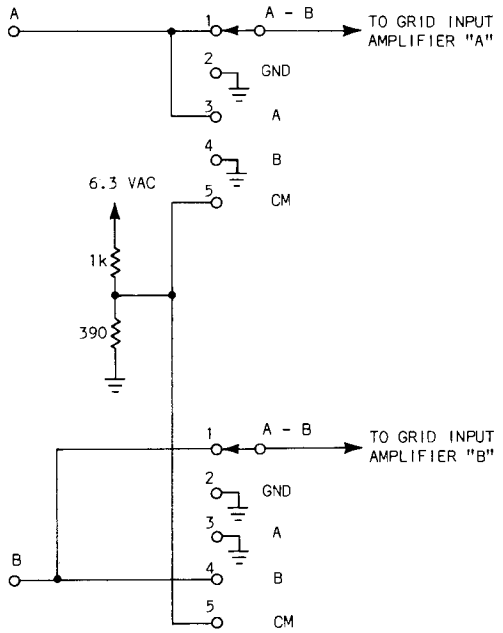


Fig. 6-82. Calibration check.

calibration check

See Fig. 6-82. Dual input selectors shown here route various inputs to amplifiers A and B:

1. A-B indicates differential drive.
2. Both inputs grounded.
3. Input A acts as a single-ended input. Input B grounded.
4. Input A grounded. Input B acts as a single-ended input.
5. 1.75 volts (RMS), in phase, signal drives both inputs. Selecting CM, an operator checks dynamic balance.

comparison voltage

A switch-selected comparison voltage extends the usefulness of a differential amplifier. Signal voltages one wishes to monitor frequently vary about a DC level. Low-frequency variations distort the least when direct coupled. If the variations are low amplitude, compared to the DC level, variations appear at the CRT as small

deflections. Use of a comparison voltage, with differential amplification, allows one to select a more convenient deflection factor.

Situation:

An operator wishes to observe 20 millivolts ripple on a 100-volt power supply. He needs to direct couple to observe all ripple frequency components.

Problem:

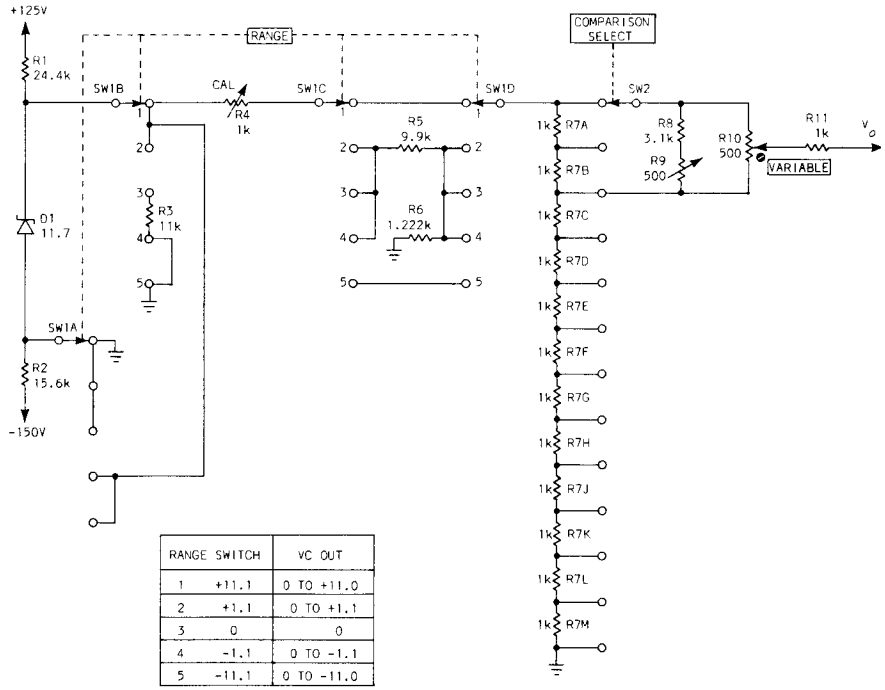
His instrument has 1 millivolt per division deflection factor and 8 divisions of CRT display area. Direct coupling requires attenuation by a factor of 10,000 to keep the trace within the CRT viewing area. Obviously, the 20 millivolt ripple attenuates to barely discernible.

Solution:

1. Monitor the power supply on channel "A". (An arbitrary choice; "B" would work as well.)
2. Select X10 attenuation. (10 millivolts per division.)
3. Inject 10 comparison volts into the "B" channel input amplifier.
4. The differential amplifier amplifies signal differences only.
5. Ripple voltages deflect 2 CRT divisions, a much more reasonable deflection range for observation.

Comparison voltage polarity must agree with monitored voltage. For maximum flexibility one includes switched comparison voltage polarity.

A calibrated variable comparison voltage makes the differential a precision null-seeking voltmeter.



RANGE SWITCH		VC OUT
1	+11.1	0 TO +11.0
2	+1.1	0 TO +1.1
3	0	0
4	-1.1	0 TO -1.1
5	-11.1	0 TO -11.0

Fig. 6-83. Differential comparison voltage.

The circuit of Fig. 6-83 develops comparison voltage in the ranges: 11 volts, 1.1 volts or 0 volts. It also provides within range, step selected, voltages and a between-step variable voltage. An operator switch selects polarity for any range but 0 volts.

RANGE selector, SW1, consists of four ganged switches. Comparison selector, SW2, is a double-pole switch.

Zener diode D1 drops 11.7 volts. Resistors R1 and R2 create a current demand to set the operating level for D1. Properly selected values of R1 and R2 set D1 at its most stable thermal operating point.

SW1A and SW1B select output polarity. Switch positions 1, 2 and 3 allow positive voltages to develop at the cathode of D1. SW1A holds D1 anode at ground. +11.7 volts develops at SW1B. Positions 1 and 2 of SW1B route this voltage to the load. Position 3 opens the load and substitutes R3 to maintain zener current constant.

Positions 4 and 5 of SW1 reverse polarity. SW1A returns the anode of D1 to R2, -150 volts and the load. SW1B holds D1 cathode at ground. SW1 applies 11.7 volts to R5 in all except position 3.

One adjusts R5, with SW1 in position 1 or 5, for exactly 11.0 volts across R7. SW1C now has a potential of +11.0 volts, -11.0 volts or 0 volts.

Five voltage conditions appear at SW1D: +11.0 volts, +1.1 volts, 0 volts, -1.1 volts or -11.0 volts. 11 volts develops across resistive network R7-R8-R9-R10, with SW1 positioned to 1 or 5. 1.1 volts develops across this network with SW1 positioned to 2 or 4. Position 3 of SW1 opens the return to D1, thus zero volts develop.

11.0 or 1.1 volts develop across 11 kΩ. Network R7-R8-R9-R10 has an equivalent of 11 kΩ resistance. R7 is a 12 kΩ resistor tapped at 1 kΩ intervals. Network R8, R9 and R10 calibrates to 2 kΩ. This network shunts two taps of R7. The total network then develops 11 kΩ resistance. Variable R10 provides the ability to vary the comparison voltage over a portion of the SW2 selected voltage.

Positioning SW1 and SW2, as shown, +11 volts develops across R7. Network R8, R9 and R10 shunts R7A and R7B. Actuating variable R5 varies comparison voltage from +11.0 volts to +10.0 volts. 1 volt develops across R10. Each step of SW2 is one volt. One selects voltages in one-volt steps, overlapping each step with the variable control. R11 prevents short circuits from loading the voltage divider.

1.1 volts develops across R7 when a user selects position 2 or 4 of SW1. 11 volts appears at SW1C. But R5 drops 90% of the voltage. SW1D shunts R6 across network R7, R8, R9 and R10, making the resistance from SW1D to ground 1.1 kΩ. 1.1 kΩ represents 10% of the resistance from SW1C to ground.

A differential amplifier able to accept high voltage levels allows the designer to include higher comparison voltages. Higher comparison voltages mean less input attenuation.

See Fig. 6-84. The circuit shown here delivers 100 volts to the VOLTAGE selector switch, SW2A. SW2 selects attenuator networks. Dependent upon the selected attenuator, 100, 10 or 1 volts develops across resistive network R9, R10 and R11. Varying R11 changes the comparison output voltage from zero volts to maximum. One adjusts R10 to match the variable network to the fixed attenuator networks.

Adjusting R8 calibrates for exactly 100 volts from SW1A to ground.

D1 and V1 drop a regulated 103 volts. SW1 position determines voltage polarity. Positioned as shown SW1C holds V1 cathode to ground, SW1A and SW1B return D1 cathode to a positive source. Q1 and Q2 act as a high-impedance current source for voltage regulator V1-D1.

SW1 positioned to (-): SW1B holds D1 cathode at ground, SW1A and SW1C return V1 cathode to a negative source. Q3 and Q4 act as a high-impedance current source for D1 and V1. One sets R7 for optimum thermal stability.

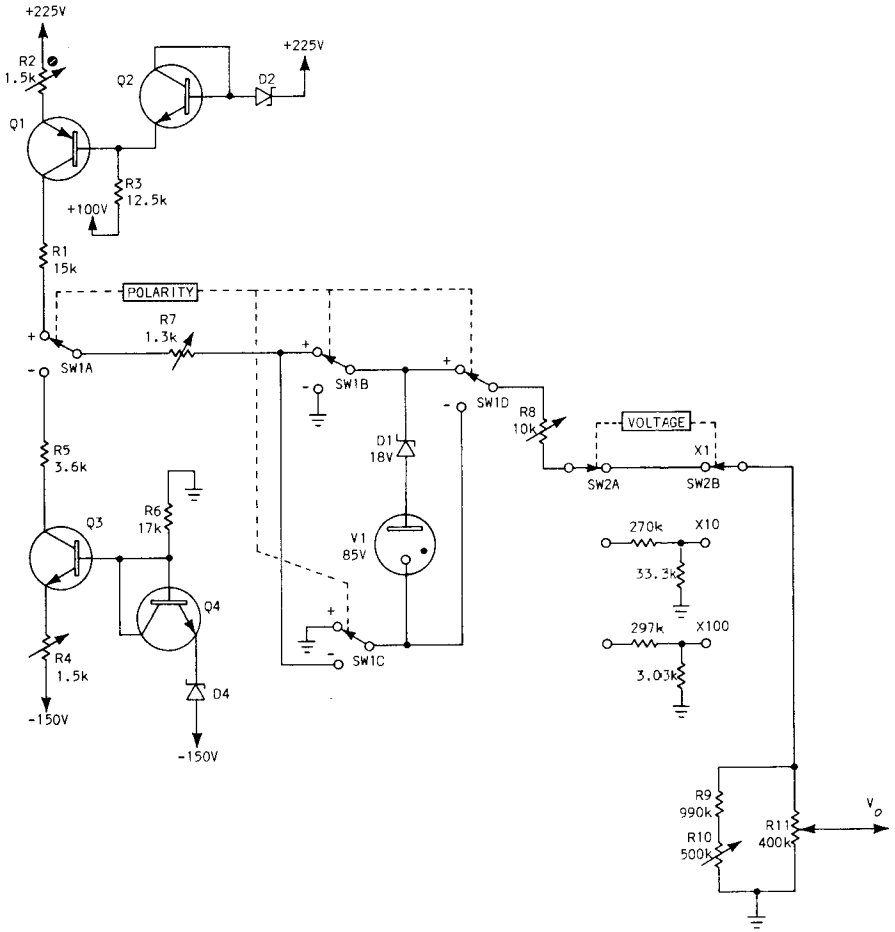


Fig. 6-84. High level comparison voltage.

Differential input amplifiers must amplify small signals under heavy current conditions. Large currents tend to stabilize a vacuum tube amplifier but they generate thermal noise. Small signal requirements make signal-to-noise ratio an important input amplifier consideration. Additive (distributed) amplifiers improve signal-to-noise ratio.

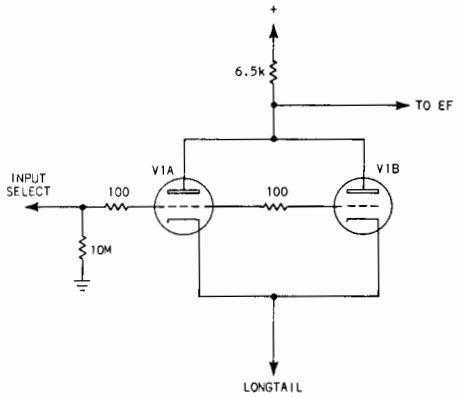


Fig. 6-85. Partial circuit of additive amplification to reduce noise.

The partial schematic Fig. 6-85 shows input active devices paralleled. Signal voltage gain of V1B adds to the signal voltage gain of V1A. Noise voltage gain of each device adds as the square root of the sum of the squares:

$$A_{V\ sig} = A_{V1} + A_{V2}$$

$$(A_{V\ noise})^2 = A_{V1}{}^2 = A_{V2}{}^2$$

An obvious signal-to-noise ratio improvement results from paralleling input devices.

More than two devices paralleled increases circuit complexities more than the improved signal-to-noise ratio justifies.

Any common cathode input amplifier described in this chapter may be modified to include parallel active devices.

7

FEDBACK AMPLIFIERS

Circuit designers incorporate feedback to stabilize or improve circuit performance. Previous chapters presented forms of feedback. For example: Unbypassed cathode, emitter, or source resistors; neutralization; and "Miller effect" degeneration to compensate negative resistance input characteristics.

Amplifiers discussed in this chapter act as null-seeking devices. Large amounts of degenerative feedback stabilizing a high-gain amplifier develop the null. Passive devices, in the feedback network, control amplifier functions.

open-loop gain

Abbreviation A_{ol} symbolizes open-loop gain. Open-loop gain refers to amplifier gain capabilities without degenerative feedback. Generally A_{ol} must be quite high. Infinite gain is optimum. Consider A_{ol} "high" when closed-loop gain represents a small fraction of open-loop gain. Although these amplifiers require high A_{ol}, open-loop characteristics need not be stable. Feedback provides stability.

inverting fedback amplifier

Using triangles to indicate open-loop gain one need only add feedback components to indicate fedback amplification as in Fig. 7-1. This is an inverting fedback amplifier. Triangle sign polarity indicates input to output voltage phase inversion.

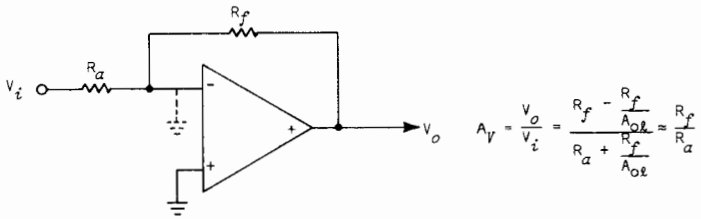


Fig. 7-1. Fed back amplifier.

constant voltage across inputs

Combined action of $A_{O\ell}$ and feedback devices, R_a and R_f, maintain voltage constant across the input terminals. This is the null the amplifier seeks. Input voltages and output voltages change, but voltage across input terminals remains fixed. Because of the null and because the (+) terminal returns to signal ground, a *virtual* ground develops at the R_a-R_f connection.

signal current flows through R_a and R_f

(-) amplifier input terminals present high impedance, but input voltages develop across R_a. E = IR. All signal current must therefore flow through R_a and R_f. The current through R_f drops a voltage between ground and the output terminal. This is V_O. Approaching fedback amplifiers in this manner leads to simplified circuit analysis:

1. A ratio of output voltage to input voltage expresses true voltage gain.
2. If signal current flows through R_f and R_a in series, and if virtual ground appears at junction R_f-R_a, then ratio R_f to R_a expresses voltage gain.

$$A_V \simeq \frac{R_f}{R_a}$$

Fig. 7-1 includes a voltage gain formula indicating R_f to R_a *approximates* voltage gain. $\frac{R_f}{R_a}$ expresses voltage gain closely enough for most circuit descriptions if one realizes the limitation imposed by open-loop gain. Fig. 7-1 indicates gain calculation accuracy increases when one includes open-loop gain. This is because $A_{O\ell}$ generates the power necessary to provide feedback currents. An insufficient $A_{O\ell}$ cannot provide current in quantities required to maintain a null across the input terminals. Reducing feedback current causes V_i to develop across R_a and a portion of R_f. $A_{O\ell}$ determines effective values of R_f and R_a.

If the (+) input terminal returns to ground, assume null seeking causes 0 volts or ground potential to also appear at the (-) input terminal. Typically though a quiescent voltage difference occurs, probably representing grid-to-cathode, base-to-emitter, or gate-to-source bias.

(+) input terminals act, for inverting fedback amplifiers, as input voltage references. Fig. 7-1 shows a ground reference. Amplifier inputs in Fig. 7-2A refer to +2 volts. Both terminals remain at signal ground. In Fig. 7-2B input terminals assume a value of -10 volts. Amplification concepts remain the same.

For single-ended amplification one assumes a null across the input terminals and ignores the (+) input terminal. Therefore, most inverting fedback amplifier symbols include but two terminals.

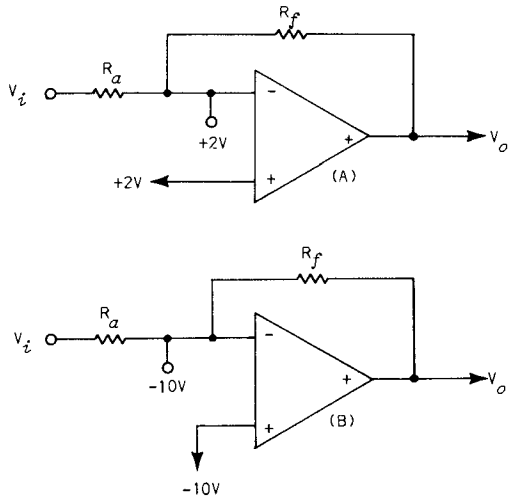


Fig. 7-2. Amplifiers seek an input null.

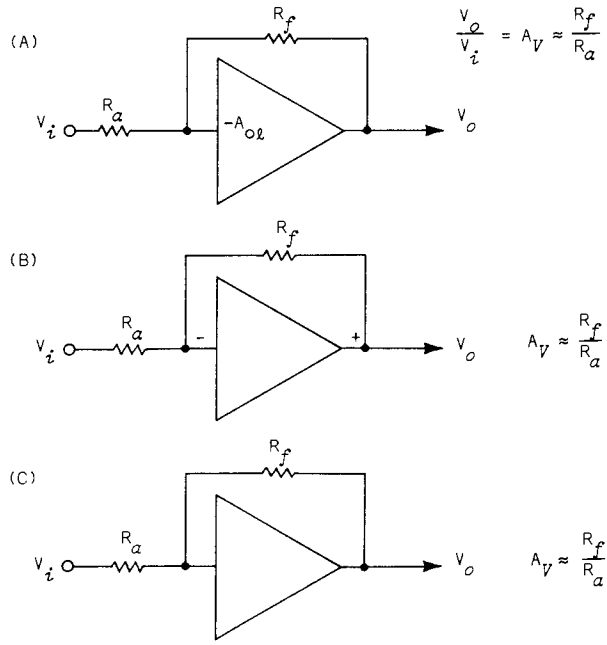


Fig. 7-3. Reducing symbol markings.

symbology

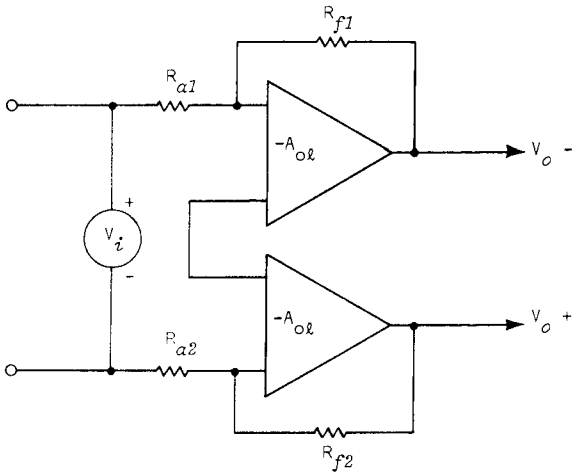
Fig. 7-3 illustrates three methods of two-terminal symbolizing an inverting fedback amplifier. The two terminals represent (-) input and (+) output terminals. A triangle represents the amplifier. Two resistive elements, R_f and R_a make up the feedback devices. Signs, adjacent to the amplifier terminals or inside the amplifier block, indicate V_O inverted from V_i.

Fig. 7-3A indicates phase inversion by ($-A_{O\ell}$) within the triangle. Fig. 7-3B indicates phase relation, input to output, with opposite signs. Fig. 7-3C merely extends the approach by assuming R_f always connects from the positive output terminal to the negative input terminal.

Two terminal symbols remove an unnecessary element from illustrations and are usually used. Remember, however, a third terminal (+input) exists and functions. Fig. 7-4 shows a symbolic differential, inverting fedback amplifier. The two (+) input terminals provide amplifier coupling.

$\frac{R_f}{R_a}$ expresses voltage gain, differential or single-ended. One may consider R_f and R_a as component sums or, if symmetrical, use either pair alone.

In symbol form, fedback amplifier action appears obviously simple. The difficulty arise when one tries to identify circuit components for symbol placement.



$$A_V = \frac{R_{f1} + R_{f2}}{R_{a1} + R_{a2}} = \frac{R_{f1}}{R_{a1}}$$

Fig. 7-4. Differential symbol.

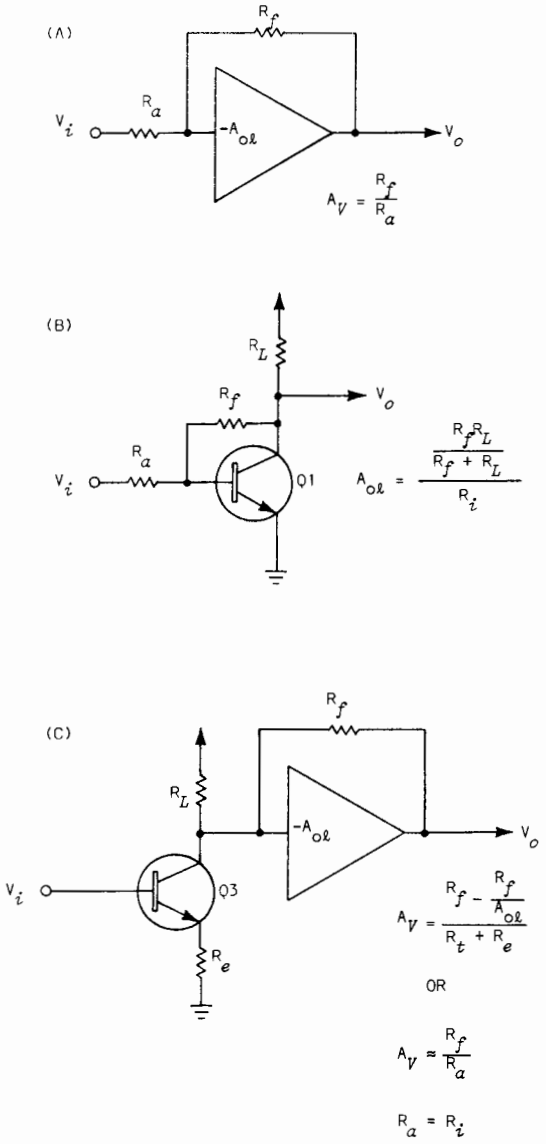


Fig. 7-5. Circuits and symbols.

Fig. 7-5A is a diagram of an inverting fedback amplifier and 7-5B and 7-5C circuit possibilities for identification of conceptual elements.

estimating $A_{O\ell}$

Refer to Fig. 7-5B: Ratio R_f to R_a defines gain if $A_{O\ell}$ is high. One estimates open-loop gain by dividing the parallel value of R_L and R_f by the emitter resistance. (Recall $A_V = \frac{R_O}{R_i}$ in common-emitter amplifiers.) He might also measure V_O, at the collector and divide it by any voltage change measured at the base (R_f-R_a connection). This gives true $A_{O\ell}$. There will be small signal voltage changes at the base of Q1. $A_{O\ell}$ must be infinite before an absolute nulling occurs between input terminals.

estimating impedances

The output and input impedance of Fig. 7-5B might also be estimated: To estimate output impedance answer the question, what value of R_O will reduce open-loop gain to the value of closed-loop gain? The R_O you resolve is a fair approximation of output impedance ($R_O = A_V R_a$). Input impedance is R_a. This is because of the virtual ground at the R_a-R_f connection.

Low input impedance is one of the characteristics of these amplifiers. Low input impedance is not always an advantage. Furthermore input impedance, or nulling, or virtual ground, depends upon open-loop gain being consistently high. This could impose severe loading on circuits driving the amplifier.

In Fig. 7-5C input circuits driving the amplifier and R_a are isolated from the loading effects of $A_{O\ell}$. Input voltage applied to the base of Q3 creates signal current in the emitter of Q3. $R_t + R_e$ determines total current flow. The current then flows in the collector. Virtual ground, due to feedback, develops at the collector. This nulling can only occur if all signal current flows through R_f. R_f/R_a yet approximates voltage gain. Q3 in this case isolates R_a from the effects of $A_{O\ell}$, and the signal generator from R_a.

signal pick-off amplifier

See Fig. 7-6, the block diagram of a signal pick-off amplifier. This amplifier delivers amplified input signal AC components to front panel, trigger and signal outputs. The pick-off amplifier accepts any 1 of 4 input sources or channels. Each input source is an identical noninverting fedback amplifier (source follower). R_a functions for both pick-off amplifier and selected input amplifier. Signal-source switching occurs at the virtual ground point, reducing capacitive switch loading.

CH 1 source follower applies input signal voltage to the vertical amplifier system. This signal voltage across R_a develops signal currents which also flow through R_f.

Pick-off amplifier output voltage results from signal current quantity through R_f. E = IR, or $V_O = I_{sig}\ R_f$.

Amplifier symbols represent either one or several stages of amplification. Triangles "pick-off amplifier" and "vertical amplifier" represent several stages of amplification. The source follower triangle is a single stage. This presentation focuses on individual stages within the pick-off amplifier triangle.

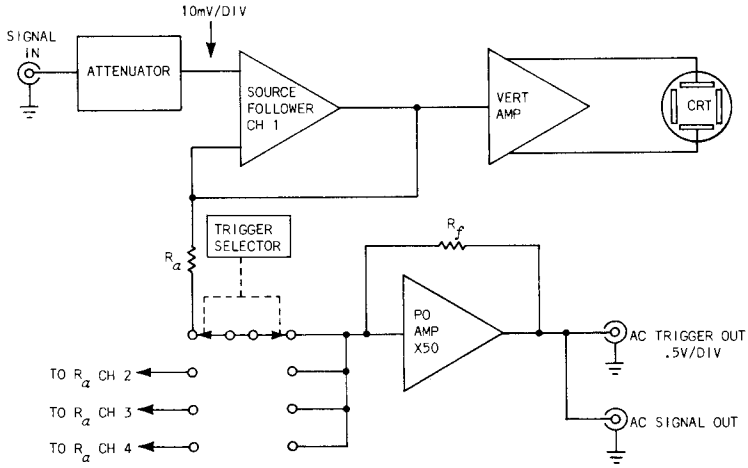


Fig. 7-6. Trigger pickoff.

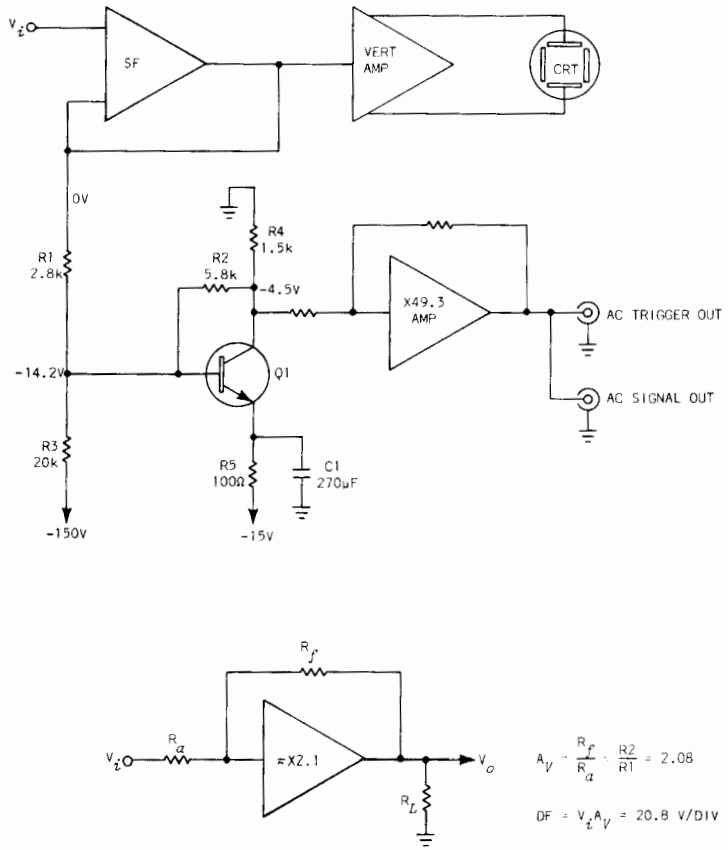


Fig. 7-7. Trigger pickoff input amplifier.

pick-off amplifier input stage

Fig. 7-7 shows the pick-off amplifier input stage. Channel switching, not shown, substitutes R1 at the base of Q1. R1 is a source-follower longtail. R3 returns R1 and the base of Q1 to -150 V. Feedback action regulates base voltage. Source follower longtailing returns to a low impedance, -14.2 V supply. C1 bypasses emitter resistor R5. R4 functions as a load resistance. Passive devices R1 and R2 establish signal voltage gain.

$\frac{R_f}{R_a} = \frac{R2}{R1} = 2.1$, as long as $A_{O\ell}$ remains high. To prove this estimate $A_{O\ell}$:

A_V (open-loop) $= \frac{R_O}{R_i}$. R_O = R2 paralleled by R4.

$$R_i = R_t \simeq r_e.$$

$$r_e \text{ (AC only)} \simeq \frac{26 \times 10^{-3}}{I_e} \simeq 15\ \Omega.$$

$$\frac{R_O}{R_i} \simeq \frac{1200}{15} \simeq 80.$$

Closed-loop gain (2.1) is not a significant fraction of open-loop gain -- ignore $A_{O\ell}$.

Notice, though, the effect of $A_{O\ell}$ at DC. R5 becomes a part of R_i, adding to R_t. Thus,

$$\frac{R_O}{R_i} = \frac{1200}{115} \simeq 10.4.$$

$\frac{R_f}{R_a}$ represents a significant fraction of $A_{O\ell}$:

1. Ignoring $A_{O\ell}$, $A_V = 2.08$.
2. Including $A_{O\ell}$, $A_V = 1.55$.

AC amplification only

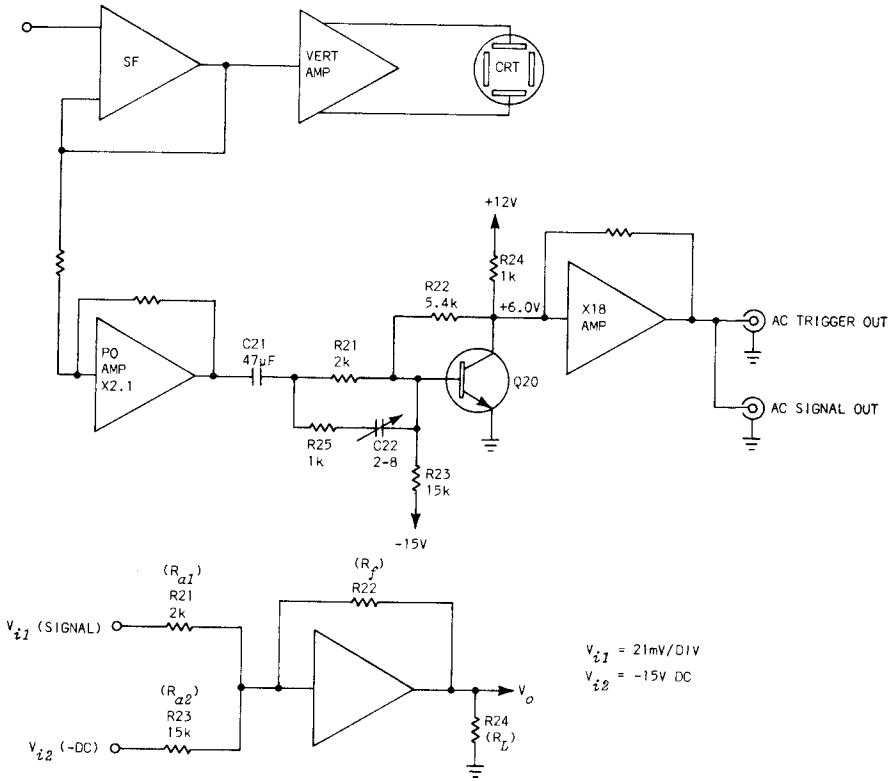
Including the DC $A_{O\ell}$ only illustrates the effects of open-loop gain. This pick-off amplifier system has no DC amplification requirement. Amplifying AC only, with a coupling capacitor to following stages, simplifies individual stage analysis.

Isolated from the previous stage DC level by capacitor C21, Fig. 7-8 illustrates three concepts:

trigger pick-off driver amplifier

1. DC transistor levels set by resistive feedback.
2. Signal gain determined by passive device ratios.
3. Compensation provides constant feedback ratios.

Q20, emitter returned to ground, requires bias circuitry for turn-on. Voltage divider R23-R22-R24 develops turn-on potential. Q2 collector current drops a voltage across load resistor R24. Feedback current adds to the collector current drop. Sufficient current flows through feedback network R22 and R23 to develop an input null. Multiplying -15 volts by $\frac{(-)\ R22}{R23}$ establishes Q20 DC voltage above Q20 base voltage.



$$A_V(\text{SIGNAL}) = \frac{R_f}{R_{a1}} = \frac{R22}{R21} = 2.7$$

$$A_V(\text{DC}) = \frac{R_f}{R_{a2}} = \frac{R22}{R23} = .36$$

$$DF_o = DF_i \left(\frac{-R_f}{R_{a1}}\right) = (21 \times 10^{-3})(-2.7) = 56.6\text{mV/DIV}$$

Fig. 7-8. Trigger pickoff driver amplifier.

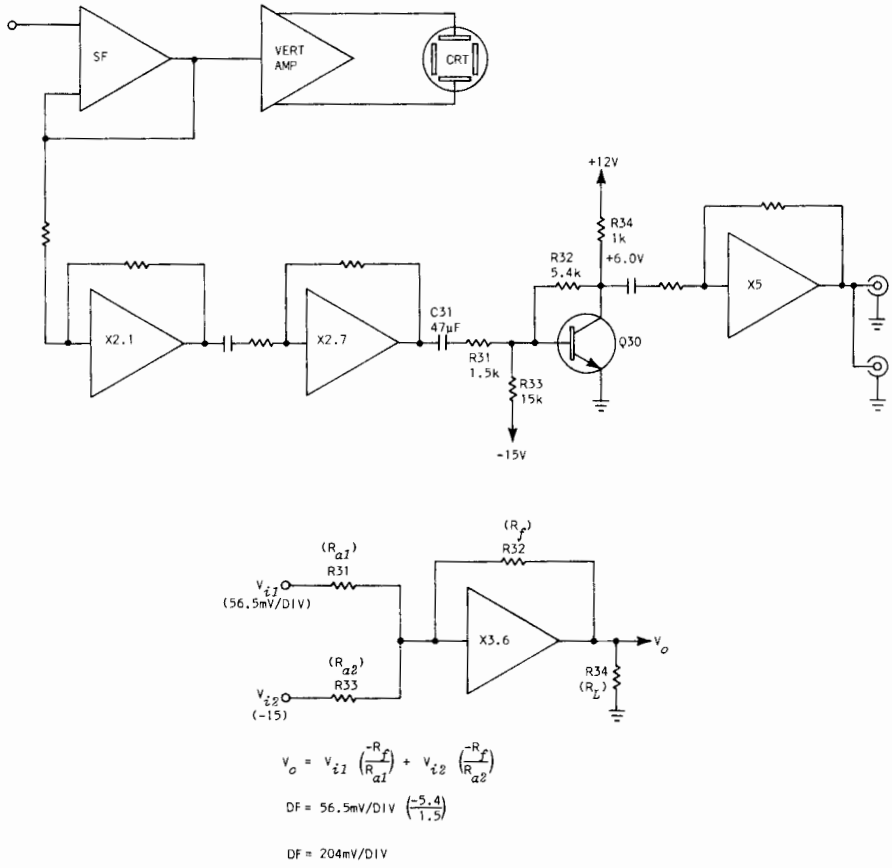


Fig. 7-9. Trigger pickoff driver amplifier.

Knowledge of 6.0 volt drop across R24 allows easy estimation of open-loop gain. R_o consists of R24 paralleled by R22. R_i is R_t. Solve for emitter current by subtracting feedback current from total current through R24. Slightly more than 1 mA through R23 forward-biases Q20. This same current flows in R22 and R24. Therefore, collector (emitter) current approximates 6.0 mA. Open-loop gain falls between 85 and 170.

Closed-loop gain for the DC network $\left(\frac{R22}{R23}\right)$ represents a negligible fraction of open-loop gain. The same applies to closed-loop gain of the signal network.

Signal voltages, coupled through C21, develop currents in R21. To maintain an input null equal currents must flow through R22. $\frac{R_f}{R_a}$ (R22 to R21 ratio) defines voltage gain. Signal voltage gain remains constant until high-frequency components cause stray reactances to change the effective value of $\frac{R_f}{R_a}$.

frequency compensation

R25 and C22 shunt R21 (R_a) compensating for reduced impedance of R22 (R_f) at high frequencies. Stray capacitance shunts R22, reducing both $A_{o\ell}$ and R_f-to-R_a ratio at high frequencies. R25-C22 cause R_a to reduce at the same rate maintaining R_f/R_a constant.

summing amplifier

The lower diagram in Fig. 7-8 simplifies the circuit to a summing amplifier. Output voltage represents the algebraic sum of all input voltage-gain products. Remember to assign (-) to each $\frac{R_f}{R_a}$ to account for amplifier signal inversion.

The circuit shown in Fig. 7-9 practically duplicates that in Fig. 7-8.

Similarities:

1. $A_{o\ell}$,
2. Collector voltage,
3. Capacitively coupled.

Differences:

1. R_a (signal) not compensated,
2. Gain ratio equals 3.6.

The illustration includes the simplification with gain and DC level calculations.

Four cascaded fedback amplifiers make up this pick-off amplifier system. Fig. 7-10 depicts the output stage.

trigger pick-off output amplifier

The output stage approaches a theoretical voltage generator, developing 1 volt per division output. This voltage appears at the common connection of R48 and R49, referenced to zero volts. 50% of the output amplifier signal appears at J1 and J2, assuming a load resistance equal to R48 or R49.

Circuit 7-10 simplifies to the symbolic circuit shown. Input signals, coupled through C44, generate current through R41. EF output voltage causes sufficient current flow, through feedback resistor R42, to maintain an input null. $\frac{R_f}{R_a} = \frac{R42}{R41}$.

Coupling output signal voltages via an emitter follower isolates the collector circuit from output loading. Ergo, amplifier output impedance approaches zero ohms and circuit loading does not change open-loop gain.

D42, D41, R43 and R47 set quiescent operating levels and allow output signals to vary about zero volts.

Quiescent conduction of Q41 drops 15 volts across R43. D41 elevates this voltage one silicon junction, representing turn-on for Q40 via R42. Q40 collector current and voltage divider D42-R47 set proper base bias for Q41.

Networks R45-C45 and R46-C46 compensate R_f and R_a, maintaining feedback ratio constant over the amplifier bandwidth.

From J1 this amplifier appears a 51-ohm source; from J2 a 91-ohm source.

After identification of passive feedback components, one experiences little difficulty simplifying inverting fedback amplifiers. Buffering or isolating feedback components with active devices aids amplifier performance and somewhat disguises one, or more, feedback elements. The circuit in Fig. 7-10 used an emitter follower to isolate the collector load from R_f and output terminals. One also finds active devices as buffers, isolating R_a from input terminals.

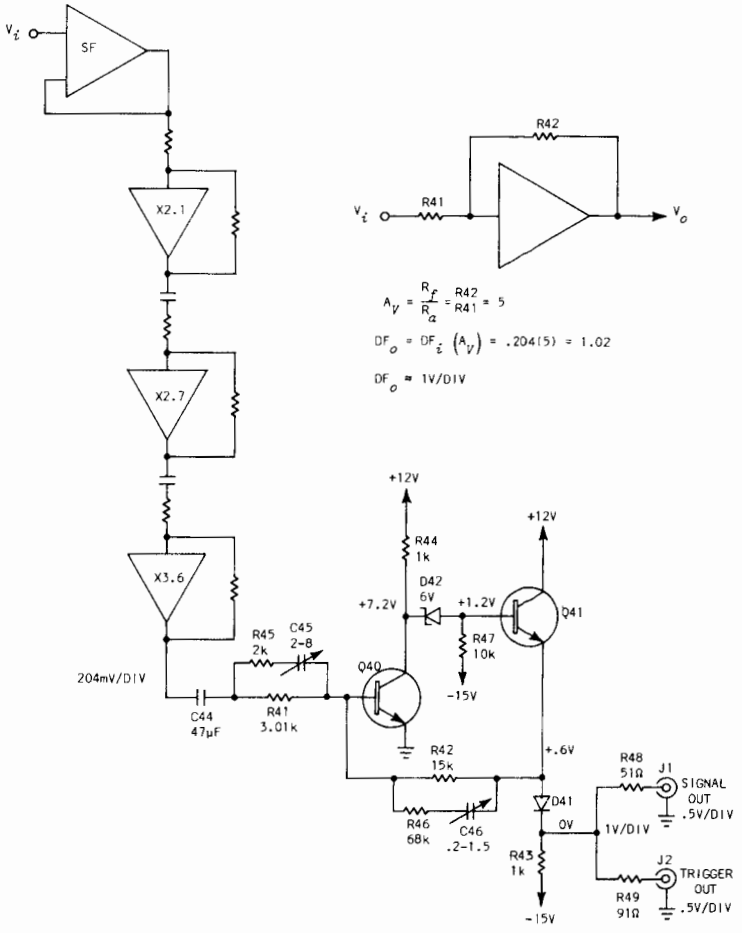


Fig. 7-10. Trigger pickoff output amplifier.

Fig. 7-11 shows three cascoded amplifiers: A vertical preamplifier, a X11 fedback amplifier, and X1 fedback amplifier. Circuitry associated with active devices Q1, Q2, Q3 and Q4 make up the first, or X11, fedback amplifier. This amplifier inverts and amplifies the preamplifier output signal, applying it to the lower CRT plate and to the second fedback amplifier. Active devices Q5, Q6 and Q7, with associated passive components, comprise the second fedback amplifier. Amplifier number two, with unity gain, inverts the lower CRT signal and drives the upper CRT deflection plate. A push-pull CRT signal, at 20 volts per division results.

To identify components designate the first amplifier A1 and the second A2.

X11 amplifier

Amplifier A1 has an R_a for signal voltages and an R_a for positional voltages. Signal currents flow through R_a found in the emitter circuit of Q1. R_a consisting of R3, R4 and R5 establishes positional output voltages. R6 is R_f.

inverting amplifier

Amplifier A2 also has an R_{a1} and R_{a2}. Signal and quiescent voltage across R12 (R_{a1}) add to the effects of the voltage across R13 (R_{a2}). These voltages and resistances create the net current flow through R14 (R_f) which develops V_o.

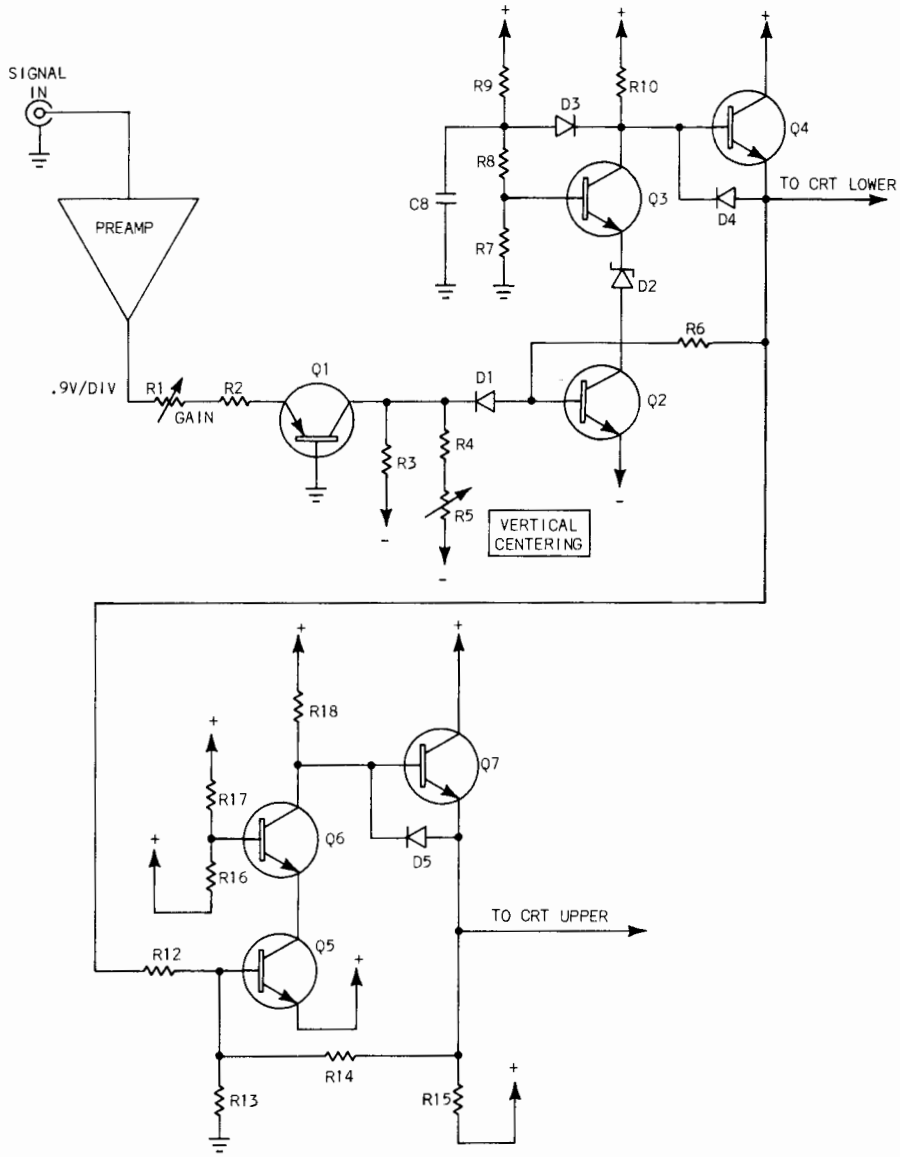


Fig. 7-11. R_a isolated.

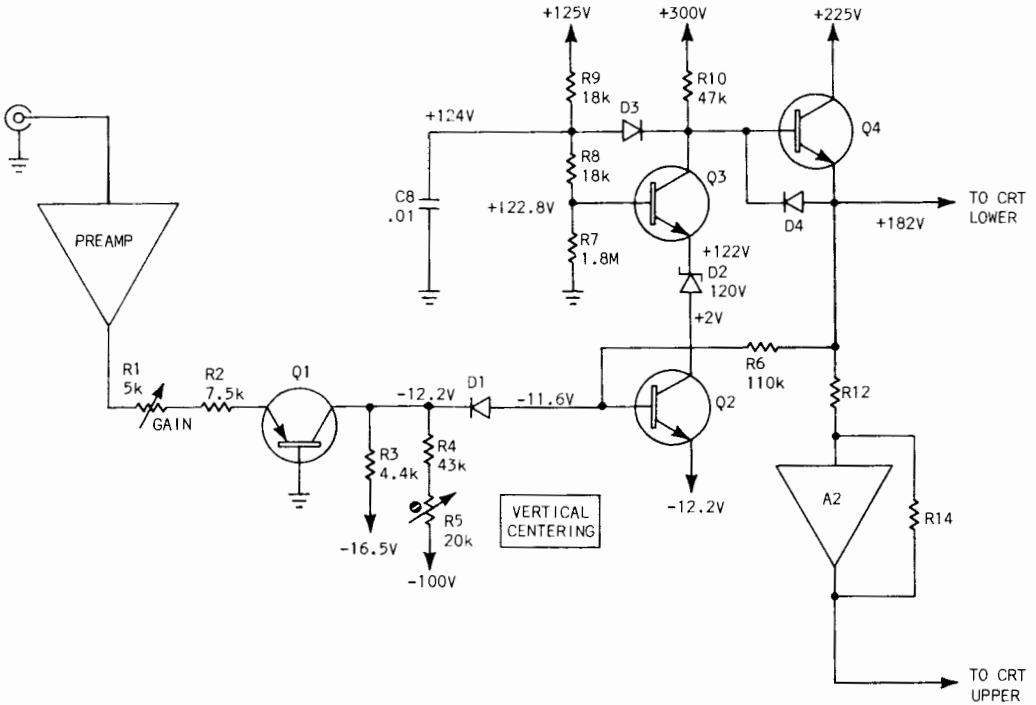


Fig. 7-12. X11 amplifier.

Fig. 7-12, the schematic of A1, includes voltage levels and resistive values. The preamplifier applies vertical signals to R1. Signals arrive at a deflection factor of 900 millivolts per division. Q1 emitter sets at virtual ground. Therefore, signal current quantity depends upon applied signal amplitude and resistive total of R1 and R2. Assume R1 set to midrange and essentially all Q1 emitter current flows as collector current.

Q1 merely isolates the emitter connection of R2 from D1 cathode potential. Virtual ground appears at the base-anode connection of Q2-D1, cathode-collector connection of D1-Q1, base and emitter of Q1. Voltage changes then do not occur. And a grounded-base amplifier contributes unity current gain.

Resistive network R3-R4-R5 returns to a negative voltage to develop position voltage and provide turn-on for coupling diode D1. An "on" diode presents very low impedance to signal current flow. Signal currents flow through D1 and feedback resistor R6. The DC drop across D1 represents Q2 forward bias.

Cascoded amplifier Q2-Q3 develops open-loop gain. Signal currents generated in Q2 flow in load resistor R10, developing signal voltages at the base of Q4. Q2-D2-Q3 cascoding allows relatively high Q3 collector voltage without dropping a large voltage across Q2 or Q3. Q2 collector sets at about +2 volts. Zener diode D2 elevates Q3 emitter 120 volts without signal attenuation. Grounded-base amplifier Q3 presents small signal attenuation. Therefore, Q2 emitter current flows through load resistor R10 developing +182 volts at the collector of Q3. +182 volts represents a centered CRT display.

Resistive network R7-R8-R9 determines Q3 base bias and establishes reference voltage for protective diode D3. R9-C1 decouple the network. R8 elevates D3 anode about 2 volts above Q3 base.

D3 prevents collector-to-base breakdown. D3 clamps negative collector excursions about one volt above Q3 base voltage. Clamping occurs when large signal voltages vary about an upward, CRT, positional voltage. Trace positioned at the maximum "up" position sets Q3 collector voltage to +142 volts.

Deflection factor at this circuit point is 10 volts per division. Assuming 10-division deflection, maximum signals vary 50 volts above or below the +142 volt position reference. The maximum negative excursion drives collector voltage toward +90 volts but D3 conducts as the excursion extends below +124 volts (an off-screen voltage) protecting Q3 collector-emitter junction.

Emitter-follower Q4 isolates load resistor R10 from circuit loading. This isolation preserves A_{OL}, maintaining passive device control of closed-loop gain.

Diode D4 provides an additional charging path for output capacitance. NPN emitter followers rapidly charge capacitance in a positive direction. They do not, however, act as low-impedance charging paths for negative excursions. As emitter voltage of Q4 lags base signal excursions, D4 conducts to charge the CRT negatively. Emitter follower Q4 applies signal voltage to the lower CRT deflection plate and to amplifier A2.

Input signal voltages develop signal current in R1 and R2. This quantity of current flows through R6, developing output signal voltage. The ratio R6 to R1 + R2 expresses voltage gain. Output DC levels result from the same action.

Preamplifier output level sets, quiescently, at +10 volts. Assuming R1 set to midrange, 1 mA quiescent emitter current flows in Q1. 1 mA also flows in R3. R4 and R5, as well as R3, return to a negative voltage. Current through the network depends upon the setting of R5. Q1 collector current and R3 current balance. Consider that the voltage across R4 and R5 multiplied by $\frac{R6}{R4 + R5}$ expresses output DC voltage, referenced to -12.2 volts. This works as long as the sum of R1 and R2 equals 10 kΩ.

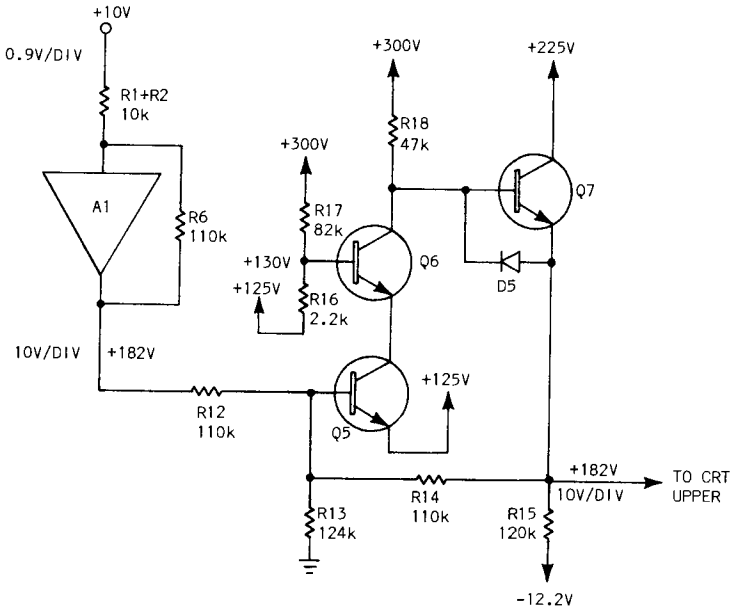


Fig. 7-13. Unity signal gain.

push-pull deflection

Amplifier A2 inverts, at unity gain, the lower deflection plate signal. Thus the CRT receives push-pull deflection. Refer to Fig. 7-13. A2 is a simple version of A1. R12 is R_a. R14 is R_f. Q5 and Q6, cascoded, develop A_{ol} across R18. Emitter follower Q7 isolates R18 from CRT loading to prevent A_{ol} deterioration.

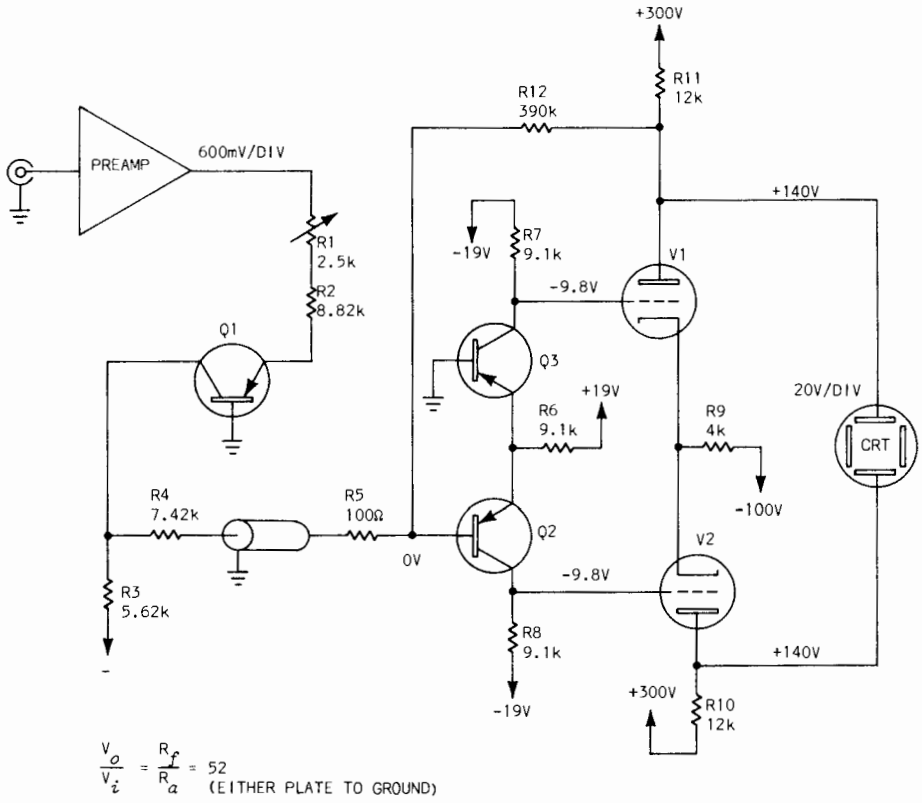


Fig. 7-14. Feedback loop in the output stage.

The circuit of Fig. 7-13 cascades fedback amplifiers, A1 and A2, to accomplish phase splitting. Including a feedback loop in a conventional paraphase amplifier develops the same result. See Fig. 7-14.

paraphase amplifier with feedback

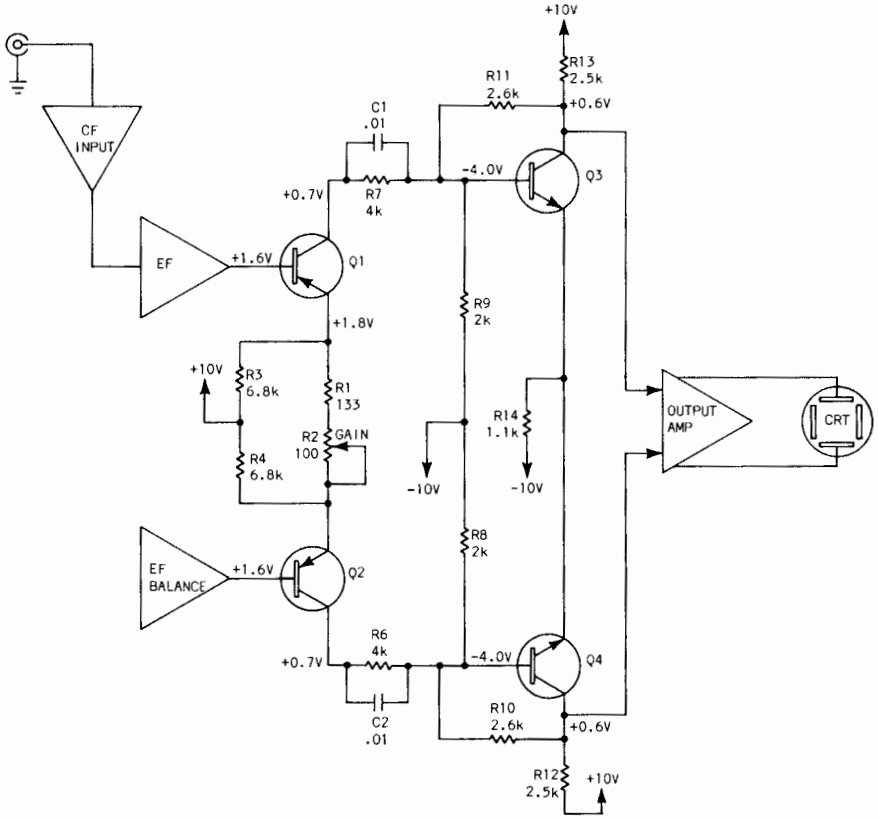
This main vertical amplifier circuit receives, from the preamplifier, a single-ended signal. The circuit amplifies and phase inverts to drive vertical CRT plates push-pull. 600 millivolts per division deflection factor affects the CRT trace.

A cursory inspection might lead one to think emitter resistors R1 and R2 constitute R_a. Not so! Q1 collector current splits. A portion flows through R3 and the remainder through R4 and R5. Total current through R4 and R5 appears to flow through R12. Therefore, R12 is R_f and R4 plus R5 is R_a.

$\frac{R_o}{R_i}$ expresses voltage gain from the input of R1 to the collector of Q1. Q1 circuitry realizes a gain less than unity, about 32%. 190 mV/div develops at the collector of Q1. This V_i across R4 and R5 generates the feedback currents which flow through R12.

Q2 and Q3 function as a longtailed phase inverter. V1 and V2 are longtailed, push-pull amplifiers. R_f (R12) connects from an inverted signal point to the input terminal. Passive network R4-R5-R12 controls amplifier gain.

$\frac{R_f}{R_a}$ expresses voltage gain from amplifier input to either triode plate. *But not from one triode plate to the other!* Feedback from V1 (plate) develops closed-loop gain. Current through R10 results from, but does not contribute to, fedback current. The ratio of feedback devices expresses voltage gain to the plate of V1. Equal-amplitude opposite-phase signals develop at V2's plate. One must double feedback resistance ratio to define push-pull CRT deflection factor.



7-15. Phase inverter gain controlled by feedback.

phase inverter

The circuit of Fig. 7-15 functions as a phase inverter, developing a balanced push-pull output. Acting as a low-impedance voltage source, the inverting fedback amplifier drives the vertical output amplifier.

Phase inverters Q1 and Q2 isolate R_a from the effects of open-loop gain. Open-loop gain degenerates with common-mode signals, aiding dynamic push-pull signal balance. Push-pull amplifiers Q3 and Q4 provide open-loop gain. The circuit simplifies to amplifier triangles enclosed by passive device feedback networks.

To simplify one need identify feedback components and estimate open-loop gain. Eliminating components other than feedback devices aids simplification:

R3 and R4 longtail phase inverters Q1 and Q2.

R6 and R7, bypassed by C1 and C2, temperature compensate Q1 and Q2.

R8 and R9 return Q1 and Q2 to V_{CC}. R8 and R9 also return Q3 and Q4 to a base bias supply.

R14 longtails push-pull amplifiers Q3 and Q4.

R12 and R13 function as push-pull amplifier collector load resistances.

Components not identified must be feedback determinants:

R_a consists of the internal impedance of Q1 and Q2, R1 and R2. Assume R2 set to midrange.

R_f is R11 and R10.

The ratio (R10 + R11) to (R1 + R2 + R_{t1} + R_{t2}) expresses dynamic voltage gain from the phase inverter input to the output across Q3 and Q4. This remains true as long as circuit open-loop gain remains high.

Q3 and Q4 circuitry determines open-loop gain. $\frac{R_o}{R_i}$ expresses A_{ol}. R_o is R11 paralleled by R12. R_i is the R_t of Q3 and Q4.

$$R_o \simeq 2500$$

$$R_i \simeq 25$$

$$A_{ol} \simeq 100.$$

isolating R_a from R_f

Isolation of R_a from R_f prevents open-loop gain from significantly affecting dynamic closed-loop gain. Closed-loop gain (22+) appears to be a significant fraction of open-loop gain (100). However, Q1 and Q2 isolate R_a so that signal voltage variations at the "null point" do not change input signal currents. Signal voltages applied to Q1's base develop across Q1 and Q2 emitter coupling. This voltage generates signal currents which flow as Q1 and Q2 collector signal currents. Collector *voltage* changes have negligible control of signal current quantity.

Feedback current, through R10 and R11, must equal signal current quantity to maintain a voltage null at the bases of Q3 and Q4. A "perfect" null occurs only if $A_{o\ell}$ is infinite. Practical amplifiers realize finite $A_{o\ell}$ and signal voltages develop at the null point. When $\frac{R_f}{R_a}$ represents a significant fraction of $A_{o\ell}$, noticeable signal voltages appear at the input terminal. The null point appears to move. Without isolation, R_f appears smaller and R_a larger. With isolation only R_f appears to change value.

$A_{O\ell}$ exerts about 2% dynamic closed-loop gain reduction upon the circuit in Fig. 7-15. Therefore, $\frac{R_f}{R_a}$ approximates voltage gain. This would not be true without the isolating effects of Q1 and Q2.

With R_a isolated, $A_V = \frac{V_O}{V_i} \simeq \frac{R_f - \frac{R_f}{A_{O\ell}}}{R_a} \simeq \frac{R_f}{R_a} \simeq 22+$

Without isolation, $A_V = \frac{V_O}{V_i} \simeq \frac{R_f - \frac{R_f}{A_{O\ell}}}{R_a + \frac{R_f}{A_{O\ell}}} \simeq 10+$

$\frac{R_f}{R_a}$ *does not* approximate quiescent or common-mode signal levels. R14 (Q3-Q4 longtail) becomes R_i for common-mode voltages. Common-mode signals drop $A_{O\ell}$ to about 2.5.

delay-line driver

The amplifier in Fig. 7-15 develops a fairly low output impedance.

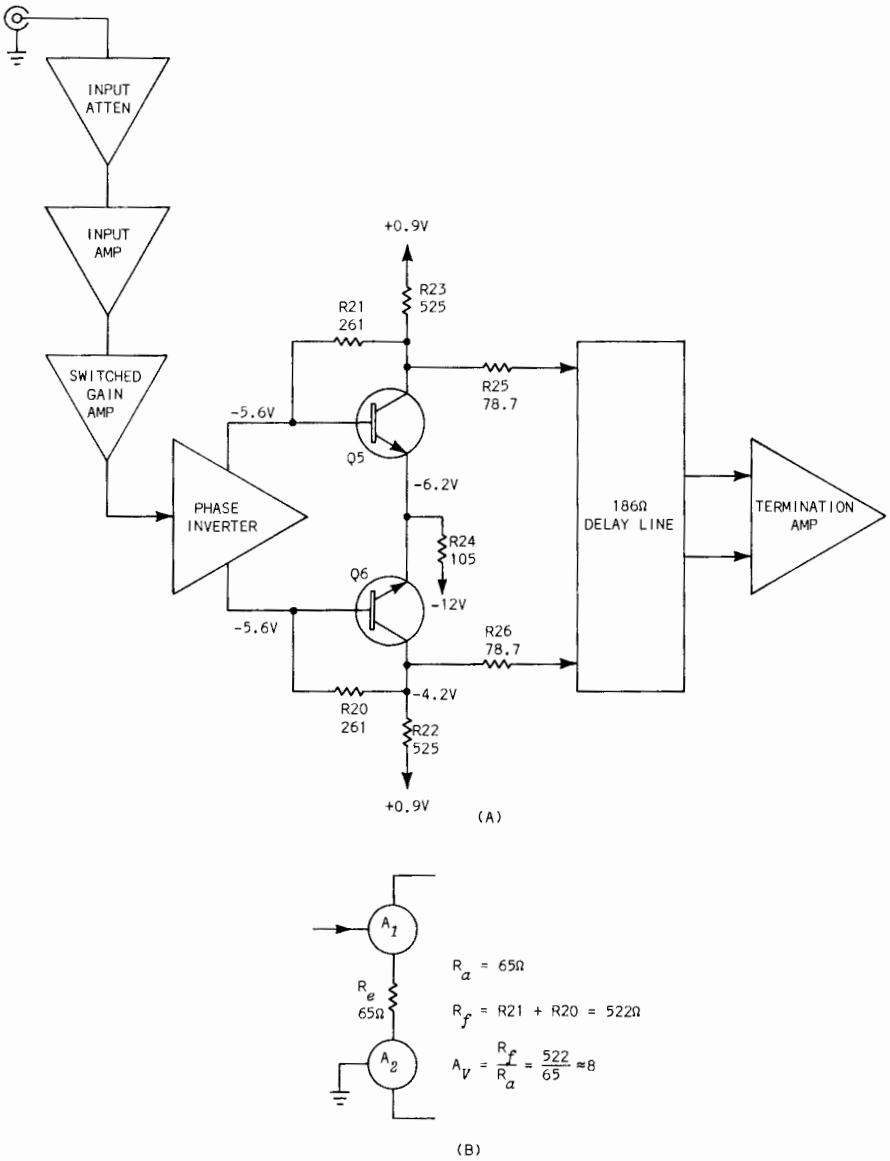


Fig. 7-16. Isolating R_a.

Low-impedance circuits provide drive to capacitive loads, switching points, and terminations. The fedback amplifier in Fig. 7-16A drives the delay line as a voltage source. Base circuits, at virtual ground, provide a switching point. Vertical systems of two or more preamplifiers could be switched at the bases of Q5-Q6.

Closed-loop gain becomes meaningless for this amplifier as a single stage. One should consider this amplifier as an integral part of the phase inverter. Meaningful voltage gain measurements refer the phase inverter signal input to the delay line driver signal output. $\frac{R_f}{R_a}$ approximates voltage gain. The phase-inverter emitter coupling is R_a. R20 and R21 sum is R_f. Phase inverter active devices isolate R_a from the effects of A_{ol}.

See Fig. 7-16B. A1 and A2 represent active devices in the phase inverter. These devices develop push-pull signal currents and isolate R_a. The accompanying formula defines closed-loop gain as a resistance ratio equal to 8. This is gain realized from phase inverter input to the output across Q5 and Q6.

output impedance

R25 and R26, of Fig. 7-16A, indicate output impedance of amplifier Q5-Q6. R25, R26 and the delay line driver output impedance match the 186-ohm delay line. Amplifier output impedance must equal the difference between delay line impedance and the sum of R25 and R26. 186 - 157.4 = 28.6 Ω. Each collector (Q5 and Q6) appears a 14.3 ohm signal voltage source.

The amplifier in Fig. 7-16 develops voltage gain as well as matching impedances. Designers use fedback amplifiers to match impedances even at the sacrifice of voltage gain. See Fig. 7-17.

Signal voltages applied to the phase inverter cause signal current flow through R3-R5 and R4-R6. The voltage that develops at the collectors of Q1 and Q2 can be estimated by multiplying input voltage by $2R_f/R_a$.

(+) phase inverter coupling is R_a since total signal current results from V_i across this resistance. R_f is R3 + R5 or R4 + R6.

Adding R7 and R8 to the amplifier output impedance causes this circuit to appear as a generator that has an output impedance matching the delay line Z_O. Voltage develops across the delay line at half the Q1 and Q2 collector amplitude.

R9 and R10 are in the feedback loop only to provide quiescent biasing.

R12-C12 is a peaking network which compensates for delay-line losses (dribble-up). The overpeaking lasts but a short period, countering, with additional current, the power lost in the line during rapid transient voltages.

To examine the effects of the network in more detail, assume C12 shorted, and recall that virtual ground develops at the input terminal of the feedback

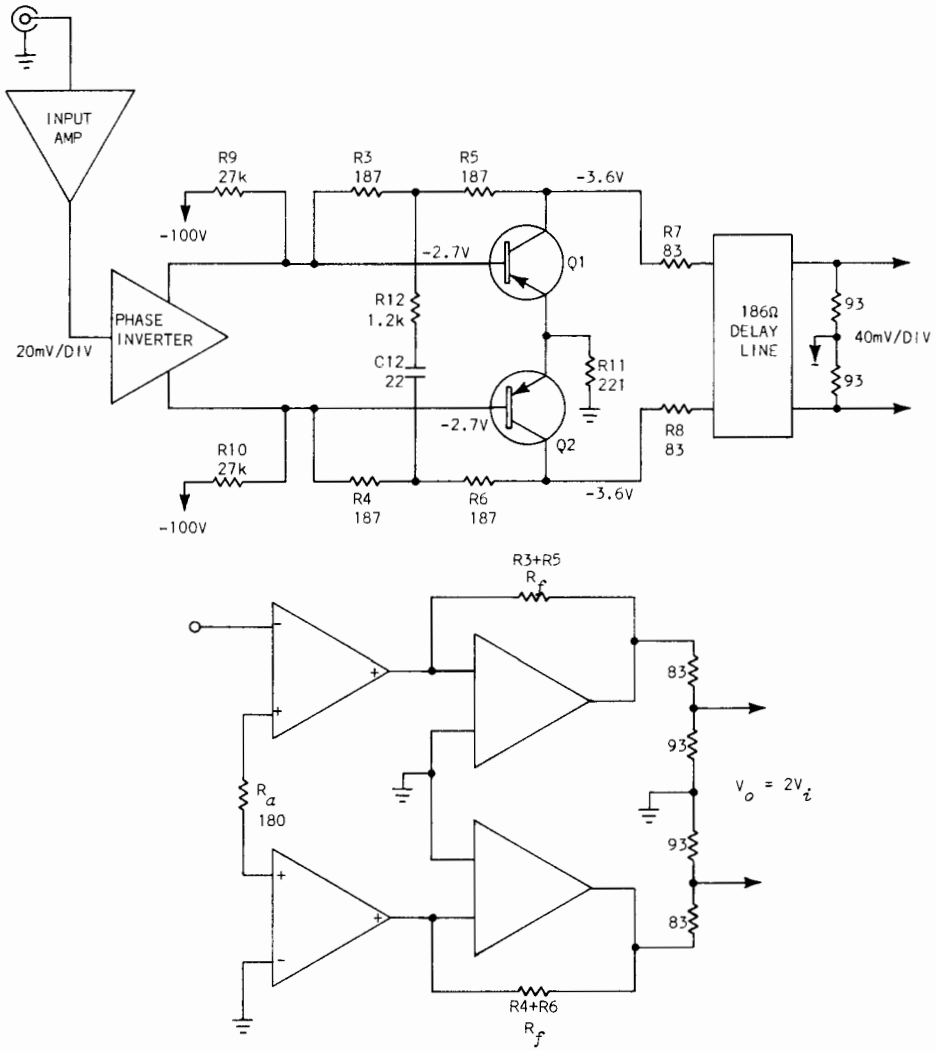


Fig. 7-17. Driving the delay line with an impedance equal to Z_o.

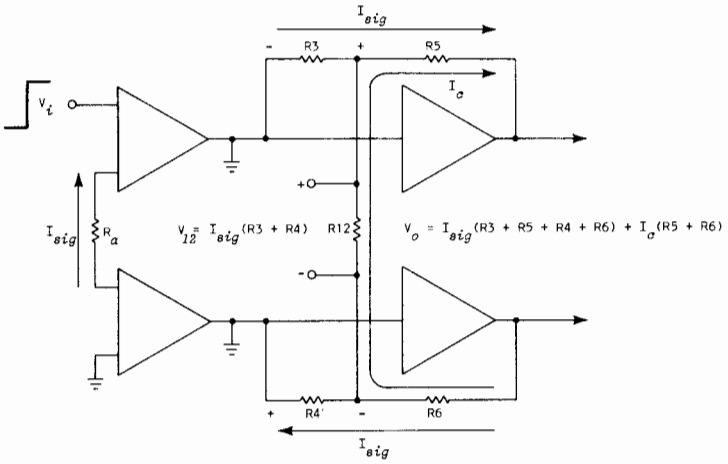


Fig. 7-18. Cross-coupling R_f increases gain.

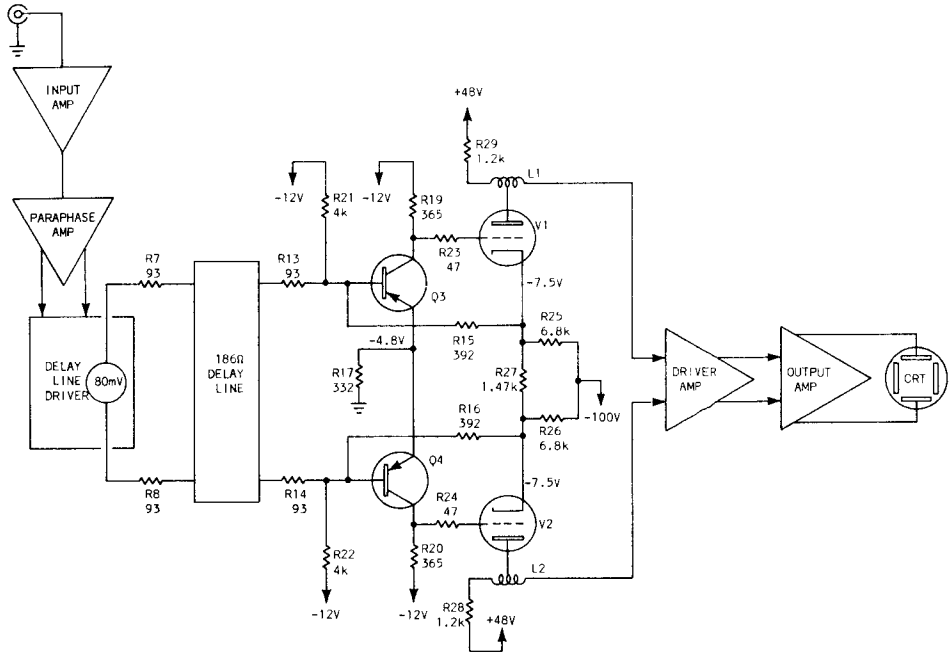
amplifiers: Fig. 7-18 shows that application of Ohm's law describes the action. V_i across R_a generates signal current (I_{sig}). I_{sig} flows through R_a, R3, R5, R6 and R4 in series. Because of the virtual grounds, equal voltages of opposite polarity develop across R3 and R4. This voltage difference appears across R12. E = IR. To maintain the input null, A_{ol} must provide the compensating current (I_c) demanded as well as signal current. Output voltage then becomes an IR sum. Cross-connecting R_f increases gain over the R_f-to-R_a ratio if A_{ol} can provide the additional current.

This type of peaking can be a single series RC, as R12-C12 of Fig. 7-17, or several parallel networks of various time constants. These are usually chosen after observing the step-response characteristics of the delay line.

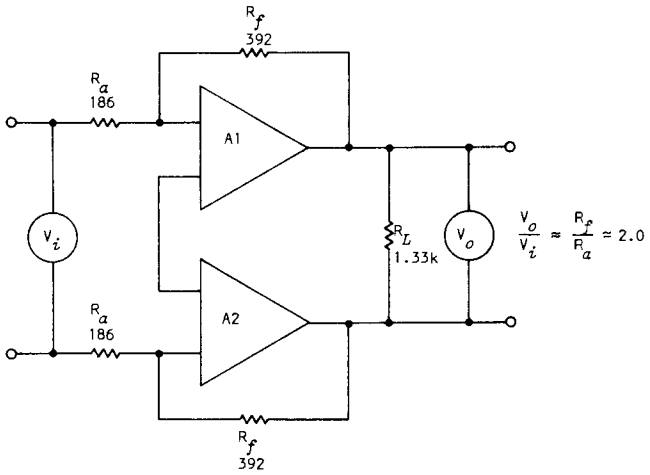
Fedback amplification causes a null-seeking action. Current through R_f must be sufficient to drop across R_a the applied input voltage. R_a establishes the quantity of current required. This current quantity through R_f determines output voltage amplitude.

termination amplifier

Apply the above statement to termination amplifier circuitry illustrated in Fig. 7-19A. Including V1 and V2 in the feedback loop causes gain to develop *independent of changing tube parameters* from delay-line driver to the output across V1 and V2.


INPUT AMP
PARAPHASE AMP
DELAY LINE DRIVER
80mV
186Ω DELAY LINE
R7 93
R8 93
R13 93
R14 93
R21 4k
R22 4k
R19 365
R20 365
-12V
+48V
R29 1.2k
L1
L2
V1
V2
R23 47
R24 47
Q3
Q4
-7.5V
-4.8V
R15 392
R16 392
R17 332
R25 6.8k
R26 6.8k
R27 1.47k
-100V
R28 1.2k
DRIVER AMP
OUTPUT AMP
CRT

(A)


R_f 392
R_a 186
A1
A2
V_i
R_L 1.33k
V_o
$\frac{V_o}{V_i} \approx \frac{R_f}{R_a} \approx 2.0$

(B)

Fig. 7-19.

Component identification:

R_a is R7 + R13 and R8 + R14.

R_f is R15 and R16.

R21 and R22 are a voltage return for the delay-line driver.

R17 reduces quiescent voltage across Q3 and Q4.

R19 and R20 are collector loads to develop grid signal voltage applied to V1 and V2.

R23 and R24 are suppressor resistors.

R25 and R26 are V1 and V2 longtail and a return for the delay-line driver.

Approximately 50% of R25-R26 current longtails V1 and V2. Remaining current flows through R15 and R16 combining with current through R21 and R22 to provide delay-line driver power.

R27 is V1 and V2 cathode coupling and, paralleled by R25 and R26, R_L for the fedback amplifier.

L1 and L2 are T-coils causing V1 and V2 plate load to appear a short section of transmission line.

R28 and R29 are plate load resistors, terminating the plate transmission lines.

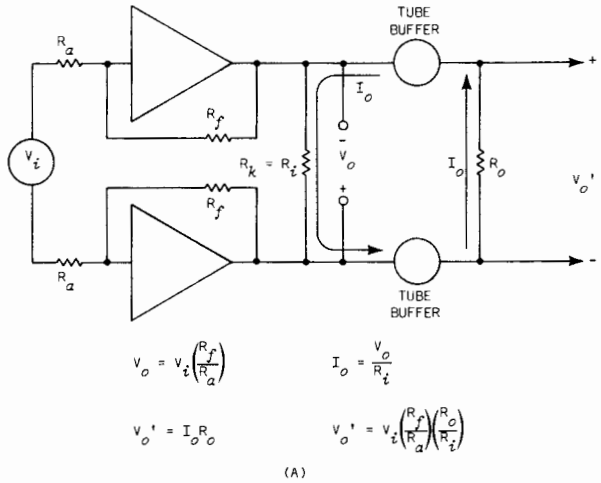
eliminating *gm* as a circuit parameter

Including V1 and V2 in the circuit reduces the voltage required across Q3 and Q4. Connecting the circuit as shown virtually eliminates V1 and V2 *gm* as a circuit parameter.

R_f/R_a times the applied voltage describes the voltage across R27. V1 and V2 cathode currents develop this voltage then flow through R28 and R29 developing voltage drive to the driver amplifier. Q3 and Q4 have sufficient gain that tube *gm* has little to do with the voltage across R27 or I_k.

V1-V2 gain is R_O/R_i. R28 and R29 is R_O and, since $A_{O\ell}$ eliminates r_k (gm), R_k alone is R_i. Although these two amplifiers interlock, they are in cascade. Fig. 7-20 suggests two methods of symbolizing this type amplification.

Whether you prefer Fig. 7-20A or Fig. 7-20B, the fedback amplifier voltage gain creates a current which flows through R_O. This current and resistance develop the ultimate output voltage.



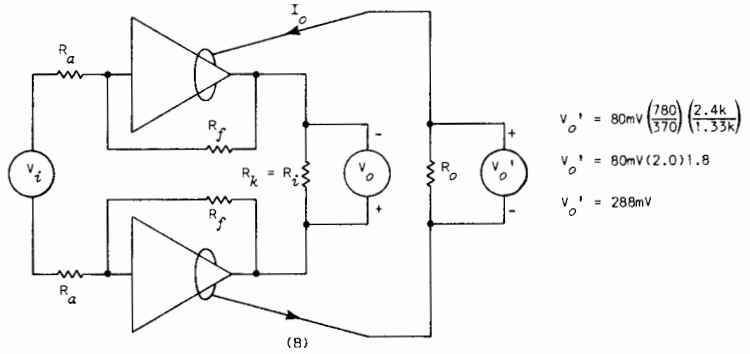


Fig. 7-20. Suggested symbols for including the triode buffers.

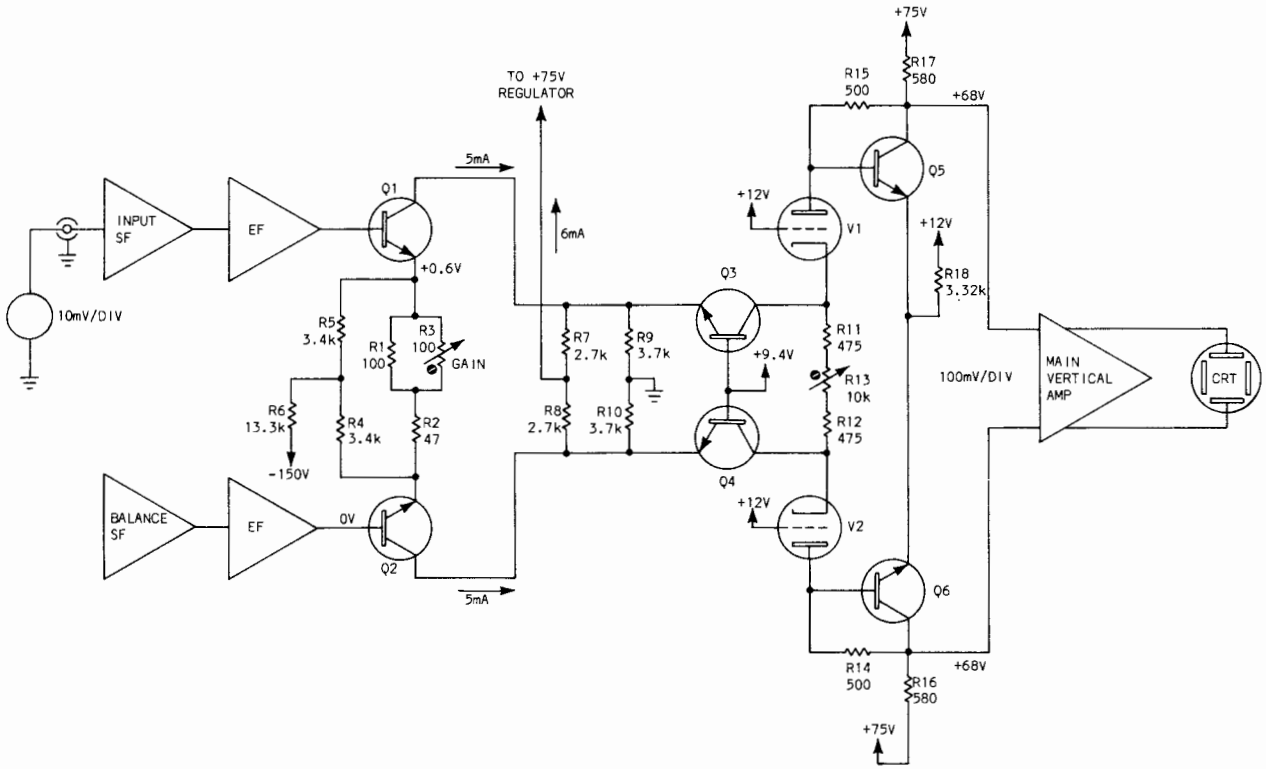


Fig. 7-21. Cascoded preamplifier.

Tube parameters can be significant. Fig. 7-21 is an example of a circuit which might leave explanatory gaps if one fails to consider r_k of grounded-grid amplifiers.

One way to begin an amplifier analysis is to first determine where signal grounds develop. Imagine how this might apply to Fig. 7-21:

> The apparent ground at the base of Q2 causes a virtual ground to develop at the emitter. Virtual ground also appears at the collector since the collector is common to the emitter of Q4.
>
> Q4 emitter and base operate at ground as does Q3.
>
> Q3 emitter and Q1 collector are common; therefore, a ground appears at the collector of Q1.
>
> V1 and V2 grids return to apparent ground; therefore, the cathodes also operate at ground. This is the error -- ignoring r_k of V1 and V2. Continuing the original reasoning, the plates tie to the input terminal of an inverting fedback amplifier and, therefore, operate at virtual ground.

Using this reasoning, voltage changes can be approximated and measured only at the base of Q1, the emitter of Q1, and the collectors of Q5 and Q6. Therefore, signal currents generated in the emitters of Q1-Q2 develop output voltage across R14 and R15. $A_V = \frac{(R14 + R15)}{R_a}$. This sounds acceptable.

It even sounds better when you consider the gain required and impedance estimates:

$A_V = \frac{DF_{out}}{DF_{in}} = \frac{100}{10} = 10.$

$R_f = R14 + R15 = 1000\ \Omega.$

R_a is assumed to equal $R_E + R_t$.

R_E is R2 in series with the parallel value of R1 and R3, 80 Ω.

If one adds about 10 Ω for R_t:

$$A_V = R_f/R_a = 1000/90 \simeq 11.$$

This could easily be rationalized into a good answer -- until someone asks: What do R13 adjustments achieve?

R13 shunts signal current only because of r_k of V1 and V2. Fig. 7-22 shows the percentage of shunting affected by R13 adjustments. The current that flows through r_{k1} and r_{k2} also flows through R14 and R15.

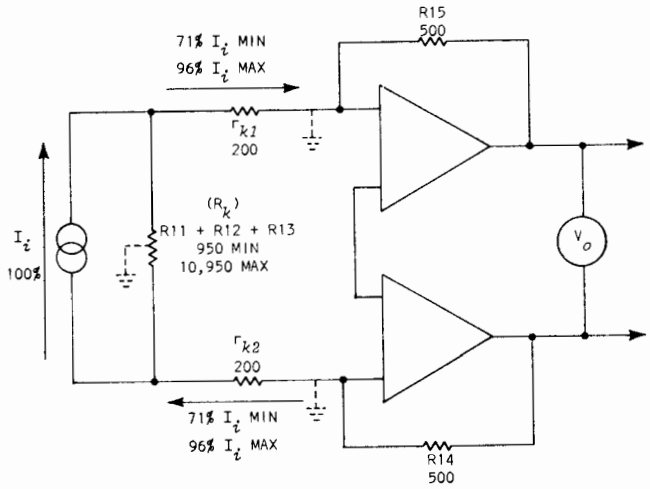
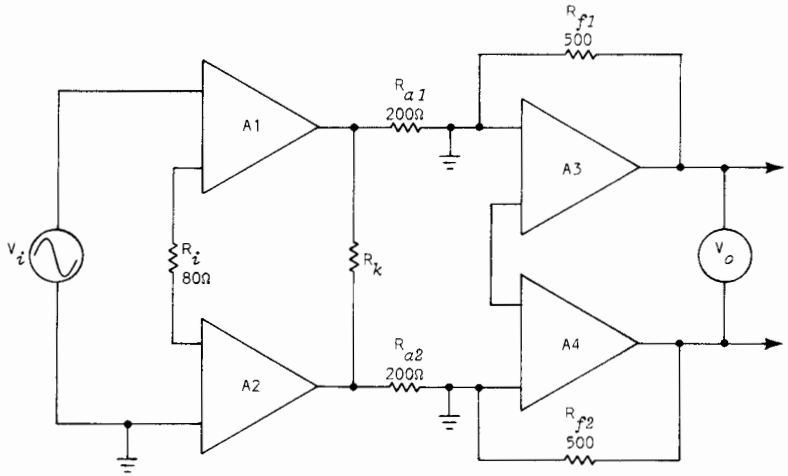


Fig. 7-22. R_k shunts r_k.

See Fig. 7-23. Consider this a fedback amplifier cascaded with a phase inverter. R_f is R14 and R15, and R_a is r_{k1} and r_{k2}. R_o is R_k shunted by r_{k1} and r_{k2} and R_i is Q1-Q2 emitter-coupling resistance. This figure shows gain variations as a result of changing R_k.

Fig. 7-21 included a gain adjustment between the emitters of Q1 and Q2. This allows gain balancing when more than one phase inverter drives grounded-base amplifiers Q3 and Q4.



$$A_V = \frac{R_o}{R_i} = \frac{R_k \quad R_{a1} + R_{a2}}{R_i} \qquad A_V = \frac{R_{f1} + R_{f2}}{R_{a1} + R_{a2}} = \frac{1000}{400}$$

A_V MAX $= \frac{386\Omega}{80\Omega} = 4.8$ WHEN $R_k = 10{,}950$ $\qquad A_V = 2.5$

A_V MIN $= \frac{280\Omega}{80\Omega} = 3.5$ WHEN $R_k = 950$

SO

$$\frac{V_o}{V_i} = 2.5(4.8) = 12 \text{ MAX OR } 2.5(3.5) = 8.8 \text{ MIN}$$

Fig. 7-23. Maximum and minimum gain estimates considering R_k.

Fig. 7-24 shows a possible switching arrangement. Q3 and Q4 emitters present such low impedance that inserting switches at this point degrades performance very little. R13 now provides an overall gain calibration. Each phase inverter contains an adjustment for matching channel gain.

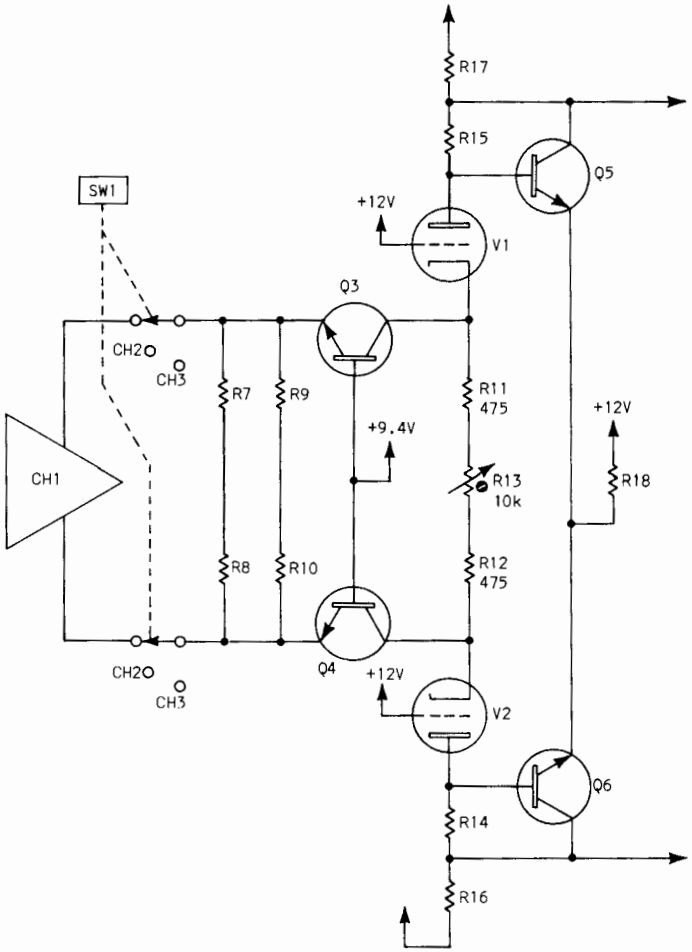


Fig. 7-24. Switching channels at a low impedance point.

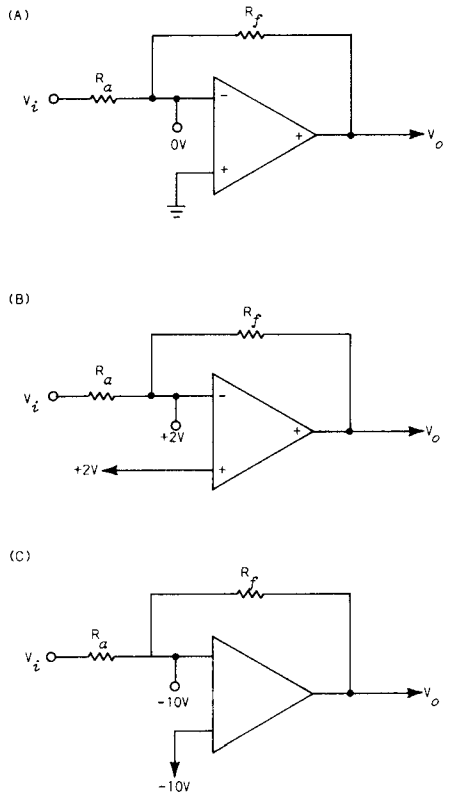


Fig. 7-25. Amplifiers seek a null between input terminals.

The introductory presentation on fedback amplifiers pointed out input terminal null-seeking characteristics of fedback amplifiers. (-) input terminals assumed the voltage at (+) input terminals. (+) input terminals functioned as reference voltage points.

See Fig. 7-25. Sections A, B and C of this figure show three inverting fedback amplifiers. Each (-) input terminal seeks the (+) input terminal voltage:

(A) Input (+) grounded. Feedback currents through R_f-R_a develop 0 volts at the (-) input terminal.

(B) Raising (+) input to +2 V causes feedback currents to develop +2 V at the (-) input terminal.

(C) (-) input terminal assumes the negative level applied to the (+) input terminal.

Inverting fedback amplifiers (+) input terminal returns to a fixed reference voltage. However, it appears that changing (+) input terminal voltage should cause changing feedback currents. If feedback currents change, then output voltage must change. This is the basis of *noninverting* fedback amplifiers.

noninverting fedback amplifiers

Fig. 7-26 symbolizes the amplifiers of Fig. 7-25 as noninverting fedback amplifiers. R_a returns to ground. V_i appears at the (+) input terminal. Current through feedback devices R_a and R_f maintains a null across the input terminals. Output voltage amplitude results from the product of null-seeking current and feedback devices. Output voltage and input voltage are in phase.

$\frac{R_f + R_a}{R_a}$ expresses noninverting fedback amplifier gain.

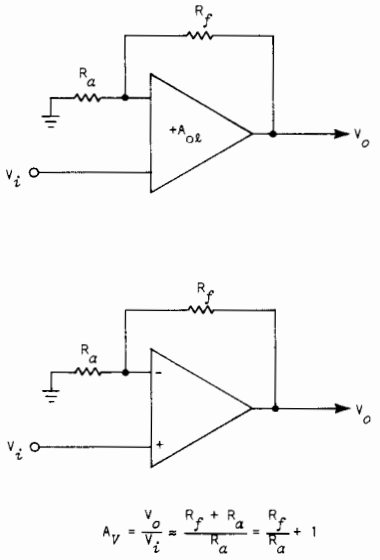


Fig. 7-26. Noninverting amplifier symbols.

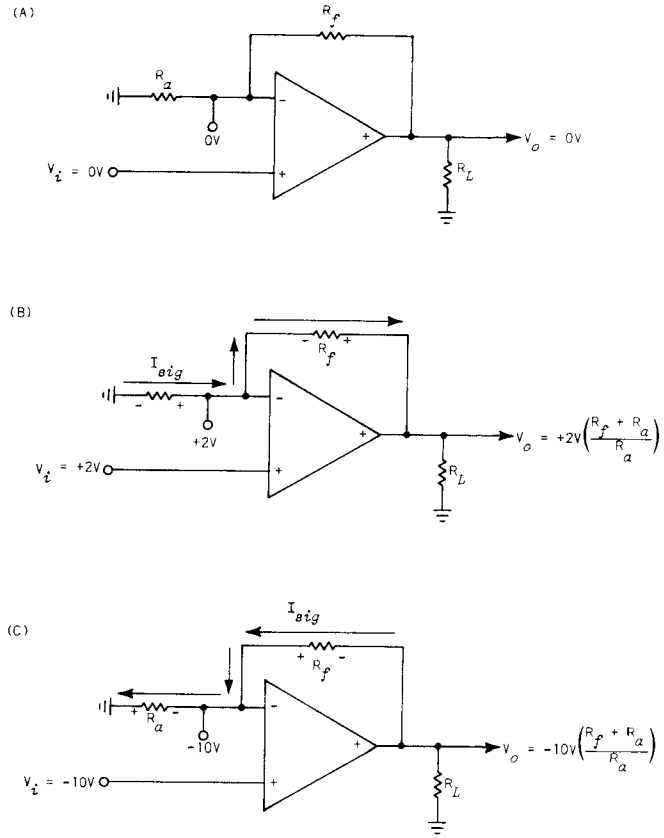


Fig. 7-27. Null seeking.

See Fig. 7-27. Sections A, B and C show current direction in terms of electron flow; polarity of voltage drops; input voltage amplitudes; and output voltage amplitude, as input voltage times voltage gain. These illustrations also include R_L returned to ground. This indicates that output voltage amplitudes refer to ground as do input voltages.

Fig. 7-27B shows feedback current through R_a and R_f, developing a positive output voltage as a result of positive input voltage.

Sufficient current must flow through R_a to drop 2 volts. This same quantity of current must flow through R_f. Output voltage develops as a result of feedback current through R_f *and* R_a. Therefore, expressing voltage gain as a resistance ratio, one must include both R_f and R_a in the dividend. V_i across R_a alone determines the quantity of feedback current. R_a alone acts as divisor.

Fig. 7-27C shows current flow resulting from a negative input voltage. Input voltage across R_a generates feedback current. Feedback current through both R_f and R_a establishes output voltage amplitude.

All gain expressions assume high open-loop gain. $A_{O\ell}$ affects noninverting fedback amplifiers in the same fashion as inverting fedback amplifiers.

Fig. 7-28 illustrates three methods of symbolizing noninverting fedback amplifiers.

circuit symbols

The first symbol indicates noninversion by including polarity signs within the triangle. Both V_O and V_i appear at (+) terminals.

$+A_{O\ell}$ within the next triangle indicates no phase inversion. This symbolization assumes junction R_a-R_f always connects to the (-) input terminal.

Illustrators using the last symbol depend upon several observer assumptions:

1. All three-terminal symbols indicate noninversion.
2. Input terminals always appear at triangle bases.
3. Feedback always connects from output to (-) input terminals via R_f.
4. R_a is the only component remaining, therefore needs no label.

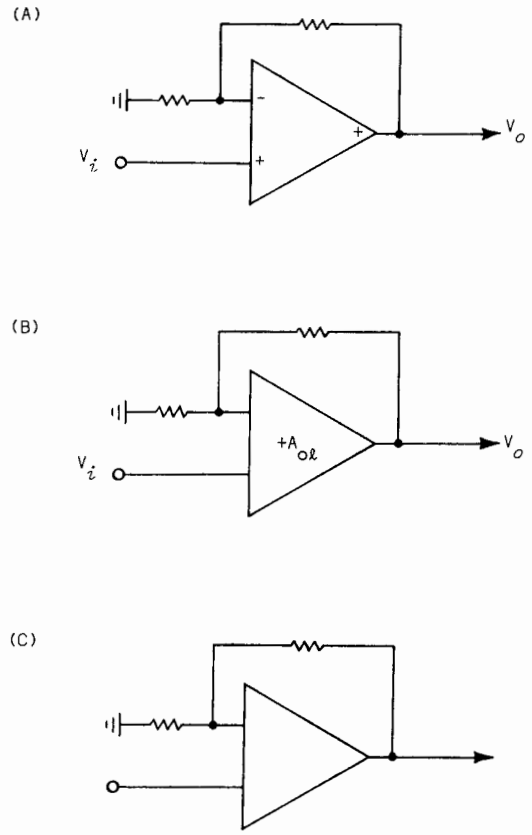


Fig. 7-28. Reducing the markings.

Previous chapters contained circuits with feedback, a longtailed follower the most common. Fig. 7-29A shows a symbolic noninverting fedback amplifier. Fig. 7-29B illustrates an emitter follower analyzed as a noninverting fedback amplifier. Fig. 7-29C shows an amplifier whose gain can exceed unity. In this circuit varying or switching values of R_a control gain. Low impedance at R_a-R_f junction and R_a returned to ground makes switching R_a practical. Minimum gain (unity) results with an infinite value of R_a. Maximum *theoretical* gain occurs when R_a is zero. For stabilized amplification R_a must have some value larger than zero ohms.

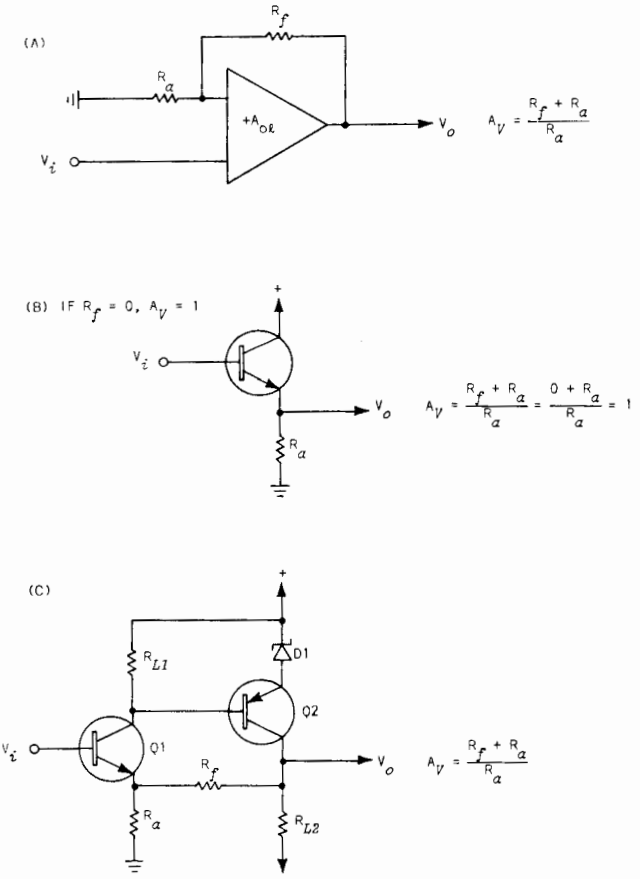


Fig. 7-29. Symbols and circuits.

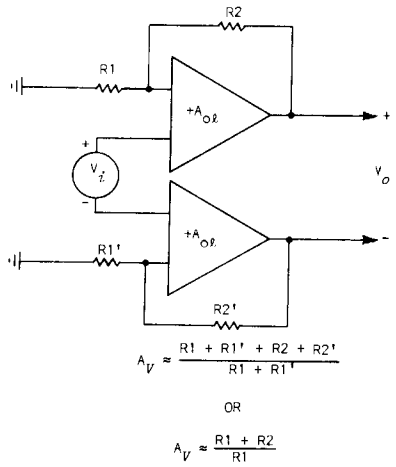


Fig. 7-30. Differential, noninverting fedback amplifier.

differential amplifier

Like inverting fedback amplifiers, noninverting fedback amplifiers appear in many circuit configurations. Fig. 7-30 shows the symbolic circuitry of a differential amplifier.

The blocked circuit in Fig. 7-31 depicts a noninverting fedback amplifier. Assuming a very high $A_{O\ell}$, the ratio of passive devices alone determines voltage gain with feedback. $+A_{O\ell}$ indicates in-phase signals at input, output and, necessarily, at the feedback component junction. Since in-phase currents flow through R_f and R_a, R_a becomes an extension of R_f. Therefore, the voltage gain formula includes the sum of R_f and R_a.

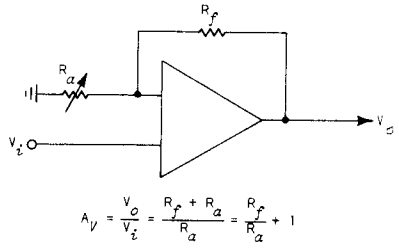
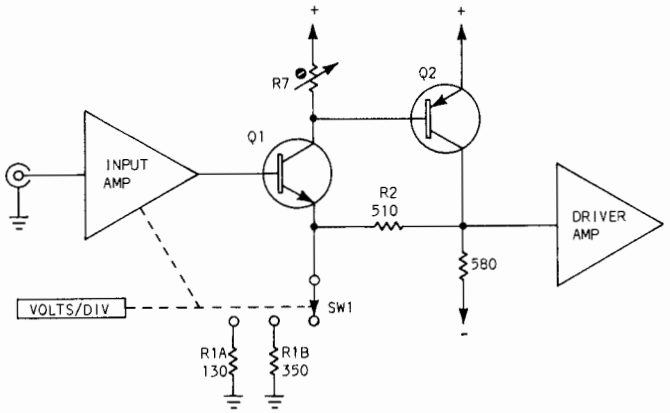


Fig. 7-31. Gain adjustment.



$$(1)\quad A_V = \frac{R_f + R_a}{R_a}$$

$$(2)\quad A_V = \frac{R2 + \infty}{\infty} \approx 1.0$$

$$(3)\quad A_V = \frac{R2 + R1A}{R1A} = \frac{860}{350} \approx 2.5$$

$$(4)\quad A_V = \frac{R2 + R1B}{R1B} = \frac{640}{130} \approx 5.0$$

Fig. 7-32. Gain selector.

Fig. 7-31 shows R_f a fixed value and R_a a variable.

variable-gain amplifier

Placing R_a to zero ohms results in an infinite voltage gain (restricted to $A_{O\ell}$). Adjusting R_a to maximum resistance results in minimum (unity) gain.

switched-gain amplifier

A switched-gain amplifier substitutes precision resistors for a variable R_a as shown in Fig. 7-32.

Changing the basic deflection factor of a vertical system in calibrated steps, coordinated with the VOLTS PER DIVISION selector, reduces the number of attenuator networks at the input.

Q1-Q2 make up a fedback amplifier whose gain is X1, X2.5 or X5. Gain is switch selectable, ganged to the VOLTS/DIV switch. R2 and the component selected by SW1 determine gain.

Since the signal at the base of Q1 and the collector of Q2 are in phase, the feedback resistance is summed with R_a, the selectable Q1 emitter resistor. The simple gain formula now applies.

$$A_V = \frac{R_f + R_a}{R_a}$$

Formula 2 has values for SW1 positioned as shown. Formula 3 has values for RIB switched in. Formula 4 has values for RIA switched in.

Properly biased, the emitter of Q1 sets at zero volts. Switching SW1 through its range causes no vertical trace displacement.

R7 is made adjustable, not so much for open-loop gain as control of Q2 operating point. R7 would be set for minimal loading effects of the following stage.

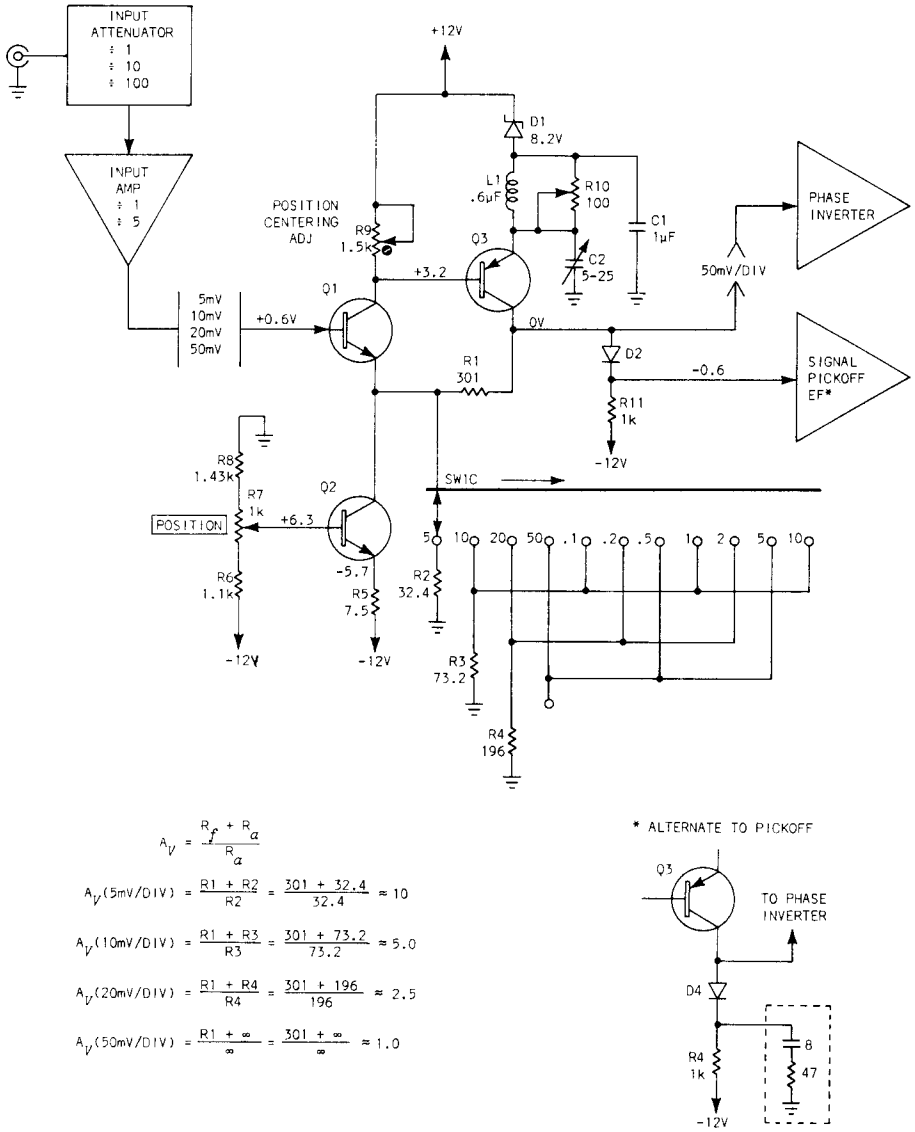


Fig. 7-33. Complex gain selection.

Fig. 7-33 shows a more complex switched-gain amplifier. A voltage gain of 1, 2.5, 5 or 10 results from switch selecting values of R_a. Mechanically ganged (with the input amplifier and input attenuator) to the VOLTS/DIV selector, this amplifier gain selection maintains a constant output deflection factor.

Resulting from input attenuator and input amplifier action, drive to Q1 represents four deflection factors: 5 millivolts, 10 millivolts, 20 millivolts and 50 millivolts per division. Proper gain selection gives output, from the selected gain amplifier, at one deflection factor: 50 millivolts per division.

Selecting R_a via SW1C sets stage gain. R1 represents R_f and remains fixed. R2, R3, R4 or an open circuit represents R_a. Gain formula included in Fig. 7-33 and SW1C labeled in deflection factor terms illustrates gain switching logic.

Fig. 7-33 illustrates no high-frequency compensation associated with SW1C or R_a. These compensating networks must occur in practical circuitry.

Q1, a longtailed common-emitter amplifier, receives drive, including DC operating level, from the input amplifier. Zero volts at Q1's emitter allows smooth gain switching since no potential exists across R_a. Longtailing device Q2 generates total collector current for Q1. Q2 base voltage determines the amount of current thus the drop across R9, so R7 becomes a POSITION control. Q1 quiescent collector voltage establishes Q3 base voltage. Named POSITION CENTER adjustment, R9, with the POSITION control centered and no signal in, is used to vertically center the CRT display.

Zener diode D1, in Q3's emitter, provides the demand for an adjustable R9. Zener diodes do not regulate at precisely the same voltage, even those of the same type and manufacture. Emitter-base voltage establishes current demand. Correct collector current, for Q3, develops a zero-volt, center-screen, collector voltage. Adjusting R9 corrects for changes in Q3 emitter voltage. Such a change might result from replacing D1.

C1, C2, L1 and R10, also in the emitter circuit of Q3, provide filtration and high-frequency compensation. C1 bypasses the noise associated with zener diodes. Network C2-R10-L1 constitutes emitter peaking, assuring high A_{ol} over a broad spectrum. R11-D2 return the collector of Q3 to a negative supply. D2 merely allows signal pick-off emitter follower drive to operate one silicon junction below the main signal level.

Many vertical preamplifiers incorporate two identical channels. To remain identical each channel must be equally loaded. Frequently only one channel provides signal pick-off and the other must be balanced. As an example, the lower right of Fig. 7-33 shows a load equivalent to the signal pick-off shunting R11.

Resistances and gain computations used reflect practical values. Input deflection factors do not. The voltages were chosen to easily associate to an input attenuator switch position. Reducing both input and output deflection factors by 20% approaches reality.

The section discussing inverting fedback amplifiers included circuits that incorporated active isolation devices. These devices performed two basic functions:

1. To isolate the fedback amplifier from following circuit loading to preserve A_{ol}.
2. To act as a voltage buffer utilizing reaction current generated by the fedback amplifier to develop output voltage across a remote load.

Noninverting fedback amplifiers utilize active device buffers in the same manner.

Fig. 7-34 shows a noninverting fedback amplifier isolated from output voltage fluctuations by a buffer. This amplifier seeks a null across the input terminals. V_i causes current flow through R_a to maintain the null. Current, resulting from feedback action, flows through R_a, R_f, the buffer and R_o. Output voltage signals develop across R_o.

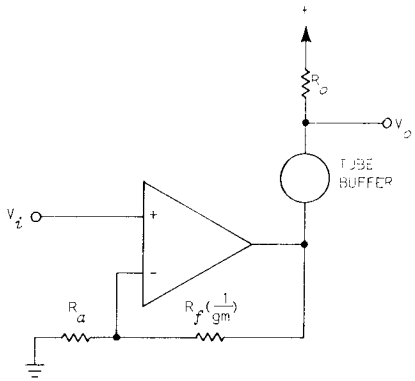


Fig. 7-34. Symbol possibility I.

Ratio R_O to R_a expresses voltage gain from the input terminal to R_O. This circuit nullifies the effects of changing active device parameters. Current through R_a determines gain. Input voltage across R develops the current that flows through R_O less screen grid losses, if any. An incidental voltage develops across R_a and R_f. Therefore, a changing tube transconductance has little effect upon circuit performance.

Fig. 7-35 illustrates a simplified schematic of the symbolic block in Fig. 7-34. (Remember to modify R_O/R_a for pentode eta.)

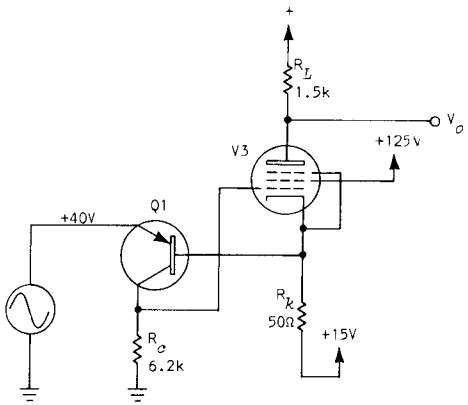


Fig. 7-35. Eliminating *gm* as a parameter.

Q1 emitter functions as the positive input terminal. Null seeking occurs between the (+) input terminal and the (-) input terminal at Q1's base. R_k is R_a. V3 acts as a tube-buffer whose r_k is R_f. Currents generated in R_k (R_a), less screen grid losses, flows through R_O to develop output voltage.

The circuit in Fig. 7-35 maintains a constant voltage across Q1's base-emitter junction. Input voltage changes at the emitter cause voltage changes across R_a. Collector voltage changes at V3's control grid, change cathode current. Cathode current through R_k develops nulling voltage at the base of Q1. 75% to 90% of cathode current flows as plate current, output voltage across R_L results.

Passive devices determine the quantity of cathode current. Cathode current through R_k, a passive device, develops null voltage at the base of Q1. V3 transconductance determines Q1 collector signal amplitude necessary to develop sufficient cathode current changes. A relatively large R_a develops open-loop gain high enough to cover wide *gm* variations.

Fig. 7-36 illustrates "reaction current" symbolization of the circuit in Fig. 7-35. An output current develops as a *reaction* to the fedback amplifier *action*. This "reaction" output current through R_O develops V_O.

output amplifier

Fig. 7-37 shows the complete circuit. V1 and V2 receive push-pull signals at 288 millivolts per division deflection factor. The circuit amplifies to apply 10 volts per division CRT deflection.

Unity gain develops from the grids of V1 and V2 to the cathodes of V3 and V4. Common-base amplifiers Q1 and Q2 receive signal voltages from cathode followers V1 and V2. Cathode followers V1 and V2 isolate the driver amplifier from the low input impedance of Q1 and Q2. Q1 and Q2 collector signals appear at V3 and V4 control grids. These signals cause V3 and V4 cathode voltage to equal Q1 and Q2 emitter voltage. About 80% of the current required to develop feedback voltage flows as V3 and V4 plate current.

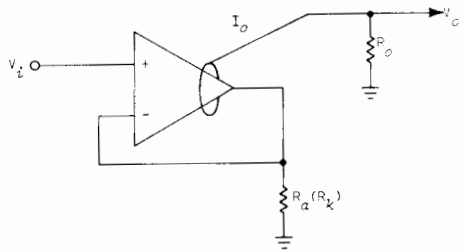


Fig. 7-36. Symbol possibility II.

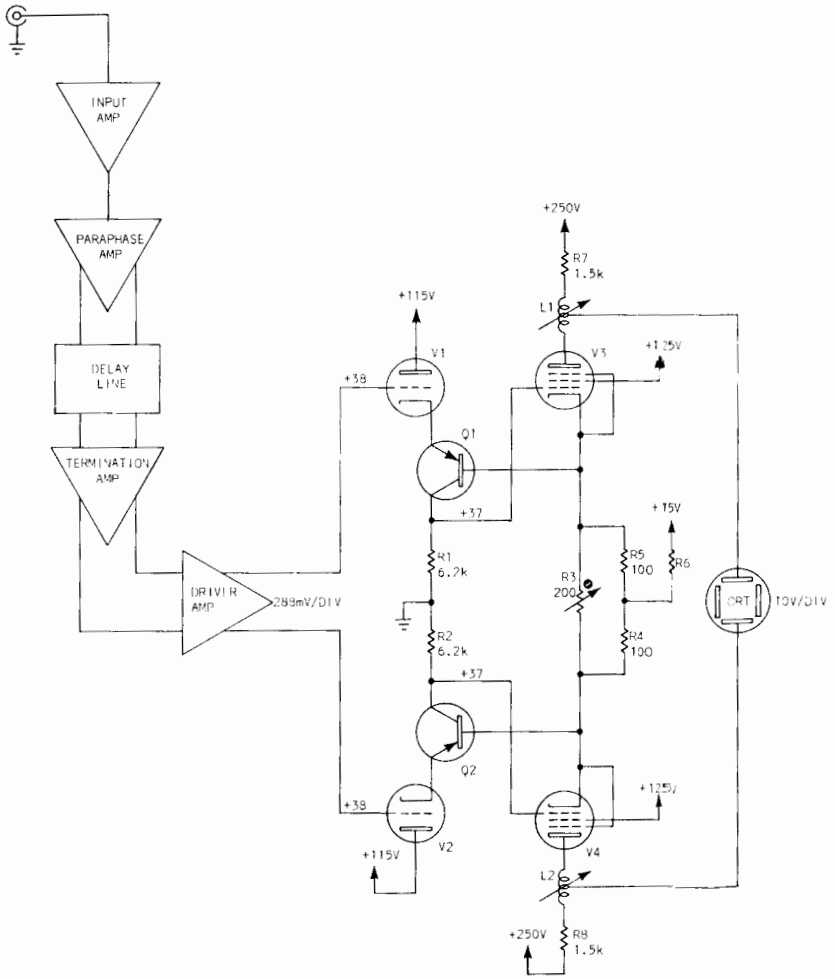


Fig. 7-37. Eliminating *gm* as a parameter.

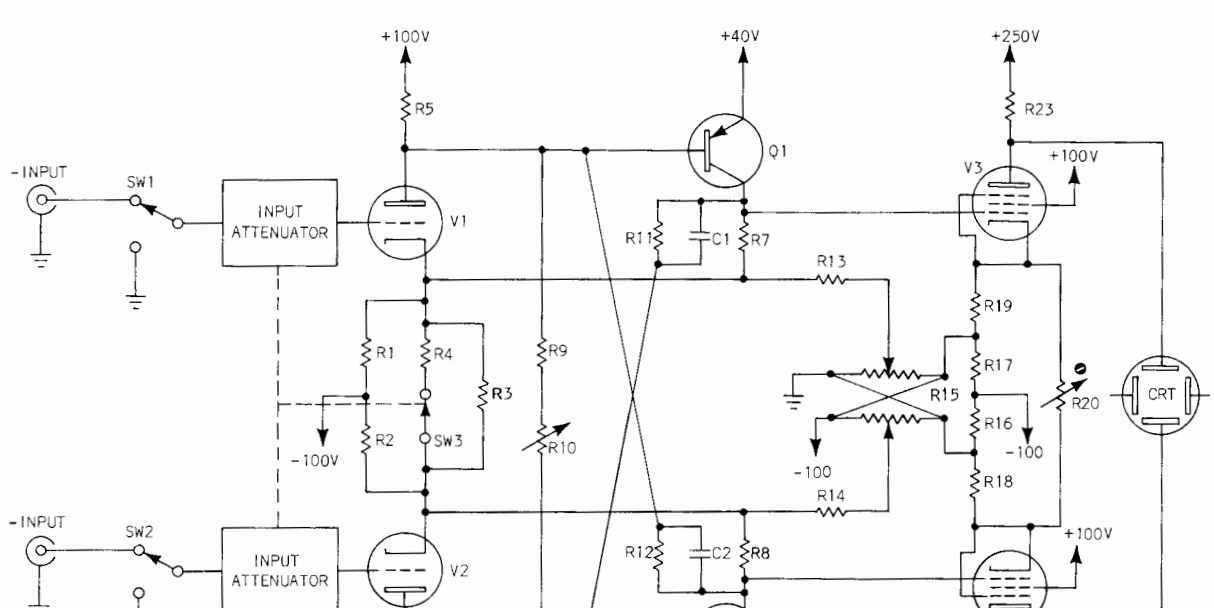


Fig. 7-38. Feedback in the differential.

Some fedback amplifiers appear forbidding because of the many circuit alternatives. Usually the alternatives can be reduced by confirming known or familiar configurations. Fig. 7-38 is an example of a circuit which can be confusing.

differential amplifier

Almost the entire circuit in Fig. 7-38 resolves to fedback symbolization. But even the symbolization becomes complicated by selecting inputs. Input selectors SW1 and SW2 allow this vertical amplifier to monitor the (-) input or the (+) input. One may also monitor both inputs, developing differential CRT deflection. At maximum calibrated gain, one millivolt input signal deflects one CRT vertical division. The CRT requires 20 volts for each vertical division.

Consider first the output stage. Output amplifiers V3 and V4 provide:

1. Final voltage gain for CRT deflection.
2. Gain adjustment for overall gain calibration.
3. Feedback currents for positional information to the input amplifiers.

Signal voltage, applied to the grids of V3 and V4, develops across R_i found in V3 and V4 cathode circuitry. R_i consists of r_k of V3, R20 and r_k of V4. Input voltage across R_i generates signal cathode currents. These currents, less screen-grid losses, develop output signal voltages across R22 and R23.

Refer now to Fig. 7-39. The cathode of V3 returns to a negative supply through R19 and R17 paralleled by R15. V4 cathode returns through R18 and R16 paralleled by R15. Under balanced circuit conditions equal voltages appear at either end of R20.

Centering POSITION control R15 balances the circuit. Equal cathode and plate currents flow. Equal voltages develop across R22 and R23. These voltages applied to the vertical CRT plates center the display.

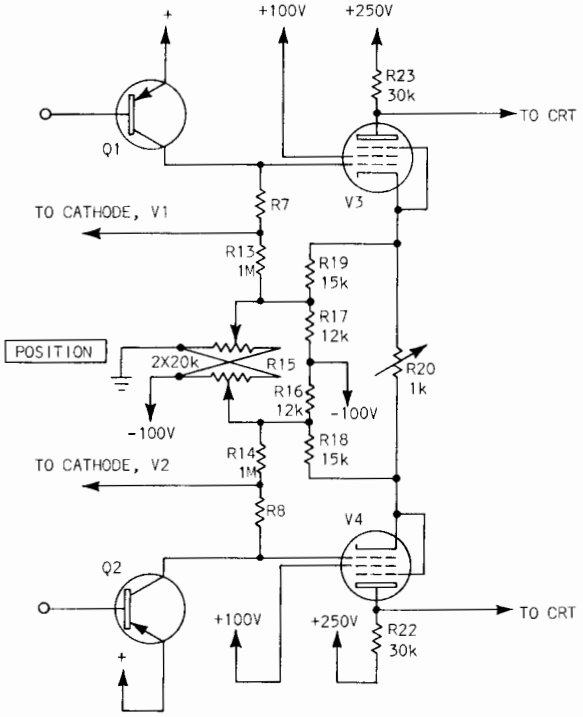


Fig. 7-39. Output amplifier.

Moving R15 off center unbalances plate current, deflecting the CRT display off center. Moving R15 left decreases V3 cathode current and increases V4 cathode current. Increasing the drop across R23 and decreasing the drop across R22 deflects CRT displays upward. Moving R15 right of center increases V4 cathode current, decreases V3 cathode current thus deflecting CRT displays downward.

Since positional currents do not flow through R20, R20 could function as a VARIABLE volts per division control. As such, actuating R20 changes displayed signal amplitude but not position. This only happens when V3 and V4 cathode voltages equal at all settings of R15.

Including R15 wiper voltages in the input amplifier feedback loop maintains V3 and V4 cathode voltages constant. R13 and R14 connect positional voltages to the feedback loop. To positional voltages the amplifier responds as an inverting fedback amplifier. Position of R15 determines V3 and V4 cathode current. R15 wiper voltage, inverted and proportioned, appears at V3 and V4 control grids to maintain cathode *voltages* equally constant. R15 wiper voltage multiplied by the R_f to R_a ratio expresses control grid positional voltage amplitude.

$$\frac{R_f}{R_a} = \frac{R13}{R7} = \frac{R14}{R8}.$$

Consider signal degeneration imposed by vertical position feedback circuit as incidental. Signal currents flow in feedback networks R13-R7 and R14-R8 developing voltages that subtract from control grid signal voltages. However, degenerative voltages are small and of constant proportion. Generous gain calibration range, R20, negates these degenerative effects.

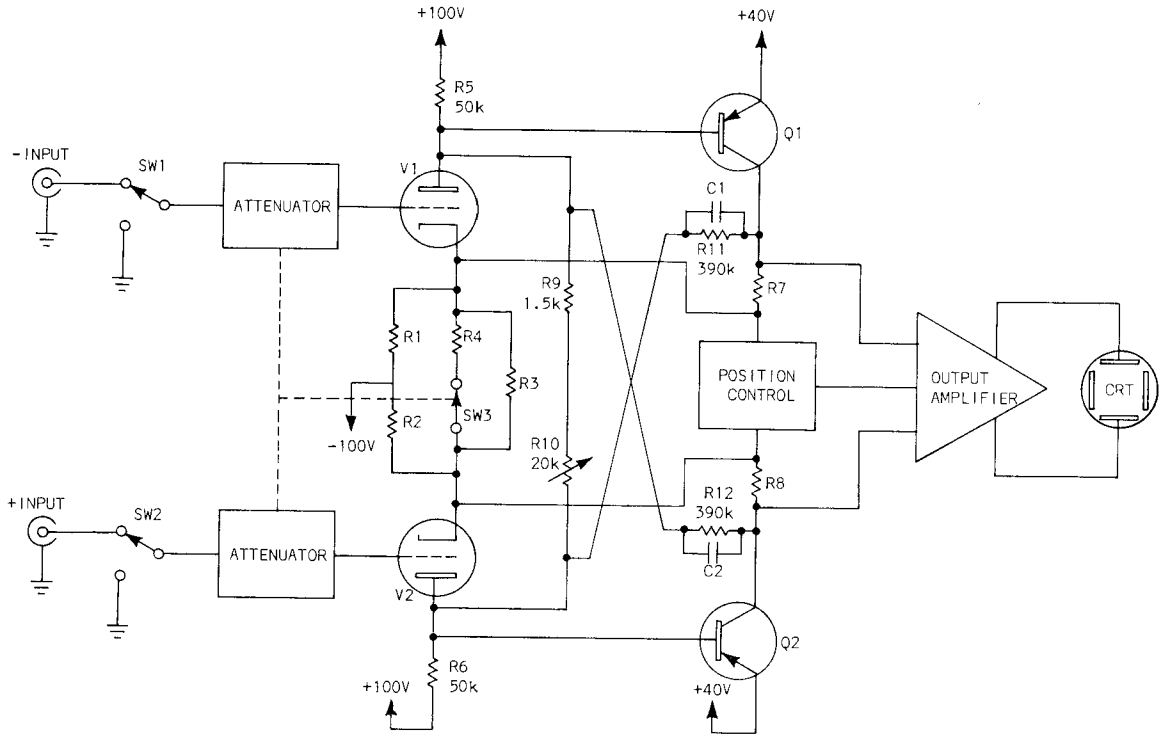


Fig. 7-40. Vertical amplifier simplified I.

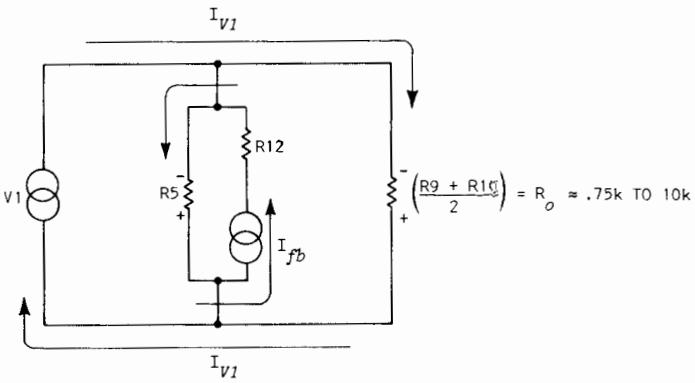


Fig. 7-41. Feedback currents increase R_o.

simplified input amplifier

This allows the simplification shown in Fig. 7-40. Further simplification is possible. Recall that open-loop gain should be high -- but not necessarily stable. Degenerative feedback provides the stability. R11 and R12 apply *regenerative* feedback to maintain $A_{o\ell}$ high.

C1 and C2 are neutralization capacitors, cancelling Q1-Q2 degeneration due to "Miller-effect."

V1 and V2 conduction, at rest, drops a voltage across R5 and R6. R11 and R12 cancel shunting effects of R5 and R6, allowing R9 + R10 to represent R_o for V1 and V2. Consider just one side of the amplifier: V1, R5, one-half of R9 + R10, and R12, as shown in Fig. 7-41. V1 generates plate current to develop output voltages. Output voltage amplitude depends upon resistance encountered in the plate circuit. R5 shunts R_o and without additional circuitry provides an additional plate current path. Regenerative feedback current via R12, however, equals the R5 current requirement. V1 signal current now flows only through R9-R10 which then defines R_o.

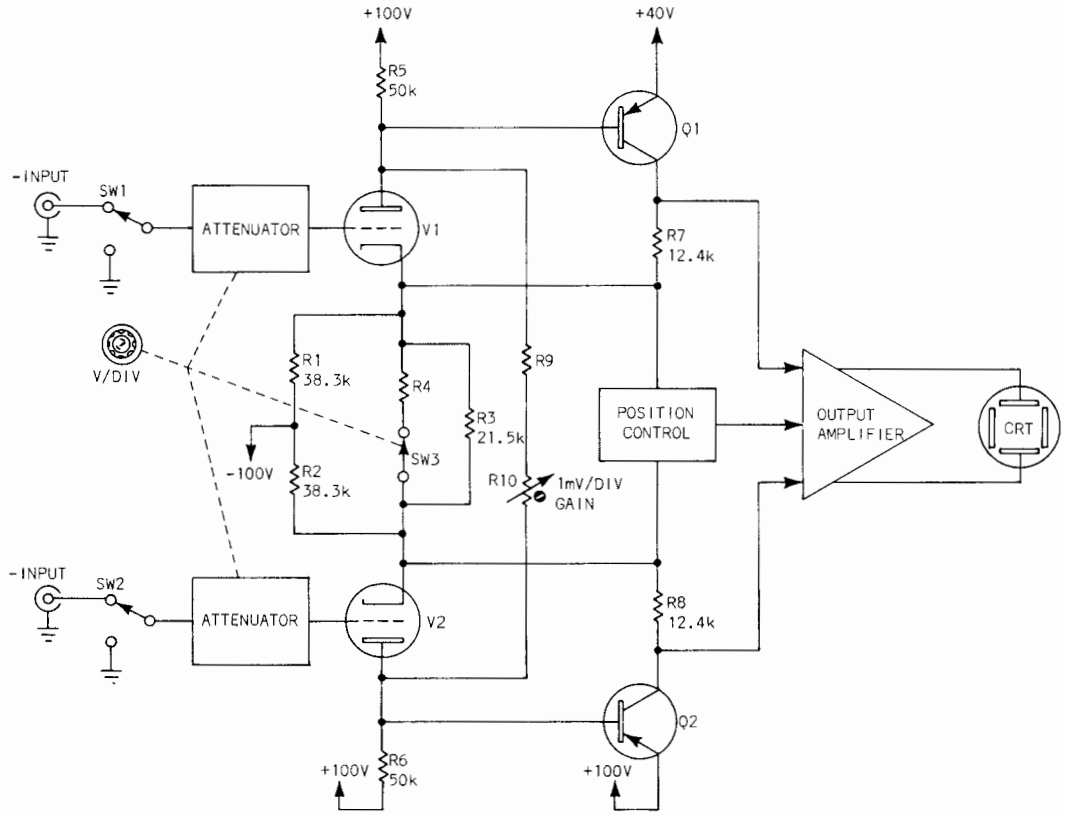


Fig. 7-42. Vertical amplifier simplified II.

Fig. 7-42 shows a simplified version of the input amplifier. Input signals appear at the grids of V1 or V2 or both via the attenuators. V1 and V2 cathode coupling mechanically gangs to the input attenuators. This reduces the number of attenuator components thereby reducing calibration balancing problems. Resistors R1, R2, R3 and R4 affect cathode coupling. R4 is shown as one resistor. Selecting a deflection factor changes R4 resistance in conjuction with the input attenuators. Plate load resistors R9 and R10 develop open-loop gain. Output amplifier drive develops at the collectors of Q1 and Q2. R7, R8 and cathode-coupling resistance make up passive feedback devices controlling gain.

Input attenuators voltage-divide in three increments: X1, X10, X100. The operator may select an input deflection factor between 1 millivolt per division and 20 volts per division in stepped sequence. Input attenuators and R4 resistance steps as listed below.

DEFLECTION FACTOR	RESISTANCE R4	INPUT ATTENUATION
1 mV/div	49.9 Ω	X1
2 mV/div	101.0 Ω	X1
5 mV/div	256.0 Ω	X1
10 mV/div	526.0 Ω	X1
20 mV/div	1.11 kΩ	X1
50 mV/div	3.33 kΩ	X1
.1 V/div	10.0 kΩ	X1
.2 V/div*	Open*	X1*
.5 V/div	1.11 kΩ	X10
1 V/div	10.0 kΩ	X10
2 V/div	Open	X10
5 V/div	1.11 kΩ	X100
10 V/div	10.0 kΩ	X100
20 V/div	Open	X100

*Selecting 200 millivolts per division deflection factor sets circuit description conditions. Input attenuators are "straight through" and R4 is open. V1 and V2 cathode coupling resolves to R3 paralleled by longtail resistors R1 and R2: 17 kΩ. R_a is R_k. R_{f1} is R7. R_{f2} is R8. The amplifier functions as a differential developing voltage gain of about 2.5.

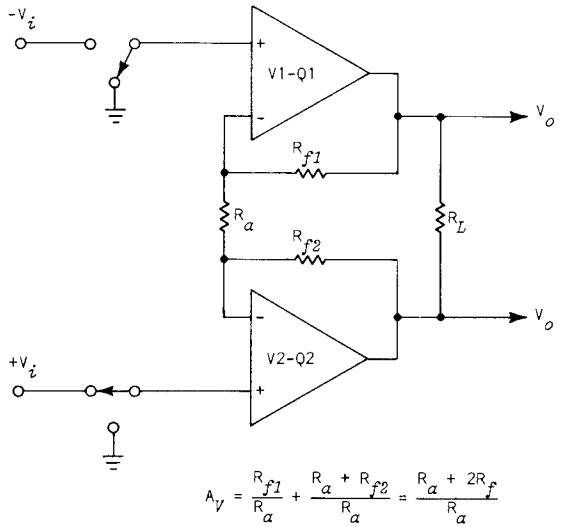


Fig. 7-43. Paraphase mode.

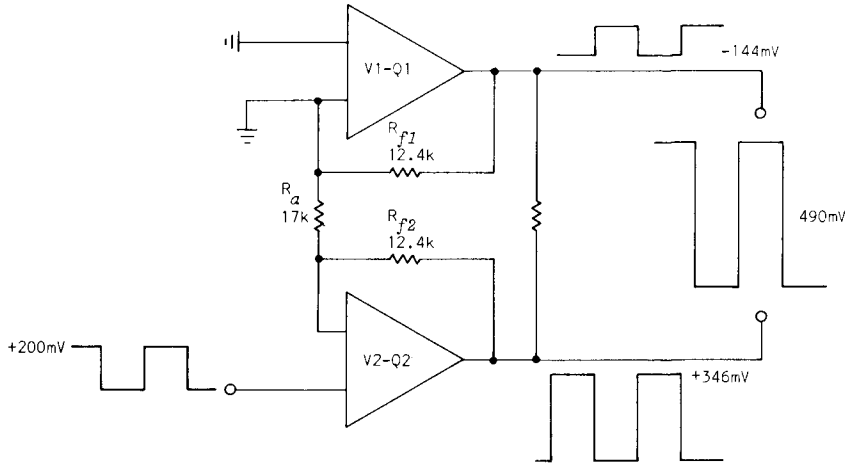
paraphase

V1-Q1 and V2-Q2 can now be represented by two triangles controlled by feedback. The configuration remains the same during any of the operating modes. Assume 0 volts at the (-) input, or SW1 positioned to ground. Fig. 7-43 represents this mode.

Amplifiers attempt to maintain an input terminal null. Feedback enhances this capability. Thus signal ground develops at the (-) input of V1-Q1 and signal voltage at the (-) input of V2-Q2. V1-Q1 performs as an inverting fedback amplifier while V2-Q2 is the noninverting type. Locating virtual ground helps define amplifier action. Fig. 7-44 depicts gain. Notice the imbalance between the output of V1-Q1 and V2-Q2. This is typical of this configuration.

differential

Applying balanced signals shifts ground to the center of R_a (Fig. 7-45). Although total gain remains the same, it becomes symmetrical. Both V1-Q1 and V2-Q2 perform as noninverting fedback amplifiers of equal gain. Signal drive determines the degree of amplifier balance or position of virtual ground along R_a. This



$$A_V = \frac{24.8 + 17}{17} \approx 2.46$$

$$A_V = V_i\ (A_V) \approx .2 \times 2.46 \approx .492$$

Fig. 7-44. Paraphase gain.

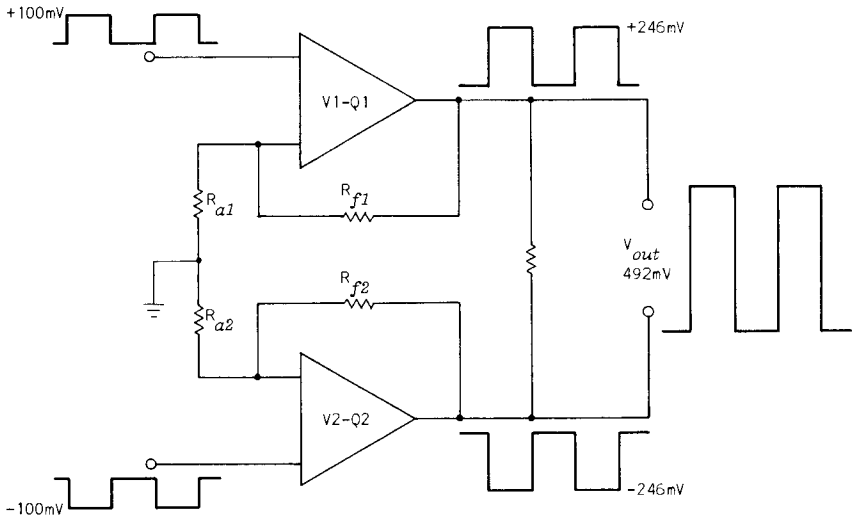


Fig. 7-45. Differential mode.

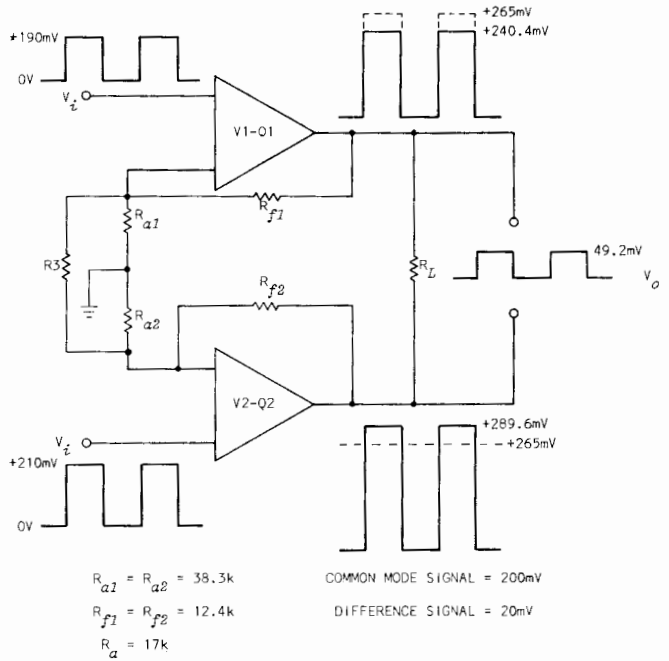


Fig. 7-46. Including a common mode component.

common-mode

is true for common-mode signals as well. Refer to Fig. 7-46.

200 mV is the average (common-mode) signal applied, 20 mV the difference. The difference signal causes virtual ground to develop halfway along the coupling component, as shown before. R_a is R3 shunted by the longtail resistors. Common-mode signals demand equal phase and amplitude currents through R_a. Current now originates at apparent ground, the power supply. Longtail components become R_a for each amplifier.

Difference and common-mode voltages, of each amplifier, algebraically add to develop the output waveform.

Voltage gain estimates of any amplifier become simple once gain determinates are identified. These in turn are frequently easy to recognize once signal grounds are located. Actual and apparent grounds present few identification problems. By assuming the amplifier seeks a null between input terminals, actual or apparent ground location frequently leads to virtual ground location.

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