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Gain and Offset Mismatch Calibration in Time-Interleaved Multipath A/D Sigma–Delta Modulators

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***Abstract*—In this paper, we propose a digital background adaptive calibration technique for correcting offset and gain mismatches in time-interleaved multipath analog–digital (A/D) sigma–delta ($\Sigma\Delta$) modulators. The proposed technique allows us to cancel the spurious tones introduced by offset and gain mismatches among the paths only by processing the digital output, without interfering with the operation of the modulator. This solution is also effective for any other time-interleaved A/D converter topology. Simulation results on a high-performance four-path bandpass $\Sigma\Delta$ modulator, operating on a 5-MHz band at a clock frequency of 320 MHz, demonstrate the effectiveness of the proposed calibration technique, which allows us to achieve significant improvements of the signal-to-noise ratio and the spurious-free dynamic range in the presence of mismatches.**

***Index Terms*—Analog–digital conversion, calibration, sigma–delta modulation, N-path circuits.**

I. Introduction

FUTURE electronic instruments and telecommunication devices require integrated analog-to-digital converters (ADCs) with high speed and, at the same time, high linearity and resolution [1]. The easiest way to fulfill such requirements is to increase the clock frequency by exploiting the features of state-of-the-art CMOS manufacturing processes with very reduced physical size, or bipolar, or bipolar-CMOS (BiCMOS) integration technologies. However, the use of these technologies implies an increase in manufacturing costs; moreover, a fast clock stresses the operations of the internal blocks of the ADC.

Alternatively, the use of time-interleaved architectures is an effective way for increasing the conversion rate: many ADCs operate in parallel, using different clock phases [2]–[4], as shown in Fig. 1.

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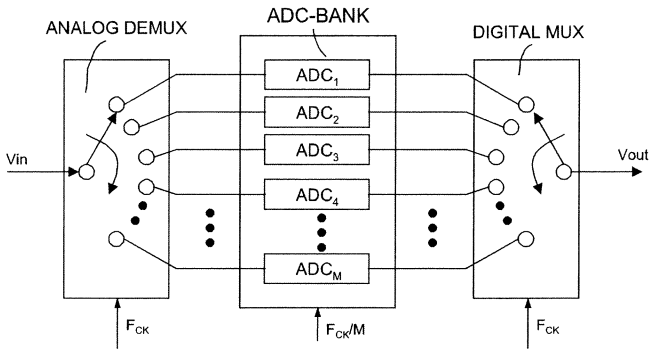

Fig. 1. Block diagram of a time-interleaved ADC.

The analog demultiplexer selects sequentially each ADC, which therefore operates at low speed. The digital multiplexer interleaves the digital output of the ADCs, thus producing the overall analog–digital (A/D) conversion result. Any type of ADC can be used, including sigma–delta ($\Sigma\Delta$) modulators [5]. Each of them operates at a clock frequency $f_{\rm ck}/M$, where $f_{\rm ck}$ is the overall sampling frequency and M is the number of channels (or paths) used. The speed requirements for each converter are therefore relaxed by a factor M.

Unfortunately, any mismatch between the time-interleaved ADC channels leads to degradation in the linearity performance. In particular, offset and gain mismatches among the parallel channels are *a priori* unpredictable and produce spurious tones in the signal band, thus worsening the spurious-free dynamic range (SFDR), as well as the signal-to-noise distortion ratio (SNDR) performance.

Generally speaking, in the past the above-mentioned limitation made difficult the use of interleaved multipath topologies for high-resolution A/D converters, especially $\Sigma\Delta$ modulators. However, spectral analysis shows that the distortion power of offset and gain dispersion is not frequency dependent and thus it could be compensated using appropriate calibration techniques, offline and online, as will be described later.

However, all of these techniques exhibit some drawbacks, especially when $\Sigma\Delta$ modulators are considered. Indeed, the stochastic behavior of $\Sigma\Delta$ modulators prevents the use of already known deterministic calibration techniques.

This paper describes a calibration method which significantly improves the SNDR and the SFDR of a time-interleaved ADC in the presence of mismatches between the different channels and

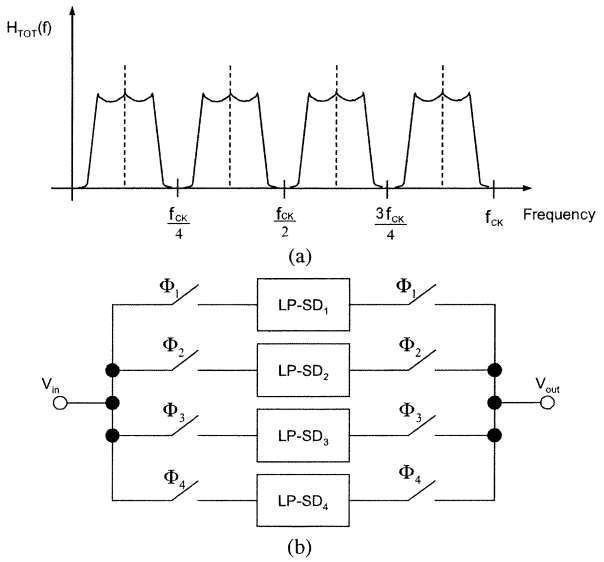

Fig. 2. (a) Four-path $\Sigma\Delta$ modulator. (b) Its noise transfer function.

is effective also when dealing with $\Sigma\Delta$ modulators. The method has been verified on a high-performance four-path bandpass $\Sigma\Delta$ modulator, operating on a 5-MHz band at a clock frequency of 320 MHz and featuring an ideal SNR better than 85 dB.

This paper is organized as follows. In Section II, the four-path $\Sigma\Delta$ modulator is briefly described. The analysis of the main mismatches (gain and offset) and the previously adopted calibration methods are presented in Sections III and IV. In Section V, the proposed solution is described in detail. Finally, in Sections VI and VII, the method is applied to the four-path bandpass $\Sigma\Delta$ modulator described in Section II.

II. Multipath $\Sigma\Delta$ Modulator

The use of $\Sigma\Delta$ modulators in a multipath architecture leads to interesting features [6]. Namely, a multipath architecture implements a bandpass response by using low-pass $\Sigma\Delta$ modulators in the single paths (Fig. 2). This simplifies the design of the ADC, since low-pass $\Sigma\Delta$ modulators are inherently less sensitive to component mismatches and, therefore, dynamic range and stability become less critical issues.

It is well known that multiple-path circuits achieve, in the sampled-data domain, the z to z^N transformation. Therefore, if $H_p(z)$ is the transfer function of the single path, the overall transfer function becomes

$$H_{\mathrm{TOT}} = \frac{V_{\mathrm{out}}(z)}{V_{\mathrm{in}}(z)} = H_P(z^N). \tag{1}$$

If $H_p(z)$ is a low-pass filter, the response folds at multiples of f_{ck}/M, as shown in Fig. 2(a), thus leading to a bandpass transfer function centered around $f_{\mathrm{ck}}/4$.

A second benefit of multipath architectures is that each channel operates at a lower frequency than the overall $\Sigma\Delta$ modulator. Finally, the multipath topology achieves the same SNDR of single-path architectures using a lower-order loop filter, with benefits in terms of stability and complexity.

TABLE I
Characteristic of Four-Path Bandpass $\Sigma\Delta$ Modulator for UMTS Base Transceiver Stations

Parameter	*Value*
Clock frequency	320 MHz
Center frequency	80 MHz
Bandwidth	5 MHz
Quantizer	9 levels
Order (of each path)	4

For a third-generation mobile communication standard, typical specifications for the A/D converter in the base transceiver station require a signal bandwidth of 5 MHz, centered around a suitable intermediate frequency (e.g., 80 MHz), thus enabling the conversion of three 1.28 Mb/s UMTS channels with 1.6 MHz of bandwidth each (CWTS standard) or a single 5-MHz channel (W-CDMA standard). Distortion specifications are demanding: the SNDR must be 85 dB (equivalent to 14 bit), the sampling jitter around 0.5 ps, and the SFDR more than 90 dBc.

Table I summarizes the main features of an ADC suitable for the above-mentioned applications. Observe that four paths working at 80 MHz clock lead to an equivalent clock frequency of 320 MHz. Moreover, a 14-bit demand for a fourth-order modulator with a nine-level quantizer, including a dynamic-element matching algorithm for the feedback path.

The architecture of the single-path modulator was studied previously and discussed in [6]. However, unfortunately, multipath $\Sigma\Delta$ modulators suffer from the typical time-interleaved ADC drawbacks. In particular, timing, offset and gain mismatches among the parallel channels produce spurious tones in the signal band, thus worsening the SNDR and SFDR performance.

III. Offset Mismatch

Assume that the ADCs in each path of the interleaved architecture of Fig. 2 are affected by offset. The ADC output will show an offset equal to the average of the offsets of the different paths and additional tones, located at $N(f_{\mathrm{ck}}/M)$ $(N = 1, \ldots, M-1)$, with amplitude proportional to the offset mismatch among paths and independent of the input signal amplitude and the frequency [8]–[10], according to

$$G(\omega) = G_s(\omega) + \frac{1}{T_{\mathrm{ck}}} \sum_{k=-\infty}^{\infty} A(k) \cdot 2\pi\delta\left[\omega - k\left(\frac{2\pi}{MT_{\mathrm{ck}}}\right)\right] \tag{2}$$

where $G_s(\omega)$ is the digital spectrum of an input sine wave sampled at $f_{\mathrm{ck}} = 1/T_{\mathrm{ck}}$, and

$$A(k) = \sum_{m=0}^{M-1} \left(\frac{1}{M} \cdot O_m\right) e^{-j2\pi\frac{km}{M}} \tag{3}$$

where O_m is the offset in the mth channel. The second term in the expression of $G(\omega)$ represents the tones caused by offset mismatches which degrade the ADC performance.

Very likely, at least one of these tones will fall inside the signal band. Therefore, the use of multipath topologies seems to be unsuitable for high-resolution ADCs, although several calibration techniques have been proposed for attenuating the spurious tones due to mismatches.

In bandpass applications the anti-aliasing filter can remove the dc components. Therefore, an online measurement of the offset is conceptually possible. Unfortunately, the sampling frequency in a single path of a time-interleaved ADC is lower than the Nyquist limit. Therefore, high-frequency signal components can be folded at low frequency. Moreover, due to the phase shift between the channels, there is no correlation among the folded dc components of the different paths.

Calibration techniques have been proposed in the past to solve the problem. They can be divided in two groups: offline and online.

The former are easier to be implemented since they can be performed in factory by trimming voltages/currents as illustrated in [10]. However, this offline solution is unable to track offset variations with temperature or ageing over time. Another solution is based on calibration procedures applied in foreground as illustrated in [11]. However, the calibration process interrupts the input signal conversion. Finally, an offline solution specifically dedicated to $\Sigma\Delta$ modulators is reported in [12]. This solution is based on finding the optimum value for a cross-coupling coefficient by carrying out extensive simulations during the design step. Again this solution cannot correct variations of the offsets with temperature or ageing.

On-line calibration techniques are more difficult to implement, since they operate in background while the ADC is working normally. Several solutions for achieving online calibration has been presented in literature, usually in the digital domain. Unfortunately, most of them are only suitable for deterministic time-interleaved ADCs and cannot be applied to $\Sigma\Delta$ modulators in view of their stochastic behavior, which makes the output signals obtained with the same input signal at different times different, depending on the previous history.

An analog online calibration method for deterministic interleaved A/D converter exploiting an additional path is illustrated in [13]. If we have $M+1$ paths available, one of them can be calibrated while the remaining M operate the conversion. Once the calibration cycle terminates another path is placed in the calibration section. Therefore, every $M+1$ calibration cycles all of the paths are calibrated and the system starts a new global calibration sequence. This technique is effective for Nyquist-rate converters, but it cannot be applied to $\Sigma\Delta$ modulators, since their output depends on the input history. Therefore, if we periodically replace one of the $\Sigma\Delta$ modulators with a calibrated one, we introduce a periodic deviation of the single path history with respect to the ideal one. This causes a discontinuity in the output in the time slots including the switching transient resulting in an unacceptable degradation of the SNDR.

A first digital online calibration technique has been proposed in [14] and [15]. This technique is based on the addition of a calibration signal, generated by a pseudo-random number generator, to the ADC input. Both signals are then processed simultaneously by means of an adaptive algorithm, which digitally filters out the output to remove residual tones at frequencies $f_{\rm ck}/M$. In this case there is no need for an extra parallel channel. This online method can be applied to any type of ADC, however it exhibits some severe limitations. Firstly, part of the full-scale input range of the ADC is used by the calibration signal. Therefore, the ADC paths require extra resolution to achieve a certain dynamic range. Moreover, the input signal cannot have frequency components at or near $f_{\rm ck}/M$ because signals at this frequency cannot be distinguished from any offset mismatch. The last effect prevents the use of this calibration method in applications like those mentioned above, where the desired signal is located around $f_{\rm ck}/M$. One way to overcome the problem is to perform the online calibration only when the input is in the idle state. However, this solution is no longer a true online offset calibration.

Another interesting online calibration method suitable to be applied to time-interleaved $\Sigma\Delta$ modulators has been presented in [16]–[18]. Its principle of operations is as follows.

- The input signal is chopped with a pseudo-random sequence consisting of $+1$ and -1 and the obtained signal is digitized by the mth-channel ADC ($\mathrm{ADC_m}$).
- The mean value of the digital outputs in one time slot is calculated and stored in a register.
- The offset value is estimated by subtracting the mean value stored in the register from the input signal digitized by $\mathrm{ADC_m}$, suitably delayed.
- The result is chopped with the same sequence as the input signal, which is thus restored.

The chopping transforms any input signal into noise with mean value equal to 0 before the estimation and cancellation of the offset. The randomization process allows us to overcome the limitation of [15], which was ineffective for signal located around $f_{\rm ck}/M$. Moreover, a new estimation of the offset value is calculated in each time slot and its value is updated during normal operations. However, this technique suffers of two problems: the chopping operates on the analog section of the converter, which is very sensitive to parasitics. Since high linearity and resolution are required, the influence of the calibration circuit on the analog first stage of the converter could be critical. Moreover, this method cannot correct any nonideality of additional front-end circuits located before the chopping.

IV. Gain Mismatch

Another source of spurious components is the gain mismatch. Channel gain mismatches result in amplitude modulation of the input samples causing scaled copies of the input spectrum to appear centered around integer multiples of the channel sampling rate $f_{\rm ck}/M$. Intuitively, this happens because each individual channel samples the input signal at a rate of $f_{\rm ck}/M$, causing the input spectrum to be repeated periodically at intervals of $f_{\rm ck}/M$. In case of perfect matching the multiplexing produces the cancellation of the alias components except at integer multiples of $f_{\rm ck}$. On the contrary, if some mismatch between

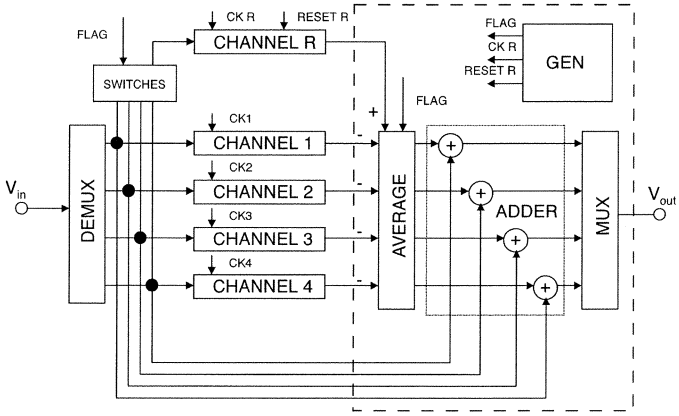

Fig. 3. Block diagram of proposed offset calibration technique.

channels is present these repetitions do not cancel completely and appear in the output spectrum. Sampling with mismatched channel gains can also be regarded as modulating the analog input by a periodic discrete-time sequence of period $MT_{\rm ck}$. For an input sinusoid at frequency $f_{\rm in}$, this modulation produces spurious mismatch tones in the output spectrum at frequencies: $f_{\rm ck}/M - f_{\rm in}, 2f_{\rm ck}/M - f_{\rm in}, 3f_{\rm ck}/M - f_{\rm in}, (\mathrm{M}-1)f_{\rm ck}/M - f_{\rm in}$.

An explicit expression for the output spectrum has been derived in [7], [11], and [19]

$$G(\omega) = \frac{1}{T_{\rm ck}} \sum_{k=-\infty}^{\infty} B(k) \cdot G_s \left[\omega - k \left(\frac{2\pi}{M} \right) \right] \tag{4}$$

where $G_s(\omega)$ is the digital spectrum of an input signal sampled at $f_{\rm ck} = 1/T_{\rm ck}$, and

$$B(k) = \sum_{m=0}^{M-1} \left(\frac{1}{M} \cdot g_m \right) e^{-j2\pi \frac{km}{M}} \tag{5}$$

g_m being the gain of the mth channel. Note that in the gain mismatch case the SNDR degradation is dependent on the input signal amplitude.

Several calibration techniques have been proposed for attenuating this spurious effect, as well. In the online category, some of them share the same circuitry used to correct offset mismatches [14], [15], [18], [21]. For this reason, they are affected by the same limitations already highlighted in the case of offset mismatch correction techniques.

Finally, errors in the sample times (timing mismatches) result in phase modulation of the input samples, which also causes scaled copies of the input spectrum to appear centered at the same frequencies as the spurious components stemming from gain mismatch [7]. To reduce this effect few techniques have been proposed so far [17], [18], [20], [22], [23], which can be applied together with the offset and gain calibration techniques proposed in this paper.

V. Proposed Calibration Technique

Fig. 3 shows the block diagram of the proposed adaptive offset calibration technique applied to a four channel A/D converter (e.g., a $\Sigma\Delta$ modulator) [24]. The solution uses an additional path, assumed to be the reference element.

As shown in the Fig. 3, instead of periodically placing one path in a calibration section, the reference path (CHANNEL R) is connected in parallel to the path that we want to calibrate. The parallel connection lasts for N clock cycles $(NT_{\rm ck})$ and can be realized by simply assigning the clock phases of the channel under calibration to the reference path.

The difference between the digital outputs of the path under calibration and the reference path is integrated over the calibration time slot $NT_{\rm ck}$ (AVERAGE). The result is a digital word proportional to the difference between the offsets of the two paths, while the signal components are cancelled.

Finally, this word is added to the ADC of the path under calibration, thus making its offset equal to the offset of the reference path. If required, the offset of CHANNEL R can be periodically calibrated in order to make the offsets of all the paths equal to zero, by introducing well know techniques, such as those in [25].

To demonstrate that, let us assume that the output y of each channels is given by

$$y = (S + O) \cdot \mathrm{STF} + N_Q \cdot \mathrm{NTF} \tag{6}$$

where STF and NTF are the signal transfer function and the noise transfer function of the low-pass $\Sigma\Delta$ modulator, respectively. The difference between the outputs of the two paths averaged over N samples becomes

$$\langle \Delta O \rangle = \mathrm{STF} \cdot \sum_{n=1}^{N} \frac{O_R - O_C}{N} + \mathrm{STF} \cdot \sum_{n=1}^{N} \frac{S_R - S_C}{N}, \\ \mathrm{NTF} \cdot \sum_{n=1}^{N} \frac{N_Q, R_{Q,C}^{-N}}{N} \tag{7}$$

where O_R, S_R, and $N_{Q,R}$ are offset, input and quantization noise of the reference path, while O_C, S_C, and $N_{Q,C}$ are offset, input and quantization noise of the path under calibration.

Since the STF is equal to one in the signal band, the first term of (7) becomes the offset mismatch. The second term is zero, being the two inputs equal $(S_R = S_C)$. The NTF in the third term is an high-pass function. Therefore, the third term vanishes as the length of the average operation goes to infinity. In practice, a suitably long averaging makes the third term negligible. It turns out that $\langle \Delta O \rangle$ represents an estimation of the offset mismatch, whose precision depends on N.

Gain mismatch possibly reduces the effectiveness of the proposed offset calibration method. Indeed, (7) in the presence of gain mismatch becomes

$$\langle \Delta O \rangle = \mathrm{STF} \cdot \sum_{n=1}^{N} \frac{O_R - O_C}{N} + \mathrm{STF} \cdot \Delta G \cdot \sum_{n=1}^{N} \frac{S}{N}, \\ \mathrm{NTF} \cdot \sum_{n=1}^{N} \frac{N_Q R_{Q,C}^{-N}}{N} \tag{8}$$

where ΔG is the gain mismatch between the path under calibration and the reference path. The second term of (8), that was supposed to be zero, has a finite value. Therefore, any signal

component around dc or multiples of $f_{\rm ck}/M$ affects the offset estimation accuracy.

The same configuration illustrated in Fig. 3 together with a more complex digital signal processing enables the measurement and correction of the gain mismatches. The measurement of the offset mismatch required to solve (6) applied to the reference and the calibrating path, accounting for the gain mismatch, results

$$\begin{aligned}\langle y_R\rangle &= \mathrm{STF}\cdot\sum_{n=1}^{N}\frac{S}{N};\\ \langle y_C\rangle &= \mathrm{STF}\cdot G_C\cdot\sum_{n=1}^{N}\frac{S}{N}+O_C\end{aligned}\tag{9}$$

where G_C and O_C are the gain and the offset of the path under calibration. We assumed zero offset and unity gain for the reference path, since the goal of the calibration is to compensate mismatches and not absolute values. This set of two equations contains three unknowns: an additional equation is required to find the solution. The request is satisfied just waiting for the successive calibration cycle and building two new equations, similar to the previous ones. The difference between the first and the second pair of equation comes from the value of input signal (S_A and S_B, respectively). The new sets of equation are

$$\begin{aligned}\langle y_{R,A}\rangle &= \mathrm{STF}\cdot\sum_{n=1}^{N}\frac{S_A}{N}\\ \langle y_{C,A}\rangle &= \mathrm{STF}\cdot G_C\sum_{n=1}^{N}\frac{S_A}{N}+O_C\end{aligned}\tag{10}$$

and

$$\begin{aligned}\langle y_{R,A}\rangle &= \mathrm{STF}\cdot\sum_{n=1}^{N}\frac{S_B}{N}\\ \langle y_{C,B}\rangle &= \mathrm{STF}\cdot G_C\cdot\sum_{n=1}^{N}\frac{S_B}{N}+O_C.\end{aligned}\tag{11}$$

The solution of (10) and (11) determines offset and gain mismatches. They are given by

$$\begin{aligned}\langle\Delta G\rangle = \langle\Delta G_C\rangle &= \frac{\langle y_{C,A}\rangle-\langle y_{C,B}\rangle}{\langle y_{R,A}\rangle-\langle y_{R,B}\rangle}\\ \langle\Delta G\rangle = \langle\Delta O_C\rangle &= \langle y_{C,A}\rangle-\langle\Delta G\rangle\langle y_{R,A}\rangle.\end{aligned}\tag{12}$$

Observe that the accuracy of the gain error depends on the difference of the input signal at $f_{\rm ck}/M$ during the two calibration cycles considered. Therefore, with zero or constant components $\langle\Delta G\rangle$ is undetermined. This situation in practical cases occurs rarely. Moreover, in idle conditions a suitable tone can be added at the input, if required.

Main advantages of the proposed offset and gain calibration algorithm are as follows.

- The accuracy of the offset and gain equalization is limited only by the allowed calibration time slot, $NT_{\rm ck}$, and hardware capability.
- There are no special requirement on the original offset and gain values (the offset could be different from 0 also in the reference channel).
- The solution works with any input signals frequencies, including signals located around $f_{\rm ck}/M$.
- The solution is independent of the ADC topology.
- The solution is simple to be implemented and robust because it is purely digital and requires only one additional path without special calibration input signals.
- The cyclic repetition of the calibration steps allows us to track offset and gain variations with temperature or ageing over time.

These benefits are obtained at the expense of the introduction of an additional channel and of some digital logic. It has to be noted that the presence of the reference channel in parallel to the channel under calibration increases the input capacitive load (i.e., we have $M/2+1$ channels instead of $M/2$ connected at the same time to the input node). This obviously increases the required driving capability of the input source. Eventually, dummy capacitors can be used to equalize the capacitive load during the different clock phases (i.e., increase the capacitive load also when the channel under calibration and hence the reference channel is not connected to the input node).

VI. Hardware Implementation

From the equations of Section V, it turns out that $\langle\Delta O\rangle$ represents an estimation of the offset mismatch, whose precision depends on N. Assume that the system requires an accuracy of the offset mismatch calibration as good as the least-significant bit (LSB) of the overall ADC after decimation. Since the resolution of $\langle\Delta O\rangle$ from (7) is $\mathrm{LSB}_{\Sigma\Delta}/N$, with $\mathrm{LSB}_{\Sigma\Delta}$ denoting the LSB of the modulator quantizer, we obtain the condition

$$N = 2^{M-K}\tag{13}$$

where M is the overall resolution (after decimation) and K is the number of bit of the multibit $\Sigma\Delta$ modulator. A larger averaging period by a given power of 2 requires truncation, but it provides a better accuracy.

The word length of the accumulators ($L_{\rm ACC}$) used in the AVERAGE block must be sufficiently large to avoid overflow. Observe that even if the two $\Sigma\Delta$ modulators connected in parallel process the same input signal, the outputs can be different even for matched offset, since the initial conditions of the integrators are different. Therefore, we have to foresee some extra room for the random difference of the outputs, leading to

$$L_{\rm ACC} = \mathrm{Round}[\log_2(N\cdot\Delta O_{\rm MAX})+1]\tag{14}$$

where $\Delta O_{\rm MAX}$ is the maximum expected offset mismatch.

The proposed calibration technique operates completely in the digital domain outside the $\Sigma\Delta$ modulator feedback loop. Indeed, the offset correction is performed by adding the estimated offset mismatch $\langle\Delta O\rangle$ to the modulator output, while the $\Sigma\Delta$ modulator operates exactly as in the absence of the calibration circuit without any SNDR degradation. When $\langle\Delta O\rangle$ is added

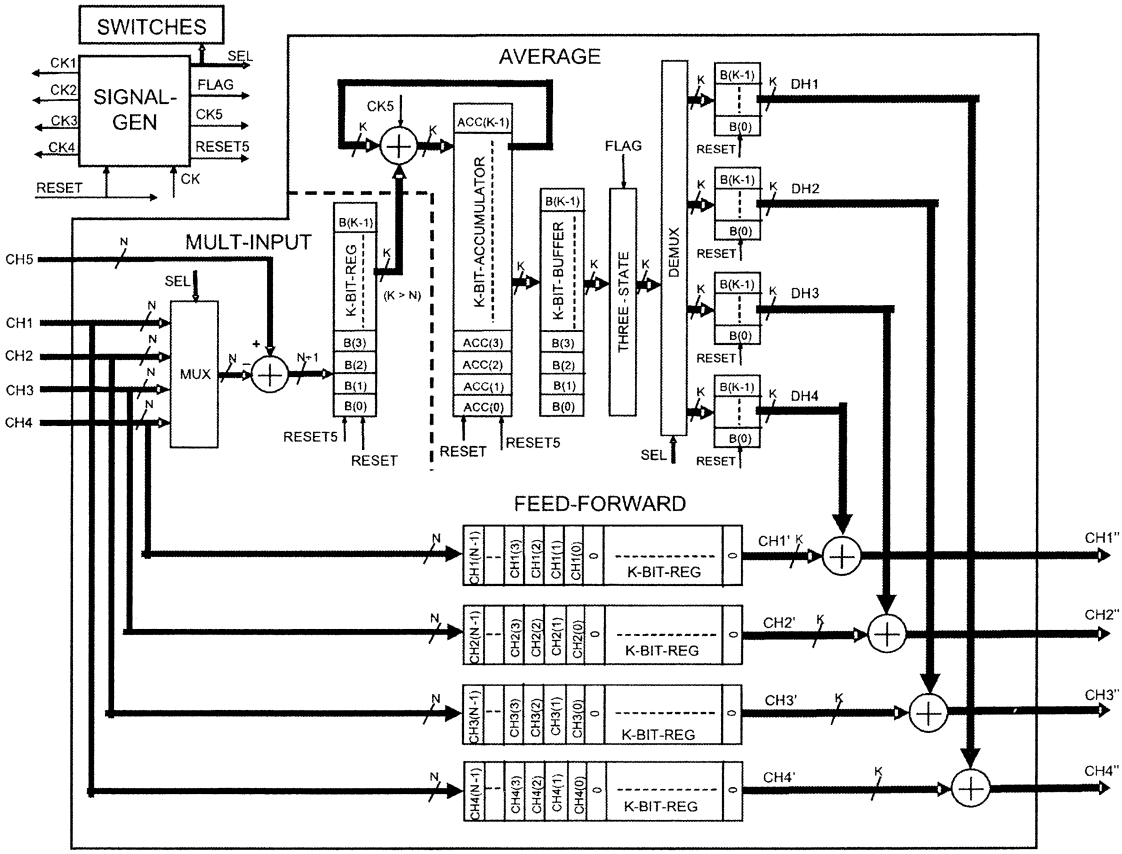

Fig. 4. Hardware implementation of the proposed offset calibration technique.

to the output of the path under calibration, its overall offset becomes equal to the offset of the reference path, as already highlighted. This procedure is repeated for the M paths of the $\Sigma\Delta$ modulator. At the end all the M paths have the same overall offset of the reference path, thus avoiding spurious tones.

The hardware necessary to correct the gain error is more complex than the simple offset compensation solution, since it requires the use of multipliers. However, the complexity is comparable with any other digital calibration methods. As for the offset case, the gain mismatch estimation and correction technique does not affect the performance of the $\Sigma\Delta$ modulator, since all the circuits operate in the digital domain.

The offset calibration algorithm have been described using VHDL language and synthesized using a 0.35-μm CMOS technology. The resulting total area occupation is 300 μm $\times$ 300 μm, while the estimated power consumption is about 15 mW with a power-supply voltage of 3.3 V and a clock frequency of 80 MHz.

Fig. 4 shows in detail the hardware implementation of the offset digital calibration circuit whose simplified diagram is shown in the dashed box of Fig. 3.

The block MULT-INPUT includes a digital multiplexer MUX driven by the 2-bit SEL signal, which sequentially selects one of the N-bit digital signals CH1, CH2, CH3, and CH4 of the paths to be calibrated. Moreover, it includes a subtractor that calculates the algebraic difference between the N-bit reference signal CH5 and the selected signal. Finally, a K-bit register transforms the word at the output of the subtractor into a K-bit word $(K > N)$ to be fed to the block AVERAGE.

The block AVERAGE includes several functions. The output of the K-bit ACCUMULATOR is fed into the K-bit BUFFER, which is isolated from the input of the DEMUX by the THREE-STATE interface, which is put in high impedance state when the ACCUMULATOR is working. At the end of the integration time slot $NT_{\rm ck}$ the assertion of the signal FLAG enables the block THREE-STATE to feed the result of the accumulated offset to the input of the DEMUX which transfers it, depending on the signal SEL, to the proper K-bit output register. The stored value remains stable until the next value is overwritten to allow offset compensation with an updated value.

Finally, section FEEDFORWARD performs the N-bit to K-bit transformation of the digital signals CH1, CH2, CH3, and CH4 of the paths and, then, the addition to the corresponding accumulated offset.

It is worth to point out that in most telecommunication applications a hardware implementation of the digital calibration circuit might not be necessary, since the available baseband digital processor (digital signal processor or microprocessor) can take care of the required functions, thus reducing the system complexity.

VII. Simulation Results

A behavioral simulation of the offset calibration method validated the proposed approach. Fig. 5 shows simulation results

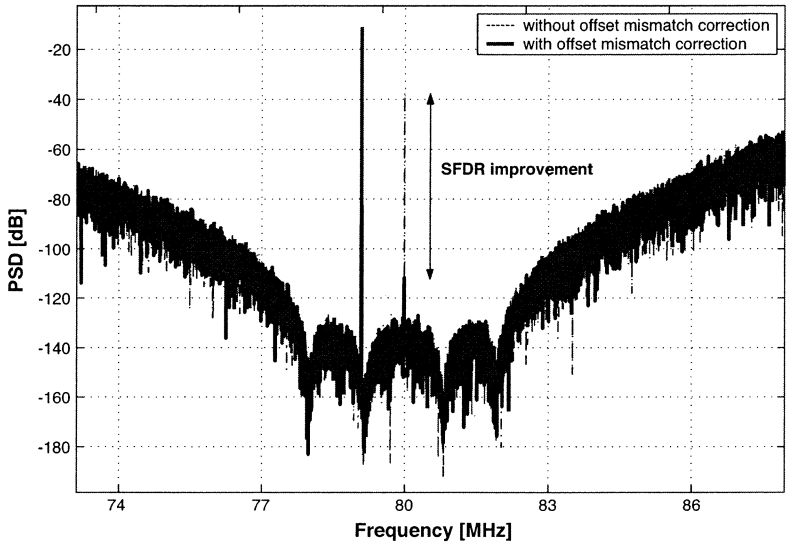

Fig. 5. Comparison between the power-spectral density of the output of a four-path $\Sigma\Delta$ modulator with (solid line) and without offset calibration.

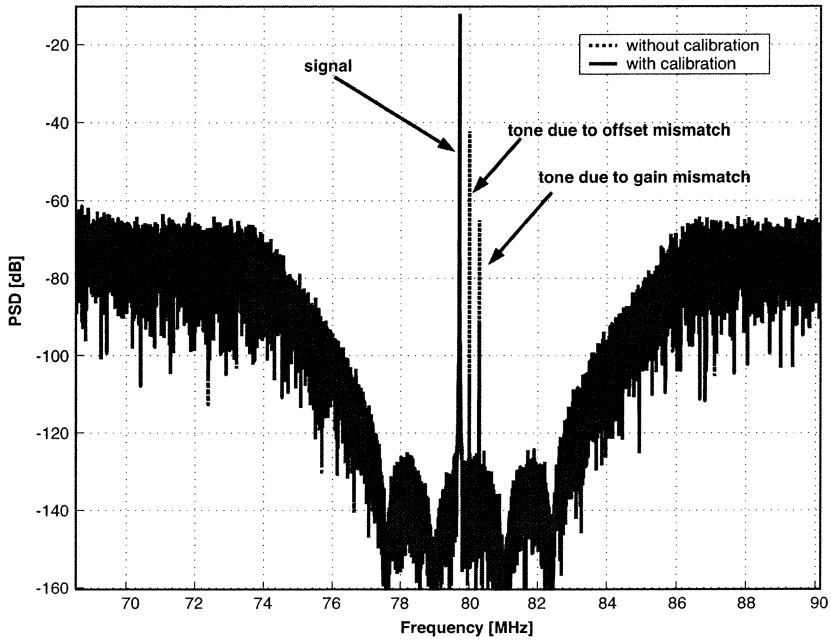

Fig. 6. Comparison between the power-spectral density of the output of a four-path $\Sigma\Delta$ modulator with (solid line) and without offset and gain calibration.

for the four-path bandpass $\Sigma\Delta$ modulator operating at 320 MHz (each path operates at 80 MHz).

The offset mismatch is a random number whose variance, δ, is as large as about 10 mV. The simulation tool is AdvanceMS [26] with VHDL-AMS [27] behavioral description of the system. The output data were post-processed with MATLAB [28]. Fig. 5 demonstrates that the large tone caused by the offset mismatch is reduced by 68 dB. We used a time slot of 2^{17} samples and an accumulator word-length of 22 bits.

A longer time slot improves the effectiveness of the calibration system. However, the hardware complexity increases as well. In actual applications the choice of the averaging time must account for other nonidealities of the $\Sigma\Delta$ modulator (especially those determining the harmonic distortion): the residual tones produced by offset mismatch must be just lower than the highest tone caused by other effects.

The combined gain and offset calibration method has been verified with behavioral simulation on the same $\Sigma\Delta$ modulator architecture used for the offset correction (four-path, bandpass $\Sigma\Delta$ modulator with 320-MHz clock frequency). An offset mismatch of 10 mV and a gain mismatch of 0.5% leads to the output spectrum shown in Fig. 6.

The method reduces the tone due to the offset mismatch by about 60 dB and the tones due to the gain mismatches by about 30 dB.

VIII. Conclusion

This paper describes a technique for offset and gain mismatch calibration in multipath $\Sigma\Delta$ modulators. The proposed method offers several advantages: the accuracy of offset and gain compensation is limited only by the allowed calibration time slot and hardware complexity. Moreover, there are no special constraints

on the original offset and gain values nor on the input signal (the technique works in the presence of signal components around f_{ck}/M). Finally, the proposed solution does not require any special calibration signal that could limit the dynamic range of the $\Sigma\Delta$ modulator and it is independent of the ADC topology. The effectiveness of the calibration technique has been verified with behavioral (VHDL-AMS) simulations on a four-path bandpass $\Sigma\Delta$ modulator. Results show significant improvements of the SNDR and the SFDR.

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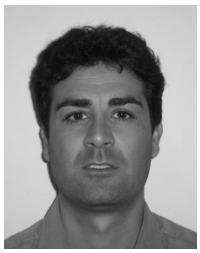

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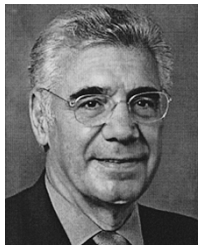

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