Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp888-889

Analog-Assisted Digital Low Dropout Regulator (AAD-LDO) with 59% Faster Transient Response and 28% Ripple Reduction

Kazuaki Mori[1], Yasuyuki Okuma[2], Xin Zhang[1], Hiroshi Fuketa[1], Takayasu Sakurai[1], and Makoto Takamiya[1]

[1] University of Tokyo, Tokyo, Japan, [2] Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan

Abstract

An analog-assisted digital low dropout regulator (AAD-LDO) is proposed to solve the problems of a slow transient response and a large output ripple in a conventional digital LDO. In AAD-LDO, a fast-response auxiliary analog LDO is added to the digital LDO in parallel. Compared with the digital LDO, the measured AAD-LDO in 180nm CMOS reduces the transient response time and the output ripple by 59% and 28%, respectively, at the same current efficiency of 97.1%.

1. Introduction

The number of on-chip voltage converters is increasing, because recent SoC's require a lot of power supply voltages. A low dropout regulator (LDO) is a reasonable choice for the on-chip voltage converters, because LDO requires no off-chip components. The low power SoC's require a low input-voltage LDO with the low quiescent current (I_Q) (= supply current for a controller in LDO) [1]. A digital LDO [1-5] achieves the low input-voltage operation with low I_Q. Problems of the digital LDO, however, are a slow transient response and a large output ripple. In order to solve the problems, an analog-assisted digital low dropout regulator (AAD-LDO) is proposed.

2. Problems of Conventional LDO's

Fig. 1 shows a conventional analog LDO. The current efficiency (η) of the analog LDO is low due to high I_Q in the operational amplifier. Fig. 2 shows a conventional digital LDO [1]. In the digital LDO, the current efficiency is high by low I_Q in the controller and the comparator, though the transient response is slow and the output ripple is large. In order to reduce the transient response time, high frequency clock (Clk) is required, which increases I_Q and decreases η [2-3]. In order to reduce the ripple, the unit gate width (W_{UNIT}) of the power transistors is reduced and the number (n) of the power transistors is increased. The increased n, however, increases I_Q and decreases η. Therefore, a new circuit is required to reduce both the transient response time and the ripple without decreasing η.

3. Proposed Analog-Assisted Digital LDO (AAD-LDO)

Fig. 3 shows a concept of the proposed AAD-LDO. In AAD-LDO, a fast-response auxiliary analog LDO is added to the digital LDO in parallel. Fig. 4 shows a detailed schematic of the proposed AAD-LDO. In AAD-LDO, the digital LDO is main and the analog LDO is auxiliary, because $W_{ANALOG} < W_{DIGITAL}$. The digital LDO slowly controls the output voltage (V_{OUT}) with a coarse digital voltage step. In contrast, the analog LDO quickly controls V_{OUT} with a fine analog voltage control. By operating both the digital LDO and the analog LDO simultaneously in parallel, AAD-LDO reduces both the transient response time and the output ripple.

4. Measurement Results and Discussion

Both AAD-LDO and the digital LDO are fabricated in 180nm CMOS. In AAD-LDO and the digital LDO, the digital LDO part is the same and only AAD-LDO has the analog LDO. Fig. 5 shows the chip microphotograph and the layout of AAD-LDO. The total chip area 1.2mm×0.5mm. The core area of the digital and analog LDO is 200μm×170μm and 30μm×50μm, respectively. Table I shows a performance summary of AAD-LDO. The fabricated AAD LDO achieved the 1.2-V input voltage and 0.95-V output voltage with 99.6% current efficiency and 14.2-μA quiescent current at 3.4-mA load current.

Figs. 6 and 7 shows the measured η dependence of the transient response time and the peak-to-peak ripple of V_{OUT}, respectively, in the conventional digital LDO and the proposed AAD-LDO. The input voltage is 1.2V, V_{OUT} is 0.95V, and the load current is 3.4mA. The reference voltage (V_{REF}) is changed from 0.8V to 0.95V and the response time of V_{OUT} is measured at the load resistance of 270Ω. The Clk frequency is varied from 1MHz to 14MHz in the digital LDO, while the bias current of the operational amplifier is varied from 1μA to 15μA in AAD-LDO at the Clk frequency of 1MHz. Compared with the conventional digital LDO, the proposed AAD-LDO reduces the response time from 40μs to 2.4μs by 94% and from 4.4μs to 1.8μs by 59% at η of 99.6% and 97.1%, respectively. Fig 8 shows the measured waveforms of V_{REF} and V_{OUT} at η of 99.6%. Similarly, AAD-LDO reduces the ripple from 10.8mV to 7.8mV by 28% at η of 97.1% as shown in Fig. 9.

Acknowledgements

This work was partly carried out as Extremely Low Power (ELP) project supported by METI and NEDO. The VLSI chips have been fabricated in the chip fabrication program of VDEC in collaboration with Rohm Corp. and Toppan Printing Corp.

References

[1] T. Okuma, *et al.*, CICC, pp. 323-326, 2010.
[2] M. Onouchi, *et al.*, A-SSCC, pp. 37-40, 2011.
[3] A. Raychowdhury, *et al.*, Symp VLSI Circuits, pp. 148-149, 2012.
[4] Y. Lee, *et al.*, Symp VLSI Circuits, pp. 178-179, 2012.
[5] C. Chiu, *et al.*, Symp VLSI Circuits, pp. 166-167, 2013.

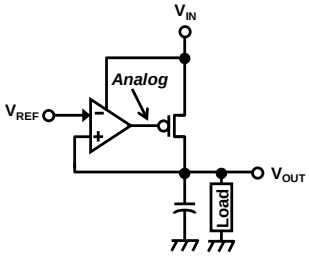


Fig. 1 Conventional analog LDO.

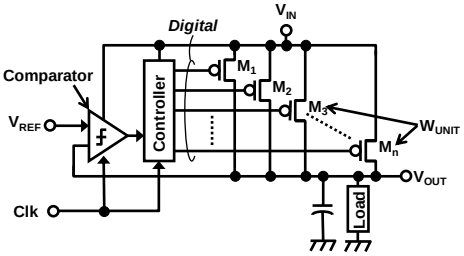


Fig. 2 Conventional digital LDO [1].

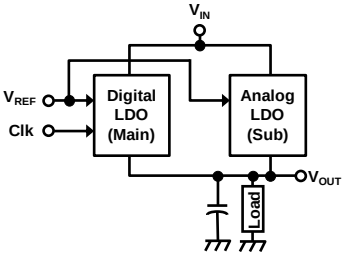


Fig. 3 Concept of proposed AAD-LDO.

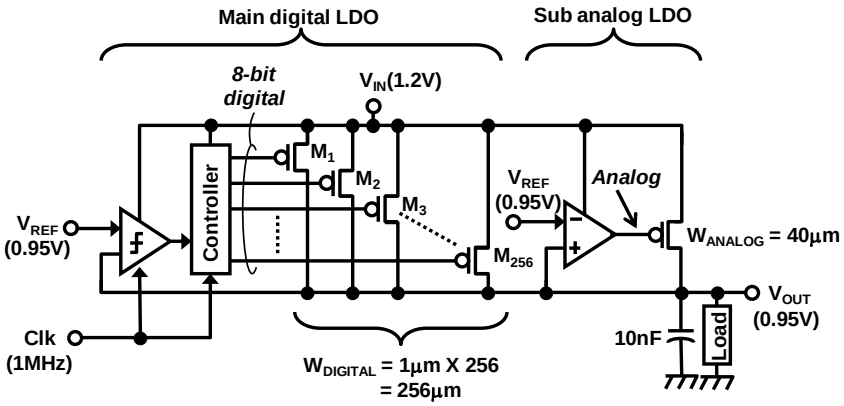


Fig. 4 Detailed schematic of proposed AAD-LDO.

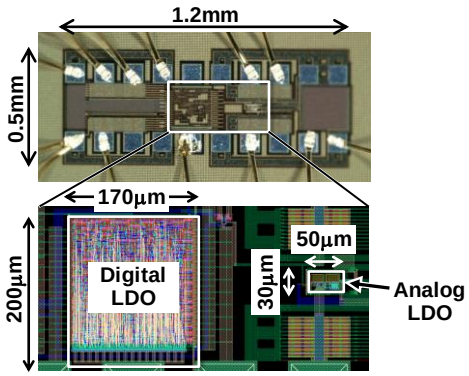


Fig. 5 Chip microphotograph and layout of AAD-LDO.

Table I Performance summary of AAD-LDO.

CMOS Technology	180 nm
Active area	0.036 mm²
Clock frequency	1 MHz
Input voltage	1.2 V
Output voltage	0.95 V
Maximum load current	11 mA
Nominal load current (I_1)	3.4 mA
Output capacitor	10 nF (Off-chip)
Quiescent current @ I_1	14.2 µA - 242 µA
Current efficiency @ I_1	93.3 % - 99.6 %

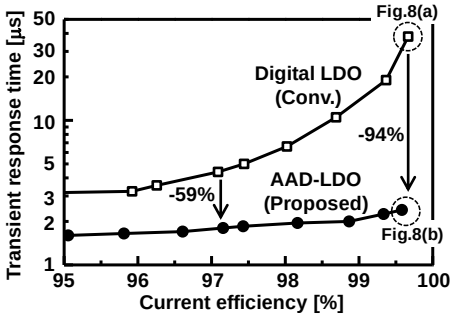


Fig. 6 Measured transient response time vs. current efficiency.

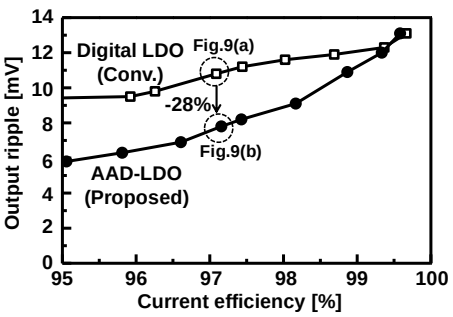
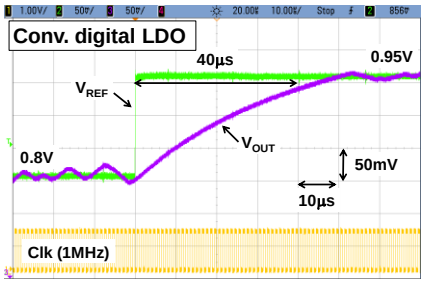
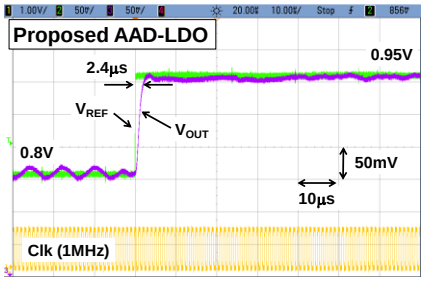


Fig. 7 Measured output ripple vs. current efficiency.

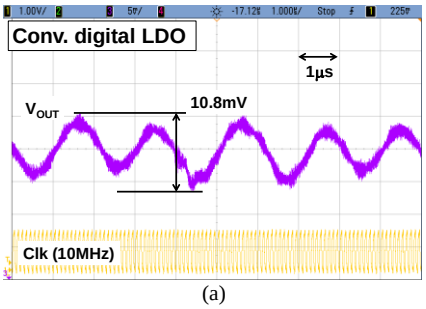


(a)

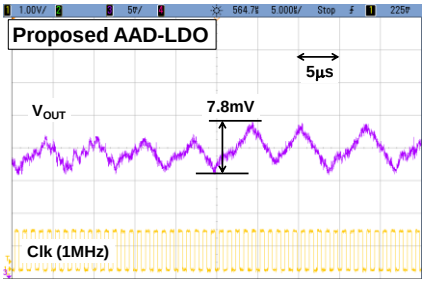


(b)

Fig. 8 Measured transient waveforms of V_{REF} and V_{OUT} at η of 99.6%. (a) Conv. digital LDO. (b) Proposed AAD-LDO.



(a)



(b)

Fig. 9 Measured output ripple waveforms at η of 97.1%. (a) Conv. digital LDO. (b) Proposed AAD-LDO.