Fully Digital Background Calibration Technique for Channel Mismatches in TIADCs

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***Abstract*—Time-interleaved analog-to-digital converter (TIADC) is a promising approach to meet the requirement of very high speed wireless communication systems. However, mismatches between the channels in a TIADC cause the spurious images in the output spectrum, thus decreasing its performance. Therefore, efficient correction techniques for these mismatches are highly required. In this paper, we present a fully digital background calibration technique for channel mismatches including offset, gain and timing mismatches in TIADCs using Hadamard transform and average offset mismatch errors. The proposed technique results in the removal of spurious images from the TIADC output spectrum, thus increases the signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR). The performance improvement of TIADCs employing this technique is demonstrated through numerical simulations.**

***Index Terms*—Fully digital background calibration, Hadamard transform, TIADC, channel mismatch.**

I. Introduction

With the advent of the new communication standards and the remarkable growth of wireless communication systems, analog-to-digital converters (ADCs) become one of the essential components and require high resolution, high speed, and low power consumption [1]. In order to achieve these goals, a time-interleaved ADC (TIADC) is a promising solution. The time-interleaving architecture was first introduced by W. C. Black and D. A. Hodges in [2] and shown in Fig. 1 which consisting of M single ADCs operating in parallel and sampling in cycle manner [1], [2]. In this architecture, each sub-ADC operates at the same sample period of MT_s leading to an M-times higher sample period.

In fact, due to Process, Voltage, and Temperature (PVT) variations lead to channel mismatches in TIADCs including offset, gain, timing, and bandwidth mismatches. They produce unwanted spurious tones at the TIADC output, degrading the signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) of the converters significantly [3], [4], [12]. In this work, we only try on solve these mismatches (including offset, gain and timing mismatches) without bandwidth mismatch as show in the Fig. 2.

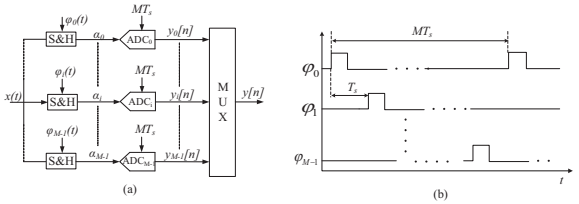

Figure 1: A simple block diagram of the M-channel TIADC

There are a lots of works coping with the channel mismaches [4]–[11]. Some of these perform the channel mismatch calibration in either analog domain [7] or mix-signal domain [8]. Thanks to CMOS technology scaling and easier to port to the next technology generation, all-digital calibration is currently preferred [9], [10], which tackling the gain and clock skew errors, but not dealing with the offset one.

Inspired by the all-digital calibration scheme in [11], in this paper, we develop a fully digital background calibration technique for all channel mismatches encompassing offset, gain and timing mismatches. The proposed technique first calibrate the offset error by taking the average of sub-ADC output samples, and then calibrate gain and timing mismatches by using pseudo aliasing signals as in [11]. The proposed technique achieves the higher performance and a faster convergence speed compared with the conventional technique.

The rest of this paper is organized as follows. Section II provides time-interleaved ADCs modeling only with offset, gain and timing mismatch. Section III develops a fully digital background calibration tech-

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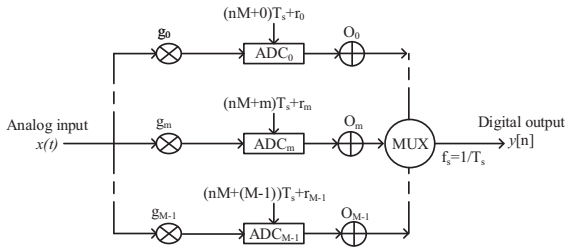

Figure 2: Model of an M-chanel TIADC with offset, gain and timing mismatches

nique for channel mismatch. The simulation results are given in Section IV. Finally, conclusions are drawn in Section V.

II. System model

A simplified block diagram and time diagram of an M-channel TIADC are shown in Fig. 1(a). It consists of M individual channel ADCs in parallel to sample an input signal in a cyclic manner and a digital multiplexer at the output. Each ADC can be any kind of single ADC architecture such as Successive-approximation-register (SAR) ADC or pipeline ADC. A simple block diagram of the M channel TIADCs is shown in Fig. 1(a). Each sub-ADC of the individual channels sequentially samples and digitizes the analog bandlimited input signal $x(t)$ at the same sampling frequency f_s/M with equally phase-shifted clocks $\phi_i\big(t\big),\ 0 \le i \le M-1$ to produce digital streams. As a result, the difference between the sampling instants of two consecutive channels is T_s as sketched in Fig. 1(b).

By assuming a bandlimited input signal $X\left(j\Omega\right) = 0$, with $|\Omega| \ge B$ and $B \le \frac{\pi}{T_s}$. The ideal digital output of the i^{th} channel ADC at sample k can be expressed by

$$y_i\left[k\right] = x\big(\big(kM+i\big)T\big) \tag{1}$$

The sub-ADC outputs $y_i[n]$ are multiplexed to reconstruct a global digital output $y[n]$.

The time-interleaving architectures increase the sampling rate of a single ADC by M while preserving the same resolution of a single path ADC. However, the performance of the TIADCs is decreased by channel mismatches (such as offset, gain and timing mismatches) due to process, voltage, temperature variations. The simplified discrete-time system model of an M channel TIADC with offset mismatch, gain mismatch and timing skew is shown in Fig. 2. Considering all the errors in Fig. 2, the i^{th} channel's digital output can be rewritten as

$$y_i\left[k\right] = \big(1+g_i\big)x\big(\big(kM+i\big)T_s + r_i\big) + O_i \tag{2}$$

where g_i, r_i and O_i, $i = 0, 1, ..., M-1$ are gain, timing and offset mismatch parameters between channels in TIADC, respectively. The time expression of the i^{th} channel is done by summing the samples over the time domain as follow

$$y_i\big(t\big) = \sum_{k=-\infty}^{+\infty} y_i\left[k\right]\delta\big(t-\big(kM+i\big)T\big) \tag{3}$$

$$\begin{aligned} y_i\big(t\big) = \sum_{k=-\infty}^{+\infty} &\big(\big(1+g_i\big)x\big(\big(kM+i\big)T_s + r_i\big) \\ &+ O_i\big)\delta\big(t-\big(kM+i\big)T\big) \end{aligned} \tag{4}$$

The overall output of the TIADC is given by

$$\begin{aligned} y\big(t\big) &= \sum_{i=0}^{M-1} y_i\big(t\big) \\ &= \sum_{i=0}^{M-1}\sum_{k=-\infty}^{+\infty} \underbrace{\big((1+g_i)x((kM+i)T_s + r_i) + O_i\big)}_{\hat{x}_i} \\ &\quad \times \underbrace{\delta(t-(kM+i)T)}_{s_i} \end{aligned} \tag{5}$$

where $\hat{x}_i$ is the i^{th} channel's output which include all mismatch errors, s_i is a train of Dirac pulse. Consequently, the output spectrum is obtained by calculating the spectrum of each $\hat{x}_i$ and s_i as follows:

$$Y\big(j\omega\big) = \sum_{i=o}^{M-1} \frac{1}{2\pi}\hat{X}_i\big(j\omega\big)S_i\big(j\omega\big) \tag{6}$$

where

$$S_i\big(j\omega\big) = \frac{2\pi}{MT}\sum_{k=-\infty}^{+\infty}\delta\big(\omega - k\frac{\omega_s}{M}\big)e^{-jki\frac{2\pi}{M}} \tag{7}$$

$$\hat{X}_i\big(j\omega\big) = \underbrace{\big(1+g_i\big)}_{Gain}\ \underbrace{e^{-j\omega r_i}}_{TimingSkew}\ X\big(j\omega\big) + \underbrace{O_i\delta\big(\omega\big)}_{Offset} \tag{8}$$

Substituting (7) and (8) in (6) gives

$$\begin{aligned} Y\big(j\omega\big) = \frac{1}{T}\sum_{k=-\infty}^{+\infty}\Bigg[\frac{1}{M}\sum_{i=0}^{M-1}\big(1+g_i\big) \\ \times e^{-j\left(\omega - k\frac{\omega_s}{M}\right)r_i}e^{-jki\frac{2\pi}{M}}\Bigg]X\big(j\big(\omega - k\frac{\omega_s}{M}\big)\big) \\ + \frac{1}{T}\sum_{k=-\infty}^{+\infty}\frac{1}{M}\sum_{i=0}^{M-1}O_i e^{-jki\frac{2\pi}{M}}\delta\big(\omega - k\frac{\omega_s}{M}\big) \end{aligned} \tag{9}$$

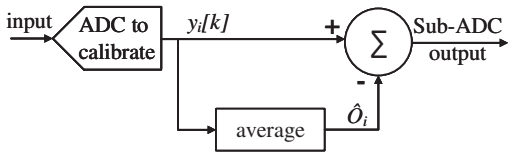

Figure 3: Offset mismatch calibration for each sub-ADC.

This expression shows that, in the presence of all the errors, the input signal is modulated by the expression between brackets which combines gain and timing mismatch errors. These errors appear at each $\pm\omega_{in} + k\frac{\omega_s}{M}$ frequency, where ω_{in} is the input frequency. Additionally, the offset mismatch tones intervene as signal independent spurious tones at each $k\frac{\omega_s}{M}$. The task is correction these channel mismatches to improve the TIADC performance. The proposed correction technique is presented in the following section.

III. Proposed fully digital background calibration technique for channel mismatches

In this section, we present a fully digital background calibration technique for channel mismatch as discussed in Section II. The proposed technique performs offset mismatch correction before gain and timing mismatches correction.

A. Offset calibration

Let assume that $\hat{O}_i$ is the estimate of the offset O_i of the i^{th} sub-ADC. Assume that quantization values are small and can be neglected. To calibrate the offset mismatch, first to estimate offset O_i of the individual ADC channels. Assuming that the input signal is Wide-Sense-Stationary (WSS), expected value of the input is approximately zero, i.e. $\frac{1}{N}\sum_{k=0}^{N-1}\big(1+g_i\big)x\big(\big(kM+i\big)T_s+r_i\big) \approx 0$. By averaging the output of each sub-ADC over N samples, the offset estimate of the i^{th} sub-ADC is given as

$$\begin{aligned}\hat{O}_i &= \frac{1}{N}\sum_{k=0}^{N-1} y_i\big[k\big] \\ &= \frac{1}{N}\sum_{k=0}^{N-1}\Big(\big(1+g_i\big)x\big(\big(kM+i\big)T_s+r_i\big)+O_i\Big) \\ &= \underbrace{\frac{1}{N}\sum_{k=0}^{N-1}\big(1+g_i\big)x\big(\big(kM+i\big)T_s+r_i\big)}_{\approx 0} + O_i \approx O_i\end{aligned} \tag{10}$$

Once offset estimate is known, offset mismatch induced error which is the second term of (2) can be subtracted from the sub-ADC output to generate the correct signal as shown in Fig. 3. Consequently, the output of TIADC consists of gain mismatch and timing mismatch only.

B. Gain and timing skew calibration

1) Mismatch correction: The calibration diagram of proposed technique is shown in Fig. 4. Assume that the sum of the mismatch in each channel is equal to zero $\big(g_0+g_1+...+g_{M-1}\big) = \big(r_0+r_1+...+r_{M-1}\big) = 0$. The DFT of the signal without offset mismatch is written as

$$\begin{aligned}Z_k\big(j\omega\big) = \frac{1}{M}\sum_{i=0}^{M-1}\big(1+g_i\big)e^{-j\left(\omega-k\frac{\omega_s}{M}\right)r_i} \\ \times e^{-jki\frac{2\pi}{M}}X\Big(j\big(\omega-k\frac{\omega_s}{M}\big)\Big)\end{aligned} \tag{11}$$

The signal without offset mismatch is called the pseudo aliasing signal. The DFT of the reconstructed signal can be expressed by

$$\begin{aligned}\hat{X}\big(j\omega\big) &= \sum_{k=0}^{M-1} Z_k\big(j\omega\big) \\ &= \sum_{k=0}^{M-1}\frac{1}{M}\sum_{i=0}^{M-1}\big(1+g_i\big)e^{-j\left(\omega-k\frac{\omega_s}{M}\right)r_i} \\ &\times e^{-jki\frac{2\pi}{M}}X\Big(j\big(\omega-k\frac{\omega_s}{M}\big)\Big)\end{aligned} \tag{12}$$

The spectrum of the reconstructed signal and the pseudo aliasing signals in the M-channel TIADC can be expressed by

$$\begin{bmatrix}\hat{X}\left(j\omega\right)\\ \hat{X}_{e1}\left(j\omega\right)\\ \vdots\\ \hat{X}_{e(M-1)}\left(j\omega\right)\end{bmatrix} = F\begin{bmatrix}Z_0\left(j\omega\right)\\ Z_1\left(j\omega\right)\\ \vdots\\ Z_{M-1}\left(j\omega\right)\end{bmatrix} \tag{13}$$

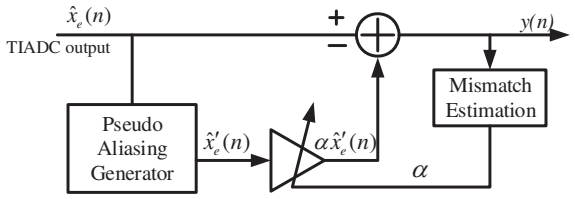

Figure 4: The calibration diagram of the proposed technique for gain and timing mismatches in TIADCs.

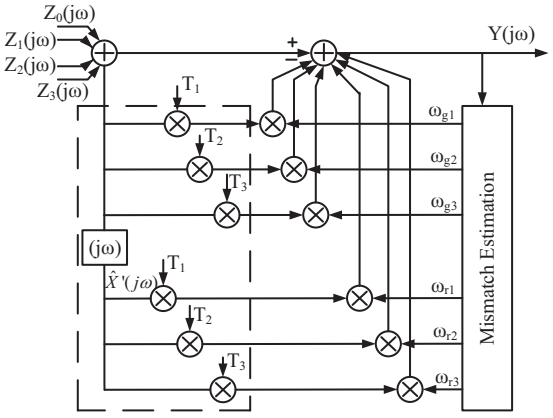

Figure 5: Proposed structure in four-channel TIADC.

where F is the Hadamard transform of order M. The derivative of the signals in formula (13) is given as

$$\begin{bmatrix} \hat{X}'(j\omega) \\ \hat{X}'_{e1}(j\omega) \\ \vdots \\ \hat{X}'_{e(M-1)}(j\omega) \end{bmatrix} = F \begin{bmatrix} Z'_0(j\omega) \\ Z'_1(j\omega) \\ \vdots \\ Z'_{M-1}(j\omega) \end{bmatrix} \tag{14}$$

where,

$$Z'_k(j\omega) = \frac{1}{M} e^{-jki\frac{2\pi}{M}} \sum_{i=0}^{M-1} e^{-j\left(\omega - k\frac{\omega_s}{M}\right)} \hat{X}\left(j\left(\omega - k\frac{\omega_s}{M}\right)\right) \tag{15}$$

The corrected signal is expressed by

$$Y(j\omega) = \hat{X}(j\omega) - \sum_{i=1}^{M-1} \omega_{gi} \hat{X}_{ei}(j\omega) - \sum_{i=1}^{M-1} \omega_{ri} \hat{X}'_{ei}(j\omega) \tag{16}$$

Let us assume the first channel is the reference channel $\omega_{g_0} = \omega_{r_0} = 0$ and g_i, r_i are much less than 1. To correct the signals with gain mismatch g_i and timing mismatch r_i, we can calculate the coefficients ω_{g_i} and ω_{r_i} as follow

$$\begin{bmatrix} \omega_{g0} \\ \omega_{g1} \\ \vdots \\ \omega_{g(M-1)} \end{bmatrix} \approx \frac{1}{M} F \begin{bmatrix} g_0 \\ g_1 \\ \vdots \\ g_{(M-1)} \end{bmatrix} \tag{17}$$

$$\begin{bmatrix} \omega_{r0} \\ \omega_{r1} \\ \vdots \\ \omega_{r(M-1)} \end{bmatrix} \approx \frac{1}{M} F \begin{bmatrix} r_0 \\ r_1 \\ \vdots \\ r_{(M-1)} \end{bmatrix} \tag{18}$$

For example, we propose the structure for four-channel TIADC as the illustration in Fig. 5. The coefficients in the four-channel TIADC as shown in Fig. 5 are

$$\begin{aligned} \omega_{g1} &= \frac{1}{4}(g_0 - g_1 + g_2 - g_3) \\ \omega_{g2} &= \frac{1}{4}(g_0 + g_1 - g_2 - g_3) \\ \omega_{g3} &= \frac{1}{4}(g_0 - g_1 - g_2 + g_3) \\ \omega_{r1} &= \frac{1}{4}(r_0 - r_1 + r_2 - r_3) \\ \omega_{r2} &= \frac{1}{4}(r_0 + r_1 - r_2 - r_3) \\ \omega_{r3} &= \frac{1}{4}(r_0 - r_1 - r_2 + r_3) \end{aligned} \tag{19}$$

Since the sum of the mismatches in each channel is zero, vectors T_1, T_2, T_3 are expressed as follow

$$T_1 = \begin{cases} 1 \\ -1 \\ 1 \\ -1 \end{cases} \quad T_2 = \begin{cases} 1 \\ 1 \\ -1 \\ -1 \end{cases} \quad T_3 = \begin{cases} 1 \\ -1 \\ -1 \\ 1 \end{cases} \tag{20}$$

where T_1, T_2, T_3 are row vectors in the Hadamard transform expect for a row vector $T_0 = (1, 1, 1, 1)$.

2) Mismatch estimation: As described in Section III-B1, gain and timing mismatch are removed output spectrum of M-channel TIADC by calculating estimation parameters (ω_{gi} and ω_{ri}) in (16). The proposed estimation technique requires only one FIR filter and uses the pseudo aliasing signals generated by Hadamard transform in the mismatch estimation. The mismatch estimation block diagram is shown in Fig. 6. It includes a notch filter, a pseudo aliasing generator, and correlators. The notch filter removes signal out of $y(n)$ at $k\pi/M$ to avoid the estimation error. Pseudo aliasing signals $\hat{y}_{ek}(n)$ and $\hat{y}'_{ek}(n)$ that the derived signal of $\hat{y}_{ek}(n)$ are generated by the pseudo aliasing generator. The correlators calculate correlations between the pseudo aliasing signals $\hat{y}_{ek}(n)$, $\hat{y}'_{ek}(n)$ and the output signal of the notch filter $y_n(n)$. Since the offset mismatch was removed before, the correlator worked correctly. The coefficients of (17) and (18) can be calculated by LMS algorithm as follow

$$\omega_{gk}(n+1) = \omega_{gk}(n) + \mu_{gk}(y_n(n)\hat{y}_{ek}(n)) \tag{21}$$

$$\omega_{rk}(n+1) = \omega_{rk}(n) + \mu_{rk}(y_n(n)\hat{y}'_{ek}(n)) \tag{22}$$

where $k = 1, ...M-1$, μ_{gk} and μ_{rk} are the adaptation step sizes for ω_{gk} and ω_{rk}.

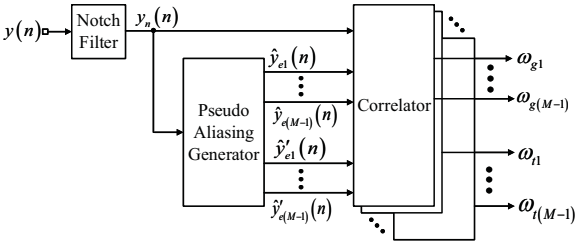

Figure 6: The mismatch estimation block diagram.

IV. Simulation Results

To illustrate the performance of the proposed structure, we have simulated a four-channel 60 dB SNR TIADC clocked at f_s = 2.7 GHz with offset, gain, and timing mismatches as shown in Tab. I. In which assumes channel 0 is a reference channel without gain and timing mismatches. In Simulations, a 33-tap fixed FIR filter is used to obtain the derivative function. The filter coefficients are determined by multiplying the exact coefficients by Hanning window to reduce the truncation error.

The simulation results in Fig. 7 and Fig. 8 show that the harmonics in the TIADC output spectrum using the proposed correction technique have been completely eliminated. The SNDR after calibration is 60.52 dB, which is an improvement of 41.19 dB compared to the uncompensated output (19.33 dB). The SFDR after calibration is 91.56 dB, which is an improvement of 69.8 dB compared to the uncompensated output (21.76 dB). Thus, the performance of TIADC is significantly improved.

The convergence behavior of the estimated offset coefficients $\hat{O}_i$ is shown in Fig. 9. The convergence behavior of the estimated offset coefficients is compared to the expected values, which corresponds well. The convergence behavior of the estimated gain coefficients ω_{gi} and the timing offset coefficients ω_{ri} are shown in Fig. 10 and Fig. 11 respectively. As can be seen, after about 50 samples, estimated offset $\hat{O}_i$ coefficients has converged; after about 10000 samples, estimated gain coefficients $\hat{\omega}_{gi}$ has converged; after about 30000 samples, estimated timing coefficients $\hat{\omega}_{ri}$ has converged.

V. Conclusion

We have developed the fully digital background calibration technique to identify and compensate offset, gain and timing mismatches for TIADCs. In the proposed technique, offset mismatch is corrected by taking the average of the output samples of each channel. The gain and clock skew mismatches are compensated by using Hadamard transform to recon-

Table I: The table of channel mismatch values

Sub ADC	Channel mismatches		
	O_i	g_i	r_i
ADC_0	-0.10675	0	0
ADC_1	0.075462	0.007622	-0.0009263T_s
ADC_2	0.044737	-0.018279	-0.000096028T_s
ADC_3	00.021234	-0.036089	0.00029001T_s

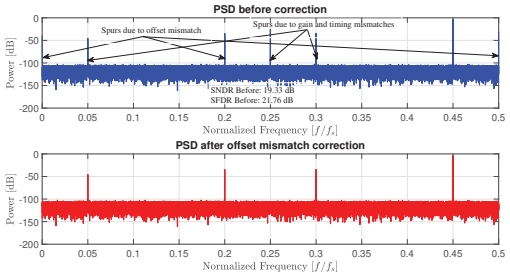

Figure 7: Spectrum of output of four-channel TIADC before/after offset calibration.

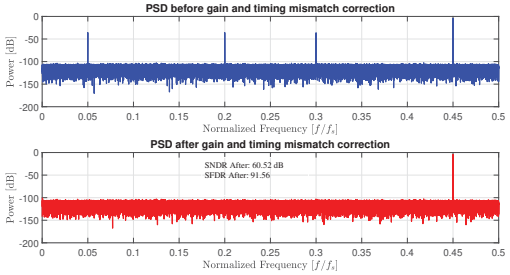

Figure 8: Spectrum of output of four-channel TIADC before/after gain and timing calibration.

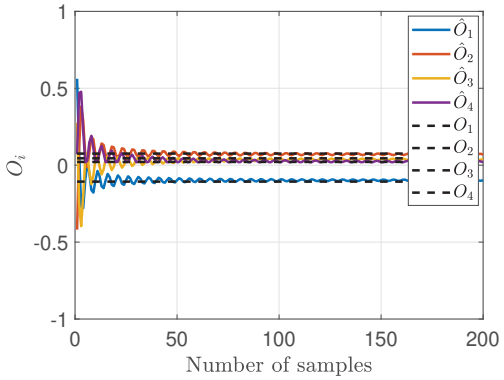

Figure 9: The convergence behavior of the offset mismatch coefficients $\hat{O}_i$

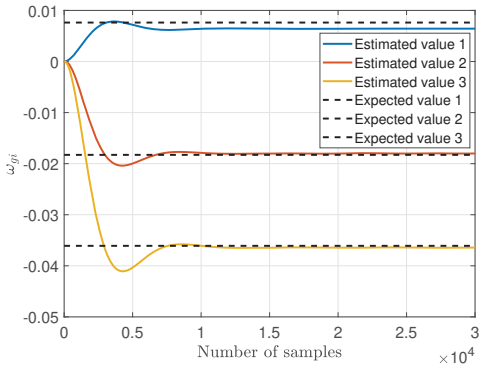

Figure 10: The convergence behavior of the gain mismatch coefficients ω_{gi} compared to their expected values of [0.007622, -0.018279, -0.036089]

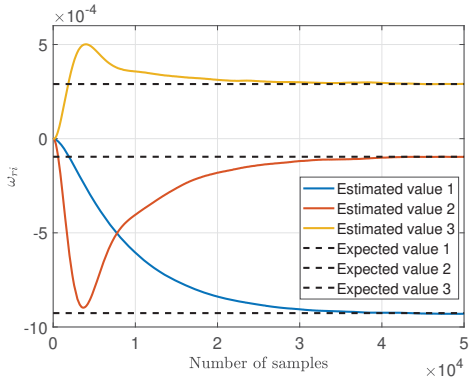

Figure 11: The convergence behavior of the timing mismatch coefficients ω_{ri} compared to their expected values of [-0.0009236, -0.000096028, 0.00029001]

struct the error signal due to gain and timing skew. The error signal is subtracted from the TIADC output to generate the corrected output of TIADC. The gain and timing coefficients are estimated by using cross-correlation between the compensated TIADC output and the pseudo aliasing signals. The simulation results show that the performance of the TIADC is improved by 41.19 dB for SNDR and 69.8 dB for SFDR.

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